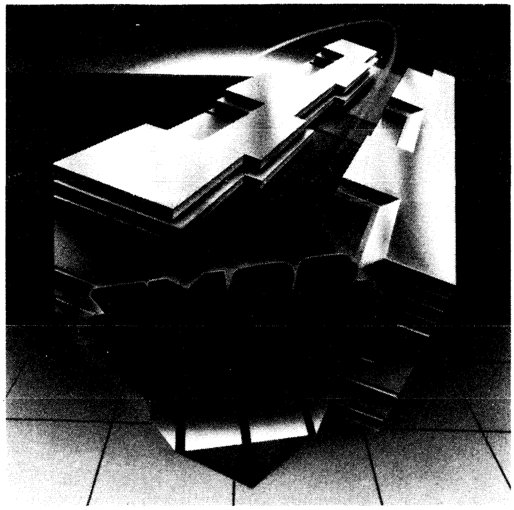
MOTOROLA

POWER MOSFET TRANSISTOR DATA



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MOTOROLA

POWER MOSFET TRANSISTOR DATA

Prepared by
Technical Information Center

Preface

After several years of development, Motorola introduced its first power MOSFETs in 1980. Several technologies were evaluated and the final choice was the double diffused (DMOS) process which Motorola has acronymed TMOS. This process is highly manufacturable and is capable of producing devices with the best characteristics for product needed for power control. Most suppliers of power MOSFETs use the basic DMOS process.

The key to success of power MOSFETs is the control of vertical current flow, which enables suppliers to reduce chip sizes comparable to bipolar transistors. This development opens a new dimension for designers of power control systems.

This manual is intended to give the users of power MOSFETs the basic information on the product, application ideas of power MOSFETs and data sheets of the broadest line of power MOSFETs with a variety of package configurations. The product offering is far from complete. New products will be introduced and old products will be improved, offering designers an even better selection of products for their designs.

Motorola has a long history of supplying high quality power transistors in large volume to the military, automotive, consumer, industrial and computer markets. Being the leading supplier of power transistors in the world, we strive to serve our customers' needs to maintain our leadership position.

Fourth Edition
Second Printing
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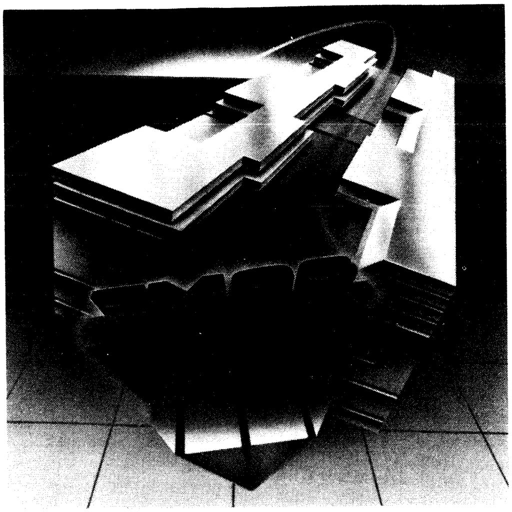
Printed in U.S.A.



Selector Guide 1

TMOS Power MOSFETs

Power MOSFETs are a Reality

MOTOROLA INC.

TMOS

Dear Valued Motorola Customer:

Prior to introducing TMOS Power FETs in 1980, Motorola spent three years in developing what was considered at that time the industry's most advanced power MOSFETs, but we weren't satisfied with that. We kept working on the product and since that time, major advancements in our technology were made. Now high volume and advanced technology allows us to offer you the broadest line of power MOSFETs of the highest quality possible at the best price. With voltage capability to 1000 Volts and current ratings as high as 100 Amperes, you can select exactly what you need.

Our latest technology utilizes high source site or cell density (over 1 million cells per square inch) for efficient utilization of silicon. This results in a smaller chip for a given $r_{DS(on)}$ or a lower $r_{DS(on)}$ for a given chip size — either way, price or performance is enhanced and our customers receive the benefits.

Motorola's commitment to quality is continuing to show significant results. The AOQ of TMOS Power FETs has been consistently reduced and now we guarantee an AOQ of 100 ppm, although currently the AOQ is well under 100 ppm. How we accomplish this is included in this manual.

As the world's largest manufacturer of power transistors we have the equipment, knowhow, and capacity to serve your needs.

Power MOSFETs are a reality and Motorola is dedicated to becoming a leading supplier of power MOSFETs just as it has become the leading source for bipolar power — we intend to attain this leadership position by earning it.

It is our intent to offer superior performance, value, service, quality, and reliability.

We invite your inquiries.

Paul W. White

Paul V. White,
Vice President and Director of Product Marketing,
Discrete and Special Technologies Group

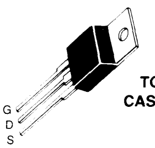
Selection by Package

The product listed in Tables 1 through 22 have been compiled on an IBM or compatible personal computer disk for quick selection of product. This versatile disk may be obtained by contacting a Motorola sale office in your area or by contacting a Motorola Literature Distribution Center listed on the back cover. Order the disk by requesting DK101/D.

Tables 1 through 22 are shown by package type. Within the tables the devices are arranged by breakdown voltage and on-resistance as the primary selection criteria. Device types shaded in Tables 1 through 8 are preferred devices recommended for new designs.

TMOS Power MOSFETs

Plastic Packages — TO-220AB



TO-220AB
CASE 221A-04

Table 1 — P-Channel

	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
	500	6	1	MTP2P50	2	75	3-407
	450			MTP2P45			3-407
	250	4	1.5	MTP3P25	3		3-427
		3	2.5	MTP5P25	5		3-447
		2	4	MTP8P25	8		3-462
NEW	200	0.5	6	**IRF9640**	11	125	3-147
NEW		0.8	3.5	**IRF9630**	6.5	75	3-145
		1	2.5	MTP5P20	5		3-442
	180			MTP5P18			3-442
	100	0.4	4	MTP8P10	8		3-457
		0.3	6	MTP12P10	12		3-493
	80	0.4	4	MTP8P08	8		3-457
				MTP12P08	12		3-493
	60	0.6	3.5	MTP7P06	7		3-651
NEW		0.3	6	**MTP2955**	12		3-806
				MTP12P06			3-493
		0.2	10	MTP20P06	20	100	3-740
	50	0.6	3.5	MTP7P05	7	75	3-651
		0.3	6	MTP12P05	12		3-493

* @ 25°C
Bold Type indicates new product.
Shaded devices are preferred devices and are recommended for new designs.

Plastic Packages — TO-220AB (continued)

Table 2 — N-Channel

	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
	1000	10	0.5	MTP1N100	1	75	3-392
		4	1.5	MTP3N100	3		3-606
	950	10	0.5	MTP1N95	1		3-392
		4	1.5	MTP3N95	3		3-606
	900	8	1	MTP2N90	2		3-402
		4	2	MTP4N90	4		3-606
	850	8	1	MTP2N85	2		3-402
		4	2	MTP4N85	4		3-606
	800	7	1.5	MTP3N80	3		3-417
NEW		3	1.7	**BUZ80A**			3-79
	750	7	1.5	MTP3N75			3-417
	600	12	0.5	MTP1N60	1		3-566
		6	1	MTP2N60	2		3-586
		2.5	1.5	MTP3N60	3		3-412
NEW		2	2.5	**BUZ90**	4		3-85
		1.2	3	MTP6N60	6	125	3-641
	550	12	0.5	MTP1N55	1	75	3-566
		6	1	MTP2N55	2		3-586
		2.5	1.5	MTP3N55	3		3-412
		1.2	3	MTP6N55	6	125	3-641
	500	8	0.5	MTP1N50	1	50	3-561
		4	1	MTP2N50	2	75	3-397
		3	1.5	IRF820	2.5	40	3-139
				MTP3N50	3	75	3-601
		2		IRF832	4		3-141
		1.5		IRF830	4.5		3-141
				MTP4N50	4		3-432
		1.1	4	IRF842	7	125	3-143
		0.85		IRF840	8		3-143
		0.8		MTP8N50			3-672
	450	8	0.5	MTP1N45	1	50	3-561
		4	1	MTP2N45	2	75	3-397
				IRF823		40	3-139
		3		IRF821	2.5		3-139
			1.5	MTP3N45	3	75	3-601
		2	2.5	IRF833	4		3-141
		1.5	2	MTP4N45			3-432
			2.5	IRF831	4.5		3-141

* @ 25°C
Bold Type indicates new product.
Shaded devices are preferred devices and are recommended for new designs.

Plastic Packages — TO-220AB (continued)

Table 2 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
450	1.1	4	IRF843	7	125	3-143
	0.85		IRF841	8		3-143
	0.8		MTP8N45			3-672
400	5	1	MTP2N40	2	50	3-581
	3.3	1.5	MTP3N40	3	75	3-596
	2.5		IRF722	2.5	40	3-133
	1.8		IRF720	3		3-133
	1.5	3	IRF732	4.5	75	3-135
	1		IRF730			3-135
		2.5	MTP5N40	5		3-437
	0.55		IRF740	10	125	3-137
			MTP10N40			3-704
350	5	1	MTP2N35	2	50	3-581
	1.5	3	IRF733	4.5	75	3-135
	1		IRF731	5.5		3-135
		2.5	MTP5N35	5		3-437
	0.55	5	IRF741	10	125	3-137
			MTP10N35			3-704
250	2	1	MTP2N25	2	50	3-576
	0.45	5	MTP10N25	10	100	3-478
200	2.4	1.25	IRF612	2	20	3-123
	1.8	1	MTP2N20		50	3-571
	1.5	1.25	IRF610	2.5	20	3-123
	1		MTP5N20	5	75	3-631
	0.8		IRF620		40	3-125
	0.7	3.5	MTP7N20	7	75	3-646
	0.6	5	IRF632	8		3-127
	0.4		IRF630	9		3-127
		4	MTP8N20	8		3-452
		3.5	BUZ73	7	40	3-75
	0.35	6	MTP12N20	12	100	3-714
	0.22	10	IRF642	16	125	3-129
	0.18		IRF640	18		3-129
150	0.8	2.5	IRF621	4	40	3-125
	0.4	5	IRF631	9	75	3-127
	0.3		MTP10N15	10		3-699
	0.25	7.5	MTP15N15	15	100	3-729
	0.22	10	IRF643	16	125	3-129

* @ 25°C
Shaded devices are preferred devices and are recommended for new designs.

Plastic Packages — TO-220AB (continued)

Table 2 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
150	0.18	10	IRF641	18	125	3-129
120	0.3	5	MTP10N12L	10	75	3-473
	0.9	2.5	MTP5N12	5	50	3-626
	1.2	1.5	MTP3N12	3		**
100	0.8	3	MTP6N10	6		3-636
		2	IRF512	3.5	20	3-115
	0.6		IRF510	4		3-115
	0.5	4	MTP8N10	8	75	3-656
			MTP8N10E			**3-661**
	0.4		IRF522	7	40	3-117
	0.33	5	MTP10N10	10	75	3-682
	0.3	4	IRF520	8	40	3-117
	0.25	**5**	**MTP10N10E**	**10**	**75**	**3-687**
		8	IRF532	12		3-119
	0.18		IRF530	14		3-119
		6	MTP12N10	12		3-488
	0.15	10	MTP20N10	20	100	3-519
			MTP20N10E			**3-734**
	0.11	15	IRF542	24	125	3-121
	0.085		IRF540	27		3-121
		12.5	MTP25N10	25		3-757
	0.075		**MTP25N10E**			**3-762**
80	0.8	2	MTP4N08	4	50	3-616
	0.5	4	MTP8N08	8	75	3-656
	0.33	5	MTP10N08	10		3-682
	0.18	6	MTP12N08	12		3-488
	0.15	10	MTP20N08	20	100	3-519
60	0.8	2	IRF513	3.5	20	3-115
	0.6		IRF511	4		3-115
		2.5	MTP5N06	5	50	3-621
	0.4	3.5	MTP7N06	7		**
		4	IRF523		40	3-117
	0.3		IRF521	8		3-117
	0.28	5	MTP10N06	10	75	3-677
	0.25	8	IRF533	12		3-119
	0.2	**5**	**MTP10N06E**	**10**		**3-467**
		6	MTP12N06			3-483
	0.18	8	IRF531	14		3-119

* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.

Plastic Packages — TO-220AB (continued)

Table 2 — N-Channel — continued

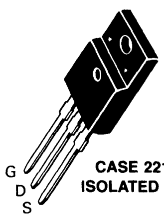
$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
60	0.16	7.5	MTP15N06	15	75	3-719
	0.15		MTP15N06E			3-503
		6	MTP3055E	12	40	3-811
	0.085	15	IRF541	27	125	3-121
	0.08	12.5	MTP25N06	25	100	3-524
			MTP25N06E			3-751
	0.055	17.5	MTP35N06E	35	125	3-781
50	0.6	2.5	MTP5N05	5	50	3-621
	0.28	5	MTP10N05	10	75	3-677
	0.16	7.5	MTP15N05	15		3-719
	0.12	6	BUZ71A	12	40	3-70
			MTP12N05E			**
			IRFZ22	14		3-165
	0.1		BUZ71	12		3-70
		7.5	MTP15N05E	15		**
			IRFZ20			3-165
	0.08	12.5	MTP25N05	25	100	3-524
	0.07		MTP25N05E			3-745
			IRFZ32			3-167
	0.06	15	BUZ11A		75	3-67
	0.05		MTP30N05E	30		3-768
	0.04		BUZ11			3-67
	0.035	29	MTP45N05E	45	125	3-539
			IRFZ42	46		3-169
	0.028	25	MTP50N05E	50		3-550
		29	IRFZ40	51		3-169

* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.

Table 3 — N- and P-Channel — Isolated TO-220

	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
NEW	60	0.3	6	MTA2955***	7	33	**
NEW		0.15		MTA3055E	10		**
NEW		0.1	7.5	MTA15N06E	15	40	**
NEW		0.028	25	MTA30N06E	30	50	**

* @ 25°C
**Contact Motorola sales office for data sheet.
***Indicates P-Channel
Shaded devices are preferred devices and are recommended for new designs.

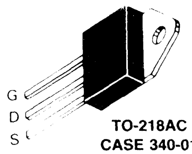


CASE 221D-01
ISOLATED TO-220

1

TMOS Power MOSFETs

Plastic Packages — TO-218AC



TO-218AC
CASE 340-01

Table 4 — P-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
200	0.7	4	MTH8P20	8	125	3-314
180			MTH8P18			3-314
100	0.15	10	MTH20P10	20		3-339
80			MTH20P08			3-339
60	0.14	12.5	MTH25P06	25		3-349
50			MTH25P05			3-349

* @ 25°C
Shaded devices are preferred devices and are recommended for new designs.

Table 5 — N-Channel

	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
NEW	1000	2	3	**MTH6N100**	6	150	3-287
		3	2.5	MTH5N100	5		3-272
	950			MTH5N95			3-272
NEW	900	1.8	4	**MTH8N90**	8	170	3-308
		3	3	MTH6N90	6	150	3-282
	850			MTH6N85			3-282
NEW	800	1.5	3.8	**BUZ355**		125	3-91
	600	1.2	3	MTH6N60		150	3-277
		0.5	4	MTH8N60	8		3-303
	550	1.2	3	MTH6N55	6		3-277
		0.5	4	MTH8N55	8		3-303
	500	0.8	3.5	MTH7N50	7		3-293
NEW		0.6	6	**BUZ330**	9.5	125	3-87
		0.4	7	MTH13N50	13	150	3-319
	450	0.8	3.5	MTH7N45	7		3-293
		0.4	7	MTH13N45	13		3-319
	400	0.55	4	MTH8N40	8		3-298
		0.3	7.5	MTH15N40	15		3-329
	350	0.55	4	MTH8N35	8		3-298
		0.3	7.5	MTH15N35	15		3-329
NEW	250	0.14	15	**MTH30N25**	20	125	3-359

* @ 25°C
Bold Type indicates new product.
Shaded devices are preferred devices and are recommended for new designs.

Plastic Packages — TO-218AC (continued)

Table 5 — N-Channel — continued

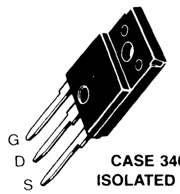
	V(BR)DSS (Volts) Min	rDS(on) (Ohms) Max	@ ID (Amps)	Device	ID (cont) Amps	PD* (Watts) Max	Page
	200	0.16	7.5	MTH15N20	15	150	3-324
		0.08	15	MTH30N20	30		3-354
	150	0.12	10	MTH20N15	20		3-334
		0.06	17.5	MTH35N15	35		3-376
	100	0.07	12.5	MTH25N10	25		3-344
		0.04	20	MTH40N10	40		3-381
	80	0.07	12.5	MTH25N08	25		3-344
		0.04	20	MTH40N08	40		3-381
	60	0.055	17.5	MTH35N06	35		3-365
				MTH35N06E			3-370
		0.028	20	MTH40N06	40		3-381
	50	0.055	17.5	MTH35N05	35		3-365
		0.028	20	MTH40N05	40		3-381
NEW			25	**MTH50N05E**	50	125	3-386

* @ 25°C
Bold Type indicates new product.
Shaded devices are preferred devices and are recommended for new designs.

Table 6 — N- and P-Channel Isolated TO-218

	V(BR)DSS (Volts) Min	rDS(on) (Ohms) Max	@ ID (Amps)	Device	ID (cont) Amps	PD* (Watts) Max	Page
NEW	500	0.4	7	**MTG9N50E**	9	70	**
NEW	200	0.08	15	**MTG20N20**	20		**
NEW	100	0.15	10	**MTG15P10*** **	15		**

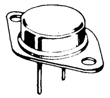
* T_C = 25°C
**Contact Motorola sales office for data sheet.
***Indicates P-Channel
Bold Type indicates new product.



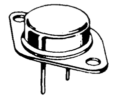
CASE 340B-03
ISOLATED TO-218

TMOS Power MOSFETs

Metal Packages — TO-204AA/AE



TO-204AA
CASE 1-06



TO-204AE
CASE 197A-02

Table 7 — P-Channel

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
500	6	1	MTM2P50	2	75	3-407
450			MTM2P45			3-407
250	4	1.5	MTM3P25	3		3-427
	3	2.5	MTM5P25	5		3-447
	2	4	MTM8P25	8		3-462
200	1	2.5	MTM5P20	5		3-442
	0.7	4	MTM8P20	8	125	3-314
180	1	2.5	MTM5P18	5	75	3-442
	0.7	4	MTM8P18	8	125	3-314
100	0.4		MTM8P10		75	3-457
	0.3	6	MTM12P10	12		3-493
	0.15	10	MTM20P10	20	125	3-339
80	0.4	4	MTM8P08	8	75	3-457
	0.3	6	MTM12P08	12		3-493
	0.15	10	MTM20P08	20	125	3-339
60	0.3	6	MTM12P06	12	75	3-493
	0.14	12.5	MTM25P06	25	125	3-349
50	0.3	6	MTM12P05	12	75	3-493
	0.2	10	MTM20P05	20	100	**
	0.14	12.5	MTM25P05	25	125	3-349

* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.

Table 8 — N-Channel

	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
	1000	10	0.5	MTM1N100	1	75	3-392
		4	1.5	MTM3N100	3	125	3-422
		3	2.5	MTM5N100	5	150	3-272
NEW		1.2	5	MTM10N100E	10	300	**

* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.

Metal Packages — TO-204AA/AE (continued)

Table 8 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
950	10	0.5	MTM1N95	1	75	3-392
	4	1.5	MTM3N95	3	125	3-422
	3	2.5	MTM5N95	5	150	3-272
900	8	1	MTM2N90	2	75	3-402
	4	2	MTM4N90	4	125	3-422
	3	3	MTM6N90	6	150	3-282
850	8	1	MTM2N85	2	75	3-402
	4	2	MTM4N85	4	125	3-422
	3	3	MTM6N85	6	150	3-282
800	7	1.5	MTM3N80	3	75	3-417
	2	3	BUZ84	5.3	125	3-83
	1.5		BUZ84A	6		3-83
750	7	1.5	MTM3N75	3	75	3-417
600	2.8	3	2N6823			3-48
	2.5	1.5	MTM3N60			3-412
	1.6	6	2N6826	6	150	3-53
	1.2	3	MTM6N60			3-277
	0.5	4	MTM8N60	8		3-303
500	4	1	MTM2N50	2	75	3-397
	1.5	2	MTM4N50	4		3-432
		3	2N6762	4.5		3-18
	0.85	4	IRF440	8	125	3-111
	0.8	3.5	MTM7N50	7	150	3-293
	0.5	7	IRF452	12		3-113
	0.4		IRF450	13		3-113
		7.75	2N6770	12		3-37
		7.5	MTM15N50	15	250	3-514
NEW	0.25	12	MTM24N50E	24	300	**
450	1.5	2	MTM4N45	4	75	3-432
	0.85	4	IRF441	8	125	3-111
	0.8	3.5	MTM7N45	7	150	3-293
	0.4	7	IRF451	13		3-113
		7.5	MTM15N45	15	250	3-514

* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.

Metal Packages — TO-204AA/AE (continued)

Table 8 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
400	1	3	IRF330	5.5	75	3-105
		2.5	MTM5N40	5		3-437
		3.5	2N6760	5.5		3-14
	0.55	5	IRF340	10	125	3-107
		4	MTM8N40	8	150	3-298
	0.3	8	IRF350	15		3-109
		9	2N6768	14		3-32
		7.5	**MTM15N40**	15	250	3-509
NEW	0.18	13	**MTM26N40E**	26	300	**
350	1.5	3	IRF333	4.5	75	3-105
			2N6759			3-14
	1		IRF331	5.5		3-105
		2.5	MTM5N35	5		3-437
	0.3	8	IRF351	15	150	3-109
		7.5	MTM15N35		250	3-509
250	0.45	5	MTM10N25	10	100	3-478
200	0.4		IRF230	9	75	3-99
			2N6758			3-10
		4	MTM8N20	8		3-452
	0.18	10	IRF240	18	125	3-101
	0.16	7.5	**MTM15N20**	15	150	3-324
	0.12	16	IRF252	25		3-103
	0.085		IRF250	30		3-103
		19	2N6766			3-27
	0.08	20	**MTM40N20**	40	250	3-534
150	0.22	10	IRF243	16	125	3-101
	0.18	16	IRF241	18		3-101
	0.12	10	MTM20N15	20	150	3-334
		16	IRF253	25		3-103
	0.085		IRF251	30		3-103
	0.06	22.5	MTM45N15	45	250	3-545
100	0.18	8	IRF130	14	75	3-93
		6	MTM12N10	12		3-488
		9	2N6756	14		3-6
	0.15	10	MTM20N10	20	100	3-519
	0.11	15	IRF142	24	125	3-95
	0.085		IRF140	27		3-95
	0.08	20	IRF152	33	150	3-97

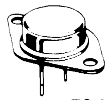
* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.

Metal Packages — TO-204AA/AE (continued)

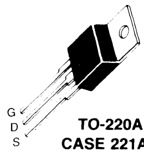
Table 8 — N-Channel — continued

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
100	0.075	12.5	MTM25N10E	25	150	**
	0.07		MTM25N10			3-344
	0.055	20	IRF150	40		3-97
		24	2N6764	38		3-22
	0.04	27.5	MTM55N10	55	250	3-556
80			MTM55N08			3-556
60	0.15	7.7	MTM15N06E	17	75	3-503
	0.085	15	IRF141	27	125	3-95
	0.055	17.5	MTM35N06	35	150	3-365
			MTM35N06E			3-370
		20	IRF151	40		3-97
	0.028	30	MTM60N06	60	250	3-556
50	0.2	6	MTM12N05	12	75	3-483
	0.055	17.5	MTM35N05	35	125	3-365
	0.035	29	MTM45N05E	45		3-539
	0.028	25	MTM50N05E	50		3-550
		30	MTM60N05	60	250	3-556

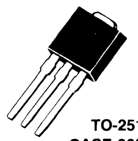
* @ 25°C
**Contact Motorola sales office for data sheet.
Shaded devices are preferred devices and are recommended for new designs.



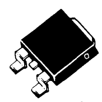
TO-204AA
(TO-3)
CASE 1-06



TO-220AB
CASE 221A-04



TO-251
CASE 369-03



TO-252
CASE 369A-04

TMOS Power MOSFETs

Logic Level Power MOSFETs

Logic level MOSFETs are fully enhanced with 5 volts applied to the gate.

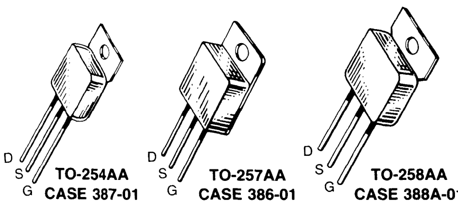
Table 9 — N-Channel Logic Level Power MOSFETs (TO-204AA and TO-220AB)

	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	$I_{D(cont)}$ Amps	P_D @ T_C = 25°C Watts	Package TO-	Page
	150	0.3	5	MTM10N15L	10	75	204AA	3-473
				MTP10N15L			220AB	3-473
NEW		0.45	4	**MTP8N15L**	8			3-667
	120	0.3	5	MTM10N12L	10		204AA	3-473
				MTP10N12L			220AB	3-473
	100	0.2	6	MTM12N10L	12		204AA	**
				MTP12N10L			220AB	3-709
		1.25	2	MTP3N10L	3			3-591
NEW	80	0.135	7.5	**MTP15N08L**	15			3-724
		0.2	6	MTM12N08L	12		204AA	**
				MTP12N08L			220AB	3-709
		1.25	2	MTP3N08L	3			3-591
NEW	60	0.06	20	**MTP40N06EL**	40	150		3-787
		0.08	12.5	MTM25N06L	25	100	204AA	3-529
				MTP25N06L			220AB	3-529
		0.15	7.5	MTM15N06L	15	75	204AA	3-498
				MTP15N06L			220AB	3-498
NEW		0.18	6	**MTP3055EL**	12	40		3-817
NEW				**MTD3055EL**			TO-252	3-266
NEW				**MTD3055EL1**			TO-251	3-266
		0.6	2	MTP4N06L	4	25	220AB	3-611
NEW	50	0.032	25	**MTP50N05EL**	50	150		3-800
		0.08	12.5	MTM25N05L	25	100	204AA	3-529
				MTP25N05L			220AB	3-529
		0.15	7.5	MTM15N05L	15	75	204AA	3-498
				MTP15N05L			220AB	3-498
		0.6	2	MTP4N05L	4	25		3-611

**Contact Motorola sales office for data sheet.
Bold Type indicates new product.
Shaded devices are preferred devices and are recommended for new designs.

TMOS Power MOSFETs

Hermetic, Isolated, Tab Mount Power MOSFETs



TO-254AA CASE 387-01 (Similar to TO-220)

TO-257AA CASE 386-01

TO-258AA CASE 388A-01 (Similar to TO-218)

Table 10 — TO-254AA, TO-257AA, and TO-258AA

ALL NEW DEVICES**

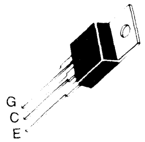
	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device	$I_{D(cont)}$ Amps	P_D @ T_C = 25°C Watts	Package TO-
NEW	1000	3	2.5	**MHR5N100**	5	125	258AA
NEW				**MHM5N100**			254AA
NEW		8	0.5	**MHT1N100**	1	50	257AA
NEW	800	6	1	**MHT2N80**	2		
NEW	500	0.4	7	**MHR15N50**	15	125	258AA
NEW				**MHM12N50**	12		254AA
NEW		1.8	3.5	**MHR7P50***	7		258AA
NEW				**MHM7P50***			254AA
NEW		1.5	3	**MHT4N50**	4	50	257AA
NEW		6	1	**MHT2P50***	2		
NEW	200	0.1	16	**MHR30N20**	30	125	258AA
NEW				**MHM25N20**	25		254AA
NEW		0.4	6	**MHT8N20**	8	50	257AA
NEW		0.75	4	**MHR8P20***		125	258AA
NEW				**MHM8P20***			254AA
NEW				**MHT8P20***			257AA
NEW	100	0.065	20	**MHR35N10**	35		258AA
NEW				**MHM25N10**	25		254AA
NEW		0.15	10	**MHM20P10***	20		
NEW		0.2	5	**MHT10N10**	10	50	257AA
NEW		0.3		**MHT12P10***			
NEW	60	0.05	15	**MHR35N06M**	35	125	CASE 388-01

*Indicates P-Channel
**Contact Motorola sales office for data sheet.
Bold Type indicates new product.
Note: All of these devices can be purchased with JTX or JTXV equivalent processing by adding HX or HXV suffix to device type.

TMOS Insulated Gate Bipolar Transistors

Gain Enhanced MOSFETs (IGBTs)

This relatively new series of power transistors combines the high input resistance of a MOSFET with the low internal on-resistance of a bipolar transistor to provide more efficient performance than either a MOSFET or bipolar device in low-frequency switching service. Recommended for motor drive circuits, home appliances, and other applications where high switching speed is not a requirement. All are N-Channel.

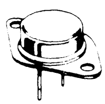


TO-220AB
CASE 221A-04

Table 11 — TO-220AB

$V_{(BR)CES}$ (Volts) Min	$r_{CE(on)}$ (Ohms) Max	@ I_C (Amps)	Device	I_C (cont) Amps	P_D* (Watts) Max	Page
500	0.27	10	MGP20N50	20	100	3-184
	1.6	2.5	MGP5N50	5	50	3-180
450	0.27	10	MGP20N45	20	100	3-184
	1.6	2.5	MGP5N45	5	50	3-180

* @ 25°C



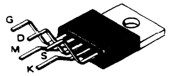
TO-204AA
(TO-3)
CASE 1-06

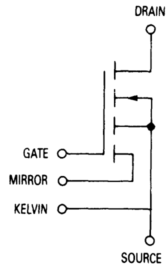
Table 12 — TO-204AA

$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
500	0.27	10	MGM20N50	20	100	3-184
	1.6	2.5	MGM5N50	5	50	3-180
450	0.27	10	MGM20N45	20	100	3-184
	1.6	2.5	MGM5N45	5	50	3-180

* @ 25°C

CASE 314B
(5 PIN TO-220)





TMOS SENSEFETs

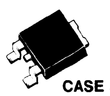
SENSEFETs are conventional power MOSFETs with an option provided to sense the drain current by measuring a small proportion of the total drain current. These devices are ideal for current mode switching regulators and motor controls.

Table 13 — Case 314B

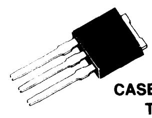
	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
NEW	60	0.04	20	**MTP40N06M**	40	125	3-793
NEW	80	0.065	15	**MTP30N08M**	30		3-774
	100	0.25	5	MTP10N10M	10	75	3-693
		0.085	12.5	MTP25N10M	25	100	**
	250	1.5	4	MTP4N25M	4	75	**
		0.45	2	MTP10N25M	10	100	**

* @ 25°C
**Contact Motorola sales office for data sheet.
Bold Type indicates new product.

DPAK



CASE 369A-04****
TO-252



CASE 369-03***
TO-251

Table 14 — Case 369A-04 Surface Mount Case 369-03 Insertion Mountable

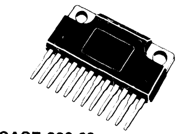
	$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D* (Watts) Max	Page
	500	4	1	MTD2N50	2	1.75**	3-219
	400	5	0.5	MTD1N40	1		3-208
	200	0.7	2	MTD4N20	4		3-224
NEW		1.5	1	**MTD2N20**	2		3-213
	150	0.3	3	MTD6N15	6		3-244
	100	0.25		MTD6N10			3-239
	80			MTD6N08			3-239
	60	0.6	2	MTD4P06†	4		3-229
		0.4	2.5	MTD5N06	5		3-234
		0.3	6	MTD2955†	12		3-255
NEW		0.15	4	**MTD3055E**	8		3-260
	50	0.6	2	MTD4P05†	4		3-229
		0.4	2.5	MTD5N05	5		3-234
		0.1	5	MTD10N05E	10		3-249

* @ 25°C
**Power rating when mounted on a board with the minimum pad size recommended.
***Add -1 Suffix to part number to order insertion mountable package.
****Available in tape and reel.
† Indicates P-Channel
Bold Type indicates new product.
Shaded devices are preferred devices and are recommended for new designs.

1

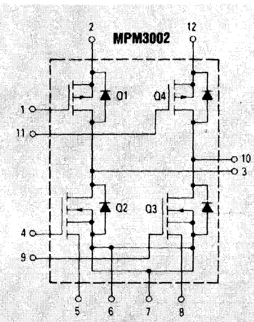
TMOS Power MOSFETs

Multiple Chip Products

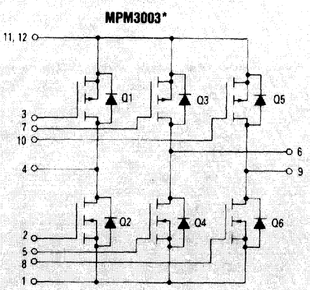


CASE 806-02

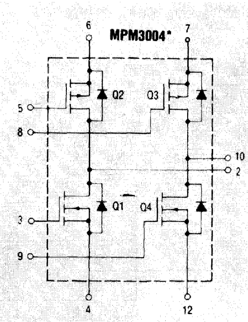
Table 15 — Multiple Chip Products in the Isolated ICePAK*



H-Bridge with Current Sensing
100 Volts and 8 Amperes
P-Channel MOSFETs — $r_{DS(on)}$ = 0.4 Ohms Max
N-Channel SENSEFETs — $r_{DS(on)}$ = 0.15 Ohms Max
See Page 3-198



Three-Phase Bridge with Complementary Outputs
60 Volts and 10 Amperes
P-Channel — $r_{DS(on)}$ = 0.28 Ohms Max
N-Channel — $r_{DS(on)}$ = 0.15 Ohms Max



H-Bridge
60 Volts and 10 Amperes
P-Channel MOSFETs — $r_{DS(on)}$ = 0.28 Ohms Max
N-Channel MOSFETs — $r_{DS(on)}$ = 0.15 Ohms Max

Table 16 — TMOS Power MOSFET Modules*

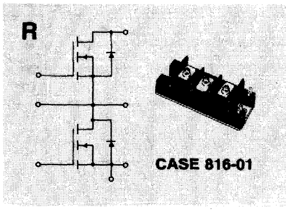
Max I_D (cont) Amps	Max V_{DSS} Volts	Device Type	Module Type	Max $V_{DS(on)}$ Volts	Conditions		Max. Resistive Switching					P_D T_C = 25°C Watts	Case No.	Circuit Config.
										Conditions				
					I_D Amps	V_{GS} Volts	t_{on} µs	t_{off} µs	t_f µs	I_D(A)	V_G			
15	450	MT15FR45 (UL)	Six-pack	6	15x6	10	0.6	2	0.5	15	10	125x6	809-01	Y
50	450	MT50BY45	Dual	7	50	10	0.8	1.3	0.2	50	10	400x2	816-01	R

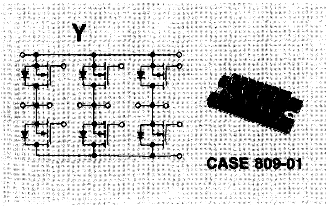
Table 17 — IGBT Power Modules*

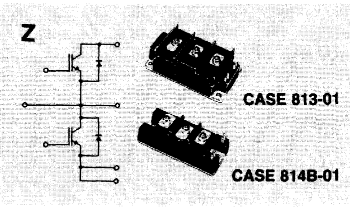
(UL) RECOGNIZED

Max I_C (cont) Amps	Max V_{CES} Volts	Device Type	Module Type	Max V_{CE} Volts	Conditions		Max. Resistive Switching					P_D T_C = 25°C Watts	Case No.	Circuit Config.
										Conditions				
					I_C Amps	V_{GE} Volts	t_{on} µs	t_s µs	t_f µs	I_C(A)	V_G(V)			
25	1000	MG25BZ100 (UL)	Dual	5	25	15	1	2	1	25	15	200x2	813-01	Z
50	1000	MG50BZ100 (UL)	Dual	5	50	15	1	1.5	1	50	15	300x2	813-01	Z
100	1000	MG100BZ100 (UL)	Dual	5	100	15	1	1.5	1	100	15	400x2	814B-01	Z
25	500	MG25BZ50	Dual	5	25	15	1	1.5	1	25	15	125x2	813-01	Z
50	500	MG50BZ50	Dual	5	50	15	1	1.5	1	50	15	300x2	813-01	Z
75	500	MG75BZ50	Dual	5	75	15	1	1.5	1	75	15	350x2	813-01	Z
100	500	MG100BZ50	Dual	5	100	15	1	1.5	1	100	15	400x2	813-01	Z

Table 18 — TMOS Power MOSFET and IGBT Power Module Circuit Configurations and Packages.*

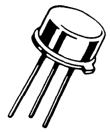






*Contact Motorola sales office for data sheets.

Small-Signal MOSFETs



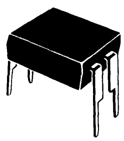
TO-205AF
(TO-39)
CASE 79-05

Table 19 — Switches and Choppers — TO-205AF

$V_{(DSS)}$ (Volts)	$r_{DS(on)}$ (Ohms)	@ I_D (Amps)	Device	$I_{D(Cont)}$ (Amps)	P_D @ $T_C = 25°C$ (Watts)	Page
240	6	0.5	VN2406B	0.63	2.5	**
	10	0.5	VN2410B	0.63	2.5	**
200	0.8	2.25	2N6790	3.5	20	**
	0.8	2	IRFF220	3.5	20	3-163
	1.5	1.5	2N6784	2.25	15	3-44
	6.4	0.25	MFE9200	0.4	1.8	3-177
170	6	0.5	VN1706B	0.63	2.5	**
	10	0.5	VN1710B	0.63	2.5	**
100	0.3	3	IRFF120	6	20	3-161
90	4	1	2N6661	0.9	6.25	3-2
60	3	1	2N6660	1.1	6.25	3-2
	5	0.5	MFE910	1	6.25	3-171
35	1.8	1	2N6659	1.4	6.25	**
30	1.2	1	VN0300B	1.25	6.25	**

**Contact Motorola sales office for data sheet.

Table 20 — 4-Pin Dip — Case 370-01



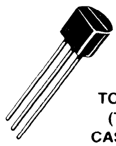
CASE 370-01

P_D @ $T_C = 25°C$ **1 Watt Max**

$V_{BR(DSS)}$ (Volts) Min	$r_{DS(on)}$ (Ohms) Max	@ I_D (Amp)	Device	$I_{D(Cont)}$ (Amp) Max	Page
200	0.8	0.4	IRFD220	0.8	3-157
	1.5	0.3	IRFD210	0.6	3-155
150	2.4	0.3	IRFD213	0.45	3-155
100	0.3	0.6	IRFD120	1.3	3-153
	0.6	0.8	IRFD110	1	3-151
	0.6	−0.8	IRFD9120	−1	**
	1.2	−0.3	IRFD9110	−0.7	**
	2.4	0.25	IRFD1Z0	0.5	3-149
60	0.4	0.6	IRFD123	1.1	3-153
	0.8	0.8	IRFD113	0.8	3-151
	0.8	−0.8	IRFD9123	−0.8	**

**Contact Motorola sales office for data sheet.

Small-Signal MOSFETs (continued)



TO-226AA
(TO-92)
CASE 29-04

Table 21 — Plastic — TO-226AA

$V_{(BR)DSS}$	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amp)	Device	$I_{D(Cont)}$ (Amp) Max	P_D @ T_C = 25°C Watts Max	Page
240	6	0.5	VN2406L	0.158	0.4	**
	10	0.5	VN2410L	0.12	0.4	**
200	6.4	0.25	BS107A	0.25	0.6	**
	6.4	0.25	MPF9200	0.4	0.5	3-195
	14	0.2	BS107	0.25	0.6	**
170	6	0.5	VN1706L	0.158	0.4	**
	10	0.5	VN1710L	0.12	0.4	**
150	12	0.1	MPF4150†	0.25	0.625	3-193
60	5	0.5	2N7000	0.5	0.4	3-58
	5	0.2	BS170	0.195	0.4	3-62
	5	0.5	VN0610LL	0.12	0.4	3-823
	7.5	0.5	VN2222LL	0.099	0.4	3-825
30	1.2	1	VN0300L	0.4	0.4	**

**Contact Motorola sales office for data sheet.
†Depletion Mode

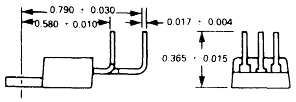
TO-236AA
(SOT-23)
CASE 318-02

Table 22 — Surface Mount — Case 318-02

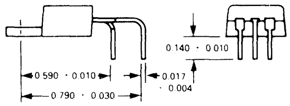
$V_{(BR)DSS}$ (Volts) Min	$r_{DS(on)}$ @ I_D (Ohms) Max	(Amp)	Device	$I_{D(Cont)}$ (Amp) Max	P_D @ T_C = 25°C Watts Max	Package	Page
100	6	0.1	BSS123	0.17	0.2	318-02	3-65
60	5	0.2	MMBF170	0.5	0.2	318-02	3-188
	7.5	0.5	2N7002	0.8	0.2	318-02	3-60

TO-220 Leadforms

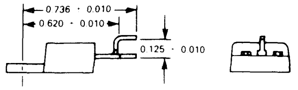
LEADFORM AJ



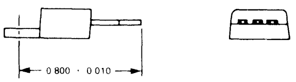
LEADFORM AK



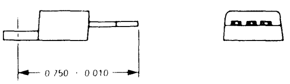
LEADFORM S



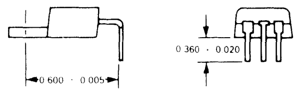
LEADFORM W



LEADFORM WC



LEADFORM 2A



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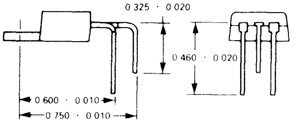

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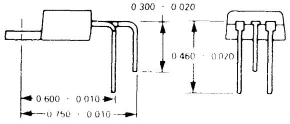

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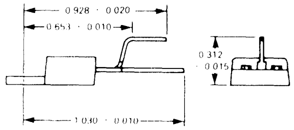

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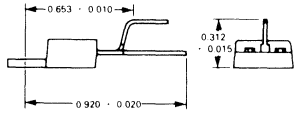

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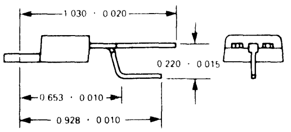
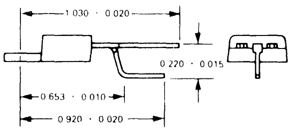
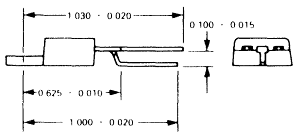


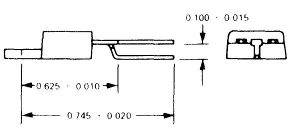
LEADFORM 5RA



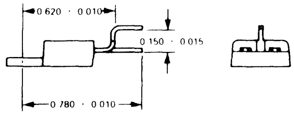
LEADFORM 10R



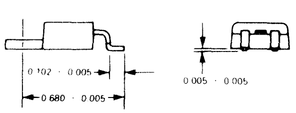
LEADFORM 10RC



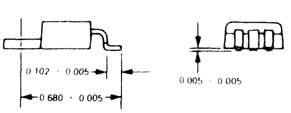
LEADFORM 15FA



LEADFORM 16



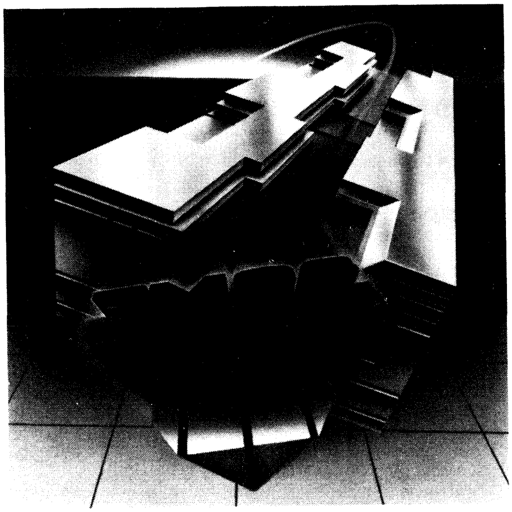
LEADFORM 16A



Ordering Information: To purchase a leadformed device, contact your local sales office and advise which leadform is required. The sales office will contact the factory and obtain a part number to be used to order the leadformed device.

Theory and Applications Chapters 1 through 15

2



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References

Chapter 1: Introduction to Power MOSFETs

Symbols, Terms and Definitions

The following are the most commonly used letter symbols, terms and definitions associated with Power MOSFETs.

Symbol	Term	Definition
C_{ds}	drain-source capacitance	The capacitance between the drain and source terminals with the gate terminal connected to the guard terminal of a three-terminal bridge.
C_{dg}	drain-gate capacitance	The same as C_{rss} — See C_{rss}.
C_{gs}	gate-source capacitance	The capacitance between the gate and source terminals with the drain terminal connected to the guard terminal of a three-terminal bridge.
C_{iss}	short-circuit input capacitance, common-source	The capacitance between the input terminals (gate and source) with the drain short-circuited to the source for alternating current. (Ref. IEEE No. 255)
C_{oss}	short-circuit output capacitance, common-source	The capacitance between the output terminals (drain and source) with the gate short-circuited to the source for alternating current. (Ref. IEEE No. 255)
C_{rss}	short-circuit reverse transfer capacitance, common-source	The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three-terminal bridge.
g_{FS}	common-source large-signal transconductance	The ratio of the change in drain current due to a change in gate-to-source voltage
I_D	drain current, dc	The direct current into the drain terminal.
$I_{D(on)}$	on-state drain current	The direct current into the drain terminal with a specified forward gate-source voltage applied to bias the device to the on-state.
I_{DSS}	zero-gate-voltage drain current	The direct current into the drain terminal when the gate-source voltage is zero. This is an on-state current in a depletion-type device, an off-state in an enhancement-type device.
I_G	gate current, dc	The direct current into the gate terminal.
I_{GSS}	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of a junction-gate field-effect transistor when the gate terminal is reverse biased with respect to the source terminal and the drain terminal is short-circuited to the source terminal.

2

2-1

Symbol	Term	Definition
I_{GSSF}	forward gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated-gate field-effect transistor with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
I_{GSSR}	reverse gate current, drain short-circuited to source	The direct current into the gate terminal of an insulated-gate field-effect transistor with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.
I_S	source current, dc	The direct current into the source terminal.
P_T, P_D	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages.
Q_g	total gate charge	The total gate charge required to charge the MOSFETs input capacitance to $V_{GS(on)}$.
$r_{DS(on)}$	static drain-source on-state resistance	The dc resistance between the drain and source terminals with a specified gate-source voltage applied to bias the device to the on state.
$R_{\theta CA}$	thermal resistance, case-to-ambient	The thermal resistance (steady-state) from the device case to the ambient.
$R_{\theta JA}$	thermal resistance, junction-to-ambient	The thermal resistance (steady-state) from the semiconductor junction(s) to the ambient.
$R_{\theta JC}$	thermal resistance, junction-to-case	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the case.
$R_{\theta JM}$	thermal resistance, junction-to-mounting surface	The thermal resistance (steady-state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	ambient temperature or free-air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.
T_C	case temperature	The temperature measured at a specified location on the case of a device.
t_c	turn-off crossover time	The time interval during which drain voltage rises from 10% of its peak off-state value and drain current falls to 10% of its peak on-state value, in both cases ignoring spikes that are not charge-carrier induced.
T_J	channel temperature	The temperature of the channel of a field-effect transistor.
T_{stg}	storage temperature	The temperature at which the device, without any power applied, may be stored.
$t_{d(off)}$	turn-off delay time	Synonym for current turn-off delay time (see Note 1)*.
$t_{d(off)i}$	current turn-off delay time	The interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain current waveform falls to 90% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
$t_{d(off)v}$	voltage turn-off delay time	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain voltage waveform rises to 10% of its off-state amplitude, ignoring spikes that are not charge-carrier induced.
$t_{d(on)}$	turn-on delay time	Synonym for current turn-on delay time (see Note 1)*.

Symbol	Term	Definition
$t_{d(on)i}$	current turn-on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain current waveform rises to 10% of its on-state amplitude, ignoring spikes that are not charge-carrier induced.
$t_{d(on)v}$	voltage turn-on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain voltage waveform falls to 90% of its off-state amplitude, ignoring spikes that are not charge-carrier induced.
t_f	fall time	Synonym for current fall time (See Note 1)*.
t_{fi}	current fall time	The time interval during which the drain current changes from 90% to 10% of its peak off-state value, ignoring spikes that are not charge-carrier induced.
t_{fv}	voltage fall time	The time interval during which the drain voltage changes from 90% to 10% of its peak off-state value, ignoring spikes that are not charge-carrier induced.
t_{off}	turn-off time	Synonym for current turn-off time (see Note 1)*.
$t_{off(i)}$	current turn-off time	The sum of current turn-off delay time and current fall time, i.e., $t_{d(off)i} + t_{fi}$.
$t_{off(v)}$	voltage turn-off time	The sum of voltage turn-off delay time and voltage rise time, i.e., $td(off)v + t_{rv}$.
t_{on}	turn-on time	Synonym for current turn-on time (See Note 1)*.
$t_{on(i)}$	current turn-on time	The sum of current turn-on delay time and current rise time, i.e., $t_{d(on)i} + t_{ri}$.
$t_{on(v)}$	voltage turn-on time	The sum of voltage turn-on delay time and voltage fall time, i.e., $t_{d(on)v} + t_{fv}$.
t_p	pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform. **Note:** The two reference points are usually 90% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge. If the reference points are 50% points, the symbol t_w and term average pulse duration should be used.
t_r	rise time	Synonym for current rise time (See Note 1)*.
t_{ri}	current rise time	The time interval during which the drain current changes from 10% to 90% of its peak on-state value, ignoring spikes that are not charge-carrier induced.
t_{rv}	voltage rise time	The time interval during which the drain voltage changes from 10% to 90% of its peak off-state value, ignoring spikes that are not charge-carrier induced.
t_{ti}	current tail time	The time interval following current fall time during which the drain current changes from 10% to 2% of its peak on-state value, ignoring spikes that are not charge-carrier induced.

Symbol	Term	Definition
t_W	average pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady-state amplitude of the waveform existing after the leading edge, measured with respect to the steady-state amplitude existing before the leading edge. **Note:** If the reference points are not 50% points, the symbol t_p and term pulse duration should be used.
$V_{(BR)DSR}$	drain-source breakdown voltage with (resistance between gate and source)	The breakdown voltage between the drain terminal and the source terminal when the gate terminal is (as indicated by the last subscript letter) as follows: R = returned to the source terminal through a specified resistance.
$V_{(BR)DSS}$	gate short-circuited to source	S = short-circuited to the source terminal.
$V_{(BR)DSV}$	voltage between gate and source	V = returned to the source terminal through a specified voltage.
$V_{(BR)DSX}$	circuit between gate and source	X = returned to the source terminal through a specified circuit.
$V_{(BR)GSSF}$	forward gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a forward gate-source voltage applied and the drain terminal short-circuited to the source terminal.
$V_{(BR)GSSR}$	reverse gate-source breakdown voltage	The breakdown voltage between the gate and source terminals with a reverse gate-source voltage applied and the drain terminal short-circuited to the source terminal.
V_{DD}, V_{GG} V_{SS}	supply voltage, dc (drain, gate, source) voltage	The dc supply voltage applied to a circuit or connected to the reference terminal.
V_{DG} V_{DS} V_{GD} V_{GS} V_{SD} V_{SG}	drain-to-gate drain-to-source gate-to-drain gate-to-source source-to-drain source-to-gate	The dc voltage between the terminal indicated by the first subscript and the reference terminal indicated by the second subscript (stated in terms of the polarity at the terminal indicated by the first subscript).
$V_{DS(on)}$	drain-source on-state voltage	The voltage between the drain and source terminals with a specified forward gate-source voltage applied to bias the device to the on state.
$V_{GS(th)}$	gate-source threshold voltage	The forward gate-source voltage at which the magnitude of the drain current of an enhancement-type field-effect transistor has been increased to a specified low value.
$Z_{\theta JA(t)}$	transient thermal impedance, junction-to-ambient	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\theta JC(t)}$	transient thermal impedance, junction-to-case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Note 1: As names of time intervals for characterizing switching transistors, the terms "fall time" and "rise time" always refer to the change that is taking place in the magnitude of the output current even though measurements may be made using voltage waveforms. In a purely resistive circuit, the (current) rise time may be considered equal and coincident to the voltage fall time and the (current) fall time may be considered equal and coincident to the voltage rise time. The delay times for current and voltage will be equal and coincident. When significant amounts of inductance are present in a circuit, these equalities and coincidences no longer exist, and use of the unmodified terms delay time, fall time, and rise time must be avoided.

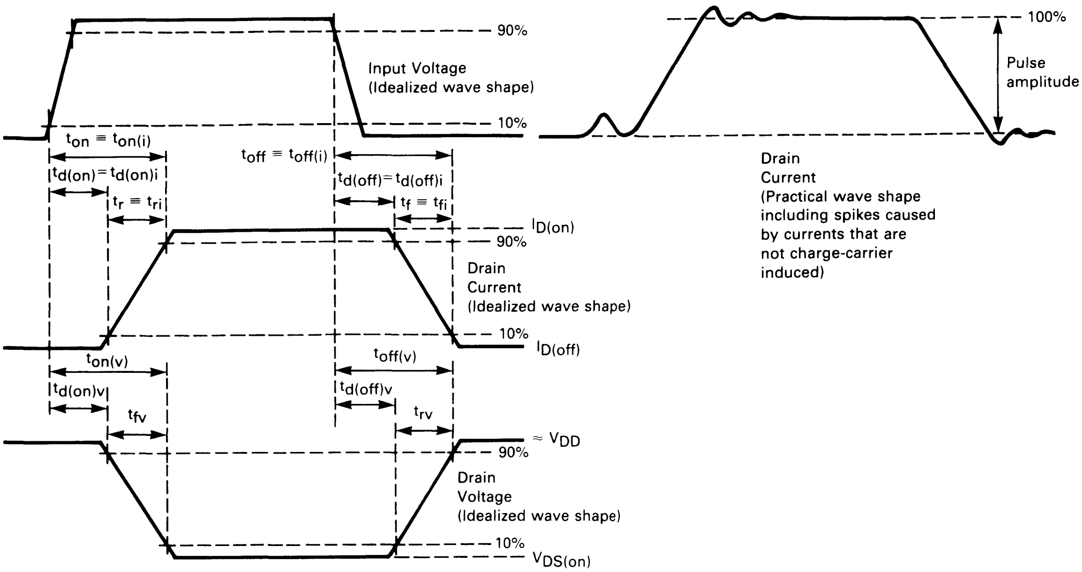
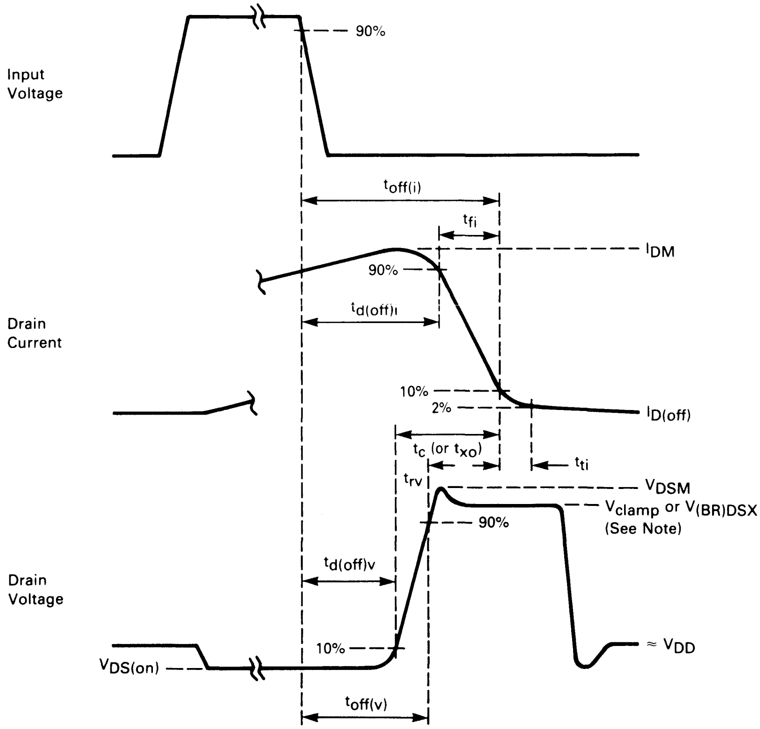


FIGURE 1-1 — WAVEFORMS FOR RESISTIVE-LOAD SWITCHING



NOTE: V_{clamp} (in a clamped inductive-load switching circuit) or $V_{(BR)DSX}$ (in an unclamped circuit) is the peak off-state voltage excluding spikes.

FIGURE 1-2 — WAVEFORMS FOR INDUCTIVE LOAD SWITCHING, TURN-OFF

Basic TMOS Structure, Operation and Physics

Structures:

Motorola's TMOS Power MOSFET family is a matrix of diffused channel, vertical, metal-oxide-semiconductor power field-effect transistors which offer an exceptionally wide range of voltages and currents with low $r_{DS(on)}$. The inherent advantages of Motorola's power MOSFETs include:

- Nearly infinite static input impedance featuring:
  - — Voltage driven input
  - — Low input power
  - — Few driver circuit components
- Very fast switching times
  - — No minority carriers
  - — Minimal turn-off delay time
  - — Large reversed biased safe operating area
  - — High gain bandwidth product
- Positive temperature coefficient of on-resistance
  - — Large forward biased safe operating area
  - — Ease in paralleling
- Almost constant transconductance
- High dv/dt immunity
- Low Cost

Motorola's TMOS power MOSFET line is the latest step in an evolutionary progression that began with the conventional small-signal MOSFET and superseded the intermediate lateral double diffused MOSFET (LDMOSFET) and the vertical V-groove MOSFET (VMOSFET).

The conventional small-signal lateral N-channel MOSFET consists of a lightly doped P-type substrate into which two highly doped N+ regions are diffused, as shown in Figure 1-3. The N+ regions act as source and drain which are separated by a channel whose length is determined by photolithographic constraints. This configuration resulted in long channel lengths, low current capability, low reverse blocking voltage and high $r_{DS(on)}$.

Two major changes in the small-signal MOSFET structure were responsible for the evolution of the power MOSFET. One was the use of self aligned, double diffusion techniques to achieve very short channel lengths, which allowed higher channel packing densities, resulting in higher current capability and lower $r_{DS(on)}$. The other was the incorporation of a lightly doped N+ region between the channel and the N+ drain allowing high reverse blocking voltages.

These changes resulted in the lateral double diffused MOSFET power transistor (LDMOS) structure shown in Figure 1-4, in which all the device terminals are still on the top surface of the die. The major disadvantage of this configuration is its inefficient use of silicon area due to the area needed for the top drain contact.

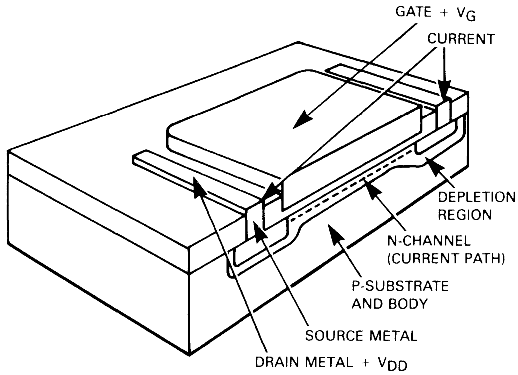


FIGURE 1-3 — CONVENTIONAL SMALL-SIGNAL MOSFET HAS LONG LATERAL CHANNEL RESULTING IN RELATIVELY HIGH DRAIN-TO-SOURCE RESISTANCE.

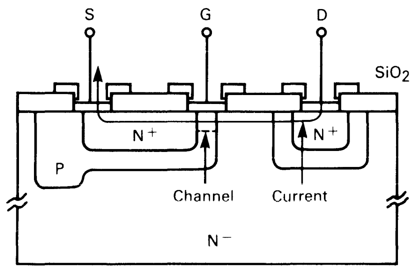


FIGURE 1-4 — LATERAL DOUBLE DIFFUSED MOSFET STRUCTURE FEATURING SHORT CHANNEL LENGTHS AND HIGH PACKING DENSITIES FOR LOWER ON RESISTANCE.

The next step in the evolutionary process was a vertical structure in which the drain contact was on the back of the die, further increasing the channel packing density. The initial concept used a V-groove MOSFET power transistor as shown in Figure 1-5. The channels in this device are defined by preferentially etching V-grooves through double diffused N+ and P− regions. The requirements of adequate packing density, efficient silicon usage and adequate reverse blocking voltage are all met by this configuration. However, due to its non-planar structure, process consistency and cleanliness requirements resulted in higher die costs.

The cell structure chosen for Motorola's TMOS power MOSFET's is shown in Figure 1-6. This structure is similar to that of Figure 1-4 except that the drain contact is dropped through the N− substrate to the back of the die. The gate structure is now made with polysilicon sandwiched between two oxide layers and the source metal applied continuously over the entire active area. This two layer electrical contact gives the optimum in packing density and maintains the processing advantages of planar LDMOS. This results in a highly manufacturable process which yields low $r_{DS(on)}$ and high voltage product.

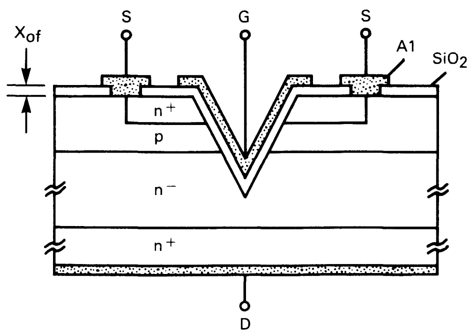


FIGURE 1-5 — V-GROOVE MOSFET STRUCTURE HAS SHORT VERTICAL CHANNELS WITH LOW DRAIN-TO-SOURCE RESISTANCE.

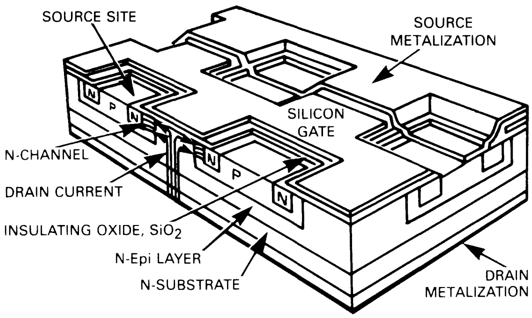


FIGURE 1-6 — TMOS POWER MOSFET STRUCTURE OFFERS VERTICAL CURRENT FLOW, LOW RESISTANCE PATHS AND PERMITS COMPACT METALIZATION ON TOP AND BOTTOM SURFACES TO REDUCE CHIP SIZE.

Operation:

Transistor action and the primary electrical parameters of Motorola's TMOS power MOSFET can be defined as follows:

Drain Current, I_D:

When a gate voltage of appropriate polarity and magnitude is applied to the gate terminal, the polysilicon gate induces an inversion layer at the surface of the diffused channel region represented by r_{CH} in Figure 1-7 (page A-8). This inversion layer or channel connects the source to the lightly doped region of the drain and current begins to flow. For small values of applied drain-to-source voltage, V_{DS}, drain current increases linearly and can be represented by Equation (1).

$$(1) \quad I_D \approx \frac{Z}{L} \mu Co \left[V_{GS} - V_{GS(th)}\right] V_{DS}$$

As the drain voltage is increased, the drain current saturates and becomes proportional to the square of the applied gate-to-source voltage, V_{GS}, as indicated in Equation (2).

$$(2) \quad I_D \approx \frac{Z}{2L} \mu Co \left[V_{GS} - V_{GS(th)}\right]^2$$

Where μ = Carrier Mobility
Co = Gate Oxide Capacitance per unit area
Z = Channel Width
L = Channel Length

These values are selected by the device design engineer to meet design requirements and may be used in modeling and circuit simulations. They explain the shape of the output characteristics discussed in Chapter 2.

Transconductance, g_{FS}:

The transconductance or gain of the TMOS power MOSFET is defined as the ratio of the change in drain current and an accompanying small change in applied gate-to-source voltage and is represented by Equation (3).

$$(3) \quad g_{FS} = \frac{\Delta I_{D(sat)}}{\Delta V_{GS}} = \frac{Z}{L} \mu Co \left[V_{GS} - V_{GS(th)}\right]$$

The parameters are the same as above and demonstrate that drain current and transconductance are directly related and are a function of the die design. Note that transconductance is a linear function of the gate voltage, an important feature in amplifier design.

Threshold Voltage, $V_{GS(th)}$

Threshold voltage is the gate-to-source voltage required to achieve surface inversion of the diffused channel region, (r_{CH} in Figure 1-7 page A-8) and as a result, conduction in the channel.

As the gate voltage increases the more the channel is "enhanced," or the lower its resistance (r_{CH}) is made, the more current will flow. Threshold voltage is measured at a specified value of current to maintain measurement correlations. A value of 1.0 mA is common throughout the industry. This value is primarily a function of the gate oxide thickness and channel doping level which are chosen during the die design to give a high enough value to keep the device off with no bias on the gate at high temperatures. A minimum value of 1.5 volts at room temperature will guarantee the transistor remains an enhancement mode device at junction temperatures up to 150°C.

On-Resistance, $r_{DS(on)}$:

On-resistance is defined as the total resistance encountered by the drain current as it flows from the drain terminal to the source terminal. Referring to Figure 1-7, $r_{DS(on)}$ is composed primarily of four resistive components associated with:

The Inversion channel, r_{CH}; the Gate-Drain Accumulation Region, r_{ACC}; the junction FET Pinch region, r_{JFET}; and the lightly doped Drain Region, r_D, as indicated in Equation (4).

$$(4) \quad r_{DS(on)} = r_{CH} + r_{ACC} + r_{JFET} + r_D$$

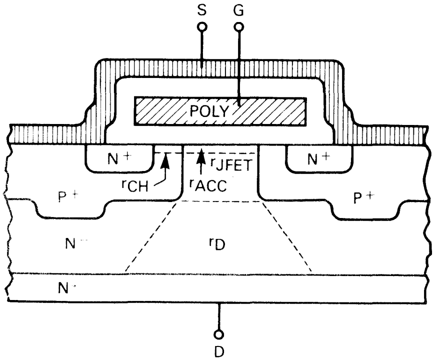


FIGURE 1-7 — TMOS DEVICE ON-RESISTANCE

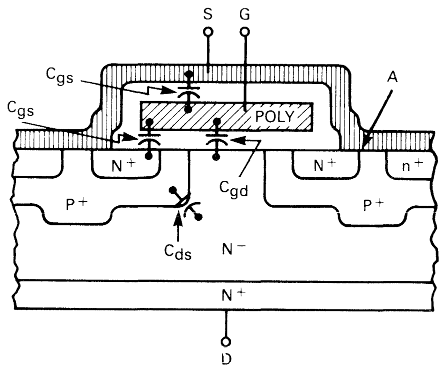


FIGURE 1-8 — TMOS DEVICE PARASITIC CAPACITANCES

Whereas the channel resistance increases with channel length, the accumulation resistance increases with poly width and the JFET pinch resistance increases with epi resistivity and all three are inversely proportional to the channel width and gate-to-source voltage. The drain resistance is proportional to the epi resistivity, poly width and inversely proportional to channel width. This says that the on-resistance of TMOS power FETs with the thick and high resistivity epi required for high voltage parts will be dominated by r_D.

Low voltage devices have thin, low resistivity epi and r_{CH} will be a large portion of the total on-resistance. This is why high voltage devices are "full on" with moderate voltages on the gate, whereas with low voltage devices the on-resistance continues to decrease as V_{GS} is increased toward the maximum rating of the device.

Note: $r_{DS(on)}$ is inversely proportional to the carrier mobility. This means that the $r_{DS(on)}$ of the P-Channel MOSFET is approximately 2.5 to 3.0 times that of a similar N-Channel MOSFET. Therefore, in order to have matched complementary on characteristics, the Z/L ratio of the P-Channel device must be 2.5–3.0 times that of the N-Channel device. This means larger die are required for P-Channel MOSFET's with the same $r_{DS(on)}$ and same breakdown voltage as an N-Channel device and thus device capacitances and costs will be correspondingly higher.

Breakdown Voltage, $V_{(BR)DSS}$:

Breakdown voltage or reverse blocking voltage of the TMOS power MOSFET is defined in the same manner as $V_{(BR)CES}$ in the bipolar transistor and occurs as an avalanche breakdown. This voltage limit is reached when the carriers within the depletion region of the reverse biased P-N junction acquire suffficient kinetic energy to cause ionization or when the critical electric field is reached. The magnitude of this voltage is determined mainly by the characteristics of the lightly doped drain region and the type of termination of the die's surface electric field.

Figure 1-9 shows a schematic representation of the cross-section in Figure 1-8 and depicts the bipolar transistor built in the epi layer. Point A shows where the emitter and base of the bipolar is shorted together. This is why $V_{(BR)DSS}$ of the power FET is equal to $V_{(BR)CES}$ of the bipolar. Also note the short brings the base in contact with the source metal allowing the use of the base-collector junction. This is the diode across the TMOS power MOSFET.

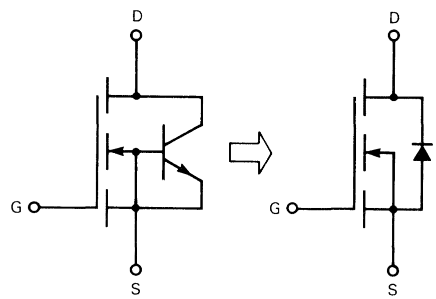


FIGURE 1-9 — SCHEMATIC DIAGRAM OF ALL THE COMPONENTS OF THE CROSS SECTION OF FIGURE 1-7.

TMOS Power MOSFET Capacitances:

Two types of intrinsic capacitances occur in the TMOS power MOSFET — those associated with the MOS structure and those associated with the P-N junction.

The two MOS capacitances associated with the MOSFET cell are:

Gate-Source Capacitance, C_{gs}
Gate-Drain Capacitance, C_{gd}

The magnitude of each is determined by the die geometry and the oxides associated with the silicon gate.

The P-N junction formed during fabrication of the power MOSFET results in the drain-to-source capacitance, C_{ds}. This capacitance is defined the same as any other planar junction capacitance and is a direct function of the channel drain area and the width of the reverse biased junction depletion region.

The dielectric insulator of C_{gs} and C_{gd} is basically a glass. Thus these are very stable capacitors and will not vary with voltage or temperature. If excessive voltage is placed on the gate, breakdown will occur through the glass, creating a resistive path and destroying MOSFET operation.

Optimizing TMOS Geometry:

The geometry and packing density of Motorola's MOSFETs vary according to the magnitude of the reverse blocking voltage.

The geometry of the source site, as well as the spacing between source sites, represents important factors in efficient power MOSFET design. Both parameters determine the channel packing density, i.e.: ratio of channel width per cell to cell area.

For low voltage devices, channel width is crucial for minimizing $r_{DS(on)}$, since the major contributing component of $r_{DS(on)}$ is r_{CH}. However, at high voltages, the major contributing component of resistance is r_D and thus minimizing $r_{DS(on)}$ is dependent on maximizing the ratio of active drain area per cell to cell area. These two conditions for minimizing $r_{DS(on)}$ cannot be met by a single geometry pattern for both low and high voltage devices.

2

2-1

Distinct Advantages of Power MOSFETs

Power MOSFETs offer unique characteristics and capabilities that are not available with bipolar power transistors. By taking advantage of these differences, overall systems cost savings can result without sacrificing reliability.

Speed

Power MOSFETs are majority carrier devices, therefore their switching speeds are inherently faster. Without the minority carrier stored base charge common in bipolar transistors, storage time is eliminated. The high switching speeds allow efficient switching at higher frequencies which reduces the cost, size and weight of reactive components.

MOSFET switching speeds are primarily dependent on charging and discharging the device capacitances and are essentially independent of operating temperature.

Input Characteristics

The gate of a power MOSFET is electrically isolated from the source by an oxide layer that represents a dc resistance greater than 40 megohms. The devices are fully biased-on with a gate voltage of 10 volts. This significantly simplifies the drive circuits and in many instances the gate may be driven directly from logic integrated circuits such as CMOS and TTL to control high power circuits directly.

Since the gate is isolated from the source, the drive requirements are nearly independent of the load current. This reduces the complexity of the drive circuit and results in overall system cost reduction.

Safe Operating Area

Power MOSFETs, unlike bipolars, do not require derating of power handling capability as a function of applied voltage. The phenomena of second breakdown does not occur within the ratings of the device. Depending on the application, snubber circuits may be eliminated or a smaller capacitance value may be used in the snubber circuit. The safe operating boundaries are limited by the peak current ratings, breakdown voltages and the power capabilities of the devices.

On-Voltage

The minimum on-voltage of a power MOSFET is determined by the device on-resistance $r_{DS(on)}$. For low voltage devices the value of $r_{DS(on)}$ is extremely low, but with high voltage devices the value increases. $r_{DS(on)}$ has a positive temperature coefficient which aids in paralleling devices.

Examples of Advantages Offered by MOSFETs

High Voltage Flyback Converter

An obvious way of showing the advantages of power MOSFETs over bipolars is to compare the two devices in the same system. Since the drive requirements are not the same, it is not a question of simply replacing the bipolar with the FET, but one of designing the respective drive circuits to produce an equivalent output, as described in Figures 1-10 and 1-11.

For this application, a peak output voltage of about 700 V driving a 30 kΩ load ($P_{O(pk)} \approx 16$ W) was required. With the component values and timing shown, the inductor/device current required to generate this flyback voltage would have to ramp up to about 3.0 A.

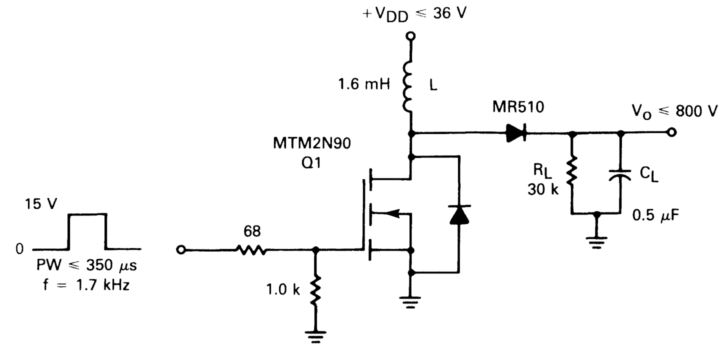


FIGURE 1-10 — TMOS OUTPUT STAGE

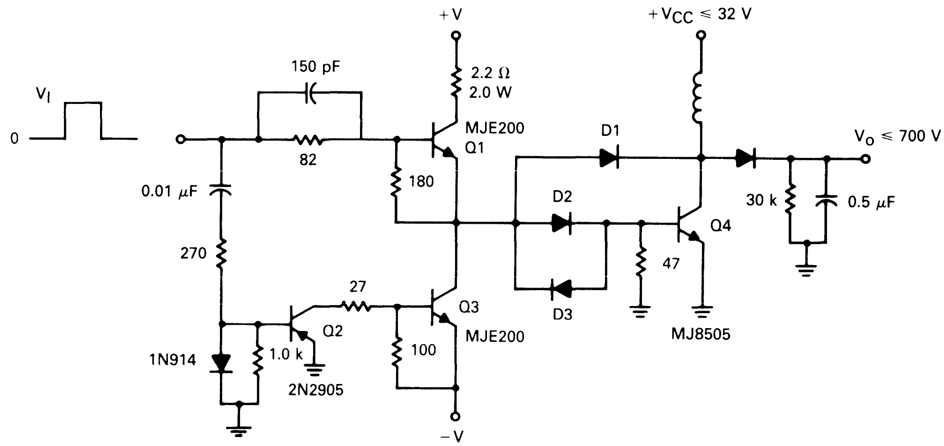


FIGURE 1-11 — BIPOLAR DRIVER AND OUTPUT STAGE

FIGURES 1-10 AND 1-11 — CIRCUIT CONFIGURATIONS FOR A TMOS AND BIPOLAR OUTPUT STAGE OF A HIGH VOLTAGE FLYBACK CONVERTER

Figure 1-10 shows the TMOS version. Because of its high input impedance, the FET, an MTM2N90, can be directly driven from the pulse width modulator. However, the PWM output should be about 15 volts in amplitude and for relatively fast FET switching be capable of sourcing and sinking 100 mA. Thus, all that is required to drive the FET is a resistor or two. The peak drain current of 3.2 A is within the MTM2N90 pulsed current rating of 7.0 A (2.0 A continuous), and the turn-off load line of 3.2 A, 700 V is well within the Switching SOA (7.0 A, 900 V) of the device. Thus, the circuit demonstrates the advantages of TMOS:

- High input impedance
- Fast Switching
- No Second breakdown

Compare this circuit with the bipolar version of Figure 1-11.

To achieve the output voltage, using a high voltage Switchmode MJ8505 power transistor, requires a rather complex drive circuit for generating the proper I_{B1} and I_{B2}. This circuit uses three additional transistors (two of which are power transistors), three Baker clamp diodes, eleven passive components and a negative power supply for generating an off-bias voltage. Also, the RBSOA capability of this device is only 3.0 A at 900 V and 4.7 A at 800 V, values below the 7.0 A, 900 V rating of the MOSFET. A detailed description of these circuits is shown in Chapter 7, TMOS applications.

20 kHz Switcher

An example of TMOS advantage over bipolar that il-

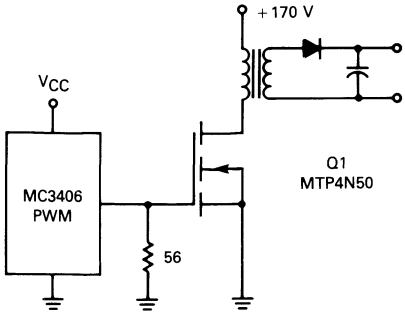


FIGURE 1-12 — TMOS VERSION

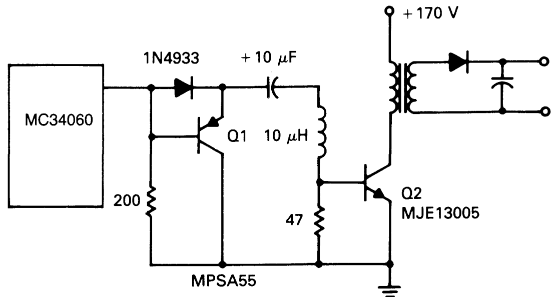


FIGURE 1-13 — BIPOLAR VERSION

FIGURES 1-12 AND 1-13 — COMPARISON OF TMOS versus BIPOLAR IN THE POWER OUTPUT STAGE OF A 20 kHz SWITCHER

lustrates its superior switching speed is shown in the power output section of Figures 1-12 and 1-13. In addition to the drive simplicity and reduced component count, the faster switching speed offers better circuit efficiency. For this 35 W switching regulator, using the same small heatsink for either device, a case temperature rise of only 18°C was measured for the MTP4N50 power MOSFET compared to a 46°C rise for the MJE13005 bipolar transistor. Although the saturation losses were greater for the TMOS, its lower switching losses predominated, resulting in a more efficient switching device. A more detailed description of this Switcher is shown in Chapter 9.

In general, at low switching frequencies, where static losses predominate, bipolars are more efficient. At higher frequencies, above 30 kHz to 100 kHz, the power MOSFETs are more efficient.

Chapter 2: Basic Characteristics of Power MOSFETs

Output Characteristics

Perhaps the most direct way to become familiar with the basic operation of a device is to study its output characteristics. In this case, a comparison of the MOSFET characteristics with those of a bipolar transistor with similar ratings is in order, since the curves of a bipolar device are almost universally familiar to power circuit design engineers.

As indicated in Figures 2-1 and 2-2, the output characteristics of the power MOSFET and the bipolar transistor can be divided similarly into two basic regions. The figures also show the numerous and often confusing terms assigned to those regions. To avoid possible confusion, this section will refer to the MOSFET regions as the "on" (or "ohmic") and "active" regions and bipolar regions as the "saturation" and "active" regions.

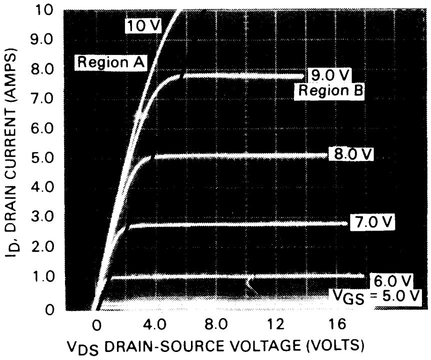


FIGURE 2-1 — I_D-V_{DS} TRANSFER CHARACTERISTICS OF MTP8N15. REGION A IS CALLED THE OHMIC, ON, CONSTANT RESISTANCE OR LINEAR REGION. REGION B IS CALLED THE ACTIVE, CONSTANT CURRENT, OR SATURATION REGION.

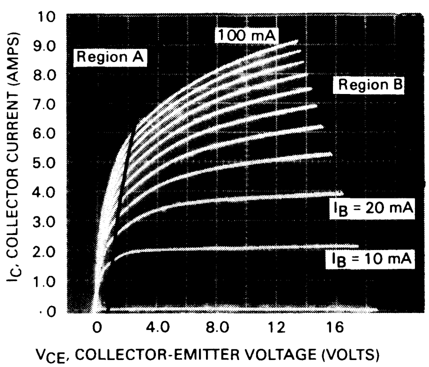


FIGURE 2-2 — I_C-V_{CE} TRANSFER CHARACTERISTICS OF MJE15030 (NPN, I_C CONTINUOUS = 8.0 A, V_{CEO} = 150 V) REGION A IS THE SATURATION REGION. REGION B IS THE LINEAR OR ACTIVE REGION.

One of the three obvious differences between Figures 2-1 and 2-2 is the family of curves for the power MOSFET is generated by changes in gate voltage and not by base current variations. A second difference is the slope of the curve in the bipolar saturation region is steeper than the slope in the ohmic region of the power MOSFET indicating that the on-resistance of the MOSFET is higher than the effective on-resistance of the bipolar.

The third major difference between the output characteristics is that in the active regions the slope of the bipolar curve is steeper than the slope of the TMOS curve, making the MOSFET a better constant current source. The limiting of I_D is due to pinch-off occurring in the MOSFET channel.

Basic MOSFET Parameters

On-Resistance

The on-resistance, or $r_{DS(on)}$, of a power MOSFET is an important figure of merit because it determines the amount of current the device can handle without excessive power dissipation. When switching the MOSFET from off to on, the drain-source resistance falls from a very high value to $r_{DS(on)}$, which is a relatively low value. To minimize $r_{DS(on)}$ the gate voltage should be large enough for a given drain current to maintain operation in the ohmic region. Data sheets usually include a graph, such as Figure 2-3, which relates this information. As Figure 2-4 indicates, increasing the gate voltage above 12 volts has a diminishing effect on lowering on-resistance (especially in high voltage devices) and increases the possibility of spurious gate-source voltage spikes exceeding the maximum gate voltage rating of 20 volts. Somewhat like driving a bipolar transistor deep into saturation, unnecessarily high gate voltages will increase turn-off time because of the excess charge stored in the input capacitance. All Motorola TMOS FETs will conduct the rated continuous drain current with a gate voltage of 10 volts.

As the drain current rises, especially above the continuous rating, the on-resistance also increases. Another important relationship, which is addressed later with the other temperature dependent parameters, is the effect that temperature has on the on-resistance. Increasing T_J and I_D both effect an increase in $r_{DS(on)}$ as shown in Figure 2-5.

Transconductance

Since the transconductance, or g_{FS}, denotes the gain of the MOSFET, much like beta represents the gain of the bipolar transistor, it is an important parameter when the device is operated in the active, or constant current, region. Defined as the ratio of the change in drain current corresponding to a change in gate voltage ($g_{FS} = dI_D/dV_{GS}$), the transconductance varies with operating conditions as seen in Figure 2-6. The value of g_{FS} is determined from the active portion of the V_{DS}-I_D transfer characteristics where a change in V_{DS} no longer significantly influences g_{FS}. Typically the transconductance rating is specified at half the rated continuous drain current and at a V_{DS} of 15 V.

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2-2

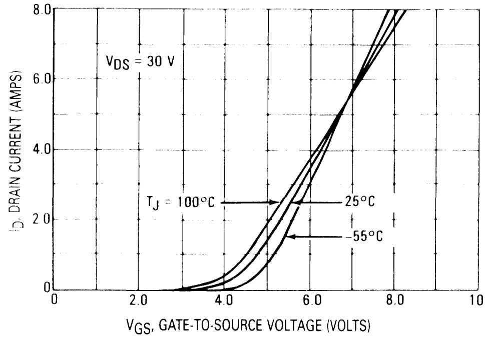


FIGURE 2-3 — TRANSFER CHARACTERISTICS OF MTP4N50

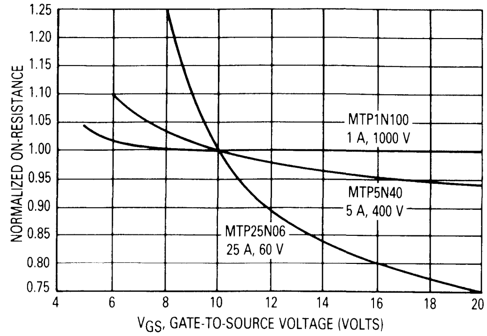


FIGURE 2-4 — THE EFFECT OF GATE-TO-SOURCE VOLTAGE ON ON-RESISTANCE VARIES WITH A DEVICE'S VOLTAGE RATING

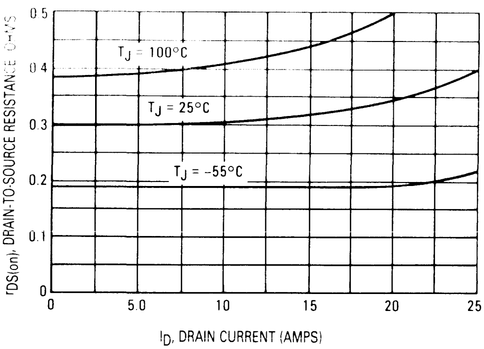


FIGURE 2-5 — VARIATION OF $r_{DS(on)}$ WITH DRAIN CURRENT AND TEMPERATURE FOR MTM15N45

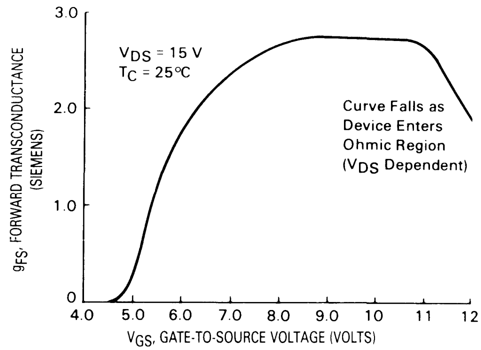


FIGURE 2-6 — SMALL-SIGNAL TRANSCONDUCTANCE versus V_{GS} OF MTP8N10

For designers interested only in switching the power MOSFET between the on and off states, the transconductance is often an unused parameter. Obviously when the device is switched fully on, the transistor will be operating in its ohmic region where the gate voltage will be high. In that region, a change in an already high gate voltage will do little to increase the drain current; therefore, g_{FS} is almost zero.

Threshold Voltage

Threshold Voltage, $V_{GS(th)}$, is the lowest gate voltage at which a specified small amount of drain current begins to flow. Motorola normally specifies $V_{GS(th)}$ at an I_D of one milliampere. Device designers can control the value of the threshold voltage and target $V_{GS(th)}$ to optimize device performance and practicality. A low threshold voltage is desired so the TMOS FET can be controlled by low voltage chips such as CMOS and TTL. A low value also speeds switching because less current needs to be transferred to charge the parasitic input capacitances. But the threshold voltage can be too low if noise can trigger the device. Also, a positive-going voltage transient on the drain can be coupled to the gate by the gate-to-drain parasitic capacitance and can cause spurious turn-on of a device with a low $V_{GS(th)}$.

Temperature Dependent Characteristics

$r_{DS(on)}$

Junction temperature variations and their effect on the on-resistance, $r_{DS(on)}$, should be considered when designing with power MOSFETs. Since $r_{DS(on)}$ varies approximately linearly with temperature, power MOSFETs can be assigned temperature coefficients that describe this relationship.

Figure 2-7 shows that the temperature coefficient of $r_{DS(on)}$ is greater for high voltage devices than for low voltage MOSFETs. A graph showing the variation of $r_{DS(on)}$ with junction temperature is shown on most data sheets.

Switching Speeds are Constant with Temperature

High junction temperatures emphasize one of the most desirable characteristics of the MOSFET, that of low dynamic or switching losses. In the bipolar transistor, temperature increases will increase switching times, causing greater dynamic losses. On the other hand, thermal variations have little effect on the switching speeds of the power MOSFET. These speeds depend on how rapidly the parasitic input capacitances can be charged and discharged. Since the magnitudes of these capacitances are essentially temperature invariant, so are the switching speeds. Therefore, as temperature increases, the dynamic losses in a MOSFET are low and remain constant, while in the bipolar transistors the switching losses are higher and increase with junction temperature.

Drain-To-Source Breakdown Voltage

The drain-to-source breakdown voltage is a function of the thickness and resistivity of a device's N-epitaxial region. Since that resistivity varies with temperature, so does $V_{(BR)DSS}$. As Figure 2-8 indicates, a 100°C rise in junction temperature causes a $V_{(BR)DSS}$ to increase by about 10%. However, it should also be remembered that the actual $V_{(BR)DSS}$ falls at the same rate as T_J decreases.

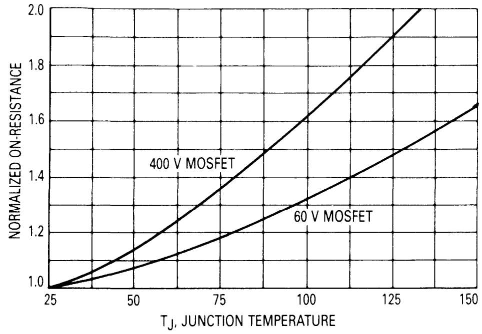


FIGURE 2-7 — THE INFLUENCE OF JUNCTION TEMPERATURE ON ON-RESISTANCE VARIES WITH BREAKDOWN VOLTAGE

Threshold Voltage

The gate voltage at which the MOSFET begins to conduct, the gate-threshold voltage, is temperature dependent. The variation with T_J is linear as shown on most data sheets. Having a negative temperature coefficient, the threshold voltage falls about 10% for each 45°C rise in the junction temperature.

Importance of $T_{J(max)}$ and Heat Sinking

Two of the packages that commonly house the TMOS die are the TO-220AB and the TO-204. The power ratings of these packages range from 40 to 250 watts depending on the die size and the type of materials used in construction. These ratings are nearly meaningless, however, unless some heat sinking is provided. Without heat sinking the TO-204 and the TO-220 can dissipate only about 4.0 and 2.0 watts respectively, regardless of the die size.

Because long term reliability decreases with increasing junction temperature, T_J should not exceed the maximum rating of 150°C. Steady-state operation above 150°C also invites abrupt and catastrophic failure if the transistor experiences additional transient thermal stresses. Excluding the possibility of thermal transients, operating below the rated junction temperature can enhance reliability. A $T_{J(max)}$ of 150°C is normally chosen as a safe compromise between long term reliability and maximum power dissipation.

In addition to increasing the reliability, proper heat sinking can reduce static losses in the power MOSFET by decreasing the on-resistance. $r_{DS(on)}$, with its positive temperature coefficient, can vary significantly with the quality of the heat sink. Good heat sinking will decrease the junction temperature, which further decreases $r_{DS(on)}$ and the static losses.

Drain-Source Diode

Inherent in most power MOSFETs, and all TMOS transistors, is a "parasitic" drain-source diode. Figure 2-9, the illustration of cross section of the TMOS die, shows the P-N junction formed by the P-well and the N-Epi layer. Because of its extensive junction area, the current ratings of the diode are the same as the MOSFET's continuous and pulsed current ratings. For the N-Channel TMOS FET shown in Figure 2-10, this diode is forward biased when the source is at a positive potential with respect to the drain. Since the diode may be an important circuit element, Motorola Designer's Data Sheets specify typical values of the forward on-voltage, forward turn-on and reverse recovery time. The forward characteristics of the drain-source diodes of several TMOS power MOSFETs are shown in Figure 2-11.

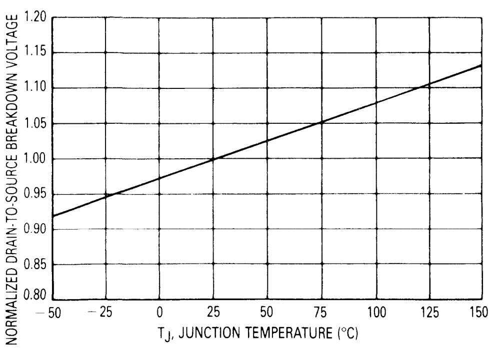


FIGURE 2-8 — TYPICAL VARIATION OF DRAIN-TO-SOURCE BREAKDOWN VOLTAGE WITH JUNCTION TEMPERATURE

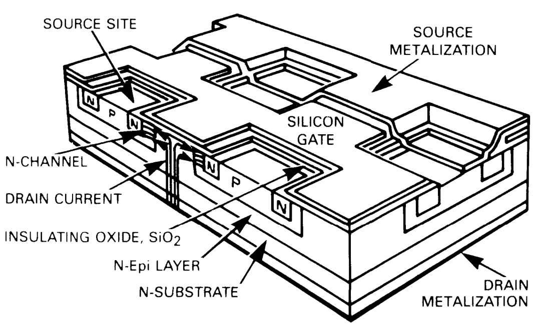


FIGURE 2-9 — CROSS SECTION OF TMOS CELL

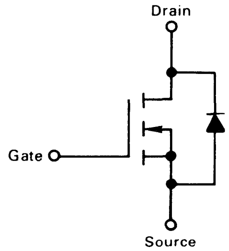


FIGURE 2-10 — N-CHANNEL POWER MOSFET SYMBOL INCLUDING DRAIN-SOURCE DIODE

Most rectifiers, a notable exception being the Schottky diode, exhibit a "reverse recovery" characteristic as depicted in Figure 2-12. When forward current flows in a standard diode, a carrier gradient is formed in the high resistivity side of the junction resulting in an apparent storage of charge. Upon sudden application of a reverse bias, the stored charge temporarily produces a negative current flow during the reverse recovery time, or t_{rr}, until the charge is depleted. The circuit conditions that influence t_{rr} and the stored charge are the forward current magnitude and the rate of change of current from the forward current magnitude to the reverse current peak. When tested under the same circuit conditions, the parasitic drain-source diode of a TMOS transistor has a t_{rr} similar to that of a fast recovery rectifier.

In many applications, the drain-source diode is never forward biased and does not influence circuit operation. However, in multi-transistor configurations, such as the totem pole network of Figure 2-13, the parasitic diodes play an important and useful role. Each transistor is protected from excessive flyback voltages, not by its own drain-source diode, but by the diode of the opposite transistor. As an illustration, assume that Q2 of Figure 2-13 is turned on, Q1 is off and current is flowing up from ground, through the load and into Q2. When Q2 turns off, current is diverted into the drain-source diode of Q1 which clamps the load's inductive kick to V+. By similar reasoning, one can see that D2 protects Q1 during its turn-off.

As a note of caution, it should be realized that diode recovery problems may arise when using MOSFETs in multiple transistor configurations. A treatment of the subject in Chapter 5 gives greater details.

TMOS power MOSFET intrinsic diodes also have forward recovery times, meaning that they do not instantaneously conduct when they are forward biased. However, since those times are so brief, typically less than 10 ns, their effect on circuit operation can almost always be ignored. Package, lead and wiring inductance are often at least as great a factor in limiting current rise time.

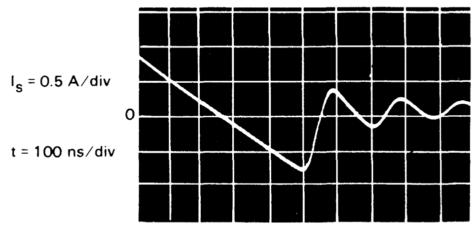


FIGURE 2-12 — REVERSE RECOVERY CHARACTERISTICS OF MTP15N15 DRAIN-SOURCE DIODE

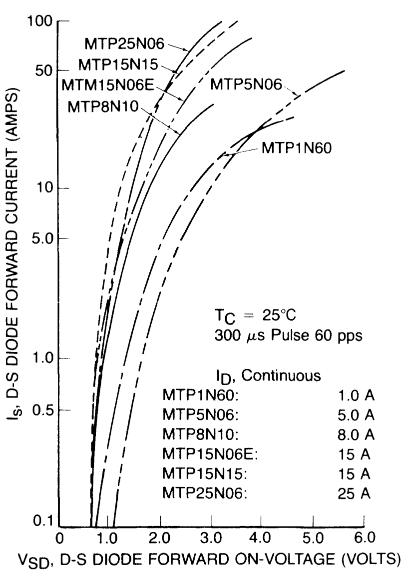


FIGURE 2-11 — FORWARD CHARACTERISTICS OF POWER MOSFETs D-S DIODES

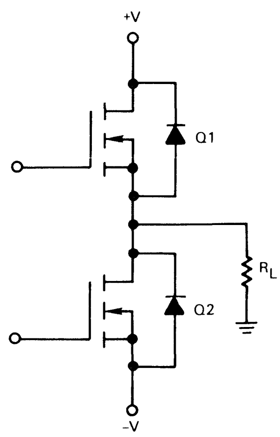


FIGURE 2-13 — TMOS TOTEM POLE NETWORK WITH INTEGRAL DRAIN-SOURCE DIODES

Chapter 3: Using the TMOS Power MOSFET Designer's Data Sheets

Motorola Designer's Data Sheets are user oriented guides that provide information concerning all the basic TMOS parameters and characteristics needed for successful circuit design. An example of the MTM4N45 data sheet is shown on the following pages. Helpful comments and explanations have been added to clarify some of the parameter definitions and device characteristics.

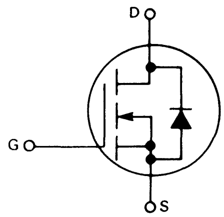
Designer's Data Sheet

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as line operated switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



MAXIMUM RATINGS
- Represent the extreme capabilities of the device.
- Not to be used as design condition.

V_{GS}
- Most Motorola TMOS power MOSFETs feature a rated $V_{GS(max)}$ of ± 20 V. Logic level devices are the exception.
- Exceeding $V_{gs(max)}$ may result in permanent device degradation.
- Limit gate voltage spikes with a small 20 V zener diode if required. (10 V for L[2] devices)

I_D — MAXIMUM CONTINUOUS DRAIN CURRENT
I_{DM} — MAXIMUM PULSED DRAIN CURRENT MAY BE LIMITED BY
- P_D
- $r_{DS(on)}$
- Wire size and metallization
- Combination of the above

P_D — MAXIMUM POWER AT A CASE TEMPERATURE OF 25°C
- Limit P_D and T_C so that $T_C + P_D \cdot R_{\theta JC} \leq T_{J(max)}$

$T_{J(max)}$ — MAXIMUM JUNCTION TEMPERATURE
- Reflects a minimum acceptable device service lifetime.
- Presently specified at 150°C for all Motorola power MOSFETs.
- Operating at conditions that guarantee a junction temperature less than $T_{J(max)}$ may enhance long term operating life.

MAXIMUM RATINGS

Rating	Symbol	MTM4N45 MTP4N45	MTM4N50 MTP4N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 4.0 10		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

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Designer's Data Sheets

Motorola TMOS Power FETs are characterized on "Designer's Data Sheets." These data sheets permit the design of most circuits entirely with the information provided. Key parameters are specified at elevated temperature to provide practical circuit designs.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM4N45/MTP4N45 MTM4N50/MTP4N50	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_C = 100°C		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc

$V_{(BR)DSS}$ (BV_{DSS})
- Maximum sustaining voltage
- No "negative resistance" region in the I-V characteristic
- Positive temperature coefficient, as shown in Figure 3-1

I_{DSS}
- Specified at 25°C and 100°C
- Gate must be terminated to source

I_{GSS}
- Specified at max. rated V_{GS}

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*				
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2.0 Adc) (I_D = 4.0 Adc) (I_D = 2.0 Adc, T_J = 100°C)	$V_{DS(on)}$	 — — —	 3.0 7.5 6.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$r_{DS(on)}$	—	1.5	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 2.0 A)	g_{FS}	1.5	—	mhos

$V_{GS(th)}$
- The gate voltage that must be applied to initiate conduction (Figure 3-3).
- Specified at 25°C and 100°C
- Negative temperature coefficient of about −6.7 mV/°C (Figure 3-4).

$V_{DS(on)}$, $r_{DS(on)}$
- $r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$
- Analogous to the $V_{CE(sat)}$ of a bipolar device
- Specified with a maximum V_{GS} of 10 V for Motorola TMOS power MOSFETs.
- Specified at 25°C and 100°C
- Positive temperature coefficient promotes current sharing when devices are paralleled.

g_{FS}
- The MOSFET "gain" parameter — analogous to h_{FE}
- Equal to the slope of the transfer characteristic (Figure 2-7).

$$g_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$$

- In current saturation region (Figure 3-3).

$$I_d = g_{FS}\,[V_{GS} - V_{GS(th)}]$$

- Relatively constant for $V_{GS(th)} < V_{GS} < V_{DS} + V_{GS(th)}$

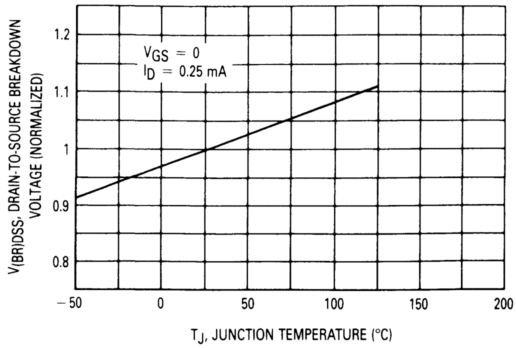


FIGURE 3-1 — NORMALIZED BREAKDOWN VOLTAGE versus TEMPERATURE

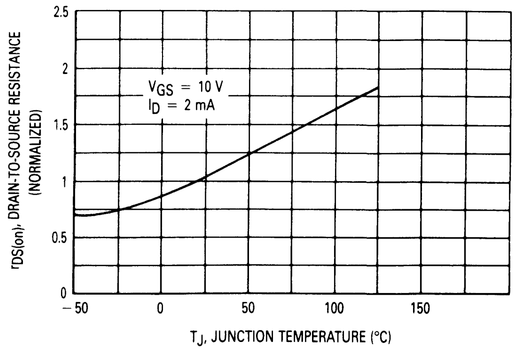


FIGURE 3-2 — NORMALIZED ON-RESISTANCE versus TEMPERATURE

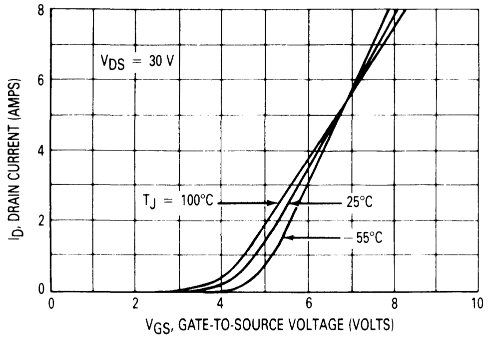


FIGURE 3-3 — TRANSFER CHARACTERISTICS

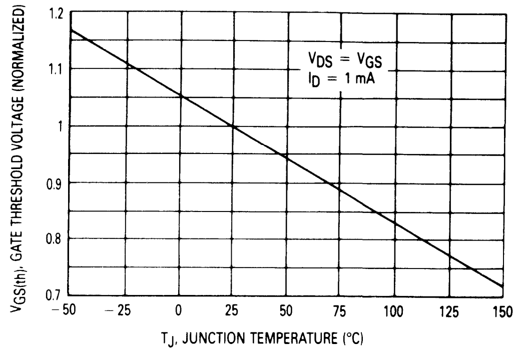


FIGURE 3-4 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Input Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, f = 1 MHz)	C_{iss}	—	1200	pF
Output Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, f = 1 MHz)	C_{oss}	—	300	pF
Reverse Transfer Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, f = 1 MHz)	C_{rss}	—	80	pF

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between the terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during the fabrication of the TMOS FET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets.

Specification of MOSFET capacitance at a V_{DS} of 25 V has become somewhat of a standard, so that information is provided in all TMOS data sheets.

(continued)

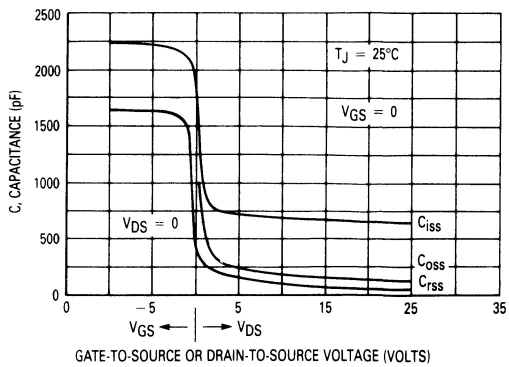


FIGURE 3-5

MOSFET CAPACITANCE (continued)

However, its usefulness in determining or comparing switching speeds or input or output capacitance is diminished since the magnitude of the capacitances vary significantly during the switching transition. Curves showing capacitance versus voltage are more indicative of device performance since the curves clearly show the capacitance variation.

The capacitance curves shown in Figure 3-5 are an extension of those originally published in data sheets. The portion of the graph to the right of zero is equivalent to the traditional representation. The additional section to the left of zero gives an indication of the input capacitance when the MOSFET is "on" or entering into its "on" state.

A graph of gate charge versus gate voltage is another and often more descriptive means of relating the magnitude of the input impedance.

In driving a MOSFET, the input capacitance, C_{iss} is an important parameter. This capacitance must be charged and discharged by the drive circuit to effect the switching function. The impedance of the drive source strongly affects the switching speed of a MOSFET. The lower the driving source impedance, the faster the switching speeds. Temperature variations have little effect on the device capacitances; therefore, switching times are affected very little by temperature variations.

SWITCHING CHARACTERISTICS* ($T_J = 100°C$)

Characteristic	Symbol	Min	Max	Unit
Turn-On Delay Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	t_r	—	100	ns
Turn-Off Delay Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	$t_{d(off)}$	—	200	ns
Fall Time (V_{DS} = 25 V, I_D = 2.0 A, R_{gen} = 50 ohms)	t_f	—	100	ns

Switching Characteristics

MOSFET switching speeds are very fast, relative to comparably sized bipolar transistors. Since they are majority carrier devices, there is no storage time associated with the turn-off time; consequently, the switching waveform components are associated with the charging and discharging of the interelectrode capacitances. Driving a MOSFET through a switching cycle involves driving these non-linear capacitances. Switching times, therefore, will strongly depend on the impedances of the driving source and drain load. Maximum limits are specified at elevated temperature.

Motorola normally uses a terminated, 50 Ω generator in the gate drive to specify switching speeds. Note that the generator and termination impedance combine to make a 25 Ω gate drive impedance. Using this gate drive as a standard helps facilitate correlation of test results. Typical switching times for various gate drive impedances, are shown in Figure 3-8.

For Resistive Switching:

- During $t_{d(on)}$ — The drive circuit charges C_{iss} to $V_{GS(th)}$. No drain current flows; V_{DS} remains essentially at V_{DD}.
- During t_r — C_{iss} is charged by the drive circuit to $V_{GS(on)}$. C_{oss} discharges from V_{DD} to approach $V_{DS(on)}$ and I_D increases from zero, approaching its maximum. As V_{DS} approaches $V_{DS(on)}$, the rapid rise of C_{oss} at low drain voltages delays the rise of I_D, likewise the increase of C_{iss} inhibits the rise of V_{GS} through the drive impedance.
- During $t_{d(off)}$ — C_{iss} begins to discharge through the gate circuit impedance. The transistor turns off and the drain supply charges C_{oss} through the load. The initial rise of V_{DS} is slowed by the high value of C_{oss} at low drain voltages.
- During t_f — C_{oss} diminishes rapidly as the drain voltage rises. Virtually no additional charge is required to be sourced by the drain supply; V_{DS} rises rapidly to V_{DD} (and beyond if inductance is present in the load).

Resistive Switching

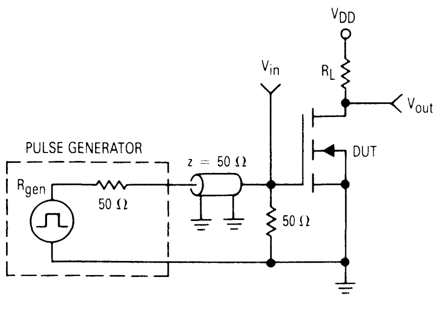


FIGURE 3-6 — SWITCHING TEST CIRCUIT

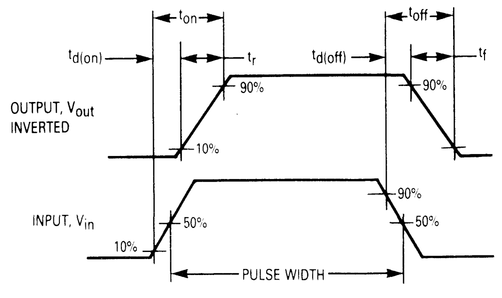


FIGURE 3-7 — SWITCHING WAVEFORMS

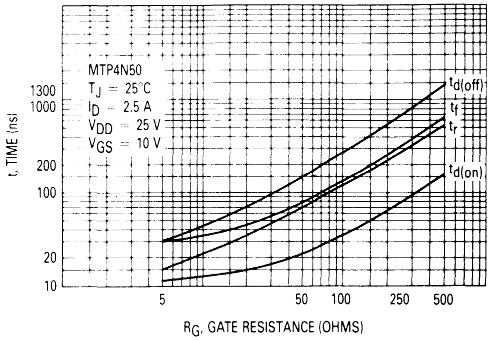


FIGURE 3-8

GATE CHARGE CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 4 Amps, V_{GS} = 10 V)	Q_g	27 (typ)	32	nC
Gate-Source Charge		Q_{gs}	17 (typ)	—	
Gate-Drain Charge		Q_{gd}	10 (typ)	—	

Gate Charge Characteristics

Fundamentally, the gate charge versus gate-to-source voltage curves are used to determine the amount of charge, defined as Q_g, required to bring C_{iss} from zero volts to 10 V. Typically, the maximum rating is specified at an I_D equal to the device's continuous rating at 25°C and at a supply voltage of 80% of maximum rated V_{DS}. Gate charge is essentially independent of load current, but it does vary with supply voltage.

In addition to typical and maximum values of Q_g, the data sheets also specify typical values of Q_{gd} and Q_{gs}. Q_{gd} is the charge required by C_{rss} (C_{gd}) during the fall of V_{DS}. This occurs during the plateau region of Figure 3-9. Q_{gs} refers to the total charge required by C_{iss} during the two intervals characterized by ramping up of V_{GS} before and after the plateau. During the first interval most of this charge flows into C_{gs} but during the second interval C_{rss} takes on the majority of the charge. Hence, the term "Q_{gs}" is somewhat of a misnomer.

A substantial amount of other data may be extracted from the curve. Estimation of the required average gate current for a given switching speed, energy transferred to the gate, and magnitude of the input capacitance are some of its other uses.

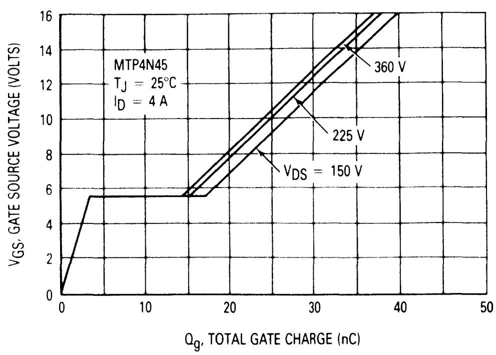


FIGURE 3-9 — Q_g TOTAL GATE CHARGE (nC)

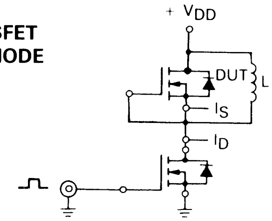
SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 4.0 A V_{GS} = 0	V_{SD}	1.1	Vdc
Reverse Recovery Time		t_{rr}	420	ns
Forward turn-on time is primarily limited by parasitic package and lead inductance.				

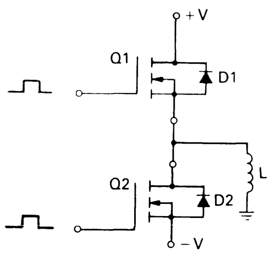
*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

THE POWER MOSFET SOURCE-DRAIN DIODE

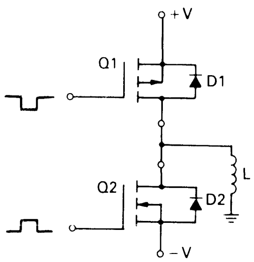
- An integral feature of all power MOSFET structures.
- Reverse recovery times are comparable with those of fast recovery rectifiers.
- Rated current equal to that of the MOSFET
- May be used as a commutator in complementary totem-pole or H-bridge configurations with inductive loads, or in a "Synchronous Rectifier" mode.



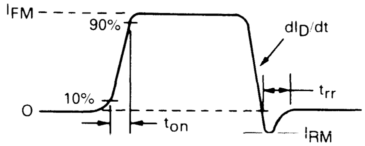
EQUIVALENT TEST CIRCUIT



TOTEM-POLE
N-CHANNEL



COMPLEMENTARY
P-CHANNEL/N-CHANNEL



DUT WAVEFORM

DURING TURN-OFF OF Q1, D2 PROTECTS Q1; LIKEWISE
DURING TURN-OFF OF Q2, D1 PROTECTS Q2

TMOS power MOSFET intrinsic diodes also have forward recovery times, meaning that they do not instantaneously conduct when they are forward biased. However, since those times are so brief, typically less than 10 ns, their effect on circuit operation can almost always be ignored. Package, lead and wiring inductance are often at least as great a factor in limiting current rise time.

FIGURE 3-10 — SOURCE-TO-DRAIN DIODE TEST CIRCUIT AND WAVEFORM

SAFE OPERATING AREA INFORMATION

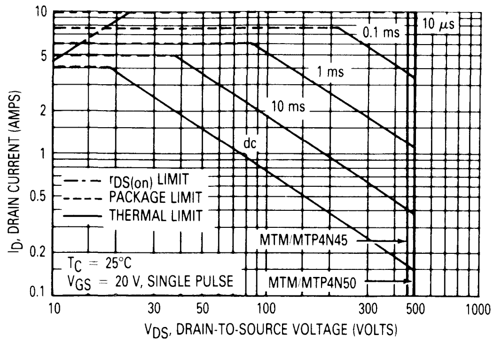


FIGURE 3-11 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

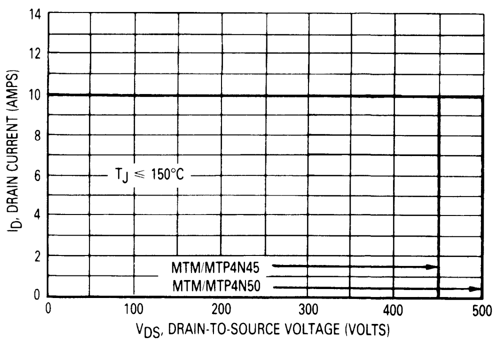


FIGURE 3-12 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

THERMAL RESPONSE

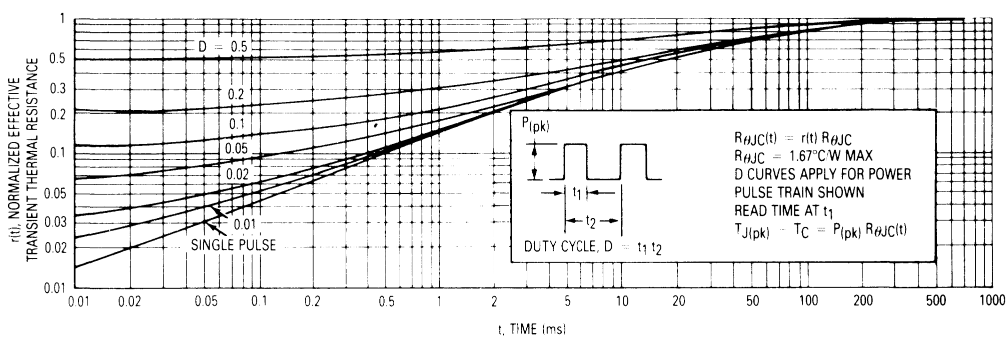


FIGURE 3-13 — MTM4N45/MTM4N50

Guaranteed Safe Operating Area

FBSOA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569. "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SSOA

The switching safe operating area in Figure 3-12 is the boundary that the load line may traverse without incurring damage to the device. The fundamental limits are the maximum rated peak drain current I_{DM}, the minimum drain to source breakdown voltage $V_{(BR)DSS}$ and the maximum rated junction temperature. The boundaries are applicable for both turn-on and turn-off of the devices for rise and fall times of less than one microsecond.

2

2-3

Chapter 4: Design Considerations in Using Power MOSFETs

Protecting the Power MOSFET

Safe Operating Areas

To provide the designer with Safe Operating Area information for the various modes of operation the TMOS transistor may encounter, two different Safe Operating Areas are defined on the TMOS data sheets: the Forward Biased Safe Operating Area, or FBSOA (often referred to as simply SOA), and the Switching SOA or SSOA. The SSOA curves of MOSFETs describe the voltage and current limitations during turn-on and turn-off and are normally used in the same manner as the RBSOA curves of bipolar transistors.

FBSOA:

An FBSOA curve defines the maximum drain voltage and currents that a device can safely handle when forward biased, or while it is on or being turned on. Of the four limits dictated by the boundaries of the FBSOA curve, the most unforgiving is the maximum drain-source voltage rating which is indicated by boundary A in Figure 4-1. If this rating is exceeded, even momentarily, the device can be damaged permanently. Thus, precautions should be taken if there may be transients in the drain supply voltage.

Maximum allowable drain current is time or pulse-width dependent and defines the second boundary of the FBSOA curve, represented by Line D. The limit is determined by the bonding wire diameter, the size of the source bonding pad, device characteristics and thermal resistance. Even though MOSFETs show rugged overcurrent capabilities, devices should not conduct more than their rated drain current for a given pulse duration. This includes transient currents such as the high in-rush current drawn by a cold incandescent lamp or the reverse recovery current required by a diode.

The third boundary, Line B is fixed by the drain-to-source on-resistance and limits the current at low drain-source voltages. Simply a manifestation of Ohm's Law, the limitation states that with a given on-resistance, current is limited by the applied voltage. The boundary does not describe a linear relationship, however, because the on-resistance increases gradually with increasing current.

The fourth limit, shown as Line C in Figure 4-1, is set by the package thermal limit. This power limited portion of the FBSOA curve is generated from the device thermal response curve, maximum allowable junction temperature and maximum $R_{\theta JC}$ rating. Operation inside this curve insures that the maximum junction temperature does not exceed the 150°C maximum rating.

Since the transient thermal resistance decreases dramatically for shorter pulse durations, the peak power handling capability increases accordingly. For example, Figure 4-2 shows that at 100 μs the normalized single pulse transient resistance of the MTM8N40 is 0.033. Multiplication by $R_{\theta JC}$ (0.033 x 0.83°C/W) results in the effective thermal impedance for a single 100 μs pulse. From the definition of thermal resistance $\left(R_{\theta JC} = \frac{T_J - T_C}{P_D}\right)$ the magnitude of the power pulse that coincides with a

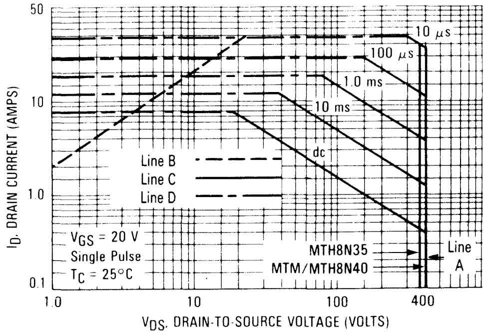


FIGURE 4-1 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA OF THE MTM8N40

T_J of 150°C and a T_C of 25°C is easily determined. In this case, (0.033 x 0.83°C/W $= \frac{150 - 25°C}{P_D}$), P_D is 4564 W. Therefore, at a V_{DS} of 200 V, the MTM8N40 can conduct about 23 A during a 100 μs pulse without exceeding the $T_{J(max)}$ rating of 150°C.

Normally the portion of the FBSOA curves that is determined by the package thermal limit is only of interest to designers who foresee a condition of simultaneous high voltage and high current for periods greater than 10 μs. This situation can occur in linear applications or in switching applications that experience a fault condition such as a shorted load. For those applications the information contained in Figure 4-1 is incomplete since the data is based on single pulse testing at a case temperature of 25°C. For multiple pulses and case temperatures other than 25°C, the maximum allowable power dissipation can be computed as shown in AN569, "Transient Thermal Resistance General Data And Its Use."

To a large extent, thermal limitations determine the SOA boundaries for MOSFETs used in linear applications. The maximum allowable junction temperature $T_{J(max)}$ also affects the pulsed current ratings applicable when the MOSFET is used as a switch. With respect to current ratings, MOSFETs are more like rectifiers than bipolar transistors in that their peak current ratings are not gain limited, but thermally limited. Since $r_{DS(on)}$, on-state power dissipation, switching losses, pulse width, duty cycle and junction to ambient thermal impedance all influence T_J, they also affect the maximum allowable pulsed drain current.

In switching applications the total power dissipation is comprised of switching losses and on-state losses. At low frequencies, the MOSFETs switching losses are small enough to ignore. However, as frequency increases the losses eventually become significant and force an increase in T_J. The break point between what is considered low and high frequencies depends on the gate drive impedance. With a low impedance gate-drive, switching losses are small below 40 to 50 kHz.

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2-4

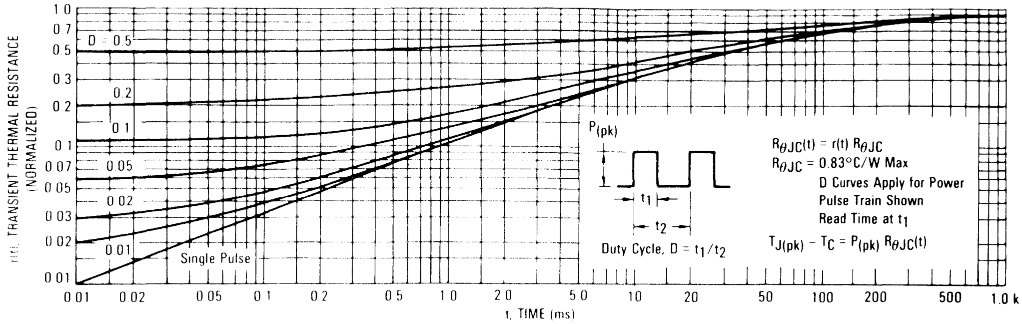

FIGURE 4-2 — THERMAL RESPONSE CURVE OF THE MTM8N40

Since the magnitude of the MOSFET capacitances and, therefore, switching speeds are nearly constant as T_J varies, power MOSFET switching losses are nearly temperature invarient. Without the additional complexity of temperature dependence, losses during the relatively high dissipation turn-on and turn-off intervals are easily modeled and estimated. These techniques are also shown in Motorola Application Note AN569.

Because on-state losses are often the bulk of the total power dissipation, they greatly affect the MOSFET's maximum allowable pulsed current capability. The computation of these losses is somewhat involved due to the variation of $r_{DS(on)}$ with temperature and drain current. After computing the heating component of the drain current (RMS value), an iterative technique is used to determine the on-state power dissipation. The following example illustrates how on-state losses and junction temperature can be determined.

Assume the drain current waveform of an MTM8N40 is trapezoidal with the current rising from 8.0 A to 16 A in 25 μs. The duty cycle is 50% and the frequency is 20 kHz. Heat sinking will be provided to keep the case temperature at 80°C. From Figure 4-2, the normalized transient thermal impedance for a 25 μs pulse and 50% duty cycle is 0.5, yielding an effective thermal impedance of 0.415°C/W. [r(t) x $R_{\theta JC}$ = 0.5 x 0.83°C/W].

Before proceeding, the on-resistance and the RMS value of the I_D waveform must be determined. Since $r_{DS(on)}$ is temperature dependent, the junction temperature must be roughly estimated. A T_J of 110°C seems appropriate in this case. From Figure 4-3, $r_{DS(on)}$ at 110°C is 1.02 Ω.

This value of $r_{DS(on)}$ is derived from a typical curve and does not represent a worst case value. To obtain a worst case estimate, the ratio between the maximum rated $r_{DS(on)}$ and the typical $r_{DS(on)}$ under the same operating conditions can be used as a multiplier. In this situation, an $r_{DS(on)}$ maximum of 0.55 ohms is specified at an I_D of 4.0 A and a T_C of 25°C. At these same conditions, $r_{DS(on)}$ is typically at 0.45 ohms (Figure 4-3). Assuming the ratio between typical and worst case values remains

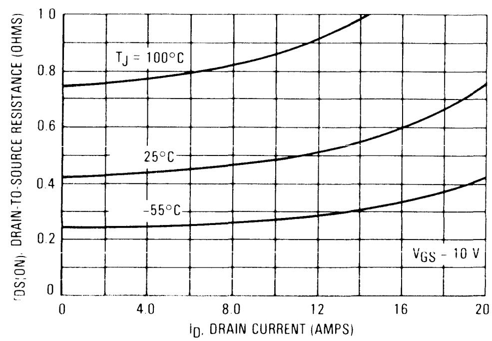

FIGURE 4-3 — ON-RESISTANCE versus DRAIN CURRENT FOR THE MTM8N40

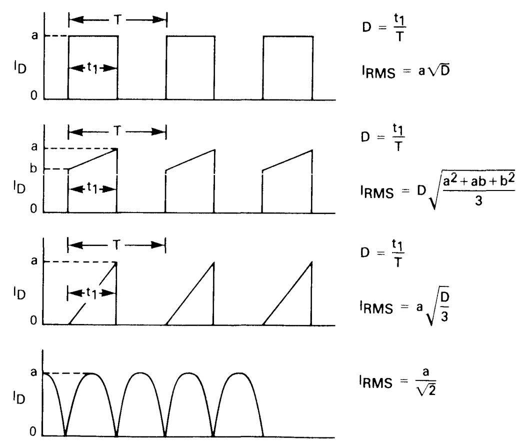

FIGURE 4-4 — RMS VALUES OF SOME COMMON CURRENT WAFEFORMS

fairly constant, the multiplier is 1.22, $\left(\frac{r_{DS(on)}\ MAX}{r_{DS(on)}\ TYP} = \frac{0.55}{0.45}\right)$. Therefore, the worst case $r_{DS(on)}$ at 12 A, 110°C is approximately 1.22 x 1.02 ohms, or 1.24 ohms.

From the trapezoid waveform in Figure 4-4:

$$
\begin{aligned}
I_{RMS} &= D\sqrt{\frac{a^2 + ab + b^2}{3}} \\
&= 0.5\sqrt{\frac{8^2 + 8 \cdot 16 + 16^2}{3}} \\
&= 6.11\ A
\end{aligned}
$$

$$
\begin{aligned}
\text{and } P_D &= I^2_{RMS}\, r_{DS(on)} \\
&= (6.11)^2\ 1.24 \\
&= 46.3\ W
\end{aligned}
$$

If switching losses are significant, they should be included at this step. Proceeding with the computation of T_J,

$$
\begin{aligned}
\Delta T_{JC} &= P_D\, R_{\theta JC} \\
&= (46.3)\ (0.415) = 19.2°C \\
T_J &= T_C + \Delta T_{JC} \\
&= 80 + 19.2°C = 99.2°C
\end{aligned}
$$

then the calculated T_J of 99.2°C replaces the original 110°C estimate and $r_{DS(on)}$, P_D and T_J are recomputed. The initial guess was close, and 97.3°C is the final solution. Therefore the transistor is operating within its thermal limitations and its current handling capabilities.

SSOA:

Switching Safe Operating Area defines the MOSFETs voltage and current limitations during switching transitions. Although an SSOA curve also outlines turn-on boundaries, it is normally used as a turn-off SOA. As such, it is the MOSFET equivalent of the Reverse Biased SOA (RBSOA) of bipolars.

Like RBSOA ratings, turn-off SOA curves are generated by observing device performance as it switches a clamped inductive load. An inductive load is used because it causes the greatest turn-off stress, but it must be clamped so as not to avalanche the transistor with an uncontrolled drain-source "flyback voltage." Switching speeds, which directly determine crossover times and switching losses, also influence the turn-off SOA.

As shown in Figure 4-5, the SSOA curve of the MOSFET is bounded by its maximum pulsed drain current, I_{DM}, and the maximum drain-source voltage, V_{DSS}, as long as switching times are less than 1.0 μs. If MOSFETs are operated within their I_{DM}, V_{DSS} and $T_{J(max)}$ ratings, their SSOA curves guarantee that a secondary breakdown derating is unnecessary.

Drain-Source Overvoltage Protection

The most common cause of failure in a power MOSFET is due to an excursion across an SOA boundary. A good portion of these failures are a result of exceeding the maximum rated drain-source voltage, $V_{(BR)DSS}$. Drain voltage transients caused by switching high currents through load or stray inductances can force V_{DS} to exceed $V_{(BR)DSS}$ and may contain enough energy to destroy the device if it begins to avalanche. Transients on the drain supply voltage can also destroy the power MOSFET.

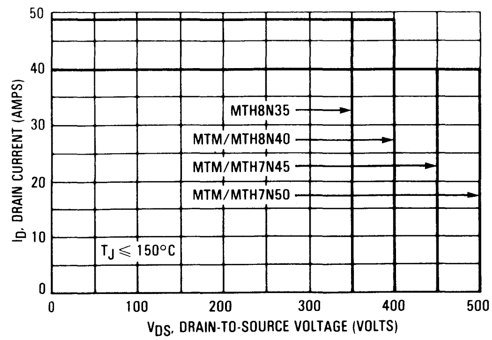

FIGURE 4-5 — MAXIMUM RATED SWITCHING SAFE OPERATING ARE OF THE MTM8N40

Fortunately, if there is any danger of these destructive transients, the solutions to the problems are fairly simple. Figure 4-6 illustrates a FET switching an inductive load in a circuit which provides no protection from excessive flyback voltages. The accompanying waveform depicts the turn-off voltage transient due to the load and the parasitic lead and wiring inductance. The MTM20N10 experiences the unrecommended avalance condition for about 300 ns at its breakdown voltage of 122 volts.

One of the simplest methods of protecting devices from flyback voltages is to place a clamping diode across the inductive load. Using this method, the diode will clamp most, but not all, of the voltage transient. V_{DS} will still overshoot V_{DD} by the sum of the effects of the forward recovery characteristic of the diode, the diode lead inductance and the parasitic series inductances as shown in Figure 4-7.

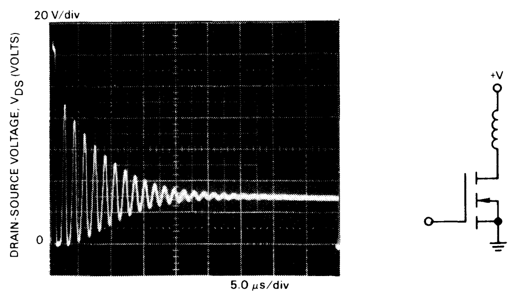

FIGURE 4-6 — V_{DS} TRANSIENT DUE TO UNCLAMPED INDUCTIVE LOAD

If the series resistance of the load is small compared to its inductance, a simple diode clamp may allow current to circulate through the load-diode loop for a significant amount of time after the MOSFET is turned off. When this lingering current is unacceptable, a resistor can be inserted in series with the diode at the expense of increasing the peak flyback voltage seen at the drain.

2

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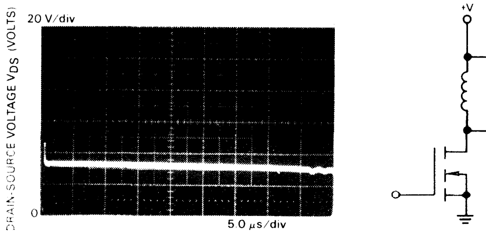

FIGURE 4-7 — V_{DS} TRANSIENT WITH CLAMPING DIODE

Protecting the drain-source from voltage transients with a zener diode, which is a wide band device, is another simple and effective solution. Except for the effects of the lead and wiring inductances and the virtually negligible time required to avalanche, the zener will clip the voltage transient at its breakdown voltage. A transient with a slow dv_{DS}/dt will be clipped completely while a transient with a rapid dv/dt might momentarily exceed the zener breakdown voltage. These effects are shown in Figure 4-8. Even though it is a very simple remedy, the zener diode is one of the most effective means of transient suppression. Obviously, the power rating of the zener should be scaled so that the clipped energy is safely dissipated.

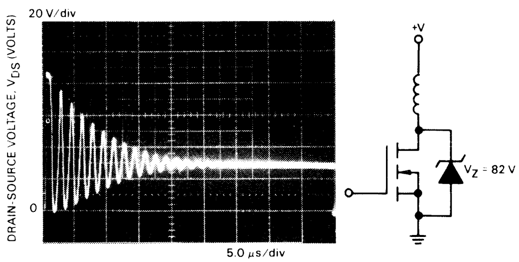

FIGURE 4-8 — V_{DS} TRANSIENT WITH ZENER CLAMP

Figure 4-9 shows an RC clamp network that suppresses flyback voltages greater than the potential across the capacitor. Sized to sustain a nearly constant voltage during the entire switch cycle, the capacitor absorbs energy only during transients and dumps that energy into the resistance during the remaining portion of the cycle. Component values may be computed by considering the power that the RC clamp network must absorb. From the power and the desired clamp voltage, the resistance can be sized. Finally, the magnitude of the capacitance may be determined by relating the RC time constant to the period of the waveform.

As an example, a similar circuit has the following characteristics:

L = 10 μH
i = 3.0 A (load current just before turn-off
f = 25 kHz
V_C = 60 V (desired clamp voltage)

The power to be absorbed by the clamp network is:

$$P = 1/2\ Li^2 \times f = 1.125\ \text{W}$$

The component values can be determined:

$$\frac{V_C^2}{P} = R = 3.2\text{K} \approx 3.3\text{K}$$

$$\text{Let } \tau = RC = 5.0 \div f = 200\ \mu s$$

$$C = 0.061\ \mu F \approx 0.05\ \mu F$$

While this is a common and efficient cricuit, the switching speeds of MOSFETs may produce transients that are too rapid to be attentuated by this method. If the flyback voltage reaches its peak during the first 50 ns, the effectiveness of the circuit will be undermined due to the forward recovery characteristic of the clamp diode and any stray circuit inductance. It may be prudent in these cases to include a zener with a breakdown voltage slightly higher than the clamp voltage. When placed directly across the drain and source terminals, the lead lengths are short enough and the zener is fast enough to catch most transients. Since the zener's only purpose is to clip the initial flyback peak and not to absorb the entire energy stored in the inductor, the zener power rating can be smaller than that needed when one is used as the sole clamping element.

A fourth way to protect power MOSFETs from large drain-source voltage transients is to use an RC snubber network like that of Figure 4-10. Although it effectively reduces the peak drain voltage, the snubber network is not as efficient as a true clamping scheme. Whereas a clamping network only dissipates energy during the transient, the RC snubber also absorbs energy during portions of the switching cycle that are not overstressing the transistor. This configuration also slows turn-on due to the additional drain-source capacitance that must be discharged.

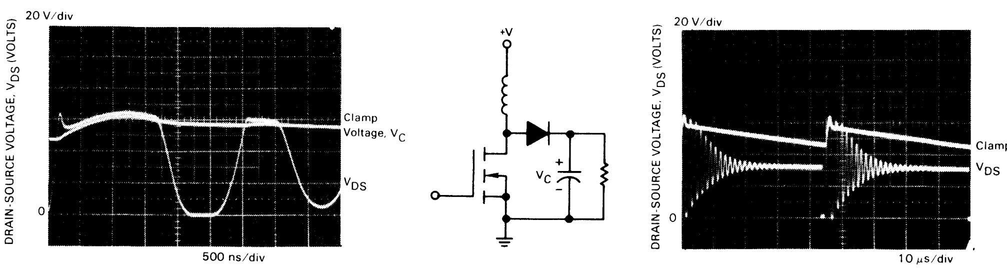

FIGURE 4-9 — V_{DS} TRANSIENT AND RC CLAMP VOLTAGE WITH RC CLAMP NETWORK

No matter which scheme is used, very rapid inductive turn-off can cause transients during the first tens of nanoseconds that may be overlooked unless a wideband oscilloscope (B.W. ≥ 200 MHz) is used to observe the V_{DS} waveform.

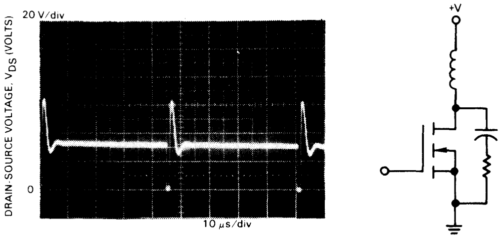

FIGURE 4-10 — V_{DS} TRANSIENT WITH RC SNUBBER

Package and Lead Inductance Considerations

The drain and source parasitic package inductance can influence the magnitude of V_{DS} during rapid switching of very large currents. In Figure 4-11, the drain and source package inductance has been combined and placed in the source because that wirebond and lead length accounts for the bulk of the inductance. The magnitudes of L_S in the TO-204, (TO-3) and the TO-220 packages are around 12 and 8 nH, which are large enough to produce appreciable voltage during a very rapid rate of change in drain current. The polarity of the induced voltage is such that the drain-source voltage appearing at the chip is greater than that appearing at the device terminals.

As an example, assume that an MTP25N06 is turned off in 50 ns after conducting 50 A. A di/dt of this magnitude will produce about 8.0 volts across the parasitic package inductance (v = L di/dt = 8.0 nH 50 A/50 ns). If the drain-source voltage at the terminals is 50 V, then V_{DS} at the die is 58 volts.

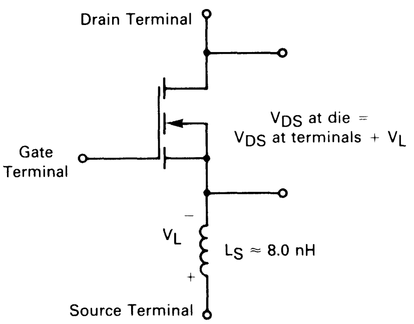

FIGURE 4-11 — VERY RAPID TURN-OFF INCREASES DRAIN-SOURCE VOLTAGE STRESS

Although all power MOSFETs experience some internally generated voltages during rapid switching, peak di/dt's are usually not extreme and the associated voltages are generally small. However, the current ratings of power MOSFETs recently have increased rapidly and, consequently, their maximum di/dt capabilities have also risen. The MTM60N06, with its pulsed current rating of 300 A, falls into the category of such a device. The very large di/dt capabilities that accompany these current ratings can produce significant V_{DS} stress in addition to that observed at the drain-source terminals.

To assure that the peak V_{DS} at the chip does not exceed the maximum V_{DSS} rating of the device, the following equation can be used:

$$V_{DS(max)} = V_{(BR)DSS} - L(di/dt)$$

where $V_{DS(max)}$ is the maximum allowable voltage appearing across the drain-source terminals, $V_{(BR)DSS}$ is the maximum device rating, L is the parasitic source inductance and di/dt is the rate of change in I_D coincident with $V_{DS(max)}$.

Voltages appearing across the package source inductance also affect the magnitude of the gate-source voltage at the chip and are of such polarity that they slow both the turn-on and turn-off transitions. If large currents are being switched, the parasitic package inductance is large enough to be the factor that limits the MOSFET's switching speeds.

Except for circuits that produce very large di/dt's, the proceeding discussion of package inductance is of academic interest only. However, wiring inductance is often much larger than the package inductance and its effects are proportionately greater. Therefore, the above considerations may become very practical problems in applications in which the di/dt's are not extreme. The quality of the circuit layout dictates the degree of concern.

Avalanche and dv/dt Limitations of Power MOSFETs

Until recently a MOSFET's maximum drain-to-source voltage specification prohibited even instantaneous excursions beyond that voltage, since the first power MOSFETs were never intended to be operated in avalanche. As is still the case with most bipolar transistors, capability was simply not specified. Some devices happened to be quite rugged, while others were not. Now it is known that a power MOSFET can be constructed to sustain substantial currents in avalanche at elevated junction temperatures, so newly designed MOSFETs are replacing the original devices. "Ruggedized" is the term being used to refer to devices that carry some form of rating to define avalanche capability.

The MOSFET's ability to withstand rapid changes in drain-to-source voltage, especially during reverse recovery of the MOSFET's intrinsic diode, is another issue that has received much attention lately. In this case the first devices were very rugged except for the case of diode recovery. Again the latest devices show performance improvements and carry ratings to inform designers of their new strength.

Because of the interest in avalanche and dv/dt issues and their importance, a discussion of these topics is provided in Chapter 5, "Avalanche and dv/dt Limitations of the Power MOSFET."

Protecting the Gate

The gate of the MOSFET, which is electrically isolated from the rest of the die by a very thin layer of SiO_2, may be damaged if the power MOSFET is handled or installed improperly. Exceeding the 20 V maximum gate-to-source voltage rating, $V_{GS(max)}$, can rupture the gate insulation and destroy the FET. TMOS FETs are not nearly as susceptible as CMOS devices to damage due to static discharge because the input capacitances of power MOSFETs are much larger and absorb more energy before being charged to the gate breakdown voltage. However, once breakdown begins, there is enough energy stored in the gate-source capacitance to ensure the complete perforation of the gate oxide. To avoid the possibility of device failure caused by static discharge, precautions similar to those taken with small-signal MOSFET and CMOS devices apply to power MOSFETs.

When shipping, the devices should be transported only in antistatic bags or conductive foam. Upon removal from the packaging, careful handling procedures should be adhered to. Those handling the devices should wear grounding straps and devices not in the antistatic packaging should be kept in metal tote bins. MOSFETs should be handled by the case and not by the leads, and when testing the device, all leads should make good electrical contact before voltage is applied. As a final note, when placing the FET into the system it is designed for, soldering should be done with a grounded iron.

The gate of the power MOSFET could still be in danger after the device is placed in the intended circuit. If the gate may see voltage transients which exceed $V_{GS(max)}$, the circuit designer should place a 20 V zener across the gate and source terminals to clamp any potentially destructive spikes. Using a resistor to keep the gate-to-source impedance low also helps damp transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

Chapter 5: Avalanche and dv/dt Limitations of the Power MOSFET

The power MOSFET's ability to withstand voltage and current transients inside and outside published safe operating areas is often of concern to design engineers. Since anticipating every possible fault condition that can occur in the field is very difficult, the use of a device that has some tolerance to transients is highly desirable.

By nature the power MOSFET is resistant to failure in certain modes. Its ability to withstand overcurrent stresses is a good example of one of its strengths. However, ruggedness in other modes is not a given, and device design and processing must target those types of failures if a MOSFET is to be robust in those modes, too.

Motorola's development of the E-FET, a "ruggedized" device sometimes referred to as TMOS IV, is a significant step toward extending the MOSFET's ruggedness to include several of the most common fault induced stresses. Designed-in ruggedness, combined with the MOSFET's ability to withstand forward bias stress, make the E-FET a very fault tolerant device in all major areas of concern, including what has been called the "commutating dv/dt" mode. The issues surrounding these significant modes of stress are discussed in detail below.

The Power MOSFET in Drain-to-Source Avalanche

The MOSFET's unique capability of high speed switching can lead to stresses that are not encountered with slower devices. Often gate drive circuits are designed for very fast switching speeds to lower switching times and increase circuit efficiency. These speeds may be so fast that the inductive kick occurring at turn off produces an extremely rapid rise in the drain-to-source voltage — perhaps so rapid that parasitic circuit elements and turn-on times undermine a protection clamp's ability to respond in time to protect the MOSFET. Such parasitics that diminish response times include the inductance in the wiring, leads, and packages. Forward recovery time of protection diodes may also delay response time.

Voltage transients of this type are usually brief, lasting only until the voltage clamp or snubber reacts. Nevertheless, for a short time the MOSFET is forced to conduct what may be a high avalanche current. Although the total energy that the device sees in breakdown is fairly small, failures may occur since ruggedness in avalanche is a strong function of the peak avalanche current. At high switching speeds such brief transients are a common source of overvoltage spikes.

Another cause of overvoltage transients is voltage spiking on the drain supply voltage. When this occurs, the peak magnitude of the associated avalanche current is difficult to predict since it depends on the nature of the transient. Pulse duration and energy may vary widely; consequently, the MOSFET's ability to survive high avalanche currents lasting for extended pulse widths is important.

The recent development of the E-FET has made available MOSFETs with the ability to survive both types of overvoltage transients. These new devices are sufficiently rugged to carry ratings that guarantee an avalanche current capability for the two types of overvoltage transients discussed above.

An energy rating alone is a poor indication of a device's ability to survive overvoltage transients. Manufacturers can easily fabricate high energy values by carefully choosing test conditions that allow dissipation of energy over a long pulse width. An extreme example is the 12 A, 60 V MTP3055E that can dissipate 75 joules if allowed to conduct 1 A in avalanche for 1 second. However, one of these devices is likely to fail with very little energy dissipation if it is forced to conduct more than 40 A in avalanche.

The bottom line is that the propensity for failure is almost exclusively a function of two parameters: peak current in avalanche and peak (not average) junction temperature. Except for raising the average junction temperature — thereby enhancing the chance of hotspot failure — the total energy dissipated has only secondary effects.

Avalanche Test Methods and Ratings

Understanding the causes of overvoltage transients and the conditions that determine the propensity for failure provide a foundation for defining the most appropriate avalanche test methods. There are two viable tests: each offers its own benefits. The most common test circuit and its associated current and voltage waveforms are shown in Figures 1 and 2. Testing in this circuit is appropriately referred to as Unclamped Inductive Switching, or UIS, as there is no diode clamp across the coil to limit the flyback voltage appearing at the drain.

Although there is controversy surrounding some of the test conditions (such as coil size, initial and final junction temperatures and peak current), circuit operation is very straightforward. The gate drive is turned on and current in the coil is allowed to ramp up to the desired test current, which is primarily set by the coil size, the supply voltage and the on time of the gate drive ($\Delta I = (V_{DD}/L)\Delta t$). When the load current reaches the desired value, the MOSFET is abruptly turned off. Since the load current cannot change instantaneously, the inductive energy drives the drain-to-source voltage to $V_{(BR)DSS}$; the MOSFET then dissipates the stored energy in avalanche.

In this circuit the total energy dissipated by the MOSFET may not be equal to that stored in the coil. During avalanche, additional energy is transferred from the V_{DD} supply to the MOSFET. For low test currents (<10 A) the total energy dissipated is approximately equal to $1/2LI^2$ times the multiplier, $V_{(BR)DSS}/(V_{(BR)DSS}-V_{DD})$, which accounts for the additional transferred energy. For higher test currents the energy dissipated in the coil's resistance may also become significant, subtracting from what is dissipated in the device. In such cases, the exact amount of energy transferred to the test unit is somewhat difficult to calculate, but it can be accurately estimated by integrating the product of the drain-to-source voltage waveform and drain current waveform over the interval of avalanche.

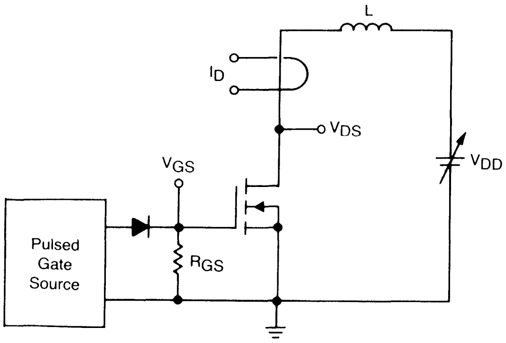

FIGURE 5-1 — TYPICAL TEST CIRCUIT FOR UNCLAMPED INDUCTIVE SWITCHING

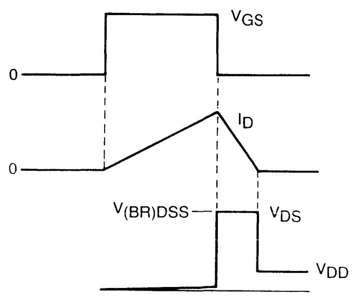

FIGURE 5-2 — WAVEFORMS ASSOCIATED WITH TEST CIRCUIT IN FIGURE 1

A second test circuit is shown in Figure 3, and again circuit operation is simple. In this case, the MOSFET conducts a fixed, controllable current in avalanche. Since there is no inductor in this circuit, results are independent of the series resistance of the test coil and the magnitude of V_{DD}. An important feature of this method is that the junction temperature continually increases during the time of avalanche. Therefore, it is clear that the greatest stress occurs at the end of the avalanche pulse when the avalanche current and junction temperature are at their maximum values.

Determining the moment of maximum stress during a UIS test is difficult since peak current occurs at the beginning of the avalanche period when the junction temperature is at its minimum. Because the relationship between failure, instantaneous current, degree of hotspotting, and average junction temperature is not well understood, it is difficult to pinpoint the moment of maximum stress or to compare the stress in the UIS test to the stress in the constant current test. Nevertheless, the UIS test is preferred over other methods since it is easy to implement and already enjoys wide acceptance as a meaningful test method.

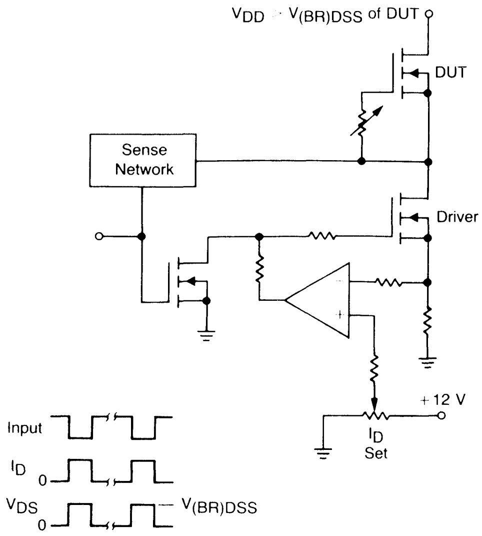

FIGURE 5-3 — ALTERNATE ASC TEST CIRCUIT THAT FORCES A CONSTANT CURRENT IN AVALANCHE

Stresses expected in the field should be used to guide the setting of UIS test conditions. Test currents should be equal to or greater than the continuous rating of the device. Junction temperatures should be elevated, bound only by the maximum rating.

There are two ways to achieve the elevated junction temperature specified in a UIS rating. The first is simply to externally heat the case of the device and the second is to begin the test at room temperature and raise the junction temperature by controlling the energy that the device under test must dissipate. However, in avalanche the many FET cells of the die may not share current evenly. This may cause the peak junction temperature to be much higher than the average. Consequently, forcing an elevated junction temperature with self heating tends to detect devices prone to hotspotting and is a more rigorous test.

Motorola's Avalanche Ratings

Motorola's E-series MOSFETs, which carry an "E" suffix, are designed to withstand the stress of drain-to-source avalanche. For E-FETs introduced to date, UIS failure can only be induced by either exceeding the device's pulsed current rating or its maximum junction temperature rating. With such a capability, an appropriate method of rating avalanche energy becomes clear. Current in avalanche is bounded by the pulsed current rating and energy dissipation is limited by thermal impedance and maximum junction temperature. The following example shows how the energy rating of the MTP3055E is calculated.

Consider the UIS rating of the MTP3055E specified at its continuous current rating of 12 A, a duty cycle of 1% and a case temperature of 25°C. For a typical $V_{(BR)DSS}$ of 70 V, peak power in avalanche is 840 W. For a maximum junction temperature rating of 150°C and a case temperature of 25°C the allowable ΔT_{JC} is 125°C.

$$\text{From } P_D\,(Z_{\theta JC}) = \Delta T_{JC} = 125°C, \text{ and}$$
$$Z_{\theta JC} = R_{\theta JC}\,(r(t)),$$

the transient thermal impedance $Z_{\theta JC}$ is calculated to be 0.149°C/W. From the thermal resistance rating of the MTP3055E ($R_{\theta JC}$ = 3.12°C/W), r(t) is found to be equal to 0.048, a dimensionless number. The next step is to use the r(t) curve on the MTP3055E data sheet to determine the pulse width corresponding to an r(t) of 0.048. That pulse width, which is the time required to attain a 150°C junction temperature, is 38 μs. The device rating, 32 mJ, is obtained by computing the avalanche energy corresponding to 840 W dissipated for 38 μs. Similar computations yield ratings for other conditions such as elevated case temperature, other drain currents or multiple pulses. E-FETs introduced in the future are expected to have ratings that can be determined in a similar manner.

The above calculations are based on a constant current during avalanche, which is quite unlike the decaying avalanche current present in UIS testing. One way to determine coil size for UIS testing is to set the energy stored in the unknown coil equal to the energy rating calculated above. In this case the equation, $W = 1/2\,LI^2\,[V_{(BR)DSS}/V_{(BR)DSS} - V_{DD}]$, yields a inductance of 143 μH for W = 32 mJ, I = 12 A, $V_{(BR)DSS}$ = 70 V, and V_{DD} = 25 V. Although the energies are the same, the UIS test is slightly less rigorous since the avalanche interval is roughly twice as long as the time of avalanche during a constant current test.

Four points regarding UIS testing are worth mentioning here. First, a UIS rating per se does not guarantee the ultimate goal, system reliability. Several other variables such as average and peak junction temperature, the quality of system design and reliability of system components also affect Mean Time Between Failure (MTBF). Millions of bipolar and MOSFET circuits have very satisfactory MTBFs even though the UIS capability of their power devices is unspecified.

Second, UIS ratings apply to only a specific set of test conditions and predictions of ruggedness outside those conditions are speculative. For example, in some devices elevated junction temperature or higher avalanche currents may substantially reduce energy handling capability.

Third, although excessive V_{DS} is a common cause of MOSFET failure, the incidence of overvoltage transients should not be blamed for all power MOSFET failures. The list of potential causes is long and investigations into the reason for failure should not be limited to the one that is currently receiving all the attention in the press. A similar situation occurred in recent years when two other prevailing scapegoats — electrostatic discharge and dv/dt — were faulted for causing many more problems than they probably deserved.

Finally, some have stated that a UIS test is a guarantee of a device's ability to handle diode recovery stress, which is discussed in detail below. Although a device that is rugged with respect to avalanching usually has a broad "Commutating Safe Operating Area," there are exceptions to this rule. In some devices, areas of the die other than those associated with the parasitic bipolar affect CSOA. The converse is also true; devices with fairly broad CSOA may fail immediately in avalanche because of inadequate die design or layout.

Drain-to-Source dv/dt Ratings

Static dv/dt

Power MOSFET performance is eventually limited by extremely rapid changes in drain-to-source voltage. These very high dv/dts can disturb proper circuit performance and even cause device failure in certain situations.

High dv/dts occur under three conditions, and each has its own dv/dt threshold before problems arise. The first is called "static dv/dt" and occurs when the device is off and is intended to remain off. A voltage transient across the drain and source can be coupled to the gate via the drain-to-gate parasitic capacitance, C_{rss}. Depending on the magnitude of the gate-to-source impedance and the displacement current flowing into the gate node (i = C dv/dt), V_{GS} may rise above $V_{GS(th)}$, causing false turn-on.

Obviously, for this case dv/dt immunity depends to a large extent on the gate-to-source impedance. This dependence underscores the importance of proper gate termination to promote good noise immunity and is one of several reasons why operation of power MOSFETs with the gate open circuited is a poor practice. With its gate shorted to its source, all Motorola TMOS devices will withstand static dv_{DS}/dts of greater than 30 V/ns, which is well in excess of values encountered in typical applications.

If the gate-to-source impedance is high and a voltage transient occurs between drain and source, false turn-on is more likely than device failure. Typically the transient will be coupled to the gate and cause the MOSFET to begin its turn-on. But as V_{GS} rises and the MOSFET begins to turn on, the rise in V_{DS} falters and the dv/dt is reduced. Thus, the phenomena is self-extinguishing and generally is not destructive to any circuit element.

Turn-on of the MOSFET's parasitic bipolar transistor, which is shown in Figure 4, is a potential route to device destruction due to static dv/dt. If the base-emitter shorting resistance is too large, displacement current flowing through C_{cb} will lower the parasitic BJT's ability to sustain collector-emitter voltage. Although such a scenario is plausible, concerns about spurious BJT turn-on are generally unnecessary because the resistance of R_{be} is kept

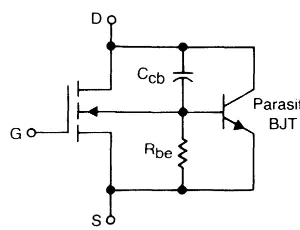

FIGURE 5-4 — INHERENT IN EVERY POWER MOSFET IS A PARASITIC BJT

low. Additionally, displacement current is lower at high voltage, when stand-off capability is most critical, because the magnitude of C_{cb} falls with increasing V_{DS}. So, the dv/dt turn-on threshold cited above (greater than 30 V/ns) also applies to the MOSFET's parasitic BJT.

Dynamic dv/dt

The second mode in which dv/dt may be a concern occurs when the MOSFET abruptly interrupts current in an inductive load and an extremely rapidly-rising flyback voltage is generated. Since the vast majority of loads appear inductive at very high switching speeds, the device experiences simultaneous stresses imposed by high drain current, high V_{DS} and displacement currents in the parasitic capacitances. Problems associated with this "dynamic dv/dt" (so named because the device is being switched off and is generating its own dv/dt) are evidenced by device failure.

Unless extraordinary circuit layout techniques are used (for example, hybrid circuits that minimize package and lead inductance) maximum attainable dv/dts in the dynamic mode range from 10 to 50 V/ns, depending on the V_{DSS} rating of the device. Among the various MOSFET types, maximum turn-off speeds do not differ widely and maximum attainable dv/dt is largely determined by the magnitude of the voltage that the drain can be switched through. Consequently, a 1000 V MOSFET can generate a greater dynamic dv/dt than a 60 V device, regardless of die size.

MOSFETs fabricated from all TMOS mask sets are tested and have been found to be immune to self generated dv/dts during very rapid, clamped inductive turn-off. The test circuit used has an extremely tight RF layout, and the switching speeds and dv/dts generated are assumed to be practical limits.

Diode recovery "dv/dt"

The third instance in which rapidly rising drain-to-source voltage has been thought to cause failure is during the reverse recovery of the MOSFET's intrinsic diode. Those that first studied this problem believed that dv/dt was the prime cause of failure, but more recent work has shown that dv/dt is only one of several factors that induce stress in a source-drain diode during reverse recovery.[1,2] Consequently, in this text these stresses are not classified strictly as dv/dt induced problems and the mode of stress is referred to as "diode recovery stress." Unlike the dv/dt modes discussed above, diode recovery stress is an occasional cause of system failure, but only when three specific conditions are met.

The first prerequisite is that the MOSFET's diode must conduct during the switching cycle. This is a necessary but not a sufficient condition for device failure. Although the MOSFET is virtually immune to dv/dt related failures, its area of safe operation may decrease greatly during reverse recovery of its diode. This dichotomy of capabilities is caused by a change in the means of conduction from minority to majority current carrier.

When a MOSFET operates as a transistor, it is not troubled by storage times or stored charge, since the MOSFET is a majority carrier device. Its diode, on the other hand, is a minority carrier device. Consequently, it has forward and reverse recovery times due to the storage of minority carrier charge.

The second condition required to induce failure due to commutating stress is that charge stored during reverse recovery must be removed rapidly. Faster removal of charge increases current densities and peak electric fields. Since the turn-on speed of the transistor in the opposite leg of the half bridge has the greatest effect on the speed of commutation, it has a great influence on device stress.

The third and final requirement is that the stored charge must be extracted through a reapplied voltage of at least 30 to 50% of the device's maximum V_{DS} rating. During reverse recovery, as the diode is driven from forward to reverse conduction, the rapidly rising drain voltage forces the stored charge into the base of the parasitic bipolar transistor. If the resulting emitter current is sufficiently high, it can, in conjunction with the re-applied drain voltage, induce the phenomenon of avalanche injection[3], the cause of bipolar transistor "second breakdown."

The criteria above excludes most circuits as candidates for diode recovery problems. All single transistor topologies are immune, and many multiple transistor topologies are not subjected to commutation stress because the third condition is not met. The following examples help define which multiple transistor applications may develop problems. The first circuit is representative of the most commonly cited problem; the second is one in which commutating dv/dt is not normally a concern.

Consider the bidirectional DC motor speed controller illustrated in Figure 5. The direction of rotation depends upon which transistor receives the PWM signal at its gate; varying the duty cycle provides speed control. When one transistor is controlling motor speed, the opposite one is inactive as a MOSFET, but its diode serves as a commutating rectifier. To reduce audible noise, designers often operate their systems at frequencies greater than 20 kHz, so switching speeds are also high.

Reviewing the motor controller operation shows how turn-on of the drive transistor, in this case Q1, impresses commutating dv/dt stress on Q2's diode. A cycle begins with the turn on of Q1, which delivers current to the load. Q1 then turns off and remains off for the rest of the cycle,

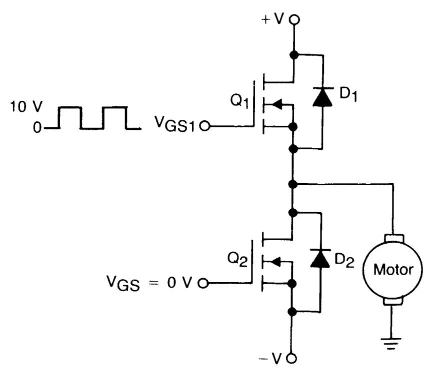

FIGURE 5-5 — A PWM DC MOTOR CONTROLLER IMPRESSES DIODE RECOVERY STRESS ON THE POWER TRANSISTORS

and the inductive load draws current from the negative supply through D2. When Q1 turns on at the beginning of the next cycle, load current begins to be supplied by Q1 instead of Q2's diode. But of greater importance, Q1 also supplies the reverse recovery charge for D2. Current in D2 and Q2's drain-to-source voltage are shown in Figure 6. The time thought to be most stressful is also depicted in the figure. Note that the three elements required for diode recovery stress are present. The diode of Q2 is experiencing the combined stress of reapplied high voltage, presence of minority carriers, and rapid extraction of charge, as evidenced by high di/dt and dv/dt.

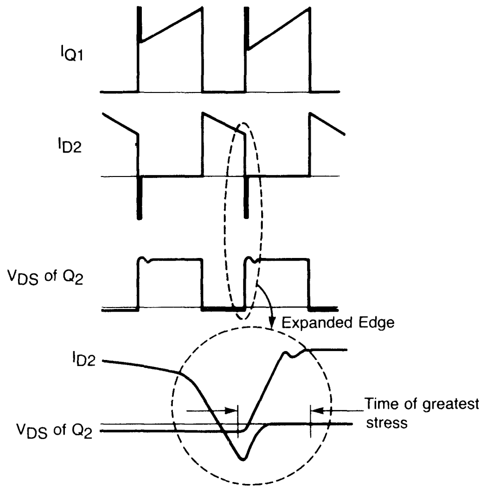

FIGURE 5-6 — TYPICAL WAVEFORMS IN A PWM DC MOTOR CONTROLLER

A second example, although it is in many ways similar to the first, is not usually subjected to commutating diode stress. It is the 1/2 bridge switch mode power supply, whose basic configuration is shown in Figure 7. The crucial difference between this system and the motor control circuit in Figure 5 is that the transistors are switching alternatively. Under normal operation one transistor will not turn on into a diode that is conducting current (which is a second, abbreviated, way to state the criteria for failure).

The idealized waveforms in Figure 8 show that output rectifiers D1 and D2 are the primary freewheeling rectifiers and the MOSFET diodes are essentially inactive. In reality, however, each intrinsic diode must clamp the energy in the transformer's leakage inductance when the opposite transistor turns off. Generally this is an acceptable situation since energies involved are small, diode conduction is brief, reapplied voltage is only a fraction of the device rating, and reverse recovery is slowed by parasitic inductance. Consequently, in these circumstances the intrinsic diode's commutation characteristics are usually not an issue.

For applications satisfying the three requirements, there are circuit solutions that deal with the problem if it occurs. One such approach is shown in Figure 9. Obviously, the intent of this circuit is to circumvent the MOSFET's limitations by not allowing the intrinsic diode to conduct and thereby accumulate stored charge. However, the higher parts count, additional cost and the voltage drop due to the diode in series with the FET are undesirable. Another solution is to limit dv/dt and voltage stress by using snubbers or by slowing the turn-on of the MOSFET in the opposite leg of the 1/2 bridge.

The optimum solution is to use devices that are indifferent to recovery stress and that have safe operating area curves that define and guarantee their capability. With the introduction of the E-FET, Motorola is making strides in both of these areas.

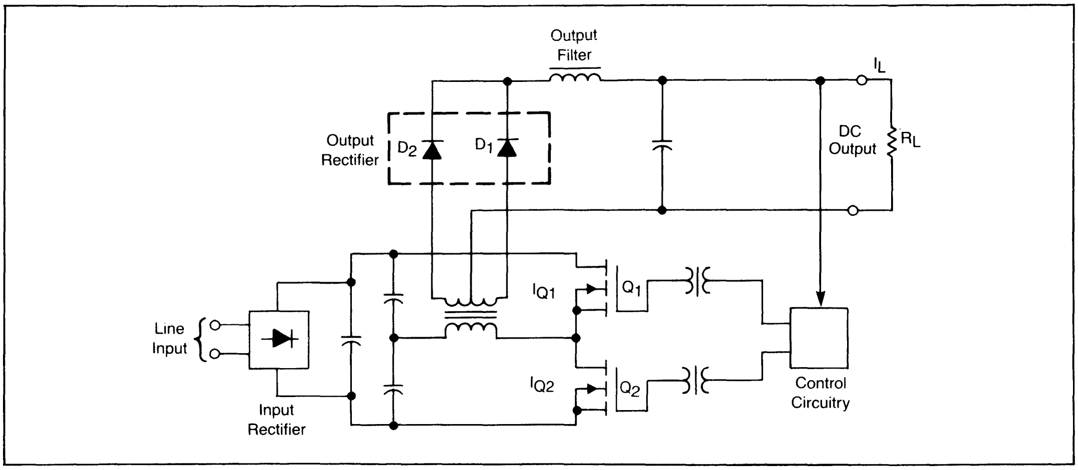

FIGURE 5-7 — ALTHOUGH THE MOSFETs INTRINSIC DIODES ACT AS FREEWHEELING RECTIFIERS IN THE 1/2 BRIDGE SMPS, THEY GENERALLY DO NOT EXPERIENCE DIODE RECOVERY STRESS

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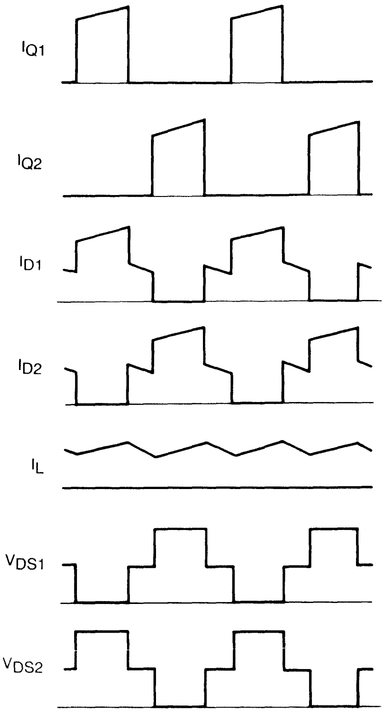

FIGURE 5-8 — TYPICAL WAVEFORMS OF A 1/2 BRIDGE SWITCHED-MODE POWER SUPPLY

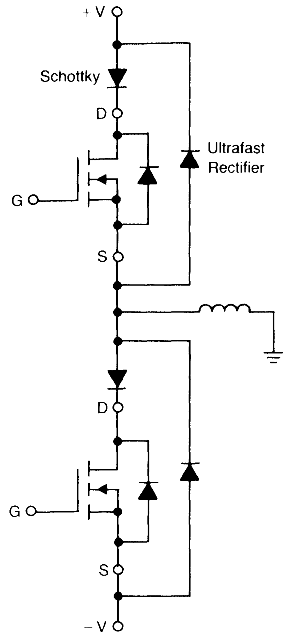

FIGURE 5-9 — ONE WAY TO AVOID REVERSE RECOVERY STRESS IN THE MOSFET's INTRINSIC DIODE IS TO USE A SCHOTTKY IN SERIES WITH THE MOSFET AND AN ULTRAFAST RECTIFIER IN PARALLEL WITH THE MOSFET AND THE SCHOTTKY

Proposed CSOA Specification

One of the tasks before the power electronics community is to eliminate commutation problems associated with the MOSFET's intrinsic diode. The necessary steps are: 1) develop devices that are more resistant to commutation stress, 2) define a test method to determine device capability, and 3) provide ratings that detail the safe operating area for the diode recovery mode. The suggested rating is a Commutating Safe Operating Area, or CSOA.

Motorola has already introduced the E-FET, which has greater CSOA than its predecessors. But even with the introduction of improved devices, users will remain cautious, unless the new capability is defined and guaranteed. Lack of a universally accepted test method to standardize CSOA specifications is now the major hindrance in this effort. Although this is unfortunate, it is understandable since specifying CSOA is fairly complex.

Figure 10 shows the relationships between the various parameters that influence CSOA. Upon inspection choosing the most meaningful and convenient independent variables for testing is not obvious. Motorola's test results indicate that the best approach is to use the three most critical circuit dependent parameters. They are the forward current in the diode just before commutation (I_{FM}), reapplied voltage (or peak drain-to-source voltage when $V_{DS(PK)} > V_R$), and speed of commutation.

An example of a CSOA specification for a 15 A, 60 V device is shown in Figure 11. This representation has the advantage of using voltage and current axes, which are common in other SOA curves. The third variable, di/dt during the first part of reverse recovery, provides the measure of commutation speed.

Establishing the format shown in Figure 11 was a key step toward quantifying the CSOA of many device families. With that information design engineers were able to identify device features that give a broad CSOA, and they are now implementing improvements in device design and processing to enhance performance in the commutating mode. An example of such a device is the recently introduced MTP3055E, a 12 A, 60 V replacement for the MTP3055A. Within its voltage, current, and temperature ratings it is virtually indestructible during rapid commutation, as shown by the square SOA of Figure 12. The practical limit of reverse recovery di/dt is bounded by the parasitic inductance of the test circuit and the voltage that is applied to the diode to force reverse recovery. For example, a supply voltage of 50 V in a circuit with 100 nH of stray inductance allows a maximum di/dt of 500 A/μs (di/dt = V_{DD}/L). For a point of reference, total D-S package inductance of the TO-220 is about 10 nH.

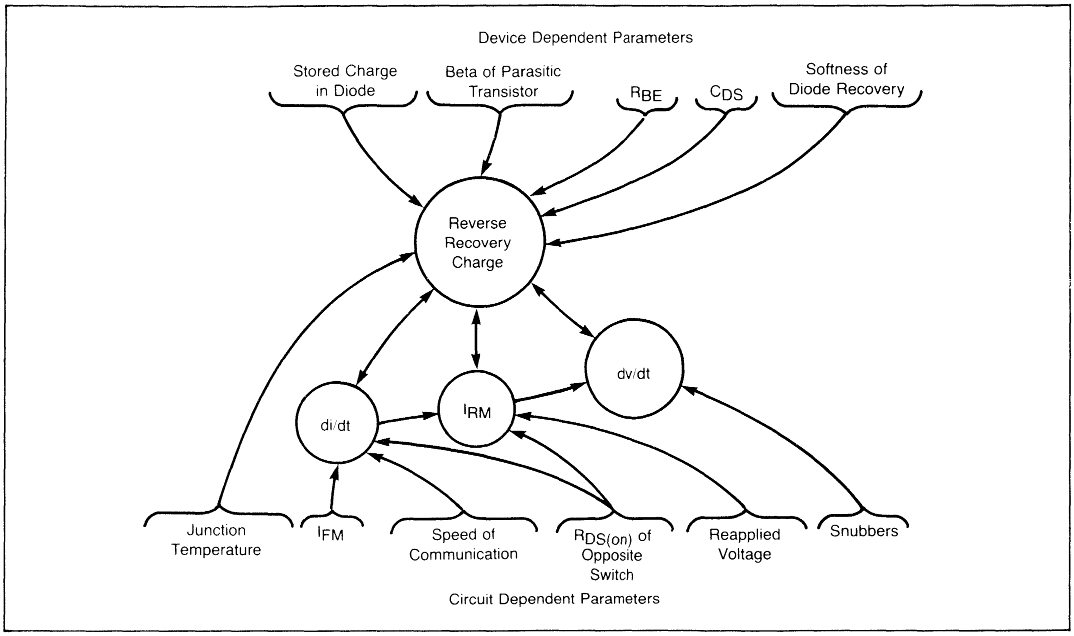

FIGURE 5-10 — DURING COMMUTATION MANY PARAMETERS AFFECT TOTAL DEVICE STRESS

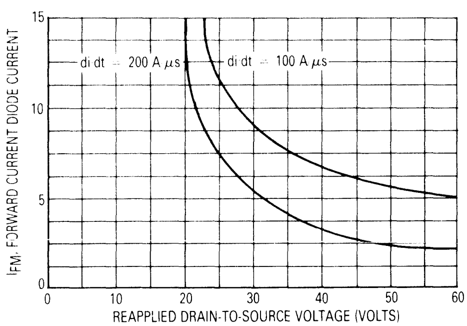

FIGURE 5-11 — TYPICAL COMMUTATING SAFE OPERATING AREA OF A 15 A, 60 V DEVICE NOT DESIGNED TO WITHSTAND DIODE RECOVERY STRESSES

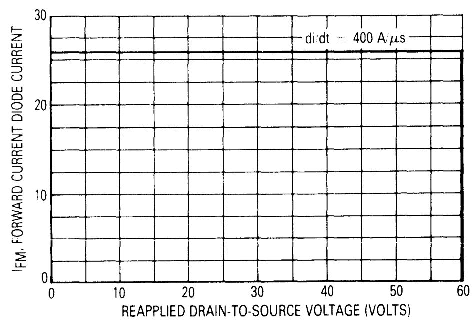

FIGURE 5-12 — COMMUTATING SAFE OPERATING AREA OF THE MTP3055E IS MUCH BROADER THAN ITS PREDECESSORS

Other methods of specifying diode recovery stress have been proposed. Using a single dv/dt value was the initial favorite because of its simplicity and the suspicion that failures are predominantly dv/dt induced. This idea was discarded for several reasons. First, devices do not fail solely due to dv/dt. In fact, when failures occur, they are rarely noted during peak dv/dt but are found later during maximum voltage stress and reduced dv/dt. Second, dv/dt varies considerably during reverse recovery and selecting a single representative value is difficult and too simplistic. Third, dv/dt during commutation is a function of device characteristics and circuit conditions and is not something that the user can easily control, except with snubbers. Fourth, displacement current caused by diode recovery dv/dt is dwarfed by reverse recovery current, making the rate of extraction of stored charge much more important. Finally, some intrinsic diodes are much snappier than others (that is, the return of the diode current from the reverse recovery peak to zero is very abrupt and the rise in V_{DS} to V_R is very fast), and those diodes should have to withstand the dv/dts that they inherently create.

A High Voltage, High Speed CSOA Test Fixture

Several CSOA test circuits have been built at Motorola. One was targeted for high current, high speed testing; in another the layout and associated slower switching speeds were intended to be similar to those of a typical motor control circuit; and a third was designed to handle a wide range of voltages and currents. A fourth fixture, the one described here, has as its strength the ability to switch the DUT into voltages up to 450 V at very fast commutation speeds.

This CSOA tester, whose schematic is shown in Figure 13, is designed to impart maximum DUT stress for a given I_{FM}, V_R and di/dt. Circuit features include a well bipassed reapplied voltage to allow maximum dv/dt and voltage stress, a drive transistor with a very low $R_{DS(on)}$ for high I_{RM}, and a complementary emitter follower gate drive for Q2 to reduce dv/dt effects on the driver when the diode under test snaps off. (The drive transistor must support a dv/dt of equal magnitude and opposite polarity of the dv/dt that appears at the DUT. A drive transistor with a high gate drive impedance will consequently limit voltage during reverse recovery.)

An important assumption that influenced circuit design is that test results are independent of duty cycle, or that failures are caused by peak instantaneous stresses and not by multiple exposures to lower levels of stress. (This is not to say, however, that propensity for failure is independent of T_J.) If this assumption is true, and testing indicates that it is, then circuit simplicity is vastly improved. Also the layout can be much tighter and speeds much faster if the Device Under Test, the DUT, requires very little heatsinking.

The circuit's timing waveforms are also illustrated in Figure 13, and circuit operation is as follows. Nor gates A1 and A2 are connected as an astable multivibrator to generate a relatively low clock frequency of 10 to 1000 Hz. The clock's rising edge triggers two monostable multivibrators formed by A3 and A4 and B1 and B2. The signal from A3 and A4 ultimately controls the on-time of the MJE13009, which acts as a constant current source to deliver the forward current, I_{FM}, to the MOSFET's intrinsic diode. I_{FM} is set by varying R_1.

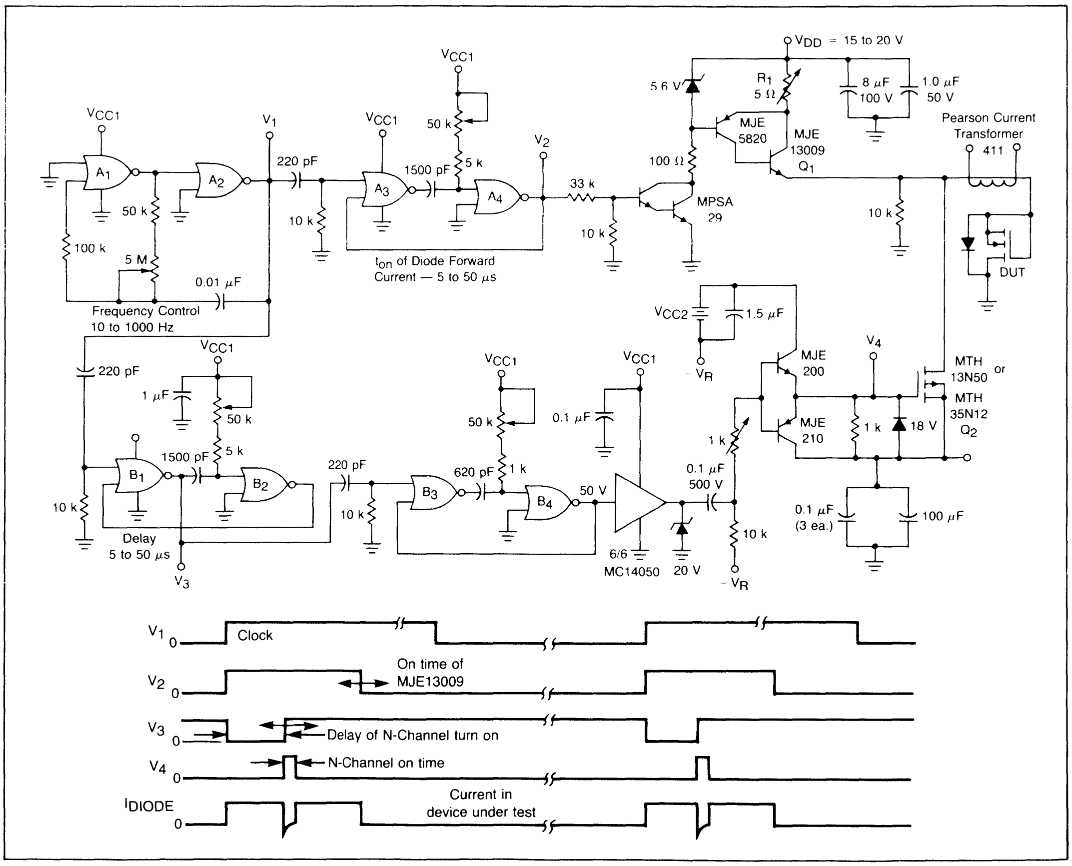

FIGURE 5-13 — SCHEMATIC AND TIMING WAVEFORMS OF A HIGH VOLTAGE, HIGH SPEED CSOA TEST CIRCUIT

The second monostable, B1 and B2, provides a delay before Q_2 is turned on. Minimum delay is set to 10 μs to allow accumulation of stored charge in the diode's junction. After that delay the monostable formed by B3 and B4 sends a turn-on signal for 2 to 10 μs. For the duration of the turn-on pulse, Q_2 applies reverse voltage to the DUT's source-drain diode and forcefully extracts reverse recovery charge. During reverse recovery the current burden of Q2 includes the current delivered by the current source. After Q2 turns off the current source is also gated off and the system remains at rest until the next cycle.

A few circuit features make device testing easier. First, the drain of the DUT is attached directly to the system groundplane. This greatly simplifies monitoring V_{DS} and improves measurement accuracy since using a differential measurement technique or floating an oscilloscope is unnecessary with this layout. Additionally, this method allows use of a probe tip adaptor that provides an excellent ground connection for the oscilloscope. These pains are needed because the magnitude of V_{DS} is the most important CSOA parameter and its rate of change can be greater than 10 V/ns.

A second mundane but very necessary feature is the capability of the circuit to withstand DUT failure. Current surges at failure are principally limited by the $r_{DS(on)}$ of the drive transistor Q_2 or its cut off current at the gate-to-source voltage that is applied. In either case the MOSFET's ruggedness with respect to current surges and the low duty cycle and limited on-time give the driver the margin of safety it needs to survive.

Using the CSOA Specification

The CSOA format was chosen to make the rating easy to relate to operating conditions in an application. The designer must only maintain V_{DS} and I_{FM} within specified limits and remember that di/dt is specified as a maximum allowable value. Pushing devices to their limit in a 1/2 bridge PWM DC motor controller produces failures that track those seen in the CSOA testers. Therefore, the test method and circuit are appropriate for simultating stress in common applications. Nevertheless, designers should be aware of how important circuit parameters can skew the comparison.

Three other circuit parameters can degrade CSOA. They are solely under the control of the design engineer and are therefore difficult to include in a CSOA specification. The first is the gate to source impedance of the DUT. If R_{GS} or L_{GS} is high during reverse recovery, V_{GS} can exceed $V_{GS(th)}$ due to the large dv/dt that the intrinsic diode generates. This dv/dt does not fully turn-on the MOSFET but forces it into the active region and slows the reverse recovery process, as seen in Figure 14. Since operating in this mode increases commutation power losses and clearly involves dv/dt turn-on (of the MOSFET, not the parasitic BJT), decreasing Z_{GS} is normally the best approach. However, slowing reverse recovery with higher gate-to-source impedance can reduce V_{DS} peaks and may even keep the device from avalanching, which is also shown in Figure 14.

Junction temperature is the second parameter that degrades CSOA. Although one might intuitively suspect that T_J has a first order effect on CSOA, test results to date indicate that it does not. These results are easier to believe when one recalls that RBSOA (Reversed Biased Safe Operating Area) of bipolars is also relatively independent of T_J. Another indication that T_J has a secondary effect is that DUT voltage and current waveforms are fairly constant as T_J changes. Varying other more dominant parameters often causes waveform changes that signal impending DUT failure.

The final parameter over which the circuit designer has strict control is the parasitic circuit inductance between the positive and negative rails of the 1/2 bridge. This inductance is unclamped and is likely to briefly avalanche the DUT at very high commutation speeds. In all cases this inductance should be minimized. The practical lower limit is in the 100 to 200 nH range.

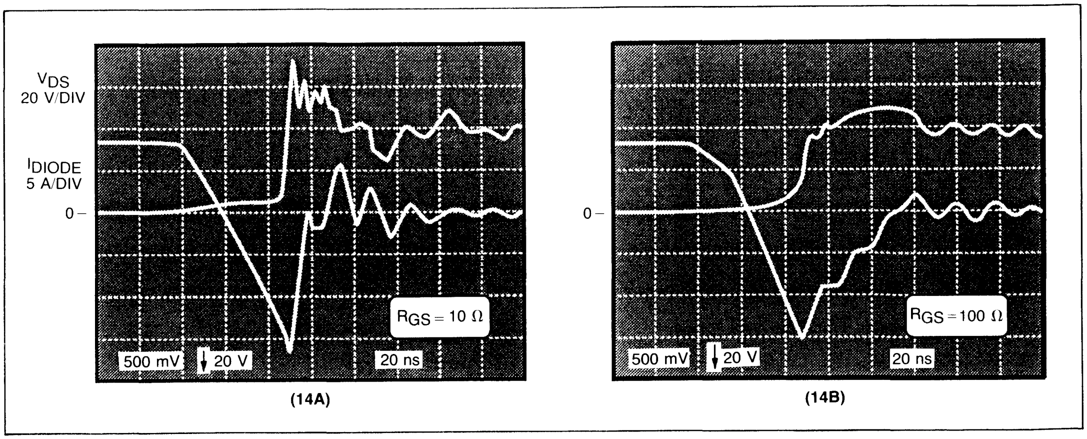

FIGURE 5-14 — IF THE MOSFET OF THE REVERSE RECOVERING RECTIFIER HAS A HIGH GATE-TO-SOURCE IMPEDANCE, REVERSE RECOVERY TIME IS LONG AND PEAK VOLTAGE STRESS IS LESS

Relationship Between CSOA and UIS

It is tempting to believe that a UIS test (Unclamped Inductive Switching) is an adequate substitute for a CSOA test. The argument given is that the common cause of device failure in the two modes is activation of the parasitic bipolar transistor due to high R_{BE}, or base-emitter shorting resistance. Although this reasoning seems to make sense, it is flawed in two ways.

The first is that some devices may pass a UIS test and then fail in the commutating dv/dt mode due to device deficiencies other than high R_{BE}. With its voltage termination rings, gate feeds, bonding pads and cell interconnections, the power MOSFET is much more than a few thousand paralleled cells. In some manufacturer's devices it is clear that these secondary structural features can limit performance in one test and not the other.

The second problem with correlation of UIS and CSOA test results is caused by a flaw in the present UIS test method. A study of UIS waveforms clarifies this point. As evidenced by different voltage waveforms in Figure 15, a device may react to overvoltage stress in at least three ways. Some devices fail immediately in avalanche and V_{DS} collapses to about zero volts. Other MOSFETs can maintain their $V_{(BR)DSS}$ during the entire transient — if the current and pulse duration are not too great. In the third case, the drain-to-source voltage of some devices may collapse to a lower level. The lower voltage in avalanche is associated with activation of the MOSFET's parasitic bipolar transistor. Thus, the magnitude of V_{DS} during avalanche is the transistor's $V_{(BR)CEO}$.

If the UIS supply voltage is increased above $V_{(BR)CEO}$, there is no mechanism to limit avalanche current and the DUT normally fails. Therefore, the magnitude of the supply voltage can have a great effect on a device's energy handling capability. Improving the present UIS test method to detect devices that exhibit $V_{(BR)CEO}$ snapback is relatively simple. Instead of checking only for device failure, the V_{DS} waveform in avalanche can be sampled to ensure that it remains above the transistor's maximum V_{DS} rating.

As switching speeds and test currents increase in the commutating dv/dt mode, the device under test is likely to see overvoltage transients. During the final phase of reverse recovery the diode current is returning from its negative peak toward zero. This current can be thought of as decreasing drain current. If the diode recovers abruptly, or snappily, the associated di/dt can be extremely large, perhaps greater than 1000 A/μs. These rates of change in current are opposed by parasitic inductances, and the polarity of the induced voltages is such that they add to the reapplied voltage and increase the voltage stress on the DUT.

Figure 16 shows the reverse recovery waveforms of a 10 A, 50 V device from manufacturer "A." The effect of the device's $V_{(BR)CEO}$ is clearly evident. The clipping of the V_{DS} waveform at the device's $V_{(BR)CEO}$ (which corresponds to the value observed in UIS testing) and the coincident drain current show that the device is in avalanche. Even though the device passes this test, reliability in this mode of operation is uncertain since the parasitic bipolar is clearly being activated. If V_R is increased to greater than $V_{(BR)CEO}$, failure is likely. Because of its tendency to break back to a $V_{(BR)CEO}$, this device could fail in the commutating dv/dt mode, yet survive a UIS test.

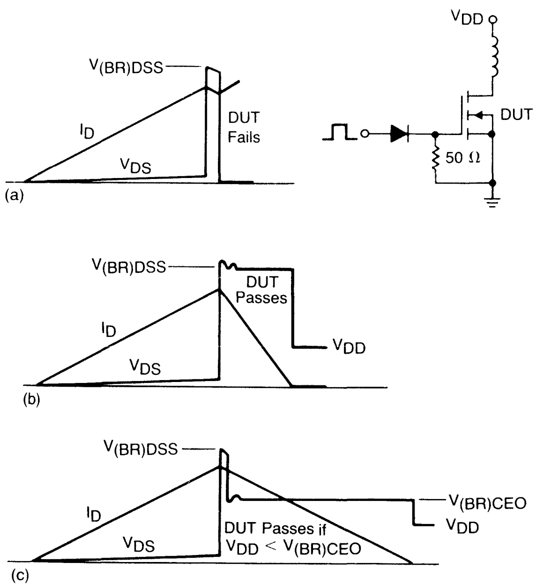

FIGURE 5-15 — A MOSFET CAN HAVE ONE OF THREE RESPONSES TO AN OVERVOLTAGE TRANSIENT

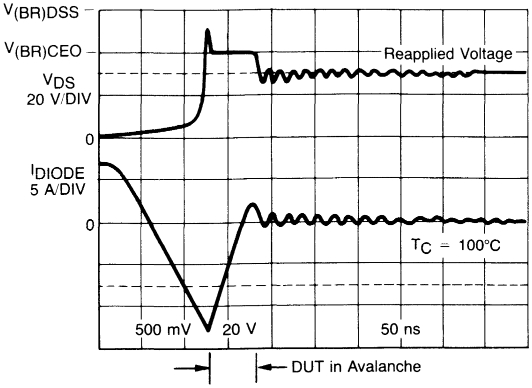

FIGURE 5-16 — COMMUTATION AT VERY HIGH SPEEDS CAN CAUSE AVALANCHING OF THE DUT

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Chapter 6: Gate Drive Requirements

Power MOSFET Gate Drive Requirements

Bipolar power transistors have been around for decades — drive circuits for these devices abound. Power MOSFETs are new arrivals. They differ from their bipolar counterparts especially in their input characteristics. These differences and their implications must be understood in order to insure that the MOSFET is operated in an optimum fashion.

Driving a power MOSFET is tantamount to driving a capacitive reactance network. Depending on the region of operation, the input "sees" either C_{iss}, the Common-Source Input capacitance, or C_{rss}, the Common-Source Reverse Transfer capacitance. C_{iss} is the sum of the gate-to-source capacitance, C_{gs}, and the drain-to-gate capacitance, C_{dg}. C_{gs} is made up of a voltage independent capacitance between the gate structure and the source metallization and a gate-to-channel capacitance which varies significantly with operating conditions. C_{rss} (C_{dg}) on the other hand, is mainly the MOS capacitance between gate and drain regions. Its value increases sharply during the latter stages of turn-on.

The device capacitances, especially the reverse transfer capacitance, and the gate-drive source impedance largely determine the device switching speed. Since the MOSFET input capacitances vary significantly with the die area, a given gate-drive will switch a smaller device such as the MTP5N06 more rapidly than the larger MTM15N40. However, two considerations complicate the task of estimating switching times. First, since the magnitude of the input capacitance, C_{iss}, varies with V_{DS}, the RC time constant determined by the gate-drive impedance and C_{iss} changes during the switching cycle. Consequently, computation of the rise time of the gate voltage by using a specific gate-drive impedance and input capacitance yields only a rough estimate. The second consideration is the effect of the "Miller" capacitance, C_{rss}, which is referred to as C_{dg} in the following discussion. An example best explains why it influences switching times.

When a high voltage device is "on," V_{DS} is fairly small and V_{GS} is about 15 V. C_{dg} is charged to $V_{DS(on)} - V_{GS}$, which is a small negative potential if the drain is considered the positive electrode. When the drain is "off" and is blocking a relatively high drain-to-source voltage, C_{dg} is charged to quite a different potential. In this case the voltage across C_{dg} is a high positive value since the potential from gate-to-source is near or below zero volts and V_{DS} is essentially the drain supply voltage.

During turn-on and turn-off, these large swings in gate-to-drain voltage tax the current sourcing and sinking capabilities of the gate-drive. In addition to charging and discharging C_{gs}, the gate-drive must also supply the displacement current required by C_{dg} ($i_{gate} = C_{dg}\, dV_{DG}/dt$). Unless the gate-drive impedance is very low, the V_{GS} waveform commonly plateaus during rapid changes in the drain-source voltage.

Input Capacitance

The traditional capacitance curves as shown in Figure 6-1 are somewhat meaningful, but they are not complete. Unfortunately, because they are incomplete, they can also be misleading. The fallacy of that presentation is that each capacitance is shown as a function of V_{DS} and not as a function of the voltage across that capacitor. For C_{oss}, Figure 6-1 is correct as shown because the independent voltage is V_{DS} with V_{GS} = 0 V. However, these curves are normally used to determine input impedance, and for C_{iss} and C_{rss} the curves omit important information. A discussion of the variation of C_{rss} with V_{DG} best illustrates this point.

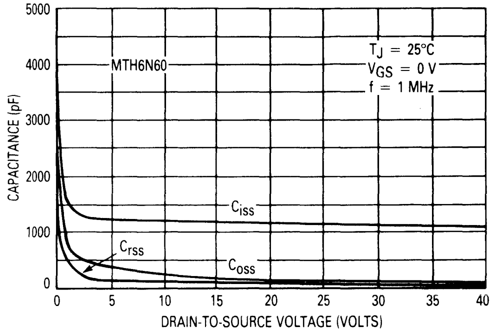


FIGURE 6-1 — THIS TRADITIONAL REPRESENTATION OF POWER MOSFET CAPACITANCES IS ACCURATE BUT NOT COMPLETE.

The first step towards understanding the variation of C_{rss} with voltage is to study the change in V_{DG} during the switching transition. When the device is off, V_{DS} is essentially at the drain supply voltage. At that same time V_{GS} is at or near zero volts, which means that V_{DG} is a high positive value. When the device is in the "on" state, a quite different situation occurs. V_{GS} is at roughly 10 V and V_{DS} is at $V_{DS(on)}$. Therefore V_{DG} is equal to $V_{DS(on)} - V_{GS(on)}$, which is normally a negative value. It is this negative swing in V_{DG} that the traditional curves do not address.

Now the importance of this additional information becomes evident. One possible presentation of the complete curve is given in Figure 6-2. The variables plotted on the abscissa (V_{GS} and V_{DS}) and the test conditions (V_{DS} = 0 and V_{GS} = 0) reflect the common source test circuit and the test conditions used to generate the two sections of the curves. Consequently, this is the format shown on Motorola's data sheets. A C_{rss} (or C_{iss}) versus V_{DG} curve is identical except that the voltage axis is simply V_{DG}, where V_{DG} takes on negative values to the left of zero and positive values to the right of zero. The dramatic

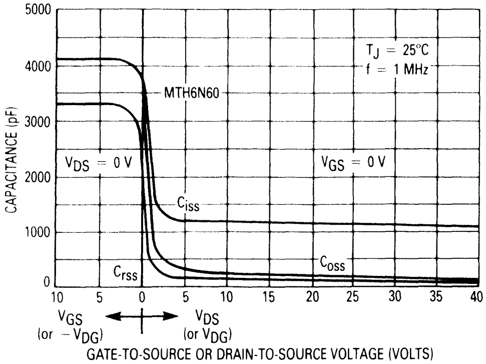


FIGURE 6-2 — EXPANDING THE TRADITIONAL CAPACITANCE CURVES TO SHOW THE VALUES OF C_{iss} AND C_{rss} AS THE MOSFET MOVES INTO THE "ON" STATE GIVES A COMPLETE PICTURE OF THE CAPACITANCE VARIATION.

rise in C_{rss} of the MTH6N60 (Figure 6-2) from around 50 pF at positive voltages to about 3300 pF at negative voltages simply cannot be ignored. This larger capacitance dominates the input impedance during the latter stages of turn-on and the first stages of turn-off.

Also it becomes apparent that the curves of C_{rss} and C_{iss} as traditionally represented often lull the user into a misconception. He might mistakenly assume that since V_{DS} never falls below $V_{DS(on)}$ in his system, then C_{rss} never becomes greater than its value at a V_{DS} equal to $V_{DS(on)}$. Again, the problem with this reasoning is that the voltage across C_{rss} when the device is "on" is not $V_{DS(on)}$ but $V_{DS(on)} - V_{GS(on)}$.

Integrating the C_{rss} curve over the entire variation in V_{DG} to determine the amount of stored charge required by C_{rss} is another convincing way to show the importance of providing the complete capacitance curves. A rough piece-wise linear approximation suffices to illustrate this point. For the two regions above and below V_{DG} = 0 V, the charge required is roughly the change in V_{DG} times the average value of C_{rss} in each region. For a 480 V bus, for example, the charge to the right of zero is 24 nC

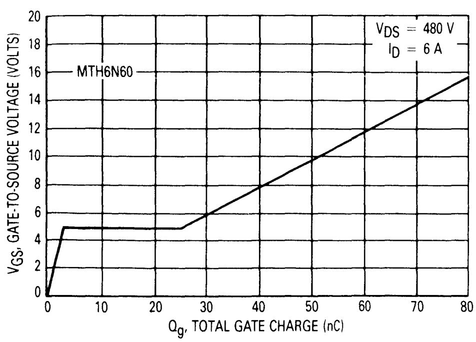


FIGURE 6-3 — INTEGRATING THE CAPACITANCE versus VOLTAGE CURVES GIVES ACCURATE VALUES OF GATE CHARGE

(480 V x 50 pF), and to the left the figure is 23 nC (7 V x 3300 pF). In this case the traditional approach of only specifying capacitances at positive voltages omits nearly half of the required gate charge and can lead to underestimation of required gate drive.

Estimation of the amount of charge transferred to the gate-to-source capacitance is also enlightening. In this case ΔV_{GS} is roughly 10 V and C_{gs} (= $C_{iss} - C_{rss}$) is about 1100 pF. The charge in this instance is 11 nC (= 1100 pF x 10 V). Interestingly, even though C_{gs} is much larger than C_{rss} at a V_{DS} of 25 V, C_{rss} under these conditions requires about four times as much charge. Also, integrating each of the two input capacitance curves over the change in voltage that each one sees as the MOSFET switches theoretically yields the required gate charge. From the numbers computed above (24 + 23 + 11), the required Q_g is 58 nC, which closely tracks with the 10 V value (52 nC) shown in Figure 6-3.

One other problem area may arise when using capacitance measurements to compare input impedance of devices from different manufacturers. Typically, C_{iss} and C_{rss} are specified at a V_{DS} of 25 V, and comparisons at that value may be a poor indication of the relative sizes at other voltages. For instance, Figure 6-4 shows the C_{rss} curves of two 500 V, 4.5 A devices from different manufacturers. At a V_{DS} of 25 V the device from manufacturer

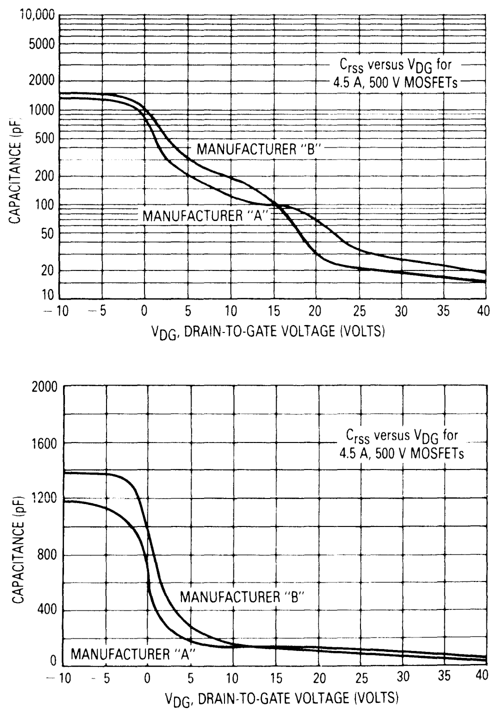


FIGURE 6-4 — SINCE CAPACITANCE CURVES OF DEVICES FROM DIFFERENT MANUFACTURERS SOMETIMES CROSS, USING A SINGLE VALUE OF CAPACITANCE TO COMPARE INPUT IMPEDANCE IS NOT A GOOD IDEA. IN THESE TWO FIGURES THE SAME INFORMATION IS SHOWN IN TWO DIFFERENT FORMATS.

"B" has a C_{rss} about 50% less than that of the device from manufacturer "A". However, the difference is actually pretty insignificant when compared to the large differences between values at other voltages. Note too that the curves cross and that overall the device from manufacturer "A" actually has the lower C_{rss}.

Photographs of switching times in Figure 6-5 confirm what might be expected from a study of the complete capacitance curves — device "A" is the faster switch. The gate charge waveforms shown in Figure 6-6 are a more dependable means of judging relative switching speed. For these reasons manufacturers are de-emphasizing the importance of capacitance specifications at a single value of V_{DS}, namely 25 V. Circuits for testing the MOSFETs inter-terminal capacitances are given in Chapter 12.

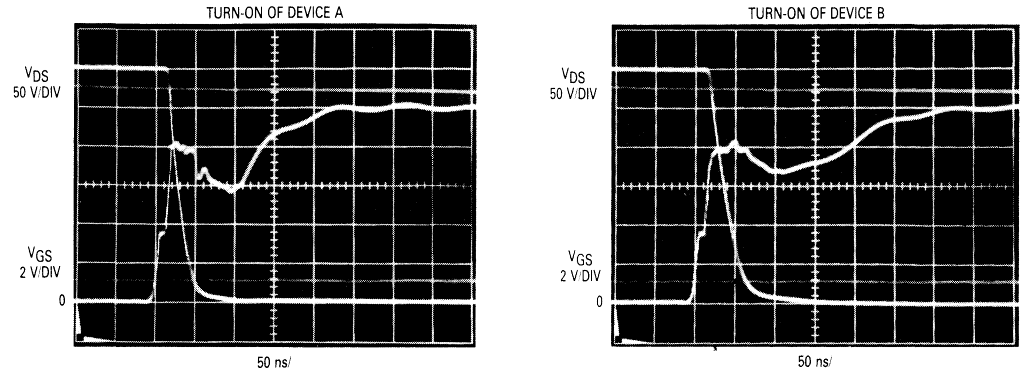


FIGURE 6-5 — ALTHOUGH DEVICE "B" HAS THE LOWER C_{rss} AT A V_{DS} OF 25 V, DEVICE "A" IS THE FASTER SWITCH SINCE ITS CAPACITANCE IS LOWER AT OTHER VOLTAGES. R_{GS} = 25 Ω, I_D = 5 A, V_{DD} = 300 V

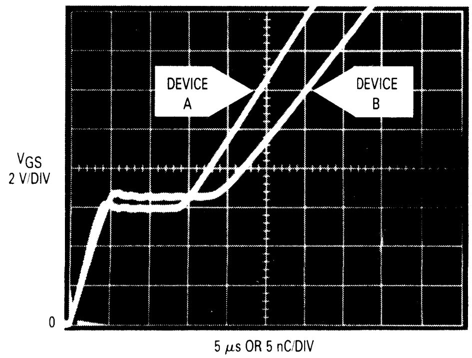
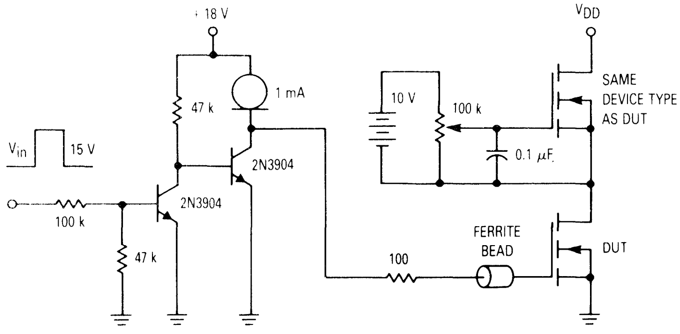


FIGURE 6-6 — GATE CHARGE WAVEFORMS ARE A MORE ACCURATE MEANS OF PREDICTING SWITCHING SPEEDS THAN CAPACITANCE SPECIFICATIONS. I_D = 5 A, V_{DD} = 300 V, I_G = 1 mA

Gate Charge Specifications

Another means of specifying the size of the input impedance of a power MOSFET is to provide a gate charge curve. As the name suggests, such a curve indicates the amount of charge that must be supplied to the gate to effect the various stages of turn-on. These curves and the associated gate charge ratings are gradually replacing input capacitance specifications because of their simple format, ease of use, and the wealth of information they contain.

Understanding the gate charge test circuit aids in the interpretation of the gate charge waveforms. All gate charge test circuits, such as the one shown in Figure 6-7, employ a constant current source to charge the MOSFET's input capacitance. A constant I_G ensures that C_{iss} is charged at a fixed rate ($i = q/t$). The V_{GS} waveform then, is a representation of V_{GS} versus gate charge as well as V_{GS} versus time.



V_{in} = 15 V_{pk}; PULSE WIDTH = 100 μs, DUTY CYCLE ≤ 10%

FIGURE 6-7 — GATE CHARGE TEST CIRCUIT

A second current source is usually used in the drain to set the desired drain test current. As will be discussed shortly, using a current source as a load helps sharpen the inflection points of the V_{GS} waveform. Gate charge waveforms can be used to show turn-off behavior, but they are normally used to describe turn-on characteristics.

Figure 6-8 shows the gate-to-source voltage, the drain-to-source voltage and the drain current waveforms during turn-on of the MTP15N06. In this instance, the gate drive is a 1 mA current source and a 15 A current source is the load in the drain.

Each inflection point on the gate charge waveform defines the beginning or end of a distinct interval during the turn-on process. The time required to deliver charge Q1 to the gate is the turn-on delay time. At Q2 the drain-to-source voltage has fallen to $V_{DS(on)}$ and all switching is complete. When a charge equal to Q3 is supplied, the gate is charged to $V_{GS(on)}$ and no more gate charge is required. The magnitude of $V_{GS(on)}$ is somewhat arbitrary, but in this case a $V_{GS(on)}$ of 10 V requires 15.5 nC of gate charge. During turn-off the amount of time required to remove Q3 minus Q2 is the delay time. Removal of Q2 minus Q1 allows the drain-to-source voltage to rise to the supply voltage, and discharging Q1 brings V_{GS} back to zero volts. Obviously, to satisfy conservation of charge, the charge supplied to the gate during turn-on is equal to and opposite that required for turn-off.

The slope of curve at any point can be interpreted as being the reciprocal of the capacitance during that portion of the switching interval (i = C dv/dt yields C = $\Delta Q_g / \Delta V_{GS}$). Even a brief look at a typical gate charge waveform reveals that the slope or input capacitance takes on at least three different values. As V_{GS} rises from zero volts, C_{iss} is relatively small, which makes charging rather easy. During the next portion of the curve, the capacitance appears to be infinite since additional charge brings little, if any, change in V_{GS}. When the plateau ends, V_{GS} is free to rise again, but not nearly as fast as it did during the first interval. The capacitance curves and a description of the change in V_{DG} during the switching transition aid in explaining why there are three distinct slopes during the switching interval.

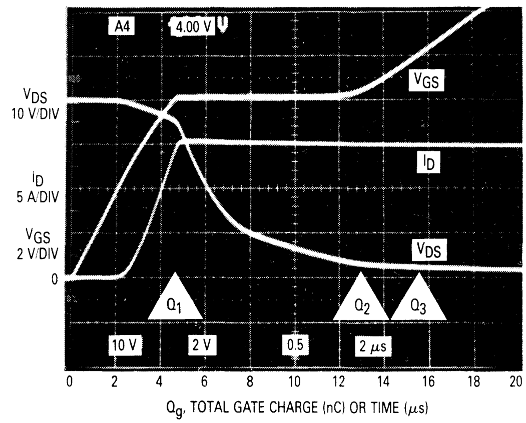


FIGURE 6-8 — GATE CHARGING WAVEFORMS ARE RIPE WITH INFORMATION REGARDING MOSFET SWITCHING

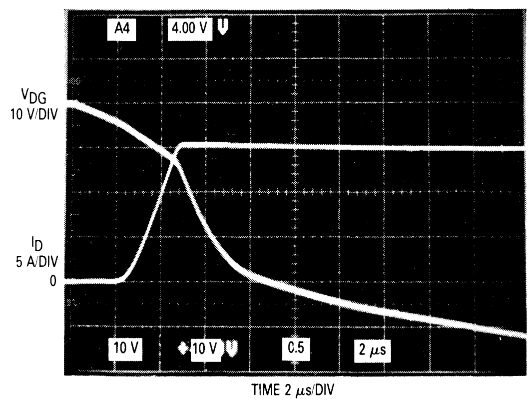


FIGURE 6-9 — AS V_{DG} APPROACHES ZERO VOLTS, SWITCHING SLOWS CONSIDERABLY DUE TO A DRAMATIC INCREASE IN C_{rss}.

The slopes of the gate charge waveform in the first and third intervals can be directly related to capacitance values shown on the capacitance curves. In the first interval the slope of the gate charge curve indicates that C_{iss} is equal to 4 nC/7 V or about 570 pF. The similarity between this value and the magnitude of C_{iss} in Figure 6-10 at higher voltages is not a coincidence. Until V_{GS} rises beyond $V_{GS(th)}$, the MOSFET remains off and V_{DS} remains constant and equal to the supply voltage. Consequently, during this interval C_{iss} is also constant.

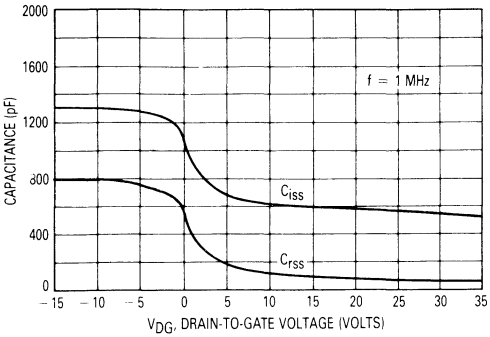


FIGURE 6-10 — COMPLETE C_{iss} AND C_{rss} CURVES OF THE MTP15N06

On the other side of the plateau, C_{iss} takes on a much larger value. There the change in charge divided by the change in V_{GS} yields a capacitance of around 1300 pF. This corresponds to the value of C_{iss} at drain-to-gate voltages below −5 V. Therefore, for circuit modeling in the first and third intervals of turn-on the magnitude of C_{iss} can be estimated by measuring slopes of the gate charge waveform or by selecting values of C_{iss} from opposite ends of the capacitance curve.

Estimation of C_{iss} during the plateau is also possible. Even though the slope of the curve is near zero, C_{iss} is not infinite as it may first appear. In this region the delta V_{GS} is approximately zero, so no charge enters C_{gs}. All the charge instead enters C_{rss}, which makes the magnitude of C_{rss} and its variation with V_{DG} the parameters of importance. The analysis is simplified somewhat if it is recognized that since $\Delta V_{GS} = 0$, $\Delta V_{DG} = \Delta V_{DS}$. That allows computation of C_{rss} from $\Delta Q/\Delta V_{DS}$ instead of $\Delta Q/\Delta V_{DG}$.

During the the V_{GS} plateau there is a distinct change in the slope of the V_{DS} waveform as the voltage nears $V_{DS(on)}$. In the first portion of the plateau C_{rss} is approximately 100 pF (4 nC/40 V), which appropriately corresponds to the highest drain-to-gate voltage in Figure 6-10. After that inflection point the turn-on process slows considerably, hinting of a much larger capacitance. Indeed, C_{rss} during the second portion of the plateau is roughly 7 nC/10 V or 700 pF. That value corresponds to a V_{DG} of around −5 V on the C_{rss} versus V_{DG} curve. So although C_{rss} varies throughout its entire range during the V_{DS} transition, it could be modeled as taking on only a pair of values. One value would correspond to positive drain-to-gate voltages and a second figure for negative voltages.

The drain-to-gate voltage waveform associated with Figure 6-8 is shown in Figure 6-9. This photograph clearly shows that just before V_{DG} changes polarity the slope changes and switching slows due to an abrupt increase in C_{rss}.

A look at the gate-to-source capacitance and its variation with V_{GS} completes the analysis of how the input impedance varies during the switching cycle. From Figure 6-10 and the equation $C_{gs} = C_{iss}-C_{rss}$, C_{gs} is easily determined. It is commonly assumed that C_{gs} is an invariant capacitor formed by the polysilicon gate and the source metallization. This belief is supported by the traditional representation of the capacitance curves. However, for many devices a large portion of C_{gs} is the capacitance between the gate and the channel, and this capacitance varies considerably as the device turns on.

The now familiar pattern of modeling the capacitor with two values reappears. From Figure 6-10 the value of C_{gs} before and during turn-on is nearly 500 pF whereas after turn-on it falls to less than 200 pF. As was previously shown for the MTH6N60, integrating these curves over the correct voltage ranges yields gate charge figures that are very close to data on gate charge curves.

There is some confusion regarding the slope of the V_{GS} waveform during the plateau region. It is often stated that during the plateau the slope is an indication of the gain of the device. This is true for resistive loads, but the reactive nature of the load also strongly affects the magnitude of the slope.

In many gate charge test circuits a MOSFET that is the same device type as the device under test is used as a constant current source in the drain. For an ideal current source the turn-on load line is capacitive, that is, the drain current reaches its steady state value just as the drain voltage begins to fall. Except for the premature dip in V_{DS} due to the MOSFET being an imperfect current source, Figure 6-8 illustrates this phase relationship quite nicely.

Figure 6-8 also clearly shows that the slope of the V_{GS} waveform in the plateau region is zero. This should be expected from the load line shown in Figure 6-11. First I_D rises to 15 A before any appreciable change in V_{DS}. Then during the entire V_{DS} transition I_D is constant, requiring no change in V_{GS}.

Once the basic concepts of gate charge characterization are mastered, understanding the effect of varying load

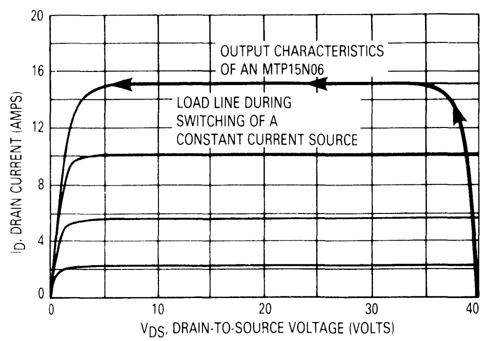


FIGURE 6-11 — CURRENT SOURCE YIELDS A CAPACITIVE LOAD LINE AT TURN-ON

current and supply voltage is simple. As I_D increases, the required gate-to-source voltage, which is dictated by the transfer characteristics, also increases. As Figure 6-12 shows, this causes the plateau to occur at higher voltages. Figure 6-13 shows the effect of changing V_{DD}. Varying V_{DD} changes the potential through which C_{rss} must be charged. The increased charge requirements account for the lengthening of the plateau at greater supply voltages.

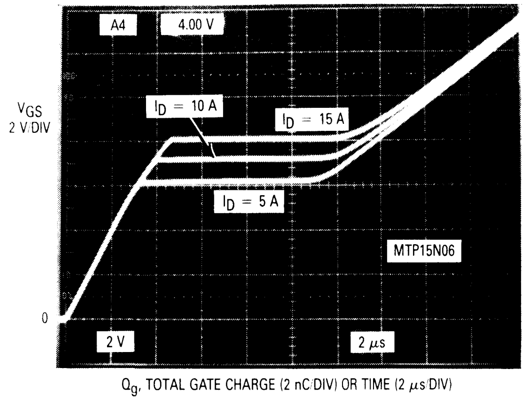


FIGURE 6-12 — INCREASING DRAIN CURRENT RAISES THE HEIGHT OF THE PLATEAU

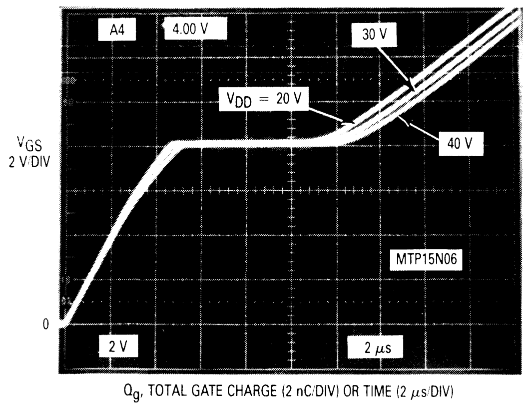


FIGURE 6-13 — INCREASING THE SUPPLY VOLTAGE CAUSES THE PLATEAU TO LENGTHEN

Uses of Gate Charge Data

Sometimes gate charge is politely thought of as an interesting, but not particularly useful, parameter. Often engineers do not develop an interest in the parameter simply because using gate charge is not the conventional method of determining input impedance. Although using gate charge may be somewhat different from typical approaches, it is not difficult, and it certainly is a useful and informative specification.

Of course, the most straightforward use of gate charge data is to help determine the amount of charge that must be supplied to the gate to fully turn-on a device. That charge can be separated into three parts, each of which coincides with the requirements of a portion of the switching interval. The first portion defines the charge needed during the turn-on delay; the second indicates the charge necessary to effect the rise or fall of V_{DS}; and the charge in the third region is associated with the turn-off delay. Also the curve clearly defines the penalty of additional charge exacted for using an unnecessarily large gate-to-source voltage.

Once the amount of charge is known, determining the current required to obtain a desired switching speed is an exercise in basic algebra ($q = it$). In Figure 6-8 the voltage fall time occurs while a charge equal to $Q_2 - Q_1$, or 8 nC, is being supplied. Therefore, a 100 ns transition requires an average I_G of 8 nC/100 ns, or 80 mA.

The major limitation of this type of analysis is that gate drives are rarely constant current sources. Most are more accurately represented as a voltage source in series with a fixed internal resistance. Therefore, what is normally of interest to a designer is the value of resistance required for a given switching speed.

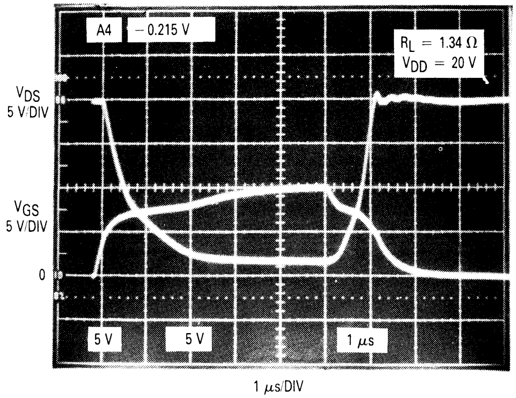
With a few reasonable assumptions, gate charge concepts can be successfully applied in this instance, too. The basic concepts here are (1) except for extraordinarily fast switching speeds (<50 ns) the rise of the gate-to-source voltage stalls in a plateau region, regardless of the type of gate drive and (2) the drain-to-source voltage excursions occur during the plateau of V_{GS}.

When the gate voltage stalls during turn-on, the voltage across the gate drive resistance is simply $V_{GG} - V_{GS(plateau)}$ and I_G is equal to this voltage drop divided by the drive impedance (Figure 6-14c). The nearly constant I_G during the fall of V_{DS} is shown in Figure 6-14b. This provides the link to the use of gate charge data.

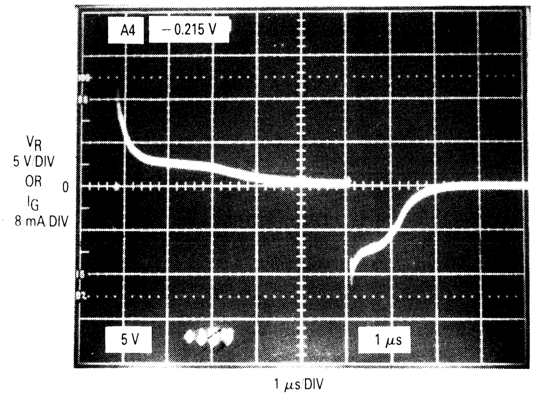
Suppose, for example, that the desired V_{DS} fall time during turn-on of the MTP15N06 is 2 μs. This time and the 8 nC of required gate charge, which is the charge during the plateau of Figure 6-12, fix the necessary gate drive current at 4 mA (8 nC/2 μs). For a 10 A load the plateau occurs at a V_{GS} of 7.5 V, and with a 10 V gate drive the potential across the gate drive internal impedance is only 2.5 V. These figures yield a gate resistance of 620 ohms (= 2.5 V/4 mA). As the oscilloscope waveforms of Figure 6-14 show, this method of selecting gate drive impedance is fairly accurate. As expected, decreasing the gate drive impedance by a factor of ten brings a tenfold decrease in switching time.

It is also enlightening to pursue the reason for the more rapid turn-off in Figure 6-14 even though the gate drive impedance at turn-on and turn-off are the same. The answer is simple; the gate current is greater due to a higher potential across the internal impedance. The current during the turn-off plateau is $V_{GS(plateau)} - V_{GS(off)}$ divided by R_G. In this case the numbers are (7.5 − 0 V) ÷ 620 ohms, or about 12 mA, instead of the 4 mA at turn-on. As it should be, the ratio of currents is proportional to the switching speed.

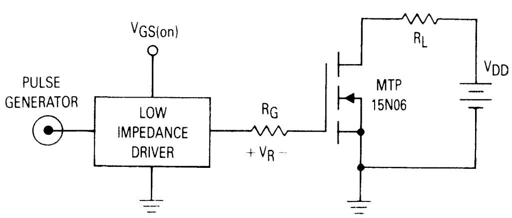
The second major benefit of the concept of gate charge is that it enhances understanding of the MOSFET's switching behavior. Three examples prove this point. First,



(a) GATE-TO-SOURCE AND DRAIN-TO-SOURCE VOLTAGE WAVEFORMS DURING RESISTIVE SWITCHING



(b) GATE CURRENT



(c) SWITCHING SPEED TEST CIRCUIT

FIGURE 6-14 — BECAUSE THE GATE-TO-SOURCE VOLTAGE AND GATE CURRENT ARE RELATIVELY CONSTANT DURING THE V_{DS} EXCURSIONS, GATE CHARGE CAN BE USED TO ESTIMATE GATE DRIVER IMPEDANCE FOR A DESIRED SWITCHING SPEED.

understanding that the MOSFET is controlled by gate charge helps in predicting the effect of the gate drive impedance on switching speeds. Theoretically, halving the impedance of the gate drive should double the rate of charging and halve the switching times. This has been shown to hold true over a five decade change in gate drive current.

Second, the concepts reveal the weakness of using or specifying only the values of capacitance at a single point on the capacitance versus voltage curves. And third, they show that even though C_{GS} is the larger of the input capacitances at a V_{DS} of 25 V, C_{rss} has the greater effect during most of the switching interval.

A more subtle benefit of the gate charge curve is that it provides the data required for accurate device modeling. As was shown earlier, the input impedance and the switching behavior of the MOSFET can be modeled by selecting values of C_{rss} and C_{gs} from the slopes of the gate charge waveform. Using these values yields results that are much more meaningful than those obtained by using a single value of each capacitor at V_{DS} of 25 V.

The trend towards the use of higher switching frequencies in such applications as the series resonant power supply make estimation of required gate charge and transferred energy of increasing importance. As operating frequencies increase, the MOSFET's "high input impedance" eventually consumes substantial drive current. Charging and discharging C_{iss} (and C_{oss}) every cycle can result in an energy loss large enough to affect overall efficiency. In addition to its other more common uses, the gate charge curve also helps in estimating the energy consumed by the gate.

The familiar formulas, $E = 1/2\ CV^2$ and $1/2\ QV$, apply only to fixed values of capacitance. For voltage dependent capacitors such as the C_{iss} of the power MOSFET, the gate voltage versus gate charge curve must be integrated between $V_{GS(off)}$ and $V_{GS(on)}$ to determine transferred energy. This energy is stored in C_{iss} during turn-on and is normally lost when the gate is clamped to the source at turn-off. Multiplication of this energy by the switching frequency gives the associated power loss.

For example, consider the energy stored in the input capacitance of the MTM15N50. For a V_{GG} of 10 V the area under the curve in Figure 6-15 is 0.625 μJ. This loss

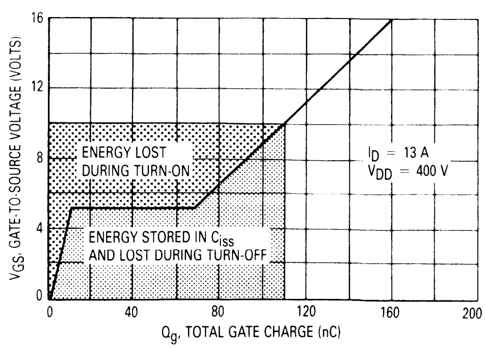


FIGURE 6-15 — THE GATE CHARGE CURVE OF THE MTM15N50 GIVES INFORMATION REGARDING THE ENERGY CONSUMED WHILE DRIVING THE MOSEFET's GATE.

normally goes unnoticed even though this device is one of the largest available. Even at a switching frequency of 1 MHz, the dissipated energy is only 0.625 watts. Note, however, that if the gate is driven to a V_{GG} of 16 V then the losses rise to 1.275 μJ and 1.275 W.

Yet to be included in this analysis of drive losses is the energy consumed by the gate drive as it delivers the required gate charge. Figure 6-16 shows the equivalent circuit of an idealized gate drive network in which S_1 completes the charging path and S_2 controls discharging.

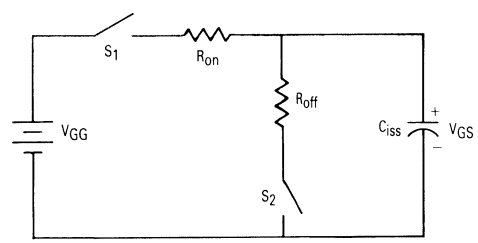


FIGURE 6-16 — IDEALIZED GATE DRIVE CIRCUIT

Regardless of the magnitude of the equivalent resistance and the rate of charging, the size of C_{iss} and $V_{GS(on)}$ determine the energy transferred during turn-on and dissipated at turn-off. Likewise, the energy dissipated in R_{on} is also independent of the size of R_{on} and the gate drive current. Again, integration of a Q versus V curve gives energy, but this time the appropriate voltage is $V_{GG} - V_{GS}$. This integration is equivalent to finding the area between the gate charge curve and $V_{GS} - V_{GG}$.

Now the picture of the gate drive losses is complete. Total losses are simply $V_{GS(on)}$ times the required gate charge.

Common Source Switching

TTL Gate-Drives

Driving a TMOS power transistor directly from a CMOS or open-collector TTL device is possible, but this circuit simplicity is obtained at the cost of slower switching speeds due to the charging current required by the MOSFET's parasitic input capacitance and the limited source and sink capabilities of these drivers.

A TTL device with a totem pole output and no additional circuitry is generally not an acceptable gate-drive network. In this case, the output voltage available is approximately 3.5 volts, which is insufficient to ensure the MOSFET will be driven into the ohmic region. A slightly more promising situation would be to use a pull-up resistor on the TTL output to utilize the entire 5.0 V supply, but even the full 5.0 V on the gate would not guarantee the MOSFET will conduct even half of its rated continuous drain current.

The open-collector TTL device, when used with a pull-up resistor tied to a separate 10 to 15 V supply, can guarantee rapid gate turn-off and ensure sufficient gate voltage to turn the MOSFET fully on (Figure 6-17). Turn-on is not as rapid because the pull-up resistor must be sized to limit power dissipation in the lower TTL output transistor. However, when concerned about dynamic losses incurred while switching an inductive load, the gate fall time is more critical than the rise time due to the phase relationship between the drain current and drain-source voltage. Figure 6-18 shows a configuration providing fast turn-on, yet reducing power dissipation in the TTL device.

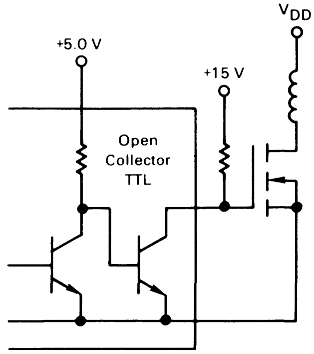


FIGURE 6-17 — DRIVING TMOS WITH OPEN COLLECTOR TTL

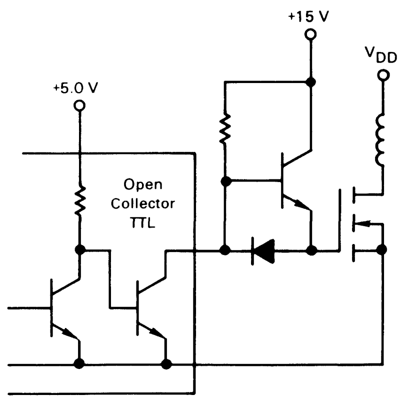


FIGURE 6-18 — OPEN COLLECTOR TTL-TMOS INTERFACE FOR FASTER TURN-ON AND REDUCED POWER DISSIPATION

When the lower transistor in the TTL output stage is turned on, shunting the MOSFET input capacitance to ground, modeling the bipolar as a saturated device may not be appropriate. The current sinking capabilities of TTL devices in the low output state is limited by the beta of the pull-down transistor and its available base current, which varies with the product line and TTL family. Table 1 shows the current source and sink capabilities of various TTL families.

Although the TTL peak current sinking capability might be twice the continuous rating, faster turn-off can be achieved by using an outboard transistor to clamp the gate-to-ground (Figure 6-19). In this configuration, the bipolars are operating as emitter followers. As such, they are never driven into saturation and their associated storage times do not significantly affect the switching frequency limit.

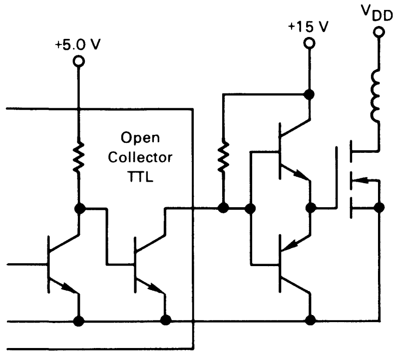


FIGURE 6-19 — OPEN COLLECTOR TTL DRIVING COMPLEMENTARY EMITTER FOLLOWER

CMOS Gate Drives

Driving the power MOSFET directly from CMOS presents a different set of advantages and disadvantages. Perhaps most important, CMOS and power MOSFETs can be operated from the same 10 to 15 volt supply. A gate voltage of at least 10 volts will ensure the MOSFET is operating in its ohmic region when conducting its rated continuous current. This benefit allows the designer to directly interface CMOS and TMOS without any additional circuitry including external pull-up resistors. Again, however, circuit simplicity results in slower MOSFET switching due to the limited current source and sink capabilities of CMOS devices. Table 2 compares the output current capabilities of standard CMOS gates to that of the CMOS buffers (MC14049, 14050). Note that while the current sinking capacity of the buffers is improved significantly over that of the standard CMOS gate, the current sourcing capacity is not. The figures in Tables 1 and 2 indicate the current at which the device can still maintain its output voltage within the proper logic level for a given logic state.

TABLE 1 — TTL Output Current Source and Sink Capabilities

	Output Drive	
Family	High (Source)	Low (Sink)
74LS00	0.4 mA	8.0 mA
7400	0.8 mA	16 mA
9000	0.8 mA	16 mA
74H00	1.0 mA	20 mA
74S00	1.0 mA	20 mA

As an illustration, with a V_{DS} of 15 V, a standard CMOS gate can typically source 8.8 mA in the HIGH state without its output falling below 13.5 volts.

If the switching speeds of CMOS buffers are not rapid enough, the discrete buffers suggested for use with TTL devices (Figures 6-18 and 6-19) can also be used to interface CMOS to TMOS. The only difference is the pull-up resistors are unnecessary for CMOS. Another difference in the two technologies that may affect the maximum switching frequency limit is that the TTL gates typically have faster switching times.

Other Gate Drives

In certain situations pulse transformers are an effective means of driving the gate of a power MOSFET. They provide the isolation needed to drive bridge configurations or to control an N-Channel MOSFET driving a grounded load. One of the simplest examples of such a circuit is the first circuit in Table 3 where the rise, fall, and delay times for this and the other circuits to be discussed are tabulated.

The diode in Circuit 1 is present simply to limit the flyback voltage appearing across the drive transistor Q1. A transformer turns ratio of one-to-one was chosen to provide an appropriate voltage at the secondary given the 15 volt primary supply voltage. A potential problem with this circuit is that the duty cycle influences the magnitude of V_{GS} because the volt-seconds produced during the on and off intervals at the secondary must sum to zero. Figure 6-20 indicates that increasing the duty cycle decreases the maximum gate-source voltage. As the duty cycle increases above 33%, for the given primary voltage of 15 volts, the peak gate voltage falls below 10 volts and may eventually drop to a point where the device is no longer operating in the ohmic region. Increasing the primary voltage to 20 volts would increase the maximum allowable duty cycle.

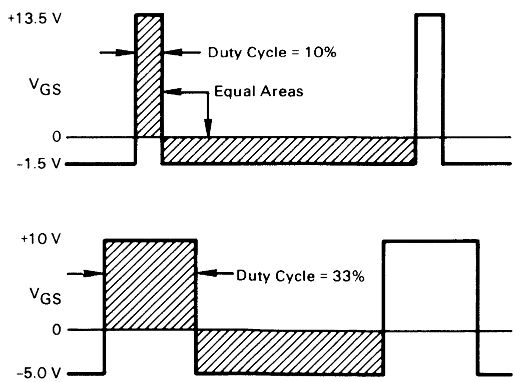


FIGURE 6-20 — VARIATION OF V_{GS} WITH DUTY CYCLE IN PULSE TRANSFORMER GATE-DRIVE

The basic pulse transformer topology of Circuit 1 also has both maximum and minimum pulse width limitations in addition to those imposed by the volt-seconds requirements. The current in the primary winding may ramp-up to excessive levels due to magnetic saturation, especially

TABLE 2 — CMOS Current Source and Sink Capabilities

			B-Series Gates (MC14001CP)		CMOS Buffers (MC14049, 14050CP)	
		V_{DD}	Min (mA)	Typ (mA)	Min (mA)	Typ (mA)
Current Source Capability	V_{OH} = 2.5 V	5.0 V	-2.1	-4.2	-1.25	-2.5
	V_{OH} = 9.5 V	10 V	-1.1	-2.25	-1.25	-2.5
	V_{OH} = 13.5 V	15 V	-3.0	-8.8	-3.75	-10
Current Sink Capability	V_{OL} = 0.4 V	5.0V	0.44	0.88	3.2	6.0
	V_{OL} = 0.5 V	10 V	1.1	2.25	8.0	16
	V_{OL} = 1.5 V	15 V	3.0	8.8	24	40

in the smaller pulse transformers, if the pulse width is too wide. On the other hand, very short pulse widths may cause two different problems. First, transformer leakage inductance may limit current sourcing capability during a significant portion of the turn-on interval of a very small pulse width. Second, the pulse width must be wide enough to allow the magnetizing current (I_m) to ramp-up significantly, because the stored energy (defined by the current in the magnetizing inductance) provides turn-off drive to the MOSFET gate. To eliminate the problem of I_m varying with pulse width and to improve turn-off drive, the circuit shown in Figure 6-21 may be used.

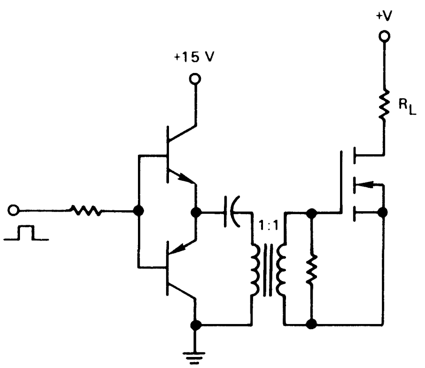


FIGURE 6-21 — CIRCUIT TO ELIMINATE THE VARYING OF I_m WITH PULSE WIDTH

A modification to the basic transformer gate-drive circuit described above is the addition of a zener diode in series with the clamping diode (Circuit 2). The zener allows additional flyback voltage to appear across the primary terminal, when Q1 is turned off. When this additional potential is induced across the secondary, it initially provides greater reset voltage levels and, thus, more rapid gate turn-off. Naturally, inherent in this circuit are the same duty cycle, pulse width and frequency limitations that accompanied Circuit 1.

Circuit 3 is very similar to Circuit 1 except the gate resistances are scaled upward and one is shunted by a diode. The purpose of this configuration is to speed up the MOSFET turn-on while leaving the turn-off slow in comparison. While the MOSFET input capacitance can charge rapidly through the diode, it must discharge through the two relatively high impedance gate resistances. This might be done to minimize inductive flyback voltage or any other undesired phenomena occurring during very rapid turn-off.

A variation of the push-pull converter is used to drive the gate of the MOSFET in Circuit 4. When Q1 is turned on, the 10 volts across the lower of the two primary windings induces the same potential in N_2. The voltage seen at the secondary, due to the 2:1 step-down ratio ($N_1 + N_2/N_3$), equals the primary supply voltage. At turn-off, the potential across N_2 reverses and is clamped to the 10 V supply by D1. Now N_2 induces its voltage in N_1 and the potential appearing at the secondary reverses in polarity but the magnitude is still 10 volts. If the pulse width is long enough to generate sufficient magnetizing current, this circuit yields good current sinking capabilities.

Two opto-coupled drive circuits are shown in Circuits 5 and 6. Circuit 5 is one of the most straightforward ways of developing a low impedance gate-drive from the output of the optocoupler. This circuit, however, is plagued by long switching delays that limit the useful operating frequency. These delays are inherent in the optocoupler and their magnitudes are affected by the phototransistor's output load impedance. If this impedance is lowered, as accomplished with Circuit 6, the gate-drive turn-off delay is significantly lower. Besides the complexity of these circuits, especially Circuit 6, the gate-drive's bipolar output transistor, Q2, must remain on the entire time that the MOSFET is off. The energy dissipated in these two drivers during low duty cycle operation may be critical if efficiency is a major concern.

Circuits 7 and 8 are similar versions of a circuit that can be used as a high performance gate-drive. The base currents for the bipolar drives must be push-pulled as shown in Figure 6-22. MOSFET turn-on is initiated during a positive transition of the input pulse. Q1 is turned on, supplying the required base current for Q3, which is Baker clamped to minimize its turn-off storage time. Both circuits have excellent turn-on times because of the low impedance path provided between the supply and the gate of the MOSFET.

TABLE 3 — Switching Speeds of Various TMOS Gate Drives

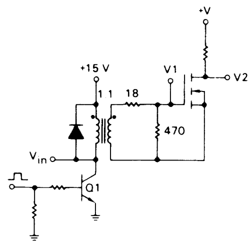
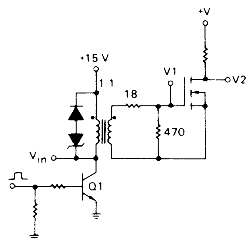
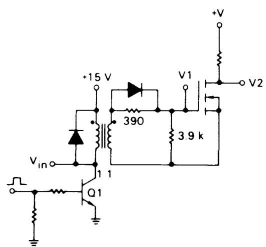
Circuit	Schematic		Gate Switching Times (ns) Turn-on Delay (V_{in} vs V_1)	Gate Switching Times (ns) Turn-on Rise Time	Gate Switching Times (ns) Turn-off Delay (V_{in} vs V_1)	Gate Switching Times (ns) Turn-off Fall Time	Drain Switching Times (ns) Turn-on Delay (V_{in} vs V_2)	Drain Switching Times (ns) Turn-on Fall Time	Drain Switching Times (ns) Turn-off Delay (V_{in} vs V_2)	Drain Switching Times (ns) Turn-off Rise Time
Circuit 1 Simple Pulse Transformer			15	85	35	230	25	25	185	20
Circuit 2 Pulse Transformer w/Flyback Zener			15	90	25	190	30	25	125	35
Circuit 3 Pulse Transformer w/Speed-up Diode		With Diode D1	30	95	220	1250	60	35	640	230
		Without Diode D1	50	1500	280	1100	220	340	660	230

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TABLE 3 — Switching Speeds of Various TMOS Gate Drives (continued)

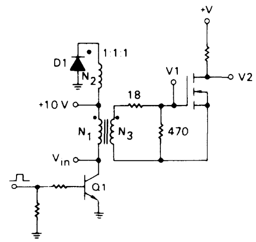
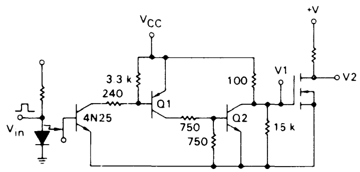
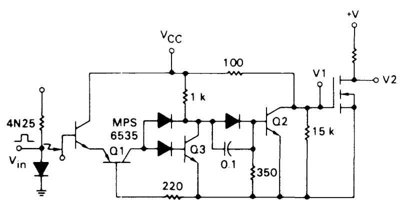
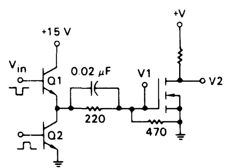
		Gate Switching Times (ns)				Drain Switching Times (ns)			
		Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 4 Quasi Push-Pull Transformer Drive		15	85	40	230	30	25	160	35
Circuit 5 Standard Opto-Coupling Circuit		3900	460	1600	140	4000	80	1750	20
Circuit 6 High B.W. Opto-Coupling Circuit		3700	420	450	120	3800	75	520	20
Circuit 7 High Performance Push-Pull Circuit		20	60	25	30	30	20	45	15

TABLE 3 — Switching Speeds of Various TMOS Gate Drives (continued)

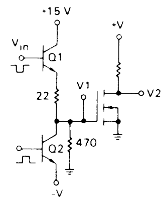
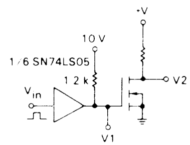
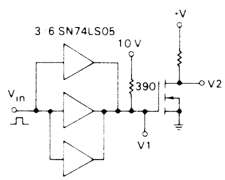
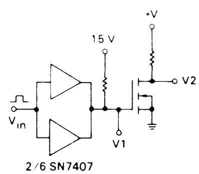
		Gate Switching Times (ns)				Drain Switching Times (ns)			
		Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 8 High Performance Push-Pull Circuit		20	60	45	70	40	25	85	15
Circuit 9 Low Power Schottky TTL		110	5000	60	600	480	1000	375	150
Circuit 10 Paralleled Low Power Schottky TTL		45	1800	30	210	180	310	140	50
Circuit 11 Paralleled SN7407 Buffers with Pull-Up Resistance		25	710	30	140	60	60	130	30

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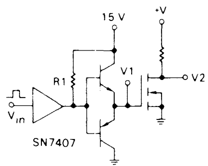
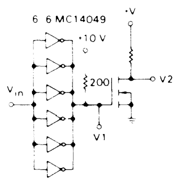
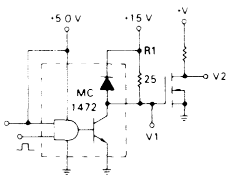
TABLE 3 — Switching Speeds of Various TMOS Gate Drives (continued)

			Gate Switching Times (ns)				Drain Switching Times (ns)			
			Turn-on Delay (V_{in} vs V_1)	Turn-on Rise Time	Turn-off Delay (V_{in} vs V_1)	Turn-off Fall Time	Turn-on Delay (V_{in} vs V_2)	Turn-on Fall Time	Turn-off Delay (V_{in} vs V_2)	Turn-off Rise Time
Circuit 12 SN7407 Buffer Driving a Complementary Emitter-Follower		R1 = 2.0 k	30	140	20	20	50	20	40	10
		R1 = 5.1 k	60	430	20	20	110	40	40	10
Circuit 13 Six Paralleled CMOS Inverters (MC14049UB)			30	920	20	130	100	160	90	30
Circuit 14 Dual Peripheral Driver (MC1472)			370	100	170	80	280	50	230	15
	*Transformer Specs: Ferroxcube 3019P3CB $N_1 = N_2 = N_3 = 10$ Turns #19 Trifilar Wound $L_P \approx 0.6$ mH									

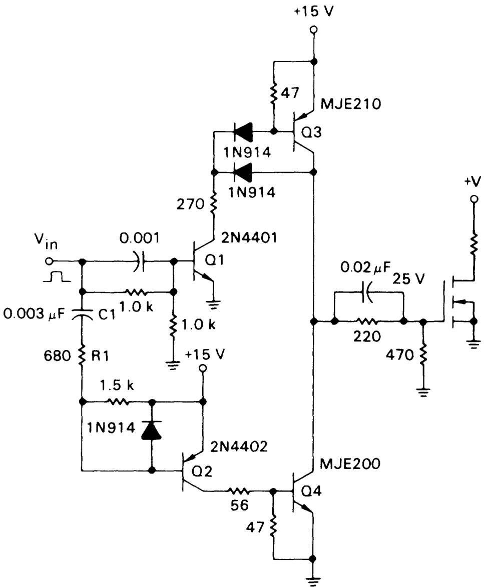


FIGURE 6-22 — PUSH-PULL BASE DRIVE FOR CIRCUITS 7 AND 8

Turn-off occurs when the falling edge of the input pulse is differentiated by the series combination of R1 and C1, thus turning on Q2. Base current is then free to flow into Q4, clamping the gate-to-ground or a negative potential. The duration of the clamping interval may be adjusted by varying the RC network. Before the occurrence of another input pulse, the MOSFET will remain off due to the 470 Ω gate-source resistance.

Circuits 9 through 12 are examples of how TTL devices may interface with the TMOS power MOSFET. The first of the circuits, number 9, has a very simple interface between the open collector, Low Power Schottky SN74LS05 hex inverter and the MTP12N10. Turn-off speed is fair, considering the circuit simplicity, but turn-on speed is poor because of the large value of R1 needed to protect the inverter from excessive power dissipation when the TTL output is low. Putting three such buffers in parallel, Circuit 10, reduces all the associated switching times by a factor of nearly two-thirds.

Another TTL device with an open collector output is utilized in Circuit 11. Two of the six buffers in the SN7407 operate in parallel with only a pull-up resistor and the gate of the MOSFET connected to the collector of the high voltage (30 volts) output transistors. The associated switching times are quite respectable given the simplicity of the drive circuit.

Another application of the SN7407, as mentioned earlier, is to use it to drive a discrete complementary emitter-follower buffer (Circuit 12). Lowering the pull-up resistor, R1, increases the turn-on speed at the expense of increasing gate turn-off power dissipation.

Figure 6-23 shows an MTM12N10 being driven by a CMOS MC14050CL Hex Buffer. To obtain the maximum output current source and sink capability, all six buffer elements are paralleled.

While the pull-up resistor is not a necessity (as it is with open-collector TTL devices), it does balance the current source and sink capabilities of the CMOS buffer. Without that resistor, one could expect slower turn-on but the drive circuit would be more efficient because the CMOS device no longer must sink the current drawn through R1 when the CMOS outputs are low. Of course, fewer than the six paralleled inverters could be used at the cost of slower switching. Figure 6-24 shows the switching waveforms without a pull-up resistor. For the six buffer elements in parallel the peak I_G during turn-on is about 350 mA and 900 mA during turn-off.

While not as fast as other more elaborate drive circuits, the MC14050CL offers an inexpensive single power supply device that interfaces directly to CMOS and MHTL circuitry.

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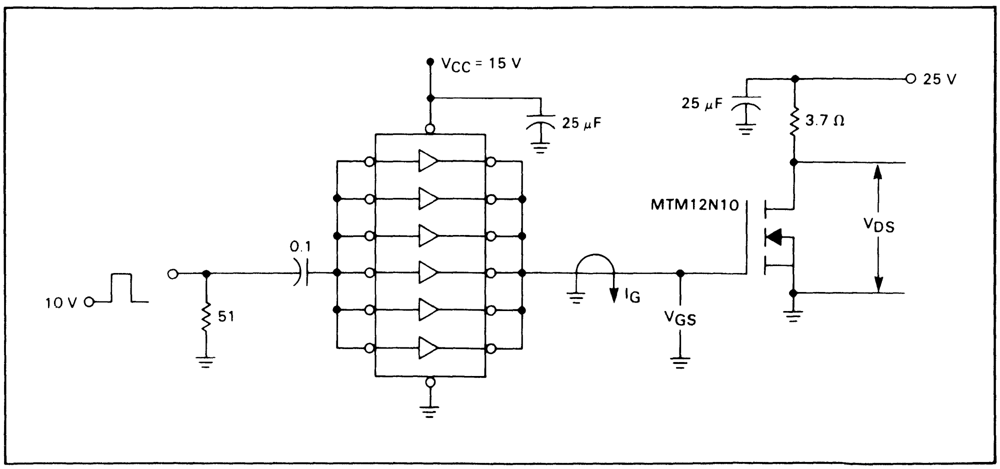


FIGURE 6-23 — MC14050CL HEX BUFFER AS A DRIVER FOR POWER MOSFET

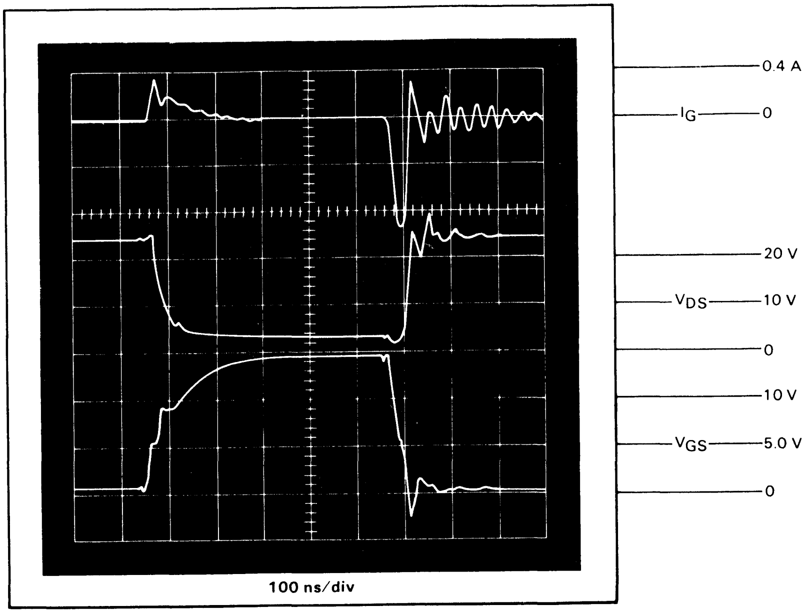


FIGURE 6-24 — POWER MOSFET SWITCHING WAVEFORMS
WITH MC14050CL HEX BUFFER
(6 BUFFER ELEMENTS IN PARALLEL)

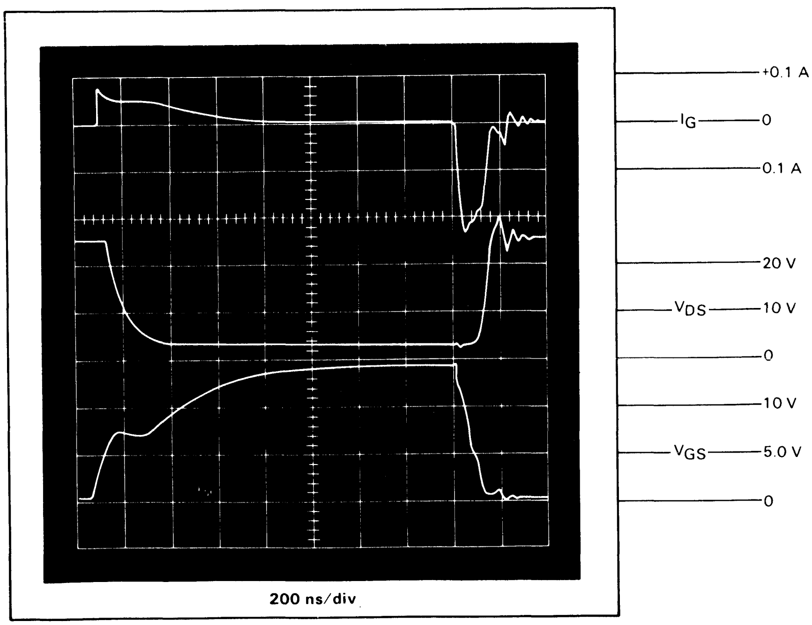


FIGURE 6-25 — POWER MOSFET SWITCHING WAVEFORMS
WITH MC14050CL HEX BUFFER
(SINGLE BUFFER ELEMENT)

Figure 6-25 shows the results of the MTM12N10 being driven by a single MC14050CL buffer element. Note the time scale has been doubled to allow V_{GS} to rise to its upper rail. The gate current scale is a factor of four smaller: peak gate currents of about 70 mA during turn-on and 240 mA during turn-off are seen.

Several ICs that were originally intended for other applications have been adopted by some circuit designers looking for fast, yet simple and efficient MOSFET gate-drive schemes. One such device is the MC1472, a dual peripheral driver, designed to interface MOS logic to high current loads such as relays, lamps and printer hammers. Because each of the two output transistors can sink 300 mA, MOSFET turn-off times are short when this device is used in a gate-drive network. Turn-on times are also short in Circuit 14 because the value of R1 is so low that it only minimally impedes the current during the charging of the MOSFET input capacitances. The advantage of this large current sourcing capability is once again offset by the significant currents that will flow whenever the MC1472 output is low to turn the MOSFET off. In fact, for the 25 ohm pull-up resistor and a V_{CC1} of 15 volts, that current approaches the combined sinking capabilities of the two output transistors in that package.

The DS0026 Clock Driver has been designed to drive high capacitance loads. It features a peak output current of 1.5 A and transition times of about 30 ns when driving capacitance loads equivalent to the C_{iss} of a power MOSFET. Input drive voltages for the DS0026 are compatible with Series 54/74 TTL devices, such as the MC7405 Hex Inverter (OC). Detailed information regarding transition times versus load capacitance and power dissipation can be found in the DS0026 data sheet.

Figure 6-26 identifies the DS0026 driving an MTM12N10. To illustrate the high peak gate currents that can be sourced by the DS0026, no resistance was included between driver output and MOSFET gate. It is important to remember that, with gate current transitions occurring in the low nanosecond range, any lead inductance between driver and gate will add (L/R_g) delay to the gate circuit. Keep the distance between driver output and gate terminal as short as possible when fast switching times are important.

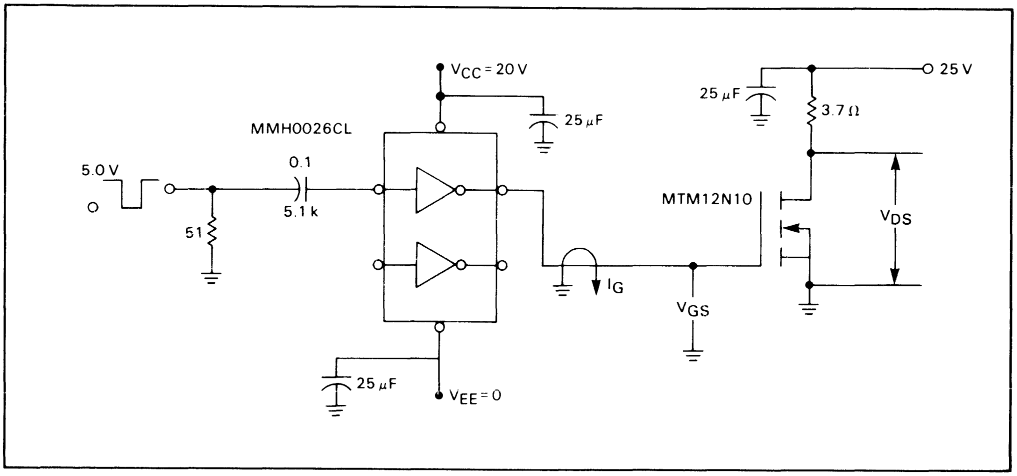


FIGURE 6-26 — DS0026 CLOCK DRIVER AS A DRIVER FOR POWER MOSFET

Input/output waveforms of the MTM12N10 are shown in Figure 6-27. Although not shown, the maximum drain current was 5.8 A. Figure 6-27 shows that 1.2 A gate current spike that occurs during the turn-on phase, and the 1.5 A negative current pulse occurring during the turn-off phase as C_{gd} is re-charged through the 3.7 ohm load resistor by the 25 V supply. The high voltage pulse that occurs as V_{DS} rises towards 25 V can be attributed to the kick-back of the 3.7 ohm load resistor's parasitic inductance of about 90 nH. This drain voltage spike can be limited by the insertion of an appropriately sized resistor in series with the DS0026 and the gate of the MTM12N10, to increase the R_gC_{iss} time constant, if the increase in turn-on time is acceptable.

Other examples of ICs that are used to drive the gate of a power MOSFET are the MC1555 timer, the TL494 pulse width modulation control circuit and the MC75451 peripheral driver. As power MOSFETs gain in popularity, more drivers specifically designed for MOSFETs will appear.

High Side Switching

In some situations, connecting the load to the negative bus is either convenient or necessary. In such instances the switching element must be referenced to the positive rail as shown in Figure 6-28. As with PNP and NPN bipolars, both P-channel and N-channel power MOSFETs

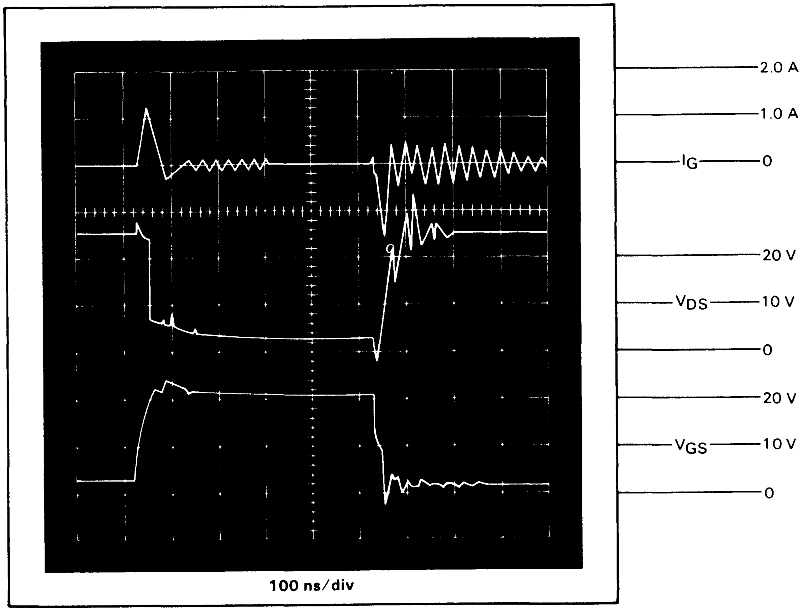


FIGURE 6-27 — POWER MOSFET SWITCHING WAVEFORMS WITH DS0026 CLOCK DRIVER

can perform this switching function. The following discussion of high side switching centers about the P-channel in a common source configuration, and an N-channel source follower as illustrated in Figures 6-29a and 6-29b. All of the concepts presented also apply to the upper switch (or switches) in totem pole or bridge configurations. Figure 6-29c shows that Q1 is essentially operating in a source follower mode when Q2 is turned off and is effectively out of the circuit.

P-Channel Power MOSFETs

To complement some of the N-channel devices, Motorola also produces P-channel power MOSFETs. Because current carriers in the P-channel devices are holes, which have lower mobility than the electron carriers of the N-channel devices, the $r_{DS(on)}$ of P-channel MOSFETs is always greater for a given die size and drain-source breakdown voltage. This impedes the development of truly complementary devices. For instance, if equal on-resistances are desired, the unequal die dimensions will mandate differences in all die area dependent parameters such as capacitances, pulsed current ratings, thermal resistance and safe operating areas.

The application will determine which of the device parameters — whether it be the on-resistance, drain-source breakdown voltage, transconductance, etc. — need be matched closely. Table 4 compares the pertinent electrical

FIGURE 6-28 — HIGH SIDE SWITCHING

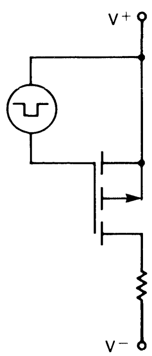


FIGURE 6-29a — P-CHANNEL IN A COMMON SOURCE CONFIGURATION

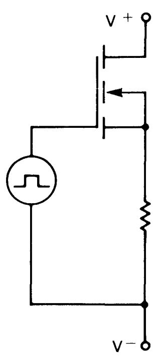


FIGURE 6-29b — N-CHANNEL AS A SOURCE FOLLOWER

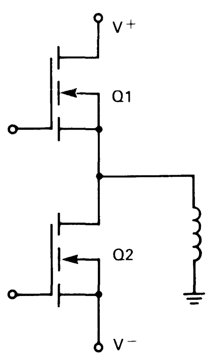


FIGURE 6-29c — TOTEM POLE NETWORK REQUIRES HIGH SIDE SWITCHING parameters of the MTP8P10 with those of N-channel devices that may be considered as device complements. Besides showing the MTP8N10 is not always the best choice for a complement to the MTP8P10, the table also indicates the die area of a P-channel device must be approximately doubled to achieve the on-resistance of an N-channel device with the same $V_{(BR)DSS}$ rating.

P-channel power MOSFETs can simplify certain circuit configurations much in the same way that PNP bipolars can. The circuit simplicity obtained when using P-channel devices to switch a grounded load, for instance, may more than offset the price differential between the N- and P-channel devices.

In Figure 6-30 the source is connected to the positive rail and the drain is attached to the load. As such, the MOSFET is off when $V_{GS} = 0$ V and begins to turn on as V_{GS} (a negative quantity) rises in absolute magnitude above the device threshold voltage. Current would then be free to flow from the source-to-drain and into the load. Still, a logic signal, which is normally referenced to ground, must be used to control the gate. A level shifter, followed by a discrete emitter-follower buffer can supply the proper logic levels while at the same time provide rapid MOSFET switching. The NPN-PNP buffer could be omitted if slower switching is desired.

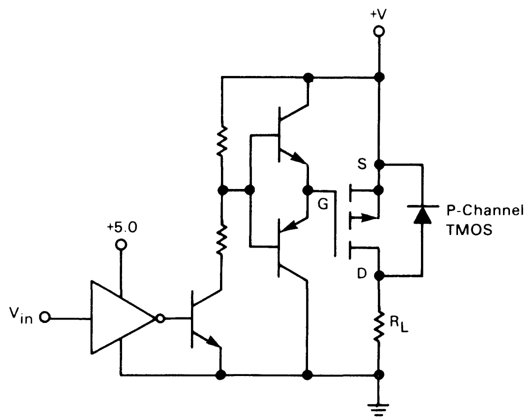


FIGURE 6-30 — LEVEL SHIFTER FOR P-CHANNEL MOSFET DRIVING A GROUNDED LOAD

2

N-Channel High Side Switching

Instead of using a P-channel as the high side switch, another choice is to use a less expensive N-channel power MOSFET with the load placed in the source circuit — a source follower.

Since there is no voltage gain in a source follower, the gate voltage must equal the output voltage plus the gate-source voltage at that particular load current. Also, for efficient power transfer, the source voltage, when switched on, should approach the positive rail (limited by $r_{DS(on)}$). Thus, the gate voltage should be well above the positive rail, i.e., $V_G = V_{GS(on)} + V_S \approx V_{GS(on)} + V_{DD}$. For hard gate turn-on, V_{GS} should be greater than 10 V. Consequently, the gate voltage for a 12 V system could approach 22 V. This higher than V_{DD} supply gate voltage can be achieved by several techniques:

1. A separate gate supply at least 10 V greater than V_{DD}.
2. Pulse Transformer
3. Optoisolator
4. Bootstrapping
5. Voltage doubler
6. Inductive (flyback)

2-6

TABLE 4 — Complements of MTP8P10

		P-Channel	N-Channel			Units
		MTP8P10	MTP8N10	MTP12N10	MTP20N10	
Drain-Source Voltage (Max)		100	100	100	100	Vdc
I_D	Continuous	8.0	8.0	12	20	Adc
	Pulsed	25	20	30	60	Adc
Max Power Dissipation		75	75	75	75	Watts
Threshold Voltage		2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	2.0 to 4.5	Vdc
On-Resistance @ $I_D/2$ (Max)		0.4	0.5	0.18	0.15	ohms
Transconductance (Min)		2.0	1.5	3.0	6.0	mhos
Input Capacitance (Max)		1200	400	1200	1400	pF
Output Capacitance (Max)		600	350	500	1200	pF
Reverse Transfer Capacitance (Max)		180	150	250	400	pF
Fall Time (Max)		150	60	100	200	ns
Rise Time (Max)		150	120	150	450	ns
Normalized Die Area		1.0	0.45	0.66	1.0	—

SEPARATE SUPPLY

The most straightfoward way to accomplish high side switching with an N-channel MOSFET is to drive its gate with a separate supply (Figure 6-31). The auxiliary supply voltage must be from 10 to 20 volts greater than V_{DD} to initiate turn-on. Inherent in the circuit simplicity is the obvious disadvantage of the need of the second supply, especially since its output must be greater than what is commonly the system's high voltage bus. Another consideration is that turn-off switching speeds will be degraded due to the flyback voltage forward biasing the gate-source unless the load inductance is clamped with a free-wheeling diode.

OPTOISOLATORS

A third way to drive a source follower is to reference the gate-drive signal to the source of the MOSFET with the aid of an optoisolator. Figure 6-33 is an example of such a drive network. As long as the V_{CC2} supply and the emitter of the optoisolator remain referenced to the source, the load can be common to either the source or the drain. The additional supply to power the output of the optoisolator must be able to raise the gate voltage above V_{DD}. Either the supply must be isolated from the V_{DD} supply or must be generated from it with a bootstrapping technique.

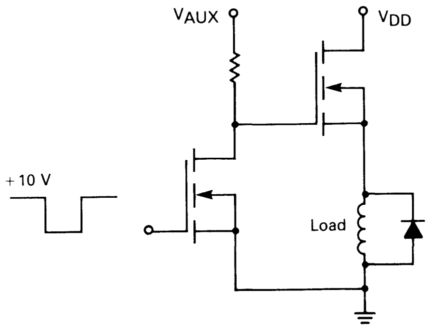


FIGURE 6-31 — HIGH SIDE SWITCHING USING AN AUXILIARY SUPPLY

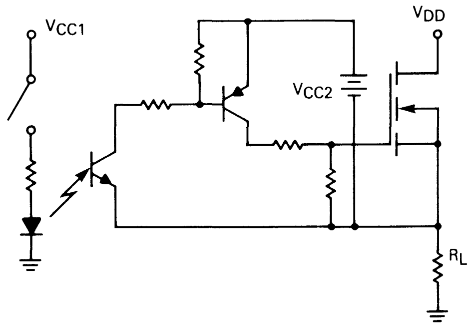


FIGURE 6-33 — DRIVING A SOURCE FOLLOWER WITH AN OPTOISOLATOR

PULSE TRANSFORMERS

Pulse transformers are a very popular and practical way of driving an N-channel MOSFET serving as the upper element in a bridge network or as any other high side switch. The beauty of the transformer drive is that the gate-drive signal is easily referenced to the source of the MOSFET, as Figure 6-32 illustrates. Circuits 1 through 4, (page 1-6-11 and 1-6-12) will perform just as well with the load common to the source and the drain tied to the positive rail. Other considerations for pulse transformer gate-drive design are also addressed in that section.

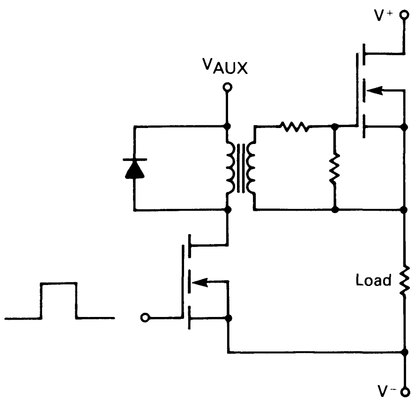


FIGURE 6-32 — PULSE TRANSFORMER DRIVER

BOOTSTRAPPING

The simplicity of bootstrapping makes that method the one of choice if its limitations are inconsequential in the specific application or they can somehow be circumvented. The bootstrapping circuit in Figure 6-34 generates the required gate-to-source signal. One of the main problems with this topology is that the load cannot remain in

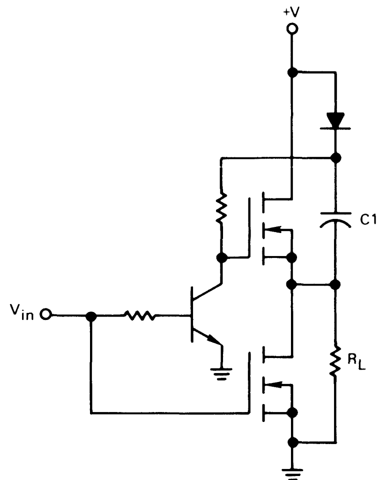


FIGURE 6-34 — BOOTSTRAPPING CIRCUIT TO DRIVE A GROUNDED LOAD WITH N-CHANNEL TMOS

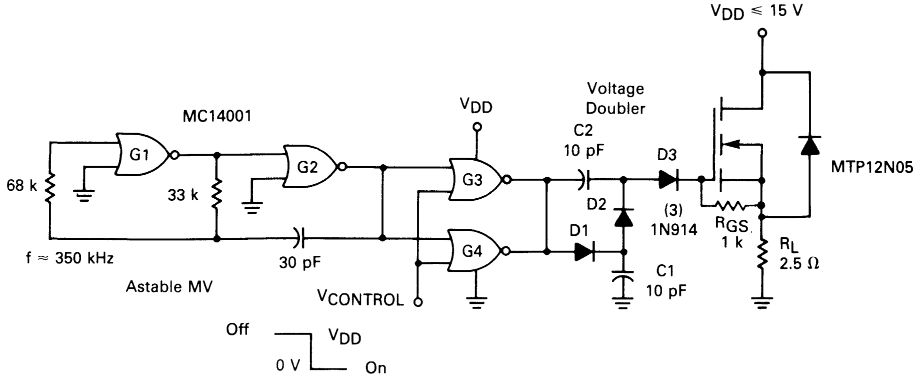


FIGURE 6-35 — N-CHANNEL SOURCE FOLLOWER WITH VOLTAGE DOUBLER DRIVE

the on state for an unlimited period of time because the finite charge stored in C1 is eventually bled off. A second problem is that this circuit cannot switch high voltages since C1 will be charged to the system supply voltage and then this potential will be impressed across the gate-to-source. Fortunately, in applications that require grounded loads, such as those in the automotive industry, the supply voltages are often compatible with this method of bootstrapping.

VOLTAGE DOUBLER

The gate voltage can be raised much higher than the source or supply voltage by using a voltage doubler, as shown in Figure 6-35. Voltage multipliers using diodes and capacitors require an oscillator input of which a simple and inexpensive method of obtaining this signal uses a CMOS astable multivibrator, designed with a quad two-input NOR gate MC14001. Gates G1 and G2 form the MV and the parallel connected gates G3 and G4 serve as a low output impedance buffer stage for driving the doubler network. When these gates are powered with the same V_{DD} supply as the power MOSFET high side switch, the output of the doubler (input to the FET gate) will approach twice V_{DD}, due to the voltage doubling effect of diodes D1–D3, capacitors C1, C2 and the input capacitance C_{iss} of the FET switch. Obviously, V_{DD} cannot exceed the maximum voltage of the CMOS (+18 V).

If greater switch output voltage is required with increasing V_{DD}, the CMOS supply can be zenered and more diode-capacitor stages cascaded to raise the gate voltage.

With the component values shown, the astable MV will oscillate at about 350 kHz. This signal and, consequently, the switch can be gated ON and OFF by applying the indicated control voltage to the second input of gates G3 and G4. However, due to the low power output of the CMOS IC, switching speeds are quite slow — tens of milliseconds — limiting this circuit to slow switching applications. Turn-off time can be substantially improved by employing an input capacitance C_{iss} discharging clamp transistor.

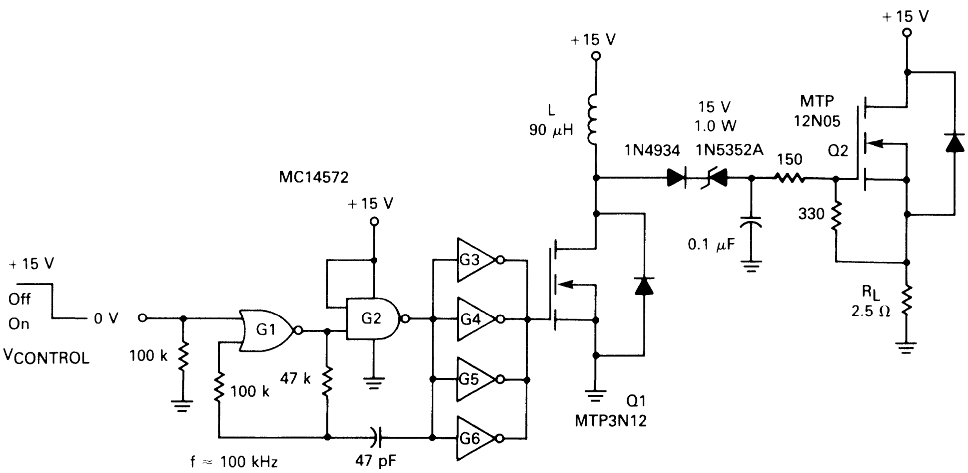


FIGURE 6-36 — N-CHANNEL SOURCE FOLLOWER WITH FLYBACK CONVERTER DRIVE

2

FLYBACK CONVERTER

Another circuit for raising the gate voltage well above the supply voltage, one that uses a flyback converter, is shown in Figure 6-36. The power switch used in this converter, an MTP3N12 power MOSFET (Q1), is easily driven by the CMOS, 100 kHz, astable multivibrator (MV). This circuit uses two of the Hex Inverter MC14572 gates (G1 and G2) as the MV with the remaining four inverters, in parallel, providing the gate-drive to the FET, about 25 mA peak to charge C_{iss}. When Q1 turns on, the drain current ramps-up to about 0.8 A and upon turn-off, the flyback voltage reaches about 60 V. This inductor stored energy is then dumped into the diode-resistor-capacitor load circuit to provide the bias for the power FET switch Q2 (MTP12N05), about 13 V gate-source (28 V gate-ground). The series connected 15 V zener diode blocks the V_{DD} supply from reaching the gate of Q2, when Q1 is off.

With this amount of gate-drive, the V_{DS} of Q2, under a 6.0 A load, measured about 0.5 V, resulting in $r_{DS(on)}$ of 0.08 Ω. This calculates to about a 97% voltage transfer (94% power transfer).

As in the previous source follower gate-drive circuit, the power switch is enabled by a zero logic level to one input of NOR Gate G1. For this circuit, however, turn-off switching speeds are much faster — about 0.15 ms — due to the relatively higher power output of the converter gate-drive.

This type of gate-drive can also be used in totem-pole (half or full-bridge) configurations, where the upper switch is also essentially a source follower. For details, see the Motor Controller Section.

Chapter 7: Paralleling Power MOSFETs

Paralleling Power MOSFETs in Switching Applications

In some applications, the most beneficial characteristic of the power MOSFET is its ability to be paralleled to increase current conduction and power switching capabilities. Current sharing among devices is important in all of the modes in which the MOSFET may conduct current. These modes are:

1 — Fully "on" during static conditions.

2 — Switching applications including transient (turn-on and turn-off) and pulsed conditions.

3 — Applications in which the drain-source diode will conduct current.

4 — Linear applications.

Since the considerations for each case are quite different, each must be investigated independently before the MOSFET can be regarded as a device that is easily paralleled. The following sections show that the MOSFET can be paralleled in each of the four modes provided certain simple recommendations are followed.

Static Current Sharing Design Considerations

Although increasing junction temperature raises the on-resistance and the conduction losses of the power MOSFET, definite benefits are attributable to the positive temperature coefficient of $r_{DS(on)}$. If a portion of the chip begins to hog current, the localized temperature will increase, causing a corresponding increase in the $r_{DS(on)}$ of that portion of the chip, and current will shift away to the cooler, less active, portions of the die. This trait accounts for the tendency of the device to share current over the entire surface of the die's active region. Because current crowding and hotspotting are eliminated under normal operating conditions, there is no need to derate power MOSFETs to guard against secondary breakdown.

The argument supporting current sharing within a device, due to the positive temperature coefficient of $r_{DS(on)}$, is easily extended to the case of paralleled devices. As within a single device with some imbalance in $r_{DS(on)}$ over the die's active area, an imbalance or mismatch of $r_{DS(on)}$ between devices will cause an initial current loading imbalance between devices. The resulting rise in junction temperature and on-resistance of the device with the lowest $r_{DS(on)}$ will decrease that device's drain current and will establish a more equal distribution of the total load current in all paralleled devices.

While this tendency is definitely observable, its influence on the degree of current sharing is often overestimated. In the power MOSFET, the current sharing mechanism is not triggered simply by high junction temperature, but by the difference in T_J between the low and high $r_{DS(on)}$ devices. Due to the generally small thermal coefficient of $r_{DS(on)}$, this difference in junction temperature sometimes must be substantial to attain a high degree of current sharing.

Since the ultimate concern is for optimum reliability, the emphasis should not be placed on obtaining large deltas in T_J to force a greater degree of current sharing. On the contrary, the effort should be focused on decreasing T_J of the hottest device. This is accomplished by close thermal coupling of the paralleled devices, provided that the total heat sinking capability is not compromised by doing so. This will tend to minimize the differences in both case and junction temperature. Before a worst case example of these concepts can be examined, some knowledge of the range of the variation of $r_{DS(on)}$ within production devices must be obtained.

Unless devices are matched for identical on-resistances, there will be at least a slight mismatch in their individual drain currents. The worst case situation is obviously the paralleling of devices with the widest possible variation in $r_{DS(on)}$. Two wafer lots of the MTP8N18 were sampled to obtain some idea of the range of variation of $r_{DS(on)}$ within the same wafer lot and between wafer lots. In addition to information on $r_{DS(on)}$, Table 1 contains data on the parameters important to dynamic current sharing which will be addressed later. From this information, one will have to design for a worst case $r_{DS(on)}$ mismatch of 30%.

TABLE 1 — Variation of $r_{DS(on)}$, g_{FS}, and $V_{GS(th)}$ in Two Wafer Lots of the MTP8N20*

	$r_{DS(on)}$		g_{FS}		$V_{GS(th)}$		Sample
	Min	Max	Min	Max	Min	Max	Size
Wafer Lot I	0.231	0.297	3.704	4.878	2.300	4.080	100
Wafer Lot II	0.239	0.305	3.571	4.878	3.685	3.910	50

*Data was taken on first generation TMOS devices. The most recent devices may give different dispersions.

$r_{DS(on)}$ is influenced by the magnitude of the drain current and the junction temperature. I_D and T_J are, in turn, a function of the power dissipation, which is strongly dependent upon $r_{DS(on)}$. The quality of heat sinking and thermal coupling between devices also affects I_D and T_J. These interdependent relationships make an analytical attempt to determine the degree of current sharing between several devices with a given $r_{DS(on)}$ mismatch rather complicated. An example of an iterative analytical process used to accomplish this end follows. The estimated I_D mismatch is somewhat dependent on the initial assumptions.

Design requirements could include the following:

1. Maximum desired junction temperature is 125°C.
2. Sufficient heat sinking will be supplied to maintain a 90°C case temperature when $T_A = 35$°C during maximum power dissipation.
3. Assume worst case $r_{DS(on)}$ mismatch for the MTP8N20 is 0.230 to 0.400 ohms @ $I_D = 4.0$ A and $T_J = 25$°C.

From these conditions, the worst case variation in I_D, P_D and T_J needs to be determined. First, the thermal coefficient of $r_{DS(on)}$, C_T, must be determined from the on-resistance versus drain current curve (Figure 7-1).

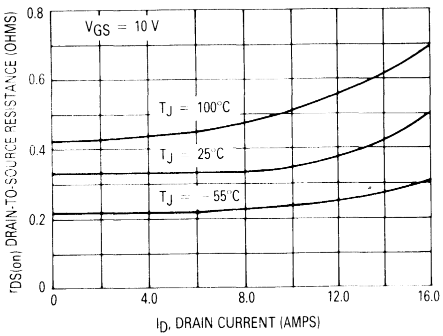


FIGURE 7-1 — ON-RESISTANCE versus DRAIN CURRENT — MTP8N18

$$C_T\Big|_{I_D=8.0\text{ A}} = \frac{\Delta r_{DS(on)}}{\Delta T} = \frac{r_{DS(on)}\Big|_{T_J=100°C} - r_{DS(on)}\Big|_{T_J=25°C}}{100°C\text{-}25°C}$$

$$= \frac{0.47 - 0.32\ \Omega}{75°C} = 0.002\ \Omega/°C$$

In addition to assuming that C_T is invariant with temperature and drain current, it is also supposed that thermal coupling between device heat sinks is negligible. From the maximum desired junction temperature (T_J = 125°C), case temperature (T_C = 90°C), and the junction to case thermal resistance ($R_{\theta JC}$ = 1.67°C/W) of the MTP8N20, the maximum power dissipation and case to ambient thermal resistance are easily calculated.

$$P_D = \frac{T_J - T_C}{R_{\theta JC}} = \frac{125\text{-}90°C}{1.67°C/W} = 20.96\text{ W}$$

$$R_{\theta CA}\ \frac{T_C - T_A}{P_D} = \frac{90\text{-}35°C}{20.96\text{ W}} = 2.62°C/W$$

Attention is then focused on the device with the lowest $r_{DS(on)}$ since it will be dissipating the most power. At a T_J of 125°C its $r_{DS(on)}$, drain current, and V_{DS} are:

$$r_{DS(on)}\Big|_{T_J=125°C} = r_{DS(on)}\Big|_{T_J=25°C} + (T_J - 25°C)\ C_T$$

$$= 0.230 + (125\text{-}25)\ .002$$

$$= 0.430\ \Omega$$

$$I_D = \sqrt{\frac{P_D}{r_{DS(on)}}} = \sqrt{\frac{20.96}{0.430}} = 6.98 \approx 7.0\text{ Amp}$$

$$V_{DS} = I_D * r_{DS(on)} = (7) * (0.430) = 3.0\text{ Volts}$$

To determine the operating conditions of a high resistance device operated in parallel with a low resistance device, an iterative technique must be employed. The approach is to estimate the junction temperature of the cooler device and from that, compute the $r_{DS(on)}$ at that T_J, the current and power dissipated, and the new junction temperature. The computations are then repeated until the process converges on the correct solution.

The first iteration proceeds as follows:

For T_J = 100°C:

$$r_{DS(on)}\Big|_{T_J=100°C} = r_{DS(on)}\Big|_{T_J=25°C} + (T_J - 25°C)\ C_T$$

$$= 0.400 + (100\text{-}25)\ 0.002 = 0.550\ \Omega$$

$$P_D = \frac{V^2}{r_{DS(on)}} = \frac{3^2}{0.550} = 16.36\text{ W}$$

$$\Delta T_{JC} = P_D * R_{\theta JC} = 16.36 * 1.67 = 27.33°C$$

$$\Delta T_{CA} = P_D * R_{\theta CA} = 16.36 * 2.62 = 42.87°C$$

$$T_J = \Delta T_{JC} + \Delta T_{CA} + T_A = 27.33 + 42.87 + 35 = 105.2°C$$

After two more iterations, the algorithm converges. The results are tabulated for comparison with those of the low resistance device in Table 2. In addition to the case of negligible thermal coupling, the idealized situation of perfect thermal coupling of the cases is also included for direct comparison. The performance trade-off between the two examples is that little thermal coupling will achieve a greater degree of current sharing at the expense of higher junction temperature in the hottest device (119°C versus 125°C). Since $T_{J(max)}$ most directly influences reliability, close thermal coupling of devices is encouraged. The manufacturer can best do this by paralleling chips on a common heat sink.

TABLE 2 — Static Current Sharing Performance of Mismatched MTP8N20

	Negligible Thermal Case Coupling		Perfect Thermal Case Coupling	
	$r_{DS(on)}$ Min Device	$r_{DS(on)}$ Max Device	$r_{DS(on)}$ Min Device	$r_{DS(on)}$ Max Device
$r_{DS(on)}$ @ T_J = 25°C (Ohms)	0.230	0.400	0.230	0.400
I_D (Amps)	7.00	5.38	7.14	5.24
P_D (Watts)	21.0	16.1	21.3	15.7
Steady State T_J (°C)	125	104	119	110
$r_{DS(on)}$ @ Steady State T_J (Ω)	0.430	0.558	0.419	0.570

A point essential to the above calculations is that the steady state thermal resistance was employed to compute the junction temperatures. For pulsed conditions $R_{\theta JC}$ can vary significantly, and the transient thermal resistance obtained from the thermal response curves must be used to make this calculation. During switching transitions, there is insufficient time to establish differences in junction temperature and power MOSFETs may not current share in the same manner.

Dynamic Current Sharing Design Considerations

The term "dynamic" is broadened here to include not only current during turn-on and turn-off, but also peak current during narrow pulses and small duty cycles. Under these conditions, not enough RMS current is present to cause differential heating of the junctions which triggers the tendencies of the devices to share current. Since the argument supporting current sharing under static conditions is based on differences in junction temperature due to an imbalance of power dissipation and drain currents, that reasoning does not support the concept of current sharing during dynamic conditions. However, even without the benefit of the positive temperature coefficient, power MOSFETs can current share reasonably well with simple and efficient gate-drive circuitry.

The issues of greatest concern to those interested in dynamic current sharing of paralleled MOSFETs are listed and described in order below.

1. Device parameters that influence dynamic current sharing.
2. Variation of pertinent device parameters from lot to lot.
3. Required device parameter matching to achieve safe levels of current distribution.
4. The effects of switching speed on dynamic current sharing.
5. The requirements and effects of circuit layout.
6. The possibility of self-induced oscillations.

Device Parameters That Influence Dynamic Current Sharing

The device parameters that influence the degree of dynamic current sharing are the transconductance (g_{FS}), gate-source threshold voltage [$V_{GS(th)}$], input capacitance, and the on-resistance $r_{DS(on)}$. However, the device characteristic that most accurately predicts how well paralleled MOSFETs will current share during turn-on or turn-off is the transconductance curve, i.e., the relationship between the drain current and the gate-source voltage. To obtain optimum current distribution during turn-on and turn-off, the ideal situation is to have all gate-source voltages rising (or falling) simultaneously on devices with identical transconductance curves. This combination would ensure that as the devices switch through the active region, none would be overstressed by a current imbalance. Figures 7-2a, 7-2b and 7-2c show the nearly perfect degree of current sharing obtainable solely by matching the g_{fs} curves. The current probe used induced a 20 ns delay in the current waveform in the oscillograms shown.

Since plotting the entire g_{fs} curve of each device is very time consuming, matching $V_{GS(th)}$ or g_{FS} at some drain current has been suggested as a simpler criterion for matching paralleled MOSFETs. While much of the literature suggests the importance of matching $V_{GS(th)}$, which is normally defined as the minimum gate voltage at which a small drain current (usually specified as 1.0 mA) begins to flow, this does not accurately indicate the shape of the I_D versus V_{GS} curve at higher currents.

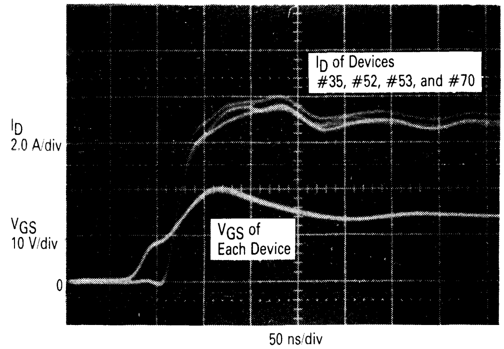


FIGURE 7-2a — PARALLELED TURN-ON

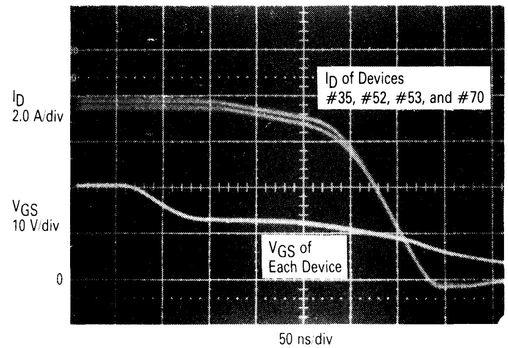


FIGURE 7-2b — PARALLELED TURN-OFF

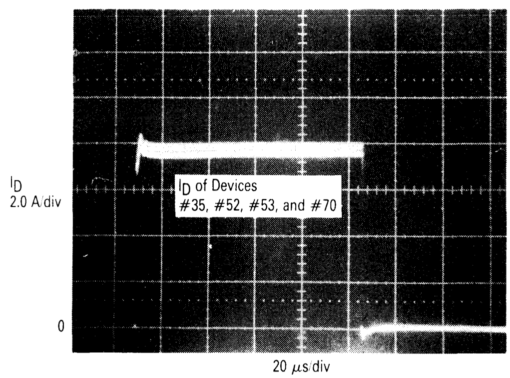


FIGURE 7-2c — COMPOSITE I_D WAVEFORM FOR TURN-ON AND TURN-OFF

FIGURE 7-2 — INDIVIDUAL I_D WAVEFORMS OF FOUR PARALLELED MTP8N18 WITH MATCHED TRANSCONDUCTANCE CURVES — RESISTIVE LOAD (DRAIN CURRENT WAVEFORMS ARE DELAYED 20 ns)

Devices with 1.0 mA thresholds that vary by as much as 2.0 volts do not usually, but can, have nearly identical transconductance curves above 100 mA. Conversely, those devices out of a group of one hundred MTP8N20 found to have the widest variation of g_{FS} curves had thresholds that varied by only 4%. Therefore, for optimum current sharing, the ideal solution is to use devices with identical curves, and comparing thresholds may not be the best way to achieve this.

Another simple, yet more consistent, method is to match devices by comparing the maximum drain current they will conduct at a gate voltage higher than $V_{GS(th)}$. For example, all four devices shown in Figure 7-2 conduct an I_D of 4.0 A at a V_{GS} of 6.0 volts and were found to have nearly identical g_{FS} curves (Figure 7-3). Though similar to matching thresholds, this method matches points on the g_{fs} curve that are more germane to the intended application of the devices.

Variation of Pertinent Device Parameters from Lot to Lot

Before any definitive statement may be made concerning the degree or type of matching required for safe dynamic current sharing, the variation of pertinent device parameters from lot to lot must be known. Two wafer lots of the MTP8N20, with sample sizes of 100 and 50 units respectively, were characterized for this pupose. The maximum and minimum values of threshold voltage, transconductance, and on-resistance are shown in Table 1. Figure 7-4 illustrates the widest variation in g_{FS} curves within Wafer Lot I and is similar to the results obtained from Wafer Lot II.

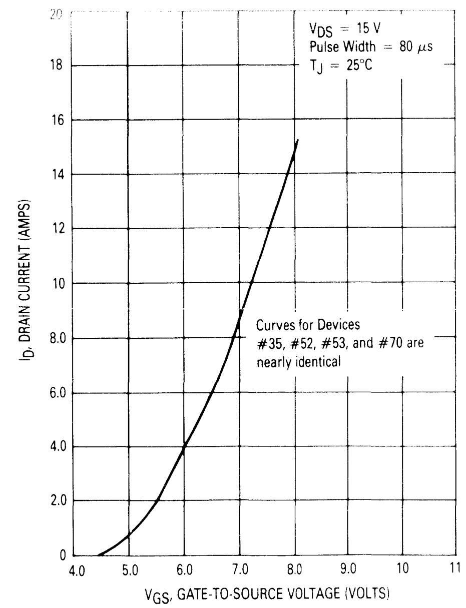


FIGURE 7-3 — TRANSCONDUCTANCE CURVES OF MATCHED MTP8N20

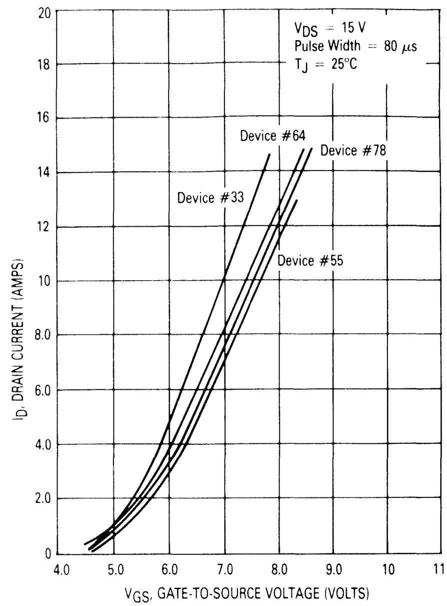


FIGURE 7-4 — WIDEST VARIATION IN TRANSCONDUCTANCE CURVES FOUND IN WAFER LOT I

Obviously, the possibility of larger than expected variations in these pertinent parameters diminishes as the number of sampled wafer lots increases. To get an adequate sampling of available devices, the user could characterize devices with different date codes or obtain units from several distributors.

Required Matching for Safe Levels of Current Distribution

After characterization and determining the degree of variation possible, the effects of matching or mismatching the critical device characteristics can be observed. The circuit used for this study is shown in Figure 7-5. Some of the possible modifications of the circuit include adding resistors in series with the gate to slow the turn-on and turn-off, and a second MOSFET may be included to clamp the gate bus to ground to observe the effects of very rapid turn-off.

In this discussion of resistive switching, Figure 7-2 will serve as a standard for comparisons since matching transconductance curves has achieved such good performance. Extreme care was taken to provide as pure a resistive load as possible. The 1.6 ohm load was constructed from 39, 62-ohm carbon composition resistors connected in parallel between two copper plates. Though the drain wiring and load inductances were very small, during rapid turn-on, the L/R time constant of the circuit may be the factor that limits the current rise times and not the switching speed of the MOSFETs.

One of the worst case situations is to parallel devices with greatly mismatched g_{FS} curves. Representing the

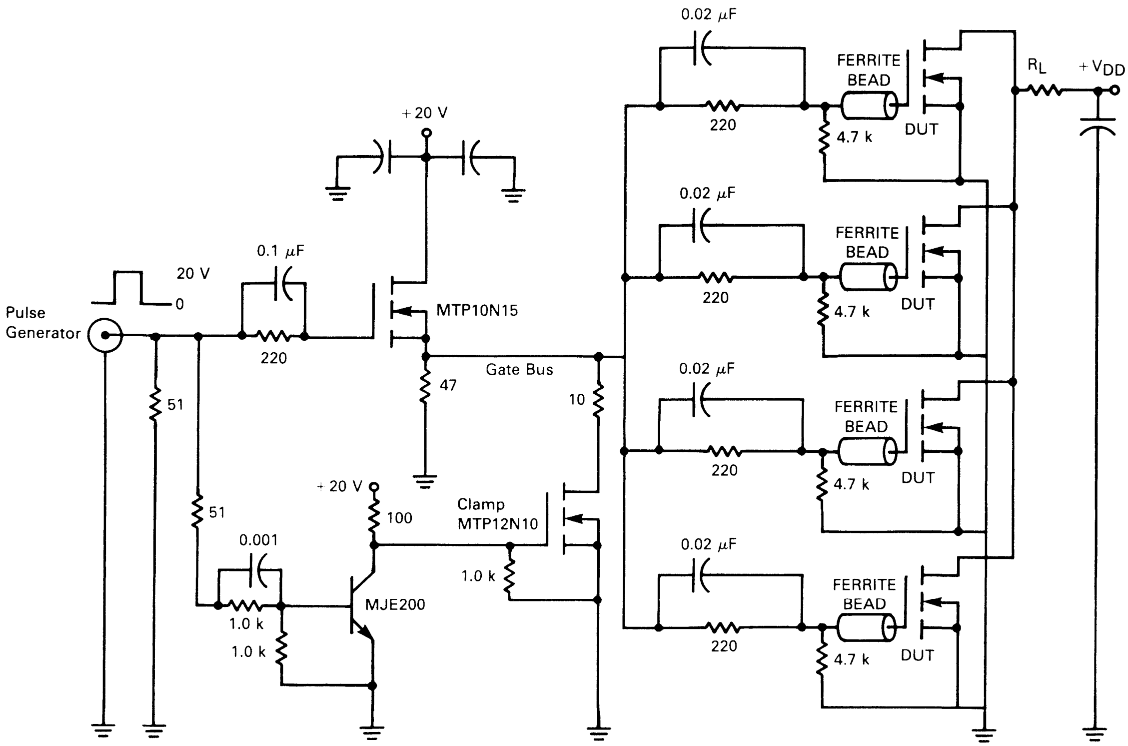


FIGURE 7-5 — DYNAMIC CURRENT SHARING TEST CIRCUIT

widest variation in the g_{FS} curves in Wafer Lot I, Figure 7-4 shows the curve of a device that will begin to turn on with a rising V_{GS} slightly sooner than the other three devices. It may be expected that device #33 will turn on first and possibly fail due to current overload. However, since the variation in the I_D versus V_{GS} curves of these mismatched devices is small, the failure will not occur. As shown in Figure 7-6, parallel operation of these mismatched devices in the given circuit poses no significant reliability hazard.

Matching the 1.0 mA thresholds does not guarantee the nearly perfect results of matching the g_{FS} curves, as shown in Figure 7-7. Although their thresholds were matched to within 2%, these devices exhibited a fairly wide variation in g_{FS} curves (Figure 7-8) which resulted in device #45 beginning its turn-off slightly sooner than the

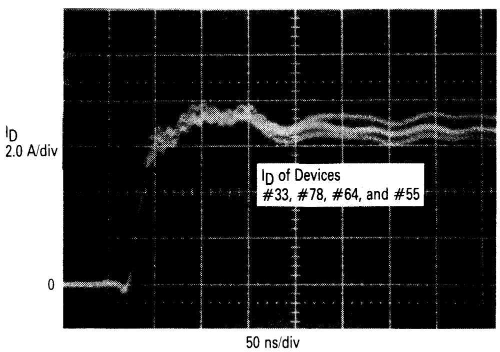


FIGURE 7-6a — PARALLELED TURN-ON

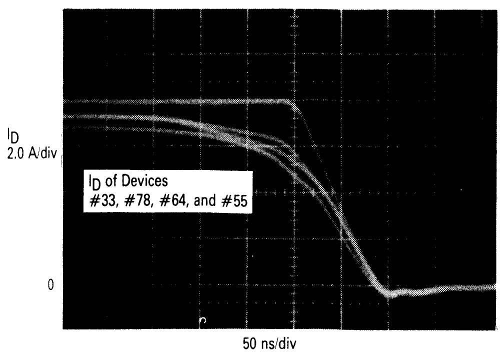


FIGURE 7-6b — PARALLELED TURN-OFF

FIGURE 7-6 — INDIVIDUAL I_D WAVEFORMS OF FOUR PARALLELED MTP8N18 WITH MISMATCHED TRANSCONDUCTANCE CURVES — RESISTIVE LOAD

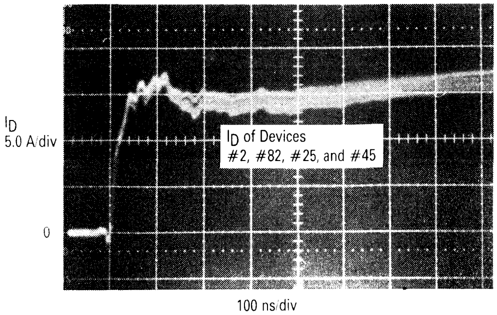


FIGURE 7-7a — PARALLELED TURN-ON

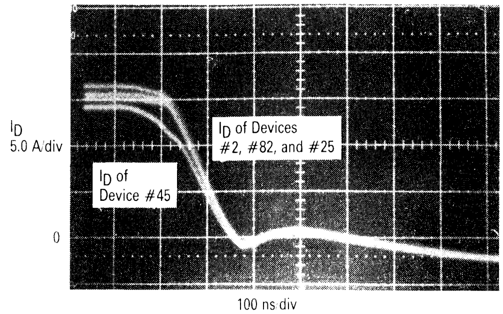


FIGURE 7-7b — PARALLELED TURN-OFF

FIGURE 7-7 — INDIVIDUAL I_D WAVEFORM OF FOUR PARALLELED MTP8N18 WITH MATCHED THRESHOLD VOLTAGES — RESISTIVE LOAD

Waveform/Curve Relations

Note: The order of the device numbers shown in all the current waveforms is important. The first number indicates the upper current waveform in each group with succeeding curves corresponding to the following device numbers. The order of waveforms is identified to enable the reader to correlate the devices' performance in the current waveforms to the devices' g_{FS} curves provided.

rest. The waveform photos again indicate that the performance of this group is also quite adequate. For comparison, the devices in Figures 7-9 and 7-10 have fairly similar g_{FS} curves even though their 1.0 mA threshold voltages vary by as much as 33%. Turn-on times for this group are almost simultaneous while the turn-off is just short of ideal.

Because the MTP8N20 of the two wafer lots were so close in characteristics, the worst conceivable mismatch that might occur could not be found. In order to study the effects of such a wide disparity between parameters, an MTP12N10 was paired with three closely matched

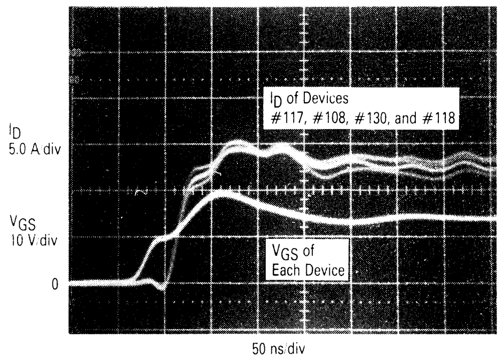


FIGURE 7-9a — PARALLELED TURN-ON

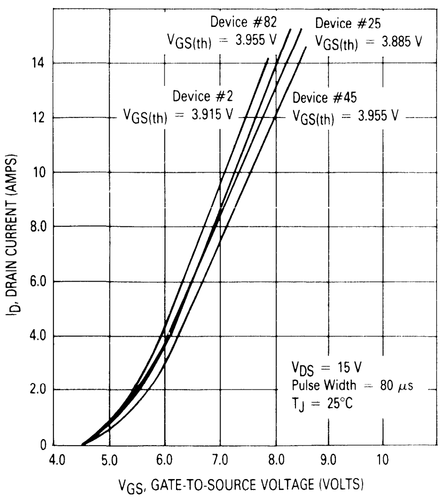


FIGURE 7-8 — TRANSCONDUCTANCE CURVES OF MTP8N20 WITH MATCHED THRESHOLD VOLTAGES

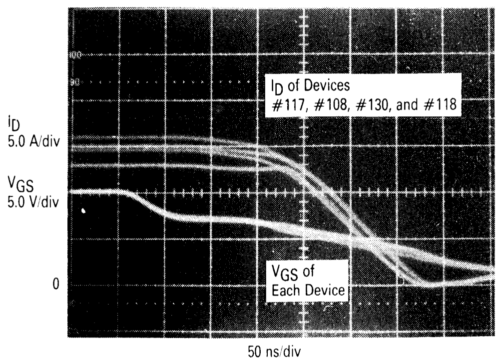


FIGURE 7-9b — PARALLELED TURN-OFF

FIGURE 7-9 — INDIVIDUAL I_D WAVEFORMS OF FOUR MTP8N20 WITH MATCHED TRANSCONDUCTANCE CURVES AND MISMATCHED THRESHOLD VOLTAGES

TABLE 3 — Parameter Comparison of One MTP12N10 and Three MTP8N20s

Device Number	Device Type	$r_{DS(on)}$ I_D = 4.0 A (Ohm)	$V_{GS(th)}$ I_D = 1.0 mA (Volts)	g_{fs} I_D = 4.0 A V_{GS} = 15 V (Volts)	C_{rss} (pF)	C_{iss} (pF)	C_{oss} (pF)
#122	MTP12N10	0.145	3.600	4.300	90	685	395
#52	MTP8N20	0.238	3.955	4.762	45	700	220
#53	MTP8N20	0.256	3.900	4.444	45	700	245
#70	MTP8N20	0.255	3.930	4.444	45	700	235

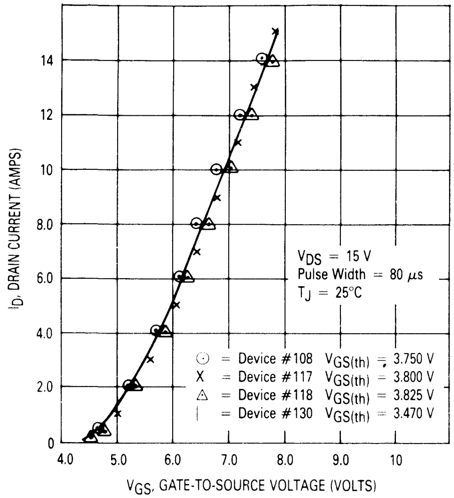


FIGURE 7-10 — TRANSCONDUCTANCE CURVES OF MTP8N20 WITH THRESHOLD VOLTAGE $V_{GS(th)}$ MISMATCH

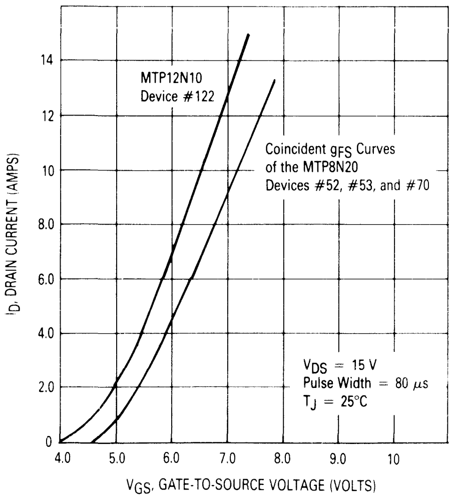


FIGURE 7-11 — TRANSCONDUCTANCE CURVES OF AN MTP12N10 AND THREE MTP8N20

MTP8N20. The MTP12N10 is a 12 A, 100 V device with the same die dimensions as the MTP8N20. Table 3 and Figure 7-11 compare the different device characteristics. The result of paralleling these four devices is shown in Figure 7-12.

The MTP12N10 is the last device to begin turn-on even though its transconductance curve rises earlier than those of the MTP8N20. This is due to the larger C_{rss} (reverse transfer or gate-drain capacitance) which is effectively multiplied in value by the device gain due to the Miller effect. Although not completely simultaneous, the turn-off is smooth. By the time the MTP8N20 have completely switched off, the MTP12N10 has moved well into the active or constant current region. At that time, the total

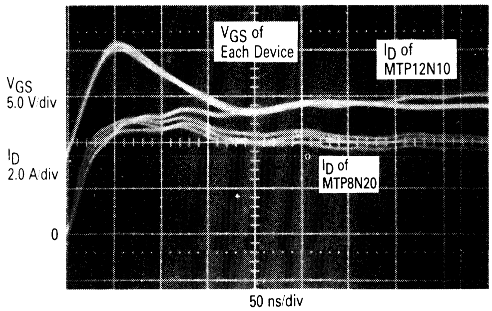


FIGURE 7-12a — PARALLELED TURN-ON

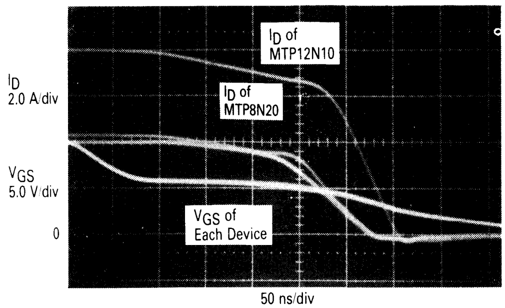


FIGURE 7-12b — PARALLELED TURN-OFF

FIGURE 7-12 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10 PARALLELED WITH THREE MTP8N20 — RESISTIVE LOAD

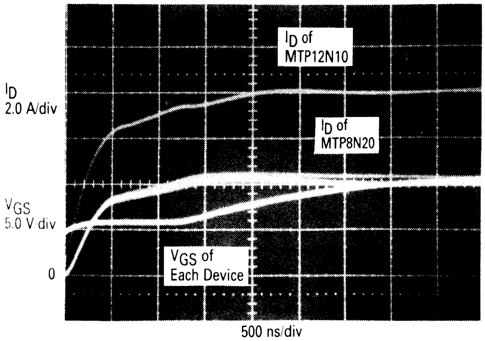


FIGURE 7-13a — PARALLELED TURN-ON

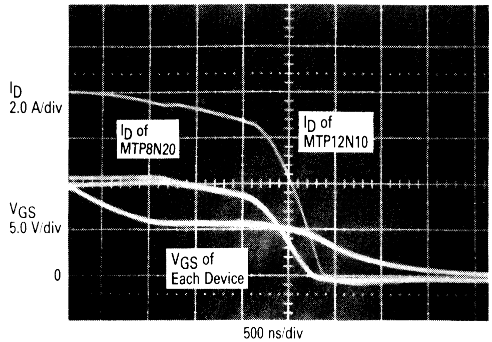


FIGURE 7-13b — PARALLELED TURN-OFF

FIGURE 7-13 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10 PARALLELED WITH THREE MTP8N20 — RESISTIVE LOAD — SLOW SWITCHING

load current has been substantially reduced and the slightly unsynchronized turn-off poses no threat to the MTP12N10 at these switching speeds.

It is apparent that for this specific application, i.e., resistive switching at moderate switching speed, device matching improves paralleled performance but is not necessary for safe operation. This recommendation will be extended to include both fast and slow switching speeds for both resistive and inductive loads provided certain circuit layout criteria are met.

Effects of Switching Speed on Dynamic Current Sharing

The gate-drive circuit used to switch the MTP12N10 and the three MTP8N20 was altered to either increase or decrease the switching speed. The four 0.02 μF speed-up capacitors were removed to determine the quality of current sharing as the gate-source voltages rise or fall at speeds that are fairly slow for power MOSFETs. The MTP12N10 is the first to turn on and the last to turn off (Figure 7-13) due to the differences in the devices' g_{FS} curves. During slow switching, the I_D versus V_{GS} curves can be used to accurately predict the I_D curves. For instance, the MTP12N10 begins to turn on when the composite gate-source voltage waveform reaches 4.0 volts, but the MTP8N20 hesitate until V_{GS} reaches 4.5 volts. Since the I_D waveforms are easily related via the g_{FS} curves to the rising or falling gate voltages and the variation in the g_{FS} curves over a product line are fairly small, slow switching of unmatched TMOS power MOSFETs can be a safe undertaking.

To judge the effects of rapid turn-off, a second MOSFET was added to clamp the gate-to-ground. This method achieves the 20 ns current fall times depicted in Figure 7-14. During such rapid switching, the V_{GS} and g_{FS} curves can no longer be used to accurately predict device performance due to package and lead parasitics such as the package source inductance. Once again however, these mismatched devices performed well as they were switched very rapidly through the active region. Although not quite as predictable, rapid resistive switching also appears safe.

A comparison of Figures 7-12, 7-13, and 7-14 indicates that faster switching tends to improve dynamic current sharing. This is in part a consequence of switching the devices through the active region at a much faster rate and correspondingly decreasing any difference in switching speeds. The parasitic source inductance also plays an important role as discussed below.

Dynamic Current Sharing With Inductive Loads

The investigation of the effects of current sharing with inductive loads was conducted using a fast recovery diode (40 A, 400 V) placed in parallel with a 135 μH inductor as a load. The diode was included not so much to protect the MOSFET against flyback voltages, but to test the paralleled transistors' ability to conduct the large peak reverse recovery current required by the diode. The standard of performance is again set by devices with matched g_{FS} curves and shown in Figure 7-15.

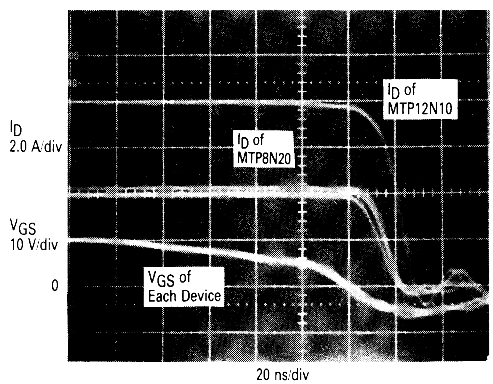


FIGURE 7-14 — INDIVIDUAL I_D WAVEFORMS OF AN MTP12N10 PARALLELED WITH THREE MTP8N20 — RESISTIVE LOAD — RAPID TURN-OFF

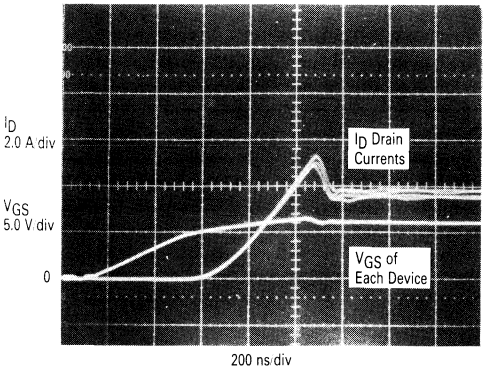


FIGURE 7-15a — PARALLELED TURN-ON

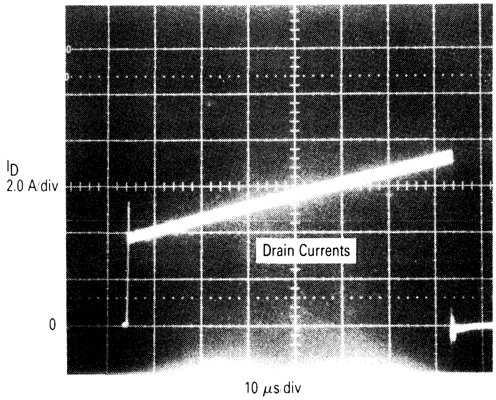


FIGURE 7-15b — COMPOSITE TURN-ON AND TURN-OFF WAVEFORM

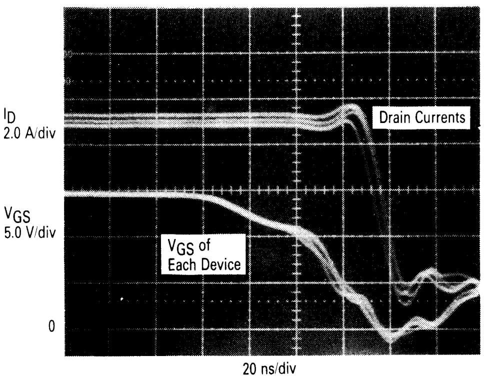


FIGURE 7-15c — PARALLELED TURN-OFF

FIGURE 7-15 — INDIVIDUAL I_D WAVEFORMS OF MATCHED MTP8N20 SWITCHING AN INDUCTIVE LOAD — DEVICES #35, #52, #53, and #70

To obtain a larger sample size for the worst case inductive testing, 250 additional MTP8N20 of unknown wafer origin were characterized for their widest variation in g_{FS} curves. The mismatched transconductance curves are shown in Figure 7-16. Figure 7-17 depicts both rapid and slow inductive turn-on and turn-off. This group of figures represents the greatest current imbalance seen in any set of mismatched MTP8N20 under any load conditions. While there are obvious current mismatches, they require only a small amount of derating to guardband against possible harmful situations. The keys to success are: 1) that pertinent device characteristics do not vary widely; and, 2) strict attention is given to the symmetry of the circuit layout.

Circuit Layout — A Critical Concern

Even with identically matched devices, dynamic current sharing between MOSFETs will be poor if an asymmetrical circuit layout is used. Obviously, if the gate-drives are different, unequal rates of gate-source voltage rise and fall can cause unsynchronized switching and even device failure in extreme cases. As the switching speeds of these devices are increased, the designer's perception as to what may constitute an important parasitic circuit element must change. When approaching the maximum switching speeds of power MOSFETs, even small variations in lead length may influence their paralleled switching performance. Unequal source wiring inductances are especially deleterious.

Figures 7-18a and 7-18b illustrate the effects of an imbalance in source wiring inductance. The devices and circuit layout are both closely matched except that an additional source lead inductance of 50 nH (1.5 inches of #22 wire formed into a 1-1/2 turn loop) was added to one device. As can be seen in the photographs, any source lead or wiring inductance will degenerate both the turn-on and turn-off speeds. Fortunately, perhaps the most important consideration for successful operation of paralleled MOSFETs is completely within easy control of the circuit designer. The circuit should be free from parasitics and as symmetrical as possible, especially for higher switching speeds.

Another obvious consideration is that the output impedance of the gate-drive circuits must be matched. Mismatched gate-drives will cause unsynchronized charging or discharging of the input capacitances, forcing the devices to begin switching at different times and rates.

The Benefit of Parasitic Source Inductance

Provided that the circuit layout is symmetrical, especially with respect to the source wiring inductance, faster switching can actually benefit the degree of current sharing between paralleled MOSFETs. During switching transitions of less than 100 ns, the source package inductance (approximately 7.0 nH) plays an important part in determining the shape of the rising and falling drain current waveform. The following example assumes the wiring inductance is negligible and relates only the effect of the source package inductance. The intent of this illustration is to show the significance of the package inductance and by extension relate the importance of the usually much larger wiring inductance.

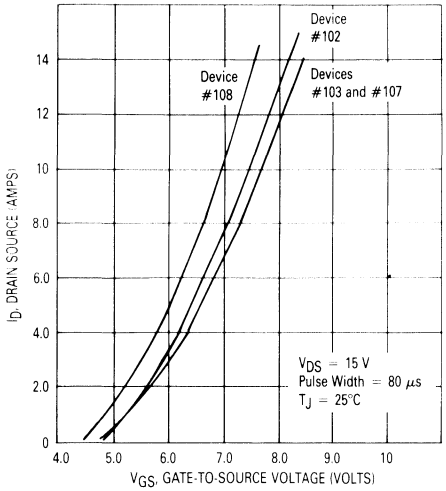


FIGURE 7-16 — WIDEST VARIATION IN TRANSCONDUCTANCE CURVES OF 250 ADDITIONAL MTP8N20

Assuming a very rapid turn-off accompanied by a di/dt of 8.0 A/50 ns, the voltage appearing across the parasitic lead inductance is approximately 1.1 volts (v = L di/dt = 7.0 nH x 8.0 A/50 ns). This inductive drop must be added to the voltage appearing across the gate-source terminals to reveal the potential impressed at the chip. A difference in gate voltage of this size makes a significant difference in the magnitude of the drain current as the device switches through the active region. Therefore, equal source inductances will tend to equalize the rate of the rise and fall of the individual drain currents during rapid switching of paralleled MOSFETs. In effect, source ballasting is achieved during rapid switching.

Protecting the Circuit From Self-Induced Oscillations

Two of the most highly esteemed characteristics of the power MOSFET can combine to cause a problem in paralleled devices. Their high input impedance and very high frequency response may cause parasitic oscillations at frequencies greater than 100 MHz. This problem occurs when all gates are driven directly from a common node as in the circuit in Figure 7-19. Without individual gate

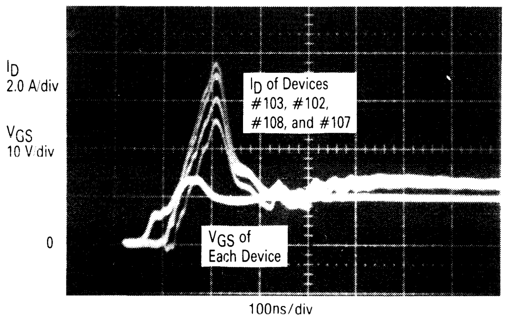


FIGURE 7-17a — RAPID TURN-ON SUPPLYING REVERSE RECOVERY CURRENT OF FREEWHEELING DIODE

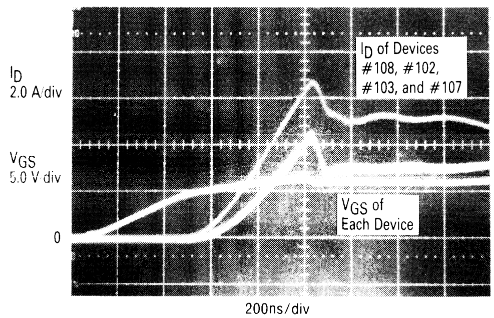


FIGURE 7-17b — SLOW TURN-ON SUPPLYING REVERSE RECOVERY CURRENT OF FREEWHEELING DIODE

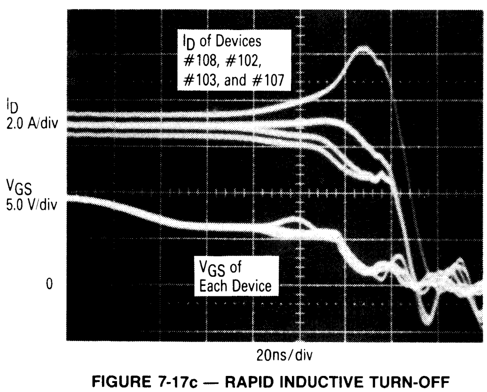


FIGURE 7-17c — RAPID INDUCTIVE TURN-OFF

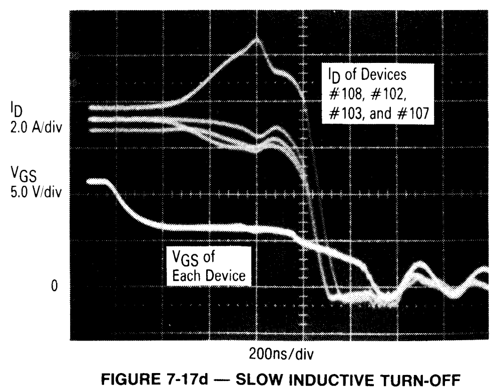


FIGURE 7-17d — SLOW INDUCTIVE TURN-OFF

FIGURE 7-17 — INDIVIDUAL I_D WAVEFORMS OF MISMATCHED MTP8N20 SWITCHING AN INDUCTIVE LOAD

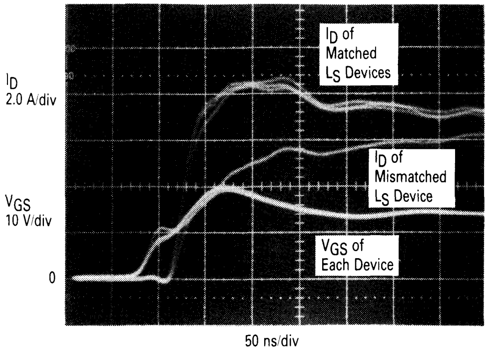


FIGURE 7-18a — TURN-ON

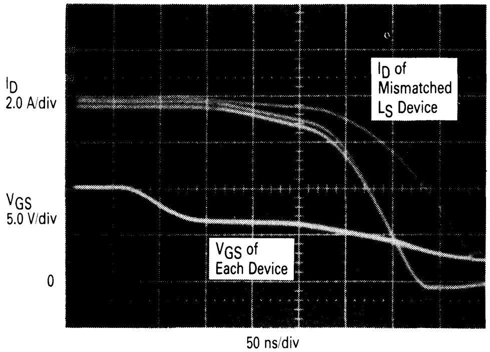


FIGURE 7-18b — TURN-OFF

FIGURE 7-18 — EFFECTS OF IMBALANCED SOURCE INDUCTANCES ON PARALLELED PERFORMANCE

resistances a high-Q network (Figure 7-20) is established that may cause the device to oscillate when operating in or switching through the active region. The device transconductance, gate-to-drain parasitic capacitance, and drain and gate parasitic inductances have all been shown to influence the stability of the circuit.

Although potentially serious, this problem is easily averted. By decoupling the gates of each device with lossy elements such as resistors or ferrite beads, the Q of the circuit can be sufficiently degraded to the point that oscillations are no longer possible (note dotted resistors shown in Figure 7-19). For the maximum switching speeds, the value of gate decoupling resistors should be kept as low as safely allowable. A value in the range of 10 to 20 ohms is generally sufficient.

A Practical Application — An Inductive Load

To show the feasibility of paralleling power MOSFETs in an application that imposes stresses typical of an inductive load, four MTP8N20's were paralleled in the circuit shown in Figure 7-21. At a 50% duty cycle and a V_{DD} of 44 V, the MOSFETs delivered about 450 W to the RC load. To minimize the power that the drain-source zener clamp must dissipate, MOSFET turn-off speed was limited by the placement of an 82 Ω resistor in series with each gate.

Again, the performance of interest is that of mismatched devices. In this case, fifty units from a newly designed mask set were tested for the widest variation in on-resistance (0.255 Ω to 0.230 Ω). The three highest $r_{DS(on)}$ devices were grouped with the lowest $r_{DS(on)}$ unit. Since a low $r_{DS(on)}$ usually indicates a high g_{FS}, the transconductance curves of these devices were also mismatched.

The degree of current sharing among these four units was well within safe operating limits. As expected, the lowest $r_{DS(on)}$ device carried the greatest on-state current. For clarity, only the on-state currents of the lowest and highest $r_{DS(on)}$ units are shown in Figure 7-22. The currents of the other two devices were nearly identical to device #8. As Figure 7-23 shows, the drain current of the lowest $r_{DS(on)}$ device, #11, peaked slightly due to its different g_{FS} curve.

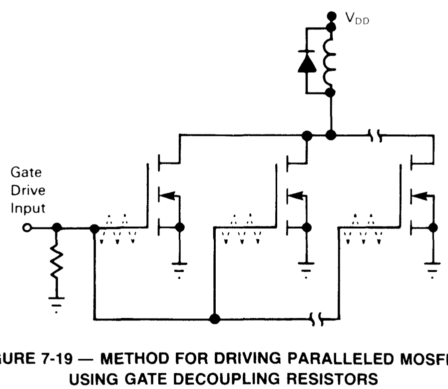


FIGURE 7-19 — METHOD FOR DRIVING PARALLELED MOSFETs USING GATE DECOUPLING RESISTORS

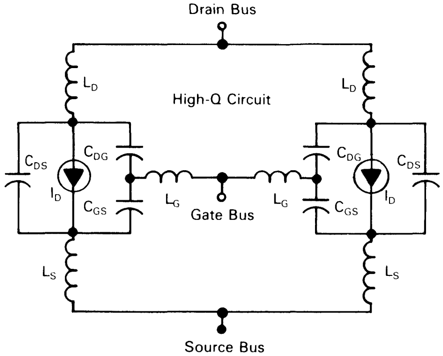


FIGURE 7-20 — PARASITIC HIGH-Q EQUIVALENT CIRCUIT OF PARALLELED MOSFETs WITHOUT GATE DECOUPLING RESISTORS

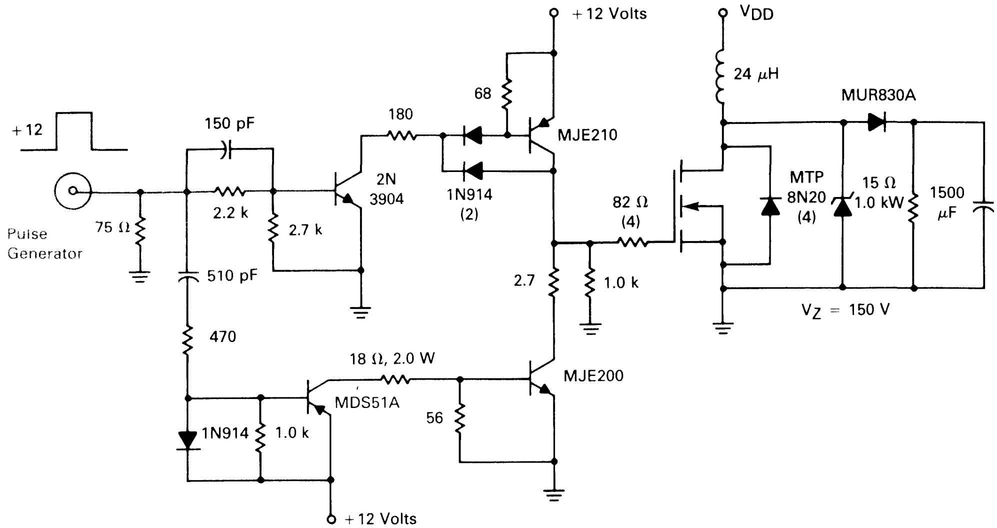


FIGURE 7-21 — CURRENT SHARING TEST CIRCUIT WITH AN INDUCTIVE LOAD

Each device was mounted on a separate heat sink, and the case temperatures were monitored to detect any thermal imbalances. Because of its low $r_{DS(on)}$, theory predicts that the case temperature of device #11 will be higher than the others. However, since the operating frequency was fairly high (40 kHz), the difference in switching losses may have also influenced the temperature comparison. Whether it was due to a variation in $r_{DS(on)}$ or g_{fs} curves, the temperature difference was very small (54.3°C for device #11 and 52.3°C for device #8) and did not significantly affect device performance, i.e., the degree of current sharing.

The following is a summary of recommendations and findings concerning static and dynamic current, sharing in paralleled power MOSFETs.

1. For static current sharing, the current mismatches are determined by the $r_{DS(on)}$ mismatch. A small degree of guardbanding or $r_{DS(on)}$ matching will ensure safe operation.
2. For dynamic current sharing, the turn-on and turn-off waveforms are largely determined by the transconductance curves. If matching is deemed necessary in a particular application, selecting devices by comparing g_{FS} curves is the most accurate approach. A simple, yet adequate, substitute is to match a single point on the g_{FS} curves at which the devices conduct significant drain currents.
3. Increasing the switching speeds in symmetrical circuits tends to equalize the rate of current rise and

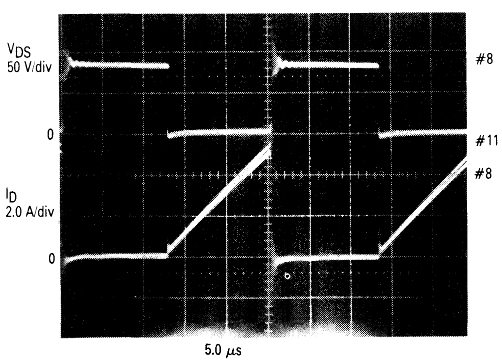


FIGURE 7-22 — I_D WAVEFORMS OF LOW AND HIGH $r_{DS(on)}$ DEVICES — INDUCTIVE LOAD

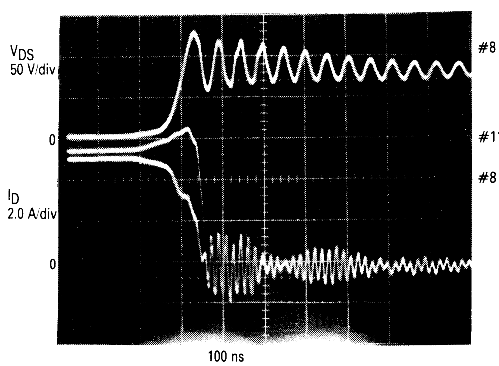


FIGURE 7-23 — I_D TURN-OFF WAVEFORMS OF LOW AND HIGH $r_{DS(on)}$ DEVICES — INDUCTIVE LOAD fall in paralleled devices due to the ballasting effect of the parasitic source inductance.

4. The circuit layout should be as symmetrical as possible with respect to the gate-drive and the source, gate, and drain parasitic inductances.
5. In all applications, the gates should be decoupled with small resistors or ferrite beads to eliminate parasitic oscillations.

Drain-to-Source Diodes

The previous text on paralleling power MOSFETs has shown the effects of parameter matching (or unmatching) on the degree of current sharing when the FETs are operating in either switching or linear applications. However, it has not described the effects on the paralleled drain-source diodes when these diodes are used as clamp or free-wheeling diodes in practical applications. These diodes can be used in multi-MOSFET switching applications (see Chapter 12 on characterizing D-S Diodes) when the diode switching speeds are commensurate with the application. In a half bridge, as an example, the diode of one FET protects the drain-source of the second FET and, conversely, the diode of the second FET protects the first FET. Whatever the circuit configuration, the equivalent circuit reduces to that of a clamped inductive load, whereby the drain-source diode is effectively across the load inductance (Figure 7-24).

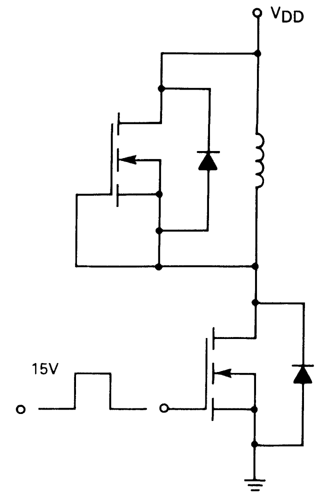


FIGURE 7-24 — INTRINSIC D-S DIODE CLAMPING AN INDUCTIVE LOAD

When power MOSFETs are paralleled in switching applications, the question arises as to how well their intrinsic diodes share the clamped current. To determine this, three MOSFETs were paralleled in the circuit shown in Figure 7-25. The test circuit (a complete schematic is shown in Figures 12-19 of Chapter 12) was duty cycle controlled to produce a continuous load current; thus, the commutated diode current indicated both the reverse recovery time t_{rr} and turn-on time t_{on}. The individual and total diode currents, as well as the driver drain current, were monitored.

To obtain some indication of a worst case condition, a modest sample (20 pieces) of MTM20N15 were characterized for parameters that affect their paralleled performance. The forward on-voltage of the diodes at 10 A ranged from 1.05 to 1.20 volts, and t_{rr} varied from 0.25 to 0.32 μs. Devices with the widest mismatch in parameters were grouped and tested in the circuit shown in Figure 7-25.

Testing indicated that current mismatches were small, even in devices with the greatest difference in D-S diode on-voltage. Figure 7-26 shows the current waveforms of

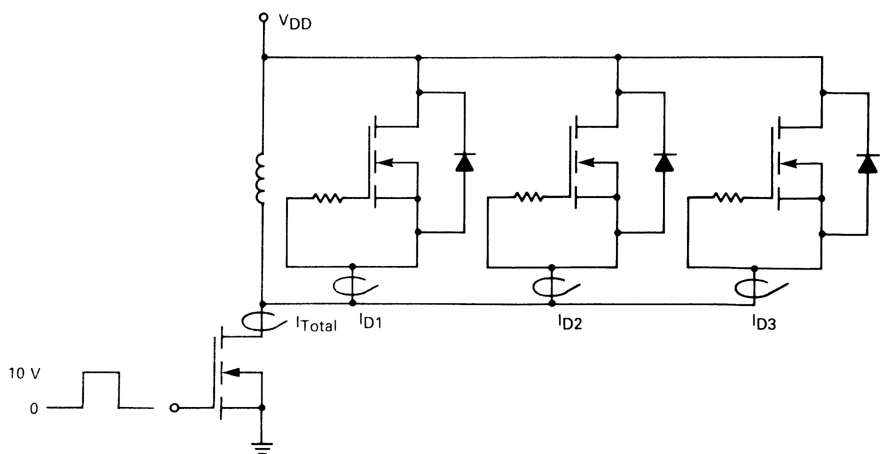


FIGURE 7-25 — TEST CIRCUIT TO OBSERVE CURRENT SHARING OF PARALLELED D-S DIODES

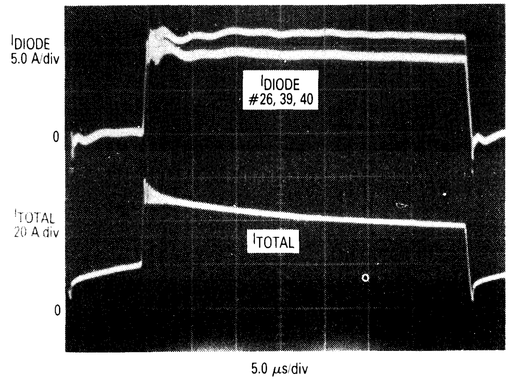


FIGURE 7-26 — DRAIN-SOURCE DIODE ON CHARACTERISTICS OF THREE MTM20N15 WITH MISMATCHED D-S DIODE ON-VOLTAGES

three paralleled diodes and the expected mild mismatch. Also shown is a representation of I_{TOTAL}, which is somewhat distorted due to the saturation of the current transformer that was used.

Current waveforms of devices with the widest variation in t_{rr} are shown in Figure 7-27. Again, even though the diodes are mismatched, the synchronized turn-on and turn-off transitions illustrate the high degree of current sharing that occurs as the load current is commutated between the freewheeling diodes and the drive transistor.

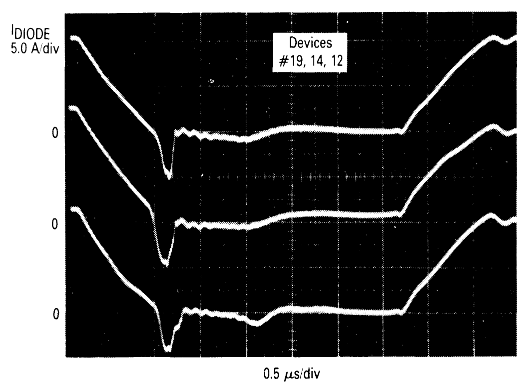


FIGURE 7-27 — PARALLELED DIODE TURN-ON AND TURN-OFF OF MTM15N20 WITH MISMATCHED t_{rr}

Paralleling Power MOSFETs in Linear Applications

Often lauded for their efficient high frequency switching capability, power MOSFETs are ideally suited for a myriad of switching applications. However, some of their other less renowned characteristics also make them attractive to designers of linear systems. Often the reason cited for their use is the inherent ruggedness of the MOSFET as evidenced by the lack of a second breakdown derating. Another characteristic that is appealing is the high input impedance that results in simplified gate-drive circuitry. Also, the transconductance is nearly linear over a wide operating range and its variation among devices in a given product line is small.

Although these benefits are significant, a method of predicting and stabilizing the operating point is necessary before linear operation can be successful. In the following sections a product line is characterized for the parameters pertinent to Q-point variation in the linear mode. The effects of a source resistor on the operating point and the small-signal transconductance are then discussed for single device operation. Finally, these concepts are extended to include the case of paralleled devices with special attention paid to the degree of current sharing.

Device Characteristics Important for Operating Point Stability

When developing a system that operates in the linear mode, it is often either desirable or imperative to accurately fix the system quiescent operating point (Q-point). The most pertinent graphs describing the operation of TMOS Power MOSFETs in the linear mode are those showing the output characteristics (Figure 7-28) and the transfer characteristics, or transconductance curves (Figure 7-29). However, since these are typical curves, they

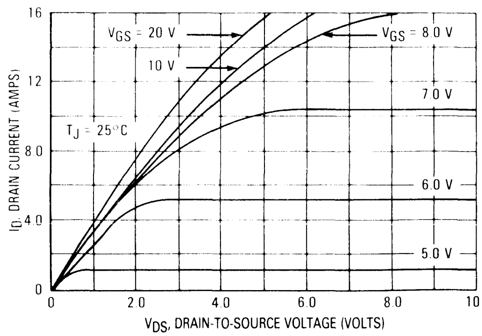


FIGURE 7-28 — TYPICAL OUTPUT CHARACTERISTICS OF AN MTP8N20

relate no information concerning how the operating point may vary within a given product line. For example, on the transfer characteristics curve a desired quiescent drain current of 4.0 amps may correspond to a gate-source voltage of 5.75 volts in a typical device. This gate voltage applied to an atypical device of the same product line may result in a drain current that ranges from 2.5 to 4.5 A.

Matching device parameters is often proposed as a means of ensuring some minimum variation in the Q-point. This approach, especially using the threshold voltage, is not the optimum solution. The gate-threshold voltage is defined as the minimum gate-source voltage at which the MOSFET conducts some small drain current, usually specified as 1.0 mA. On the scale that the transfer characteristics are usually drawn, this 1.0 mA drain current is very small and the exact threshold voltage is indiscernable. It is not difficult to find two devices with nearly identical transfer characteristics that have thresholds that vary by nearly 2.0 volts. Conversely, devices with matched thresholds can have significantly different transfer curves, usually due to a g_{FS} mismatch. Attempting to match devices by comparing transconductance or on-resistance also gives little assurance that the transfer curves will be similar.

If component screening is desired, the most direct method is to actually compare each I_D versus V_{GS} curve. Since this is often impractical, one of two other courses may be taken. The criteria for matching could be the drain current at the gate voltage that is typical of the desired quiescent current. Referring back to the previous example, one may select devices on the basis of I_D at a V_{GS} of 5.75 volts. The other solution, which completely eliminates any device screening, involves the use of source resistors and is detailed in the next section.

Junction temperature is another important variable that influences the quiescent operation point. Figure 6-25 shows that the g_{FS} curve of the MOSFET can be divided into two regions. Below a V_{GS} of 6.1 volts, an increase in T_J increases I_D. This is due to the negative temperature coefficient of $V_{GS(th)}$ dominating the positive coefficient of $r_{DS(on)}$. As T_J rises, the threshold voltage falls and I_D increases despite an increase in $r_{DS(on)}$.

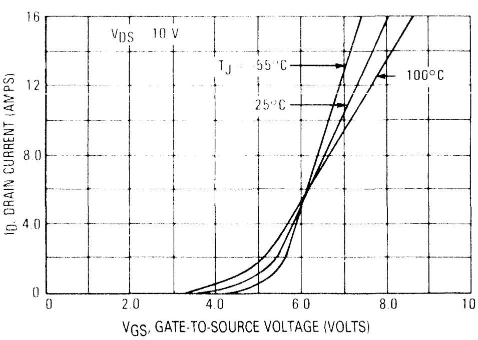


FIGURE 7-29 — TYPICAL TRANSCONDUCTANCE CURVES OF AN MTP8N20

At gate-to-source voltages greater than 6.1 volts, the temperature dependence of $r_{DS(on)}$ governs the change in I_D. Even though $V_{GS(th)}$ is falling as T_J rises, the effect of the increase in $r_{DS(on)}$ begins to dominate, causing I_D to decrease. The temperature dependence of I_D necessitates the consideration of the effect that T_J has on the Q-point, especially at low drain currents where the percentage change in I_D is high.

Using a Source Resistor to Stabilize the Q-Point

Operating point stability can be improved without preselecting devices by using a source resistor. The placement of such a resistor provides degenerative feedback to the gate by decreasing V_{GS} by an amount proportional to the drain current (Figure 7-30). Equations for the small-signal transconductance and voltage gain with and without the source resistor are derived in Table 4.

Determining the effect of a source resistor on the operating point of a power MOSFET is a simple geometric exercise. The first step is to obtain, usually with a curve tracer, the transconductance curve of the device in question. With no source resistance ($R_S = 0\ \Omega$), a vertical

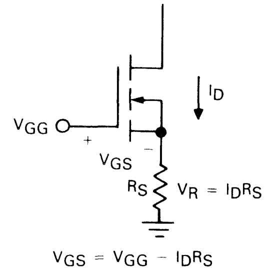
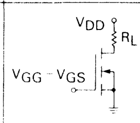
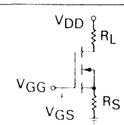


FIGURE 7-30 — SOURCE RESISTOR SUPPLIES NEGATIVE FEEDBACK TO THE GATE

TABLE 4 — Equations for the Small-Signal Transconductance and Voltage Gain With and Without a Source Resistor

	With No Source Resistor	With A Source Resistor
Small-Signal Transconductance	$g_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$	$g_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$ $g_{FS}(\Delta V_{GG} - \Delta I_D R_S) = \Delta I_D$ $g_{FS}\Delta V_{GG} = \Delta I_D(1 + R_S g_{FS})$ $g'_{FS} = \frac{\Delta I_D}{\Delta V_{GG}} = \frac{g_{FS}}{1 + R_S g'_{FS}}$
Small-Signal Voltage Gain	$A_v = -\frac{\Delta V_{DS}}{\Delta V_{GS}}$ $= -\frac{\Delta I_D R_L}{\Delta I_D / g_{FS}}$ $\therefore A_v = -g_{FS} R_L$	$A'_v = -g_{FS} R_L$ $= -\frac{R_L g_{FS}}{1 + g_{FS} R_S}$ $\therefore A'_v = -\frac{R_L}{1/g_{FS} + R_S}$
Circuits		

Primed numbers indicate the effective values for the MOSFET and source resistor combination.

line through the g_{FS} curve will indicate the drain current at a given V_{GS}. For instance, the device depicted in Figure 7-31 will conduct 0.375 A at a V_{GS} of 4.7 volts.

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If a source resistor is included, the abscissa represents the gate-to-ground voltage (V_{GG}). The relationship between V_{GG} and I_D is determined by an R_S load line through a given V_{GG} with a slope of $-1/R_S$. Figure 7-31 shows that for an R_S of 2.0 Ω and a V_{GG} of 5.45 V, the Q-point is fixed so that I_D is still 0.375 A. The effects of varying the gate-to-ground voltage can be determined by constructing parallel lines through the gate voltages of interest. Changing the slope of the line graphically models changes in R_S.

To use the technique of employing a source resistor to improve Q-point stability, the worst case variation in the g_{FS} curves needs to be determined for the product line in question. For this study, 350 MTP8N18's from the same wafer lot were checked for the greatest difference in transconductance curves. The results are shown in Figure 7-32. With these curves, actually sizing R_S and determining the gate voltage for a desired operating point (with a defined allowable variation) is a very simple geometric exercise.

Assume that the desired conditions are as follows:

I_D quiescent = 0.4 A

Allowable I_{DQ} variation from 0.4 A is 0.05 A

T_J = 100°C

An R_S load line drawn through points A and B and extending down to the gate voltage axis determines both the required magnitude of R_S and the quiescent gate voltage. The figure could also be used to show the effects of swinging the gate voltage above and below the quiescent V_{GG}. The dashed curves in Figure 7-32 represent the transfer characteristics at a junction temperature of 25°C. Obviously, the curves vary enough to influence the selection of R_S if the device experiences large swings in T_J.

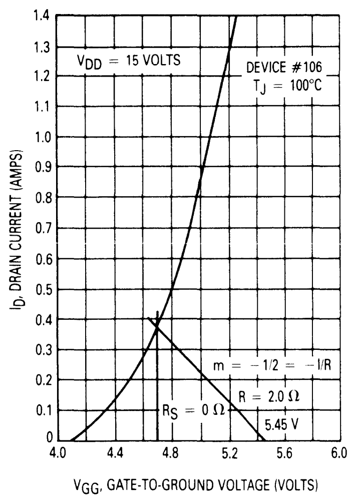

FIGURE 7-31 — GRAPHICAL METHOD OF PREDICTING THE EFFECT OF A SOURCE RESISTOR ON THE QUIESCENT OPERATING POINT

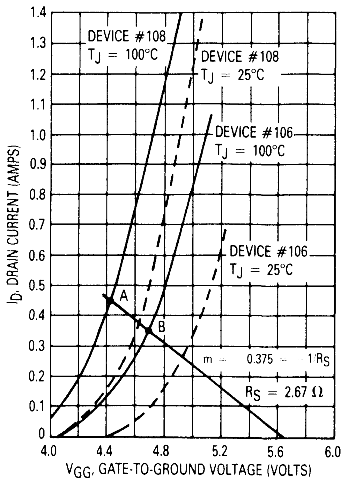

FIGURE 7-32 — USING A SOURCE RESISTOR TO STABILIZE THE QUIESCENT OPERATING POINT

Paralleling MOSFETs in the Linear Mode

In many applications using MOSFETs in the linear mode, the quest is to obtain large swings in the load voltage and utilize as much of the maximum drain-to-source voltage rating as possible. With a large quiescent drain voltage, I_{DQ} must be fairly small to keep the MOSFET power dissipation within manageable levels.

Unfortunately, paralleling in the linear mode at a low I_{DQ} and a high V_{DSQ} is not as straightforward as paralleling in switching applications, for instance. Since this is the most difficult and most common case of paralleling in the linear mode, it is the one that is addressed here.

One problem is that at low currents the potential I_D mismatches, as a percent of the total load current are much greater. As an illustration, one device may conduct 0.3 A at a V_{GS} of 5.0 V, whereas a second device may conduct 1.25 A at the same V_{GS}. If these two devices are operated in parallel in the linear mode, the second would dissipate far more power than the first. Unlike MOSFETs that are paralleled in switching applications, the difference in junction temperature forces an even greater disparity in the amount of current each device conducts.

As explained earlier, at low drain currents the temperature dependence of the drain current is dominated by the negative temperature coefficient of $V_{GS(th)}$ rather than the positive coefficient of $r_{DS(on)}$. Consequently, the device that is dissipating the most power will heat up, carry more current and dissipate even more power.

Although the situation appears to be hopeless — very wide variations in g_{FS} curves causing even greater differences in power dissipation — the use of source resistors can minimize the differences and dramatically improve the chance of success.

Using a source resistor to stabilize the operating point of devices with widely differing g_{FS} curves is also applicable to improving current sharing among MOSFETs operated in the linear mode. If the Q-points are closely matched, then the paralleled devices will, by definition, carry nearly the same drain currents and incur approximately the same power dissipation.

In this study, the devices with widest variation in g_{FS} curves were paralleled in the circuit shown in Figure 7-33. Individual source resistances of 3.3 Ω were chosen as a good compromise between a stable Q-point and the lower system gain are poorer efficiency attributable to an increase in R_S. Table 5 establishes the equations for g_{fs} and small signal voltage gain of paralleled MOSFETs with and without source resistors.

Figure 7-34 shows the results of pairing the devices with the widest mismatch in g_{FS} curves. Note how the drain currents can be predicted by relating the g_{FS} curves (Figure 7-35) to the instantaneous gate voltage. Case temperatures were also monitored, but the difference was not as great as expected. While the device that carried the most current ran hotter, it did so by only a couple of degrees (83 versus 85°C). A difference of 5 to 10°C was expected but did not materialize, most likely due to slight variations in the heat sinks. The MOSFETs were mounted on separate heat sinks, again to simulate a worst case condition. Close thermal coupling by placing units on the same heat sink is recommended to minimize variations in T_C and T_J and therefore decrease any thermally induced differences in g_{FS} curves.

The benefits of device matching are shown in Figure 7-36. The nearly identical drain currents were obtained by matching devices by comparing the drain currents they would conduct at a V_{GS} of 4.7 volts and a junction temperature of 25°C. The slight mismatch at higher drain currents is mainly due to a small difference in g_{FS} curves at a T_J of 100°C. The case temperatures of these two devices were essentially identical. The 20 Ω gate resistors

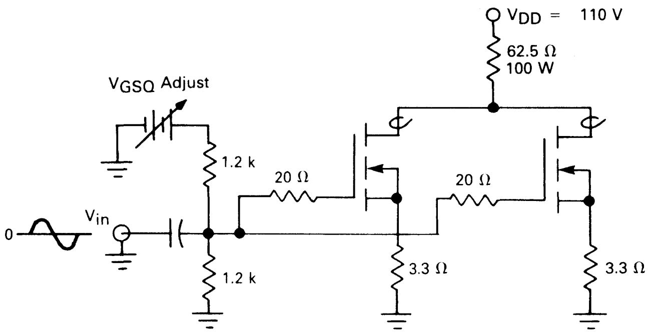

FIGURE 7-33 — CIRCUIT TO TEST CURRENT SHARING IN PARALLELED MOSFETs OPERATING IN THE LINEAR MODE

TABLE 5 — Equations for the Small-Signal Transconductance and Voltage Gain of Two Paralleled MOSFETs With and Without Individual Source Resistances.

	With No Source Resistors	With Individual Source Resistors, R_S
Small-Signal Transconductance	$\Delta I_{D1} = \frac{g_{FS1}}{\Delta V_{GS}}, \Delta I_{D2} = \frac{g_{FS2}}{\Delta V_{GS}}$ $\Delta I_{D1} + \Delta I_{D2} = \frac{g_{FS1} + g_{FS2}}{\Delta V_{GS}}$ $g_{FS1} + g_{FS2} = \frac{\Delta I_{D1} + \Delta I_{D2}}{\Delta V_{GS}}$ $\therefore g_{FST} = g_{FS1} + g_{FS2}$	$g_{FS1}(\Delta V_{GS1}) = \Delta I_{D1}, g_{FS2}(\Delta V_{GS2}) = \Delta I_{D2}$ $g_{FS1}(\Delta V_{GG} - \Delta I_{D1} R_S) + g_{FS2}(\Delta V_{GG} - \Delta I_{D2} R_S) = \Delta I_{D1} + \Delta I_{D2}$ $g_{FS1}(\Delta V_{GG}) + g_{FS2}(\Delta V_{GG}) = \Delta I_{D1}(1 + g_{FS1} R_S) + \Delta I_{D2}(1.0 + g_{FS2} R_S)$ $(g_{FS1}+g_{FS2})(\Delta V_{GG}) = (\Delta I_{D1} + \Delta I_{D2})(1.0 + \bar{g}_{FS} R_S)$, where $\bar{g}_{FS} = \frac{g_{FS1} + g_{FS2}}{2}$ $\therefore g'_{FST} = \frac{\Delta I_T}{\Delta V_{GG}} \doteq \frac{g_{FS1} + g_{FS2}}{1.0 + \bar{g}_{FS} R_S}$
Small-Signal Voltage Gain	$A_V = \frac{-\Delta V_{DS}}{\Delta V_{GS}}$ $= \frac{-\Delta I_{DT} R_L}{\Delta I_{DT}/g_{FST}}$ $\therefore A_{VT} = -g_{FST} R_L$	$A'_{VT} = g'_{FST} R_L$ $= \frac{-R_L(g_{FS1} + g_{FS2})}{1.0 + \bar{g}_{FS} R_S}$

Primed variables indicate the effective value for the MOSFET and source resistor combination.
Subscript "T" indicates the total value for all MOSFETs in parallel.

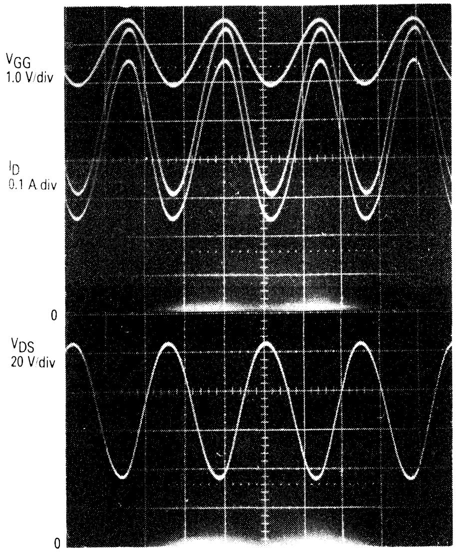

FIGURE 7-34 — V_{GG}, I_D AND V_{DS} WAVEFORMS OF MISMATCHED MTP8N20 PARALLED IN THE LINEAR MODE R_S = 3.3 Ω

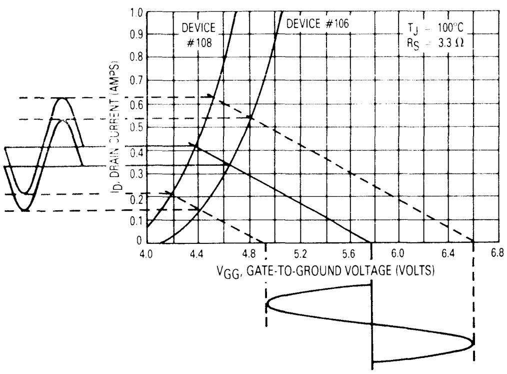

FIGURE 7-35 — TRANSFER CHARACTERISTICS AND R_S LOADLINE OF MISMATCHED MTP8N18

in Figure 7-33 serve an important function. The high input impedance and high frequency capabilities of the MOSFET present the possibility of self-induced oscillations in paralleled devices. Inserting small resistances in series with each gate defuses the problem by degrading the Q of the LC network formed by the gate-and-drain inductances and the MOSFETs gate-to-drain capacitance. The magnitude of R_S necessary to allow trouble-free operation depends on the value of each of the circuit parasitics. The circuit in Figure 7-33 oscillated with series gate resistances of 10 Ω, but stabilized with 20 Ω. Increasing R_S results in a more stable circuit at the expense of lower bandwidth.

In conclusion, the same method used to stabilize the operating quiescent point of small signal MOSFETs can be easily extended to linear applications of power MOSFETs. After sampling a product line to obtain the widest expected variation in g_{FS} curves, a simple graphical technique can be used to accurately predict the Q-point associated with a given source resistor and gate-to-ground voltage.

Since small variations in Q-point limit possible variations in drain current, successful paralleling is also achievable with this same method. The only additional consideration is the need to limit potential self-induced oscillations with individual gate suppression resistors.

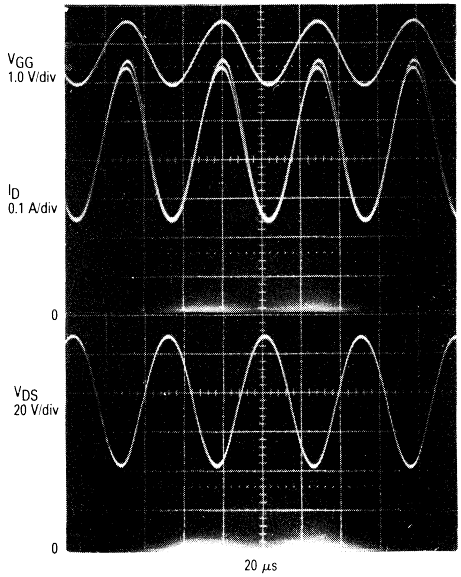

FIGURE 7-36 — V_{GG}, I_D AND V_{DS} WAVEFORMS OF MATCHED MTP8N20 PARALLELED IN THE LINEAR MODE R_S = 3.3 Ω

Applications of Paralleling MOSFETs

Paralleling Power MOSFETs in a Very Fast, High Voltage High Current Switch

There are many applications requiring an extremely fast high voltage, high current semiconductor switch, especially for device characterization, where the switch must be much faster than the device under test (DUT). Power MOSFETs serve this function extremely well, but they are presently limited in current capability. However, they can be readily paralleled to increase the current, without using current sharing ballast resistors, due to the inherent positive temperature coefficient of the drain-source ON-resistance $r_{DS(on)}$. For example, if the transconductance g_{FS} of the FETs are unmatched, the FET with the highest g_{FS} would tend to take initially the largest drain current, but due to the greater dissipation ($I_D^2 r_{DS(on)}$) and resulting temperature rise, $r_{DS(on)}$ would increase, thus, self-limiting the current. This process tends to equalize the drain currents of the respective devices.

A circuit for generating this fast pulse is shown in Figure 7-38. It uses 15 N-Channel power MOSFETs in parallel as the output power switch to achieve the system capability of 150 A of peak, pulsed current. The FETs used were unmatched TO-220 MTP5N40(2.7 V < $V_{GS(th)}$ < 3.9 V) with 400 V blocking capability $V_{(BR)DSS}$, 5.0 A continuous drain current rating (10 A pulsed) and specified $r_{DS(on)}$ of 1.0 Ω max. The TO-220 devices lend themselves to efficient circuit layout and packaging (Figure 7-37).

The particular application for which this circuit was designed required the DUT to be referenced to ground (drain circuit); consequently, the switch is powered with a negative, high voltage supply ($-V_{SS}$) tied to the FETs sources. Thus, the ground referenced pulse generator output must be level translated to this negative supply. For fast switching, this translator must have the current drive capability for quickly charging the power MOSFETs input capacitances C_{iss} and reverse transfer capacitance C_{rss}. To accomplish this, two P-Channel MTP2P45's are

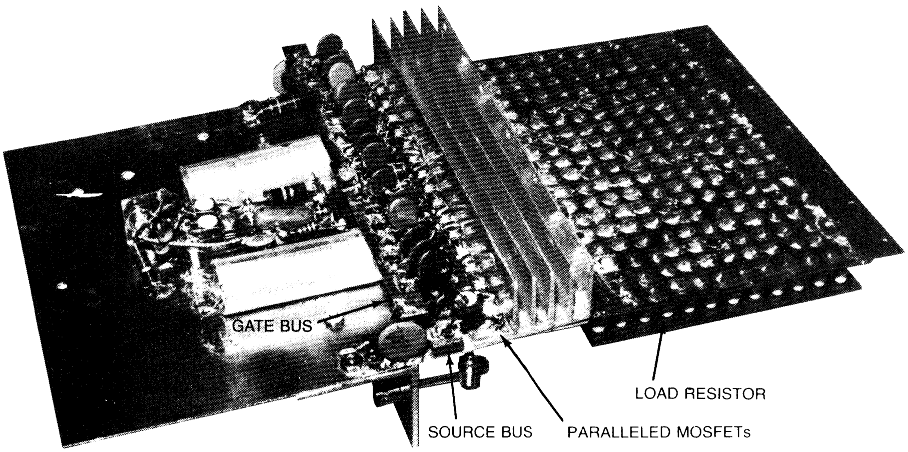

FIGURE 7-37 — BREADBOARD LAYOUT OF THE SWITCH ILLUSTRATING TIGHT PACKAGING CONCEPTS

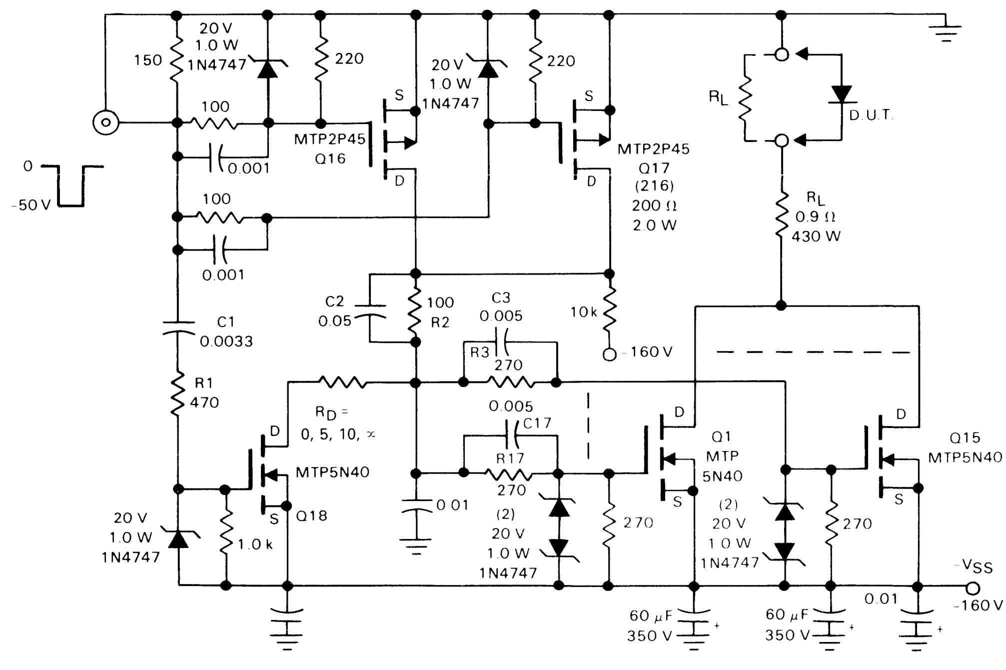

FIGURE 7-38 — PARALLELED POWER MOSFETs 150 A SWITCH

configured as a parallel connected, series switch. These FETs are turned on by the negative going input pulse derived from a 50 V, 10 ns rise time pulse generator. A 20 V zener diode is used to protect the gate-source and still allows adequate gate-drive for rapid switching of the drain circuit. Connected to the drain is a current limiting resistor R2 (with speed-up capacitor C2) feeding the 15 respective gate circuits (only circuits 1 and 15 are shown); each circuit consists of a direct-coupled resistor, speed-up capacitor and protection zener diodes. The zener diodes come into operation when high V_{SS} (-160 V) is used. When V_{SS} is reduced to as low as 40 V, the gate-drive voltage dividers still provide adequate drive. For low duty cycles ($<$ 1.0%), the resistors can be relatively low wattage. The circuit can be operated within the blocking voltage capability of the FETs (to 400 V), but the passive circuit elements should be scaled up accordingly.

To improve the turn-off switching times of the power switch, the FET capacitance must be quickly discharged. This is accomplished by the N-channel FET clamp Q18 which, when turned on, supplies the reverse gate voltage to the power switch through the voltage storing effect of C3 across R3. FET Q18 is turned on coincident with the trailing edge of the input pulse by means of the differentiating network C1-R1, the derived positive-going pulse supplying the gate-drive and duration for the clamp action.

The complete pulse-width voltage and current waveforms are shown in Figure 7-38 with the time expanded turn-on and turn-off waveforms shown in Figures 7-39 and 7-40.

For these test conditions ($V_{SS} = -160$ V, R1 $\approx$ 0.93 Ω), approximately 150 A at 140 V (21 kW peak) was switched in extremely fast times; the voltage turn-on time was less than 10 ns and the current rise time being circuit inductance limited to about 250 ns.

Without the turn-off clamp circuit of Q18 the drain voltage (and resistive load drain current) turn-off time was about 1.0 μs (Figure 7-41a) due to the time required to discharge the FET's capacitances.

With the clamp, this time can be substantially reduced (0.2 μs) as shown in the photos of Figures 7-41b and 7-41c, the capacitance discharge limiting resistance R_D being 10 Ω and 5.0 Ω respectively. As this resistor value is decreased, the FET will turn-off faster, but consequently be subjected to greater switching perturbations (Figure 7-40, $R_D = 0$). Thus, the turn-off characteristics can be somewhat tailored to the requirements.

Care should be exercised in the layout of the fifteen parallel FET's, especially with the gate-source drive circuitry. The fifteen FET's are mounted side-by-side with the gates and sources tied to their two respective, parallel run busses (Figure 7-37). Device lead lengths should be made as short as possible and the source buss should be RF by-passed at several points along its length to minimize reactive effects.

Obtaining high power resistive loads with low inductance is a problem. For a pulsed current of 150 A and a low resistance of about 0.93 Ω, the peak power would be about 21 kW. Obviously, the duty cycle has to be very low for this application to avoid overheating the load resistor. This resistor was fashioned with 216,200 Ω, 2.0 W, metal oxide resistors sandwiched in parallel. This resulted in a load resistor of approximately 430 W capability. Therefore,

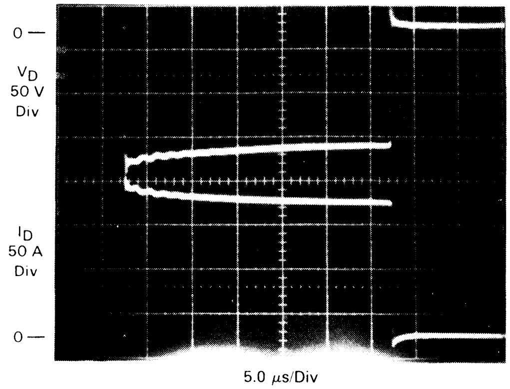

FIGURE 7-38 — SWITCHED VOLTAGE AND CURRENT

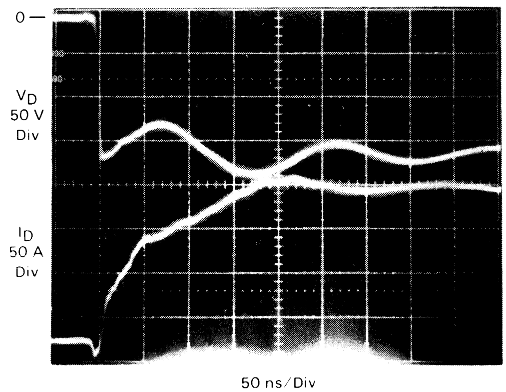

FIGURE 7-39 — TURN-ON DRAIN VOLTAGE AND CURRENT

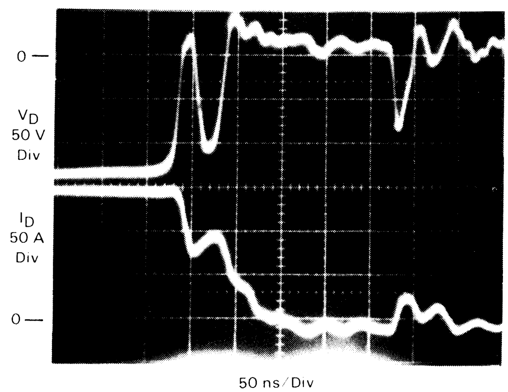

FIGURE 7-40 — TURN-OFF WITH CLAMP, $R_D = 0$

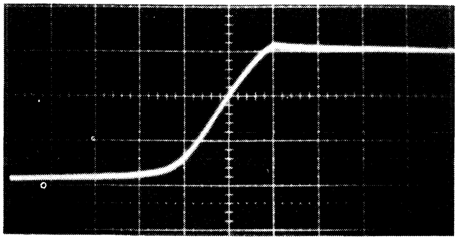

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FIGURE 7-41a — TURN-OFF DRAIN VOLTAGE $R_D = \infty$

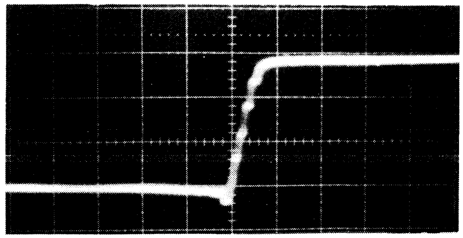

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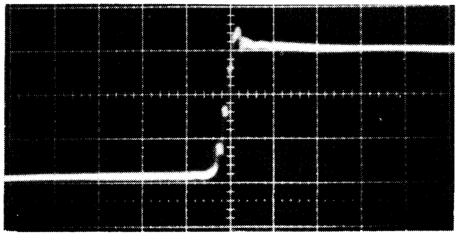
FIGURE 7-41b — TURN-OFF DRAIN VOLTAGE $R_D = 10\ \Omega$



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Vert. = 500 V/Div
Horiz. = 500 ns/Div

FIGURE 7-41c — TURN-OFF DRAIN VOLTAGE $R_D = 5.0\ \Omega$

duty cycles of less than 1.0% should be used to ensure operation within the load rating while still offering good oscilloscope viewing.

Fast, Complementary Power MOSFET Switch

Many present day semiconductors require test circuits that can supply large pulsed currents and fast voltage transitions.

In today's real world circuits, rectifiers are vital components in motor controls and in switching power supplies as the operating frequency and power level increases. Rectifier characteristics and selection can be critical for these applications.

Due to its fast switching speed, the complementary power FET switch, shown in Figure 7-42, is useful in measuring forward (t_{fr}) and reverse (t_{rr}) recovery times of fast recovery rectifiers, as well as for general uses requiring a complementary power signal.

The internal collector-emitter diode in power Darlington transistors and the drain-source diode in power FETs can be of great interest to the circuit designer. Rectifier operation is dependent on several conditions, two of which are the turn-off rate (di/dt) of forward current and the rate of rise (dv/dt) of the reapplied blocking voltage.

In some switching power supplies, a designed-in dead time is required between the switching transistors to avoid simultaneous conduction. The duration of the dead time and the dv/dt of the reapplied blocking voltage can be critical, especially for some power MOSFETs. This complementary switch, with dv/dt adjustment and control of the dead time, can help determine the capability of power FETs in circuits when the above conditions are important.

Circuit Configuration and Operation

Two CMOS Quad 2 input NOR gates (MC14001) are used for pulse generation and signal delay. Gates A1 and A2 are configured as an astable multivibrator (MV), clocking the respective delay and pulse width monostable MV's. The turn-on pulse is frequency (R1) and width adjustable (R4) whose output feeds, in order, cascaded bipolar transistors Q5, Q6, power FET Q7 and the N-Channel output switch Q8.

Pulse delay (R2) and width control (R3) for the P-Channel switch (Q4) are obtained with Gates B1, B2, B3 and B4 which drives two cascaded bipolar transistors Q1, Q2 and power FET Q3.

Transistor Q9 drives power FET Q10 as an optional clamp to turn-off Q8 rapidly by discharging gate capacitance through a low impedance path. Duration of the clamp interval is dictated by the RC differentiating circuit in the base of Q9.

The complementary output FETs Q4 and Q8 consist of four P-Channel (MTP8P10's) in parallel and four N-Channel (MTP20N10's) in parallel. A limiting resistor R_D is shown in the drain of Q8 but may be in the drain of Q4 or in both drains. The external load may be a test rectifier or any other load requiring the unique drive characteristics of this tester: fast, adjustable, complementary waveforms.

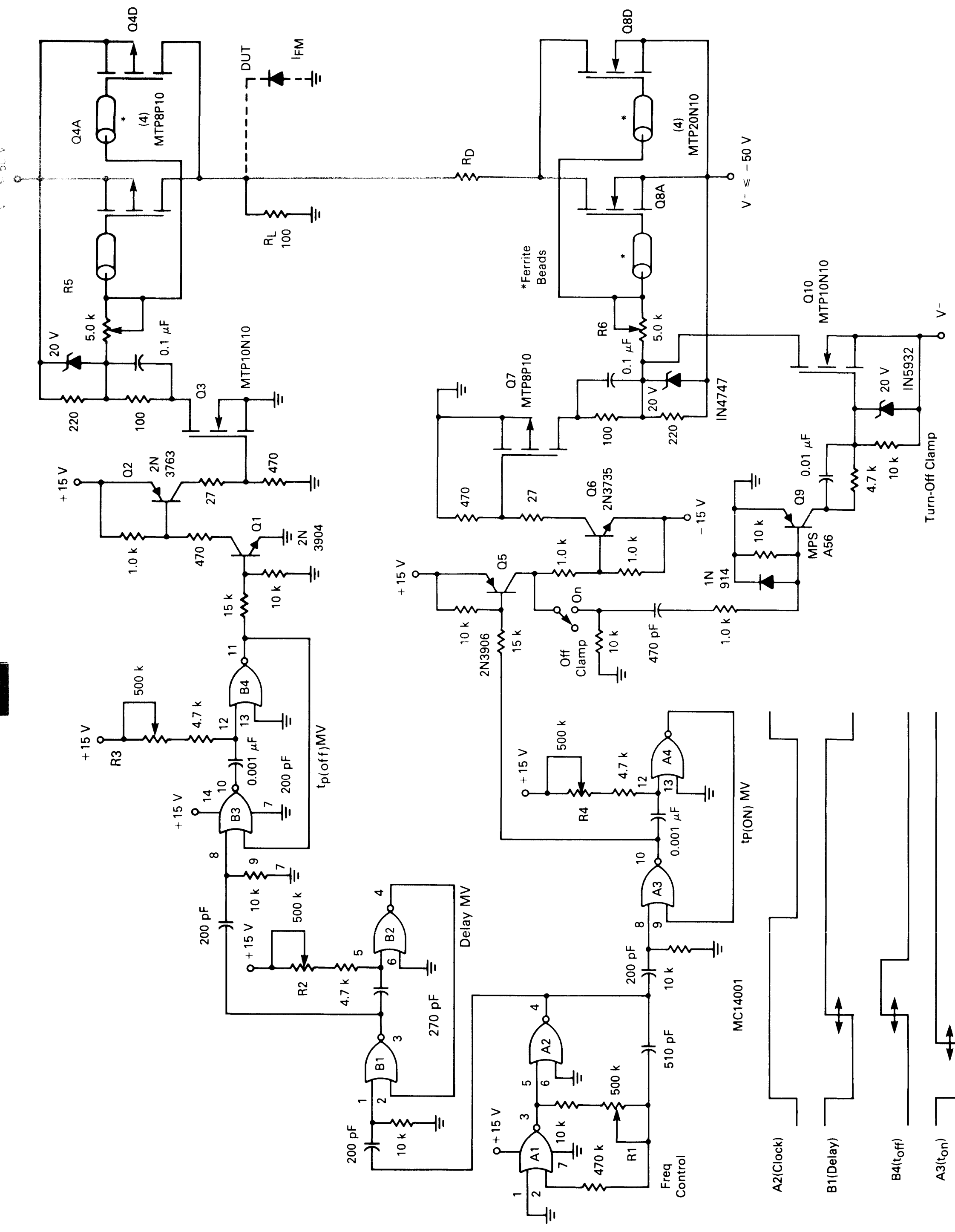

FIGURE 7-42 — FAST, COMPLEMENTARY POWER FET SWITCH

The negative output switch Q8 (N-Channel) is capable of switching at least 100 A, whereas the positive switch Q4 (P-Channel) is limited to about 50 A due to the differences in the respective on-resistances. Additional devices can be paralleled for either switch for higher currents, if so required. Also, power FETs with higher V_{DSS} ratings may be used.

Output Waveforms

The negative and positive switched output waveforms are shown in Figures 7-43a and 7-43b, with the positive voltage delayed about 2.0 μs, in Figure 7-43a. The external load resistor R_L is about 2.0 ohms, with the switched voltages of about ± 42 volts.

In Figure 7-43a, the switched negative and positive voltages have very fast leading edges (about 10 ns) and slow trailing edges (about 3.0 μs and 1.0 μs, respectively). Figure 7-43b shows the same switched voltages but with the clamp transistor (Q10) switched on. This discharges Q8 gates through a low impedance path and speeds up the trailing edge of the negative voltage to about 25 ns instead of 3.0 μs.

In Figure 7-45, a MR821 fast recovery rectififer is shown as the load, with I_{FM} = 40 A, di/dt = 300 A/μs, and the dv/dt of the applied blocking voltage about 2500 V/μs.

Adjustment of dv/dt is accomplished with R5 for the positive switched voltage and with R6 for the negative voltage.

Figure 7-44 shows the transition time of about 35 ns between the negative and positive voltages, with both the clamp on and with Q4 diverting current from Q8.

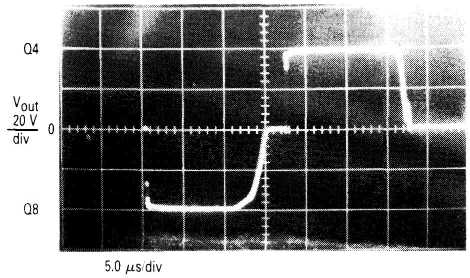

FIGURE 7-43a — FAST LEADING EDGE

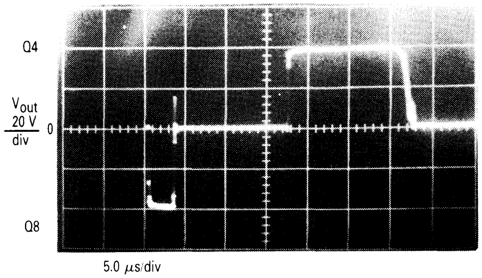

FIGURE 7-43b — FAST TRAILING EDGE, NEG. VOLTAGE, TURN-OFF CLAMP Q10 "ON"

FIGURE 7-43 — NEGATIVE AND POSITIVE SWITCHED OUTPUT VOLTAGE WITH R_L – 2.0 Ω, V^- AND $V^+ \approx$ 42 V, DRAIN Q8

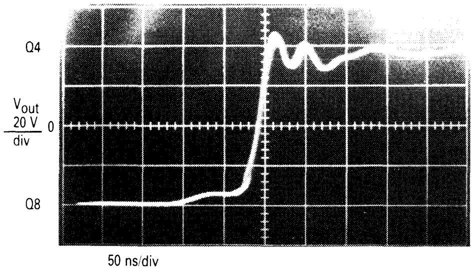

FIGURE 7-44 — NEGATIVE AND POSITIVE TRANSITION, DRAIN Q8, TURN-OFF CLAMP Q10 "ON"

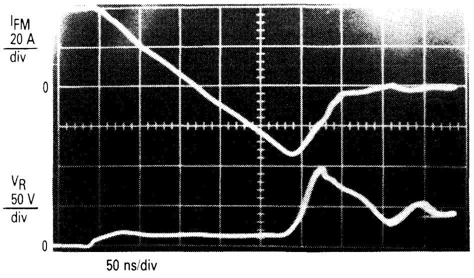

FIGURE 7-45 — REVERSE RECOVERY (t_{rr}) OF MR821 FAST RECOVERY RECTIFIER

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Chapter 8: TMOS Applications

100 kHz Switch Mode Power Supply

Power FETs have proven themselves to be performance competitive and cost effective in flyback regulators operating at 100 kHz to 200 kHz.

The circuit described here proves the point. It is a 60 W 100 kHz FET switcher with four output voltages ± 5.0 V and ± 12 V. It operates from 120 Vac, has an efficiency of 75% and the total parts cost is approximately $35.

Components unique to this high frequency design include the following:

- Motorola's MTP5N40 power FET. This 5.0 A, 400 V device has only one ohm of on-resistance and is driven directly from a linear IC. It not only switches in less than 50 ns but has enough RBSOA to eliminate the need for snubbers.
- Pulse Engineering's PE63133 power transformer. This is a continuous mode flyback transformer which is ideally suited to high frequency operation. Zener clamps are not required because the clamp winding is interleaved with primary halves. Regulation of the auxillary outputs is within ± 10% under varying conditions of line and load.
- Motorola's MC34060 Switchmode control IC, 4N27 optoisolator, and MC1723 linear regulator. These devices are used in a practical demonstration of a low-cost, three-chip control system. The MC1723 is the error amplifier, the MC34060 is a fixed frequency PWM, and the 4N27 couples the feedback signal from the MC1723 to the MC34060.
- Motorola's MBR1035 (TO-220) Schottky rectifier was used to rectify the +5.0 V output at half the cost of a comparable DO-4. Similar cost savings result from using the TO-220 fast recovery rectifiers, i.e., the MUR805 in the ± 12 V outputs.
- Mepco/Electra's 3428 series of output capacitors. These high frequency electrolytics feature low ESR and high RMS current ratings. Only 50 to 70 mV (PP) of ripple occurs at the outputs. Power loss is less than 0.5 W.

Circuit Design

The goal of most low-power flyback designs is for reduced parts count (or size) and reduced cost. The 60 W 100 kHz switcher shown schematically in Figure 8-1, met these requirements. At 100 kHz, the transformer size and cost are reduced by about 30% compared with a 20 kHz design. Also, at 100 kHz, a FET can be driven directly from logic circuits (100 to 200 mA) and still switch very efficiently. This eliminates the need for drive interface circuits. The output caps used are about 50% smaller and they cost less as well. Finally, a relatively new three-chip control system is used. It replaces an expensive and performance limited drive transformer with a lower-cost optocoupler.

The FET is the control element for the flyback transformer and is directly driven from the MC34060 linear IC. A rather standard off line starter circuit is used to initially power the control circuit and this is also lower in cost than the filament transformer supply which is often used to power a single-chip system. The design procedure followed here was:

1. Design and test the power stage.
2. Add and stabilize the control loop.
3. Change from dc to ac power.

The FET waveforms obtained with the design are shown in Figure 8-2. The exceptional switching speed of the FET can be varified here (less than 50 ns) and ringing on the current waveform is due to the layout which includes a current-sense loop and noise pickup on the scope probe.

The input capacitor does not reduce in size like the outputs because it is needed for energy storage which still occurs at 60 Hz. Noise filters used here include a toroid from PE and the economical 41GS series of tan-

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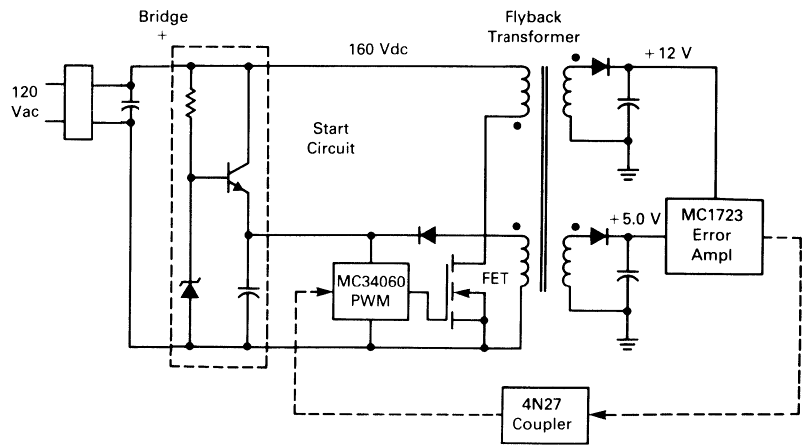


FIGURE 8-1 — REGULATOR BLOCK DIAGRAM

talum capacitor from M/E. The 12 V output rectifiers were Motorola's MUR805 ultrafast recovery button rectifiers which are housed in a TO-220 package. They were ideally suited to this relatively high current (10–15 A peak) application because the correct amount of heat sinking was easily attained by simply bolting a fin to the tab.

The relatively new MBR1035 TO-220 Schottky rectifier is the best choice for rectifying the 5.0 V output. It is about half the cost of the equivalent DO-4 version, a 1N6095.

The overall efficiency of this regulator (including the control circuits) is 75%. As usual, most of the losses are associated with the power handling components as noted in Table 1.

TABLE 1 — Efficiency Data

1. Input Power				
V_{in}	**I_{in}**	**P_{PRMS}**	**P_A**	**P_F**
160 Vdc	0.6 A	96	96	100%
120 Vac	1.4 A	170	95*	56%
*Note using Clark-Hess wattmeter.				
2. Output Power				
Winding	5.0	−5.0	+12.0	−12.0
Load (ohms)	1.0	10.0	8.0	8.0
Voltage	5.1	5.1	13.2	13.3
Power	2.5	2.6	21.5	22.0
3. Efficiency				
Eff. = P_O/P_{in} = 72 W/95 W = 75%				
4. Estimated Losses				
FET	4.0 W	Fast Recovery (both)		8.0 W
Schottky	4.0 W	Misc.		5.0 W
Transformer	2.0 W			

The control loop contains three chips as noted earlier. The functional diagram of this arrangement is shown in Figure 8-3. The first chip is an MC1723 linear regulator. It is used here to provide a 5.0 V reference and an error amplifier. It is powered from the +12 V output winding and receives feedback or control signal from the +5.0 V output. The MC1723 drives the second chip, a 4N27 optocoupler. The coupler maintains isolation between the primary and secondary windings and couples the dc control signal to the input of the third chip, a MC34060. The MC34060 performs a fixed frequency pulse width modulator (PWM) function and is used to directly drive the FET power switch which is connected to the primary or energy storage winding.

The key regulating blocks are the 0 to 3.0 V sawtooth oscillator and the feedback comparator. As the feedback signal is raised from 0 to 3.0 V, it gradually narrows the on time of output pulse coming from the comparator. During start up, the feedback is missing and resistor divider network controls the second or dead-time comparator to ensure that on time cannot exceed 45%. This, and the soft start capacitor, prevents transformer saturation problems during start-up. Pull down of the gate voltage is accomplished as shown in Figure 8-3 with the addition of a low cost TO-92 PNP transistor (Q3). In this design, the MC34060 is started off line with the addition of a 200 V transistor (Q2) and 12 V zener as shown in Figure 8-4. It ultimately (at normal line voltage) runs off the 12 V auxiliary winding which back biases this transistor. Because it and the FET gate draw so little current from the line, about 20 mA, undervoltage inhibiting common to bipolar designs was not required here and this current becomes functional and runs safely when the input reaches 40 Vac.

The performance of this 100 kHz switcher is similar to most others. It is relatively easy to keep output ripple, both

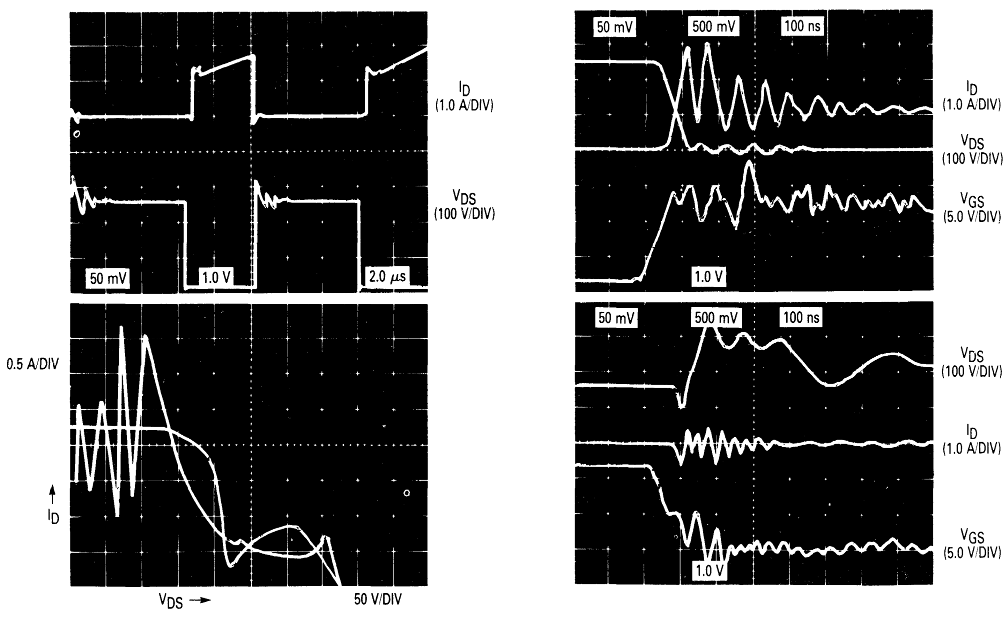


FIGURE 8-2 — FET WAVEFORMS — 120 Vac, FULL LOAD

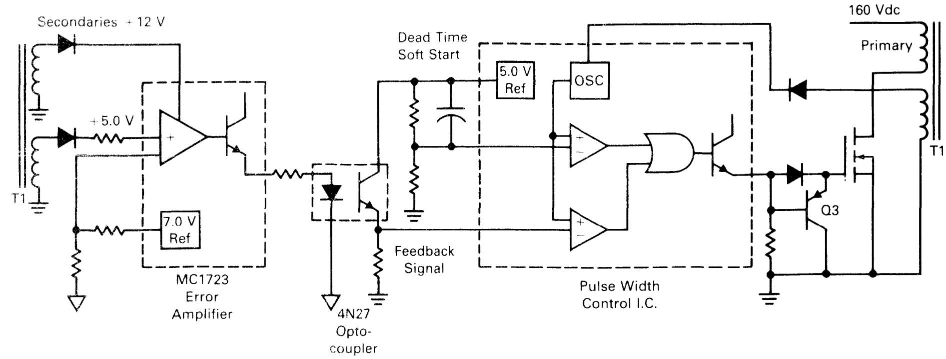


FIGURE 8-3 — THREE CHIP CONTROL SYSTEM

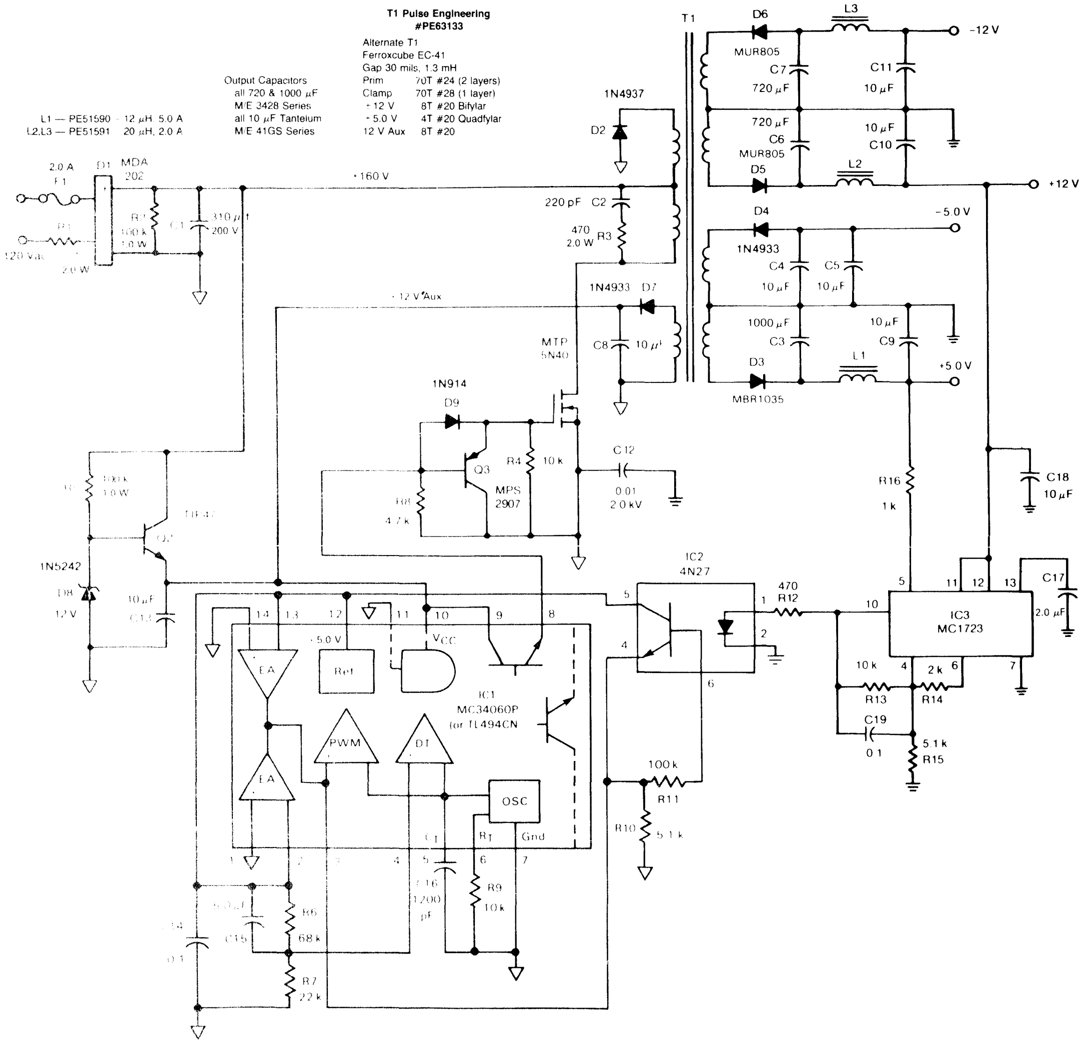


FIGURE 8-4 — 100 kHz FET REGULATOR

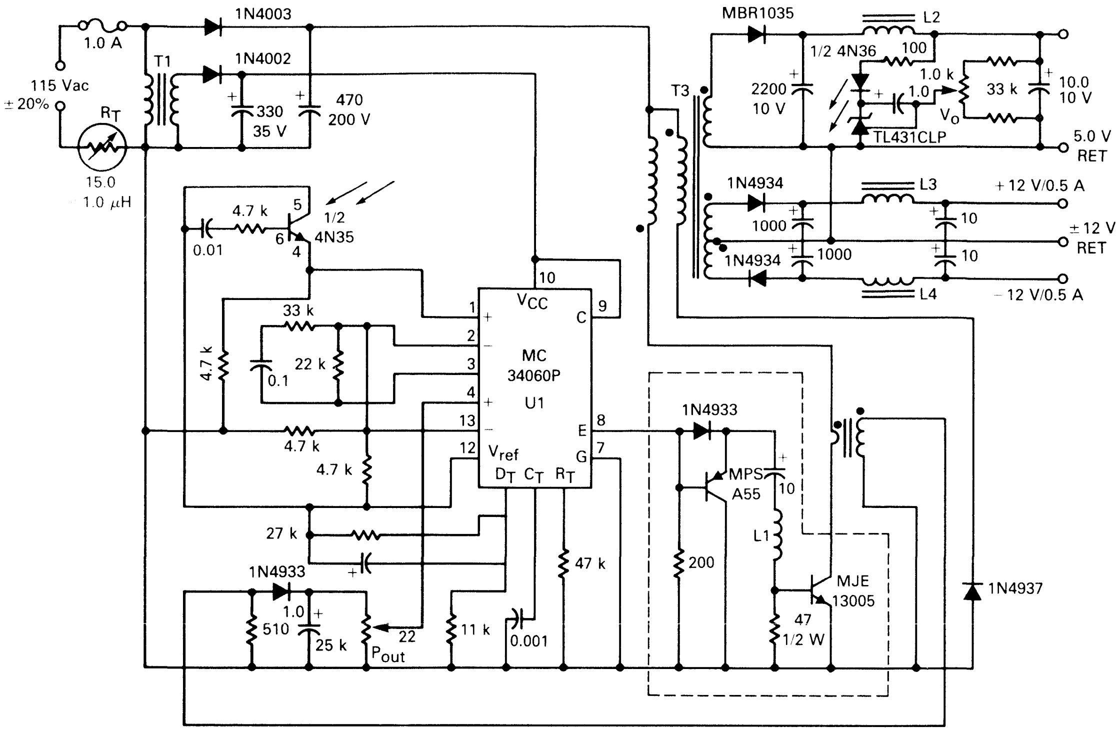


FIGURE 8-5 — 20 kHz SWITCHING POWER SUPPLY USING A BIPOLAR SWITCH

Unless otherwise noted:
All resistors are 1/2 W
All capacitors rated 25 V

Transformer Data

T1: Internal power supply transformer for switching regulator
TRAID F90X Primary — Black-red and black green. Secondary — Blue and green

T2: Collector current sense transformer Coilcraft D1870
Core: Ferroxcube 768T183-3C8
Windings: Primary — 1 turn, #26 Awg. lead from primary of T3 looped through center of T2, note dots.
Secondary — 100 turns, #28 Awg.

T3: High frequency output transformer
Core: Coilcraft 11-464-16, 0.025 gap in each leg.
Bobbin: Coilcraft 37-573
Windings: Primary — 2 windings 75 turns each, #26 Awg, bifilar wound. One winding is connected to the MJE13005 and the second is connected to the 1N4937, note dots.
Secondary — 5.0 V, 6 turns, #16 Awg.
12 V, 14 turns, #22 Awg, bifilar wound.

L1: Base drive inductor
Core: None
Bobbin: Ferroxcube 1408F1D
Winding: 39 turns, #28 Awg., 10.5 μH

L2: 5.0 Volt output filter inductor
Coilcraft Z7156, 15 μH at 5.0 A

L3,L4: 12 V output filter inductors
Coilcraft Z7257, 25 μH at 1.0 A

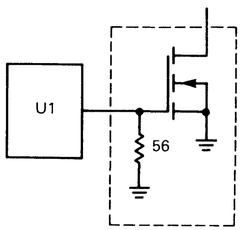


FIGURE 8-6 — POWER MOSFET VERSION

60 Hz and 100 kHz, below 100 mV on all outputs. (See Table 2.) Line regulation here was excellent, less than 0.1%, but load reg (2.0%) could have been better. Normally tight layouts and higher loop gain can get this down to 0.1 to 0.5% as well. Efficiency (75%) and cross regulation (±10%) are also similar to other multiple output switcher designs.

TABLE 2 — Output Data

1. Ripple Voltages (120 Vac, Full Load)				
Winding	+5.0	−5.0	+12	−12
100 k Ripple (PP)	60 mV	300 mV	70 mV	50 mV
60 Hz Ripple (PP)	20 mV	50 mV	70 mV	60 mV
Noise Spikes (PP)	2.0 V	2.0 V	2.0 V	2.0 V
2. +5.0 V Regulation				
Line	100 Vac	100 Vac	130 Vac	130 Vac
Load	Full	Half*	Full	Half
Voltage	5.10	5.21	5.10	5.21

*Note: +5.0 V Load increased to 2.0 ohms and −12 V load removed.
Load Reg. = $\Delta V_O/V_O$ = 0.11/5.1 = 2.2%.
Line Reg. $\Delta V_O/V_O$ = 0.005/5.1 = 1.0%.

20 kHz Switcher

A less novel 20 kHz flyback switcher provides a good illustration of the interchangeability of FETs and bipolar transistors. The 35 watt supply shown in Figure 8-5 was originally designed around the MJE13005 bipolar output transistor. With the bipolar, crossover time and case temperature rise were measured with V_{in} at 160 Vdc and outputs fully loaded.

A view of the crossover waveforms is shown in Figure 8-7. At the full load case temperature of 71°C, the MJE13005 is turning on in a crossover time of slightly under one microsecond, (46°C case temperature rise), providing a good relative measure of its efficiency as a switching element.

When an MTP4N50 FET is substituted for the bipolar transistor, the drive circuit is greatly simplified as illustrated in Figure 8-7. Now the MC34060 control circuit is capable of directly driving the FET, eliminating the complex base drive circuitry required for the bipolar. The end result is that the FET can be substituted for the bipolar by removing five components and changing one resistor value. Thus, the FET substitution results in a reduced components count.

Performance wise, the FET is the better choice, with a considerably improved crossover time, Figure 8-8, and a case temperature rise of only 18°C.

Automotive DC-DC Converter

In the previous example, FET drive circuitry was maximally simplified. The penalty for this simplification is that turn-on gate-source voltage, applied across a relatively low gate-source resistor, draws approximately as much drive power as a bipolar would. This example illustrates how the FET's low drive power requirements can be used advantageously. The circuit, shown in Figure 8-9, is a 25 watt DC-DC converter that is designed for automotive use. It uses the same control IC as the previous example. The significant difference is the addition of Q1, D3, & D6 to the drive loop. This arrangement provides a low impedance loop for fast turn-off, while drawing a negligible amount of current from the IC after the FET is turned-on.

The FET and this circuit work well together. Efficiency was measured at 78% with V_{in} at 13.6 volts, load regulation at 0.4%/Amp., and line regulation at 0.01%/volt. In general, the comparatively low $r_{DS(on)}$ of FETs with 100 V (or less) ratings makes the FET a particularly good choice for this type of application.

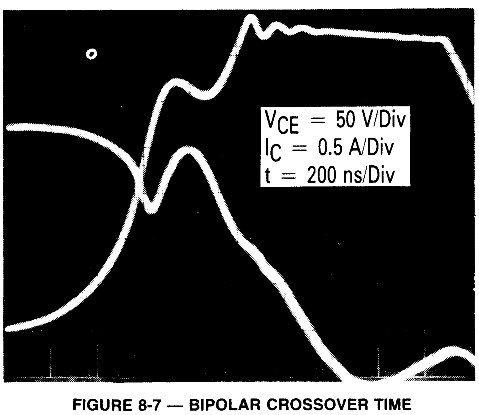


FIGURE 8-7 — BIPOLAR CROSSOVER TIME

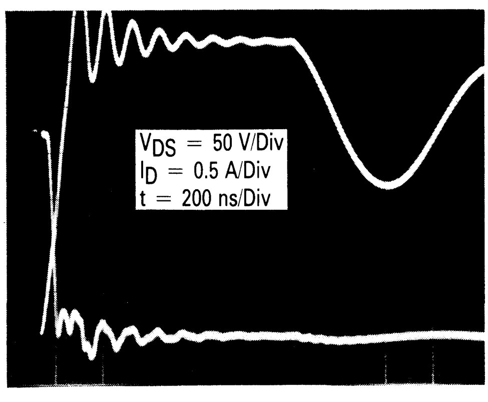
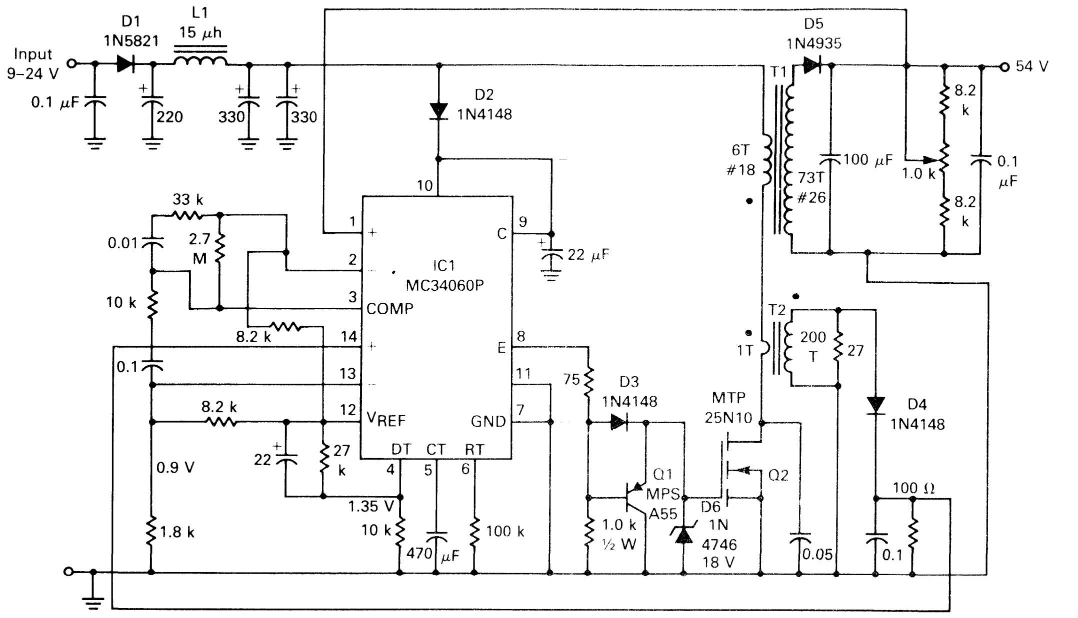


FIGURE 8-8 — FET CROSSOVER TIME



T1: CORE = FERROXCUBE 3019-L00-3C8
BOBBIN = FERROXCUBE 3019F-1D
GAP = 0.015″

T2: COILCRAFT D1871 CURRENT SENSE XFMR.

T3: CORE = COILCRAFT 11-464-41 EE-19
BOBBIN = COILCRAFT 37-612-001
GAP = 0.0075″

L1: COILCRAFT Z7156, 15 μH
L2: COILCRAFT Z7157, 25 μH

FIGURE 8-9 — AUTOMOTIVE DC-DC CONVERTER

High Voltage Flyback Converter

The advantages of power MOSFETs over bipolars — high input impedance (low drive power), fast switching, freedom from second breakdown — have been cited many times and can clearly be shown when the two technologies are used in the same application. Such is the case when a HV flyback converter, initially designed with a bipolar, was redesigned for the power MOSFET.

The first design used a Switchmode high-voltage bipolar MJ8505 output transistor in a PWM flyback converter, Figure 8-10c. This transistor has breakdown voltage ratings $V_{CEO(sus)}$ and V_{CEV} of 800 V and 1400 V, respectively, and a continuous collector current of 10 A. But, most important, it has a reverse bias safe operating area (RBSOA) curve, shown in Figure 8-11a, which allows a peak flyback voltage of about 700 V, generated by a peak collector current in the 3.0 to 4.0 A range.

To achieve this RBSOA capability an off-bias voltage, $V_{BE(off)}$, of about −5.0 V is required. Also, since there is a trade-off of β with high-voltage transistors (β_{min} = 7.5 at I_C = 1.5 A), a low forced beta β_F of about 2.5 (I_{BI} ≈ 1.5 A) was chosen to ensure device saturation. To produce clean, monotonic, relatively fast clamped inductive turn-off waveforms, the Baker Clamp network of diodes (D2–D4) is suggested. Consequently, a power amplifier consisting of an I_{BI} forward base current circuit (transistors Q1 and Q2) and an off-bias circuit (transistors Q3 and Q4) is required to interface the low level PWM with the MJ8505. The PWM (U1), for this example, need only provide a +5.0 V pulse to the power Amp with about 20 mA sourcing and sinking capability.

If, however, the output device is a comparably rated power MOSFET, MTM2N90 the drive circuitry can be greatly simplified, with the resulting savings in cost and improved reliability. Moreover, the faster switching

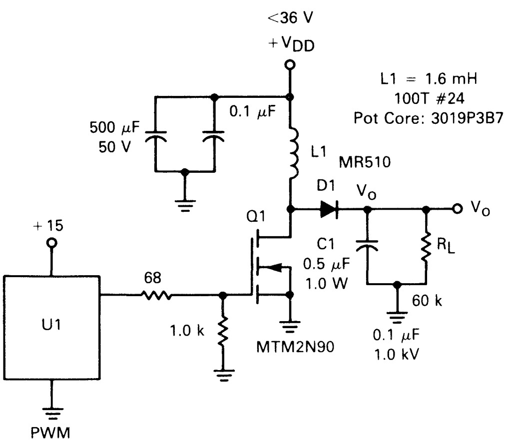


FIGURE 8-10a — SINGLE MOSFET OUTPUT

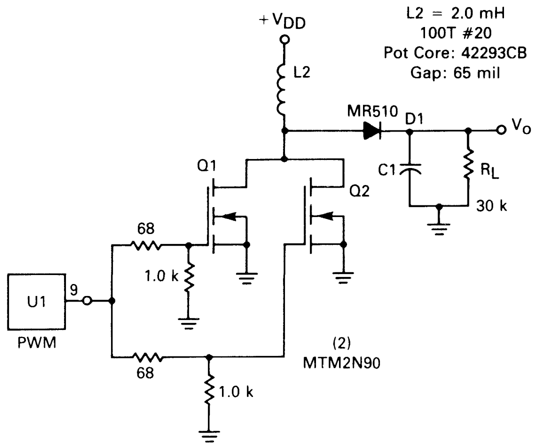


FIGURE 8-10b — TWO PARALLEL MOSFET OUTPUT

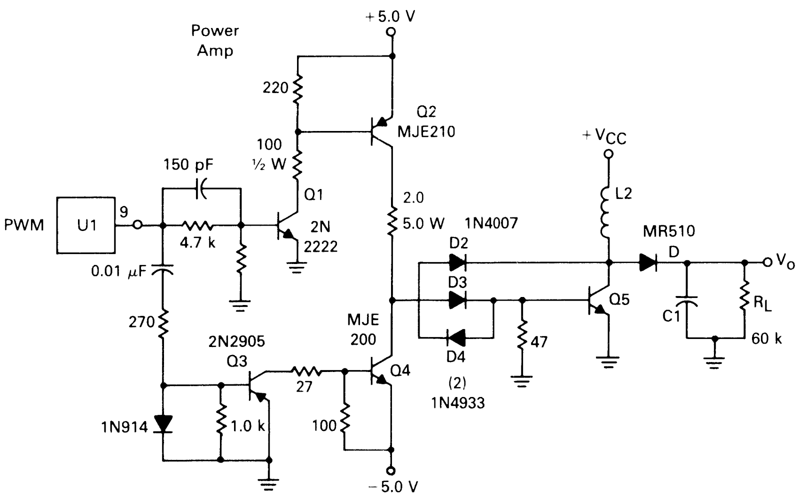


FIGURE 8-10c — DRIVER WITH BIPOLAR OUTPUT

FIGURE 8-10 — HIGH VOLTAGE FLYBACK CONVERTER WITH POWER MOSFET & BIPOLAR OUTPUTS

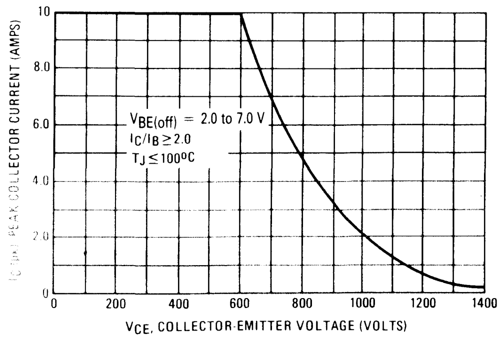


FIGURE 8-11a — RBSOA, REVERSE BIAS SWITCHING SAFE OPERATING AREA

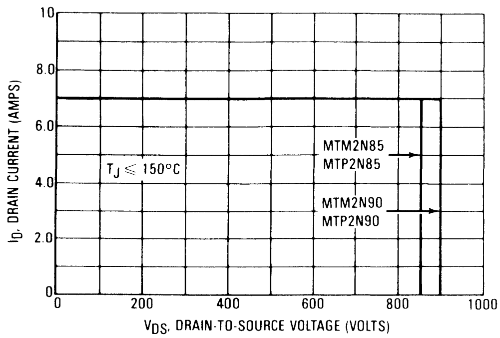


FIGURE 8-11b — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

MOSFET improves system efficiency and as subsequently described, greater RBSOA or turn-off switching SOA is achieved (see Figure 8-11 for comparison of the MTM2N90 with the MJ8505).

The PWM can be any of the 15 V powered I.C.'s with source and sink capability in the 100 mA range. This current level is amendable to driving power MOSFETs at a relatively fast switching speed, the current sourcing, charging up the FET input capacitance C_{iss} and the sinking, discharging the capacitance for fast turn-off switching. Also, the near 15 V PWM output ensures that the FET is well turned on.

This is exactly what was done for the second version of the high voltage Switchmode power supply; the PWM directly drives the FET gate. Using a single N-channel, high-voltage TMOS MTM2N90 transistor $V_{(BR)DSS}$ = 900 V, I_D = 2.0 A), a high-voltage output of 750 V peak, capable of driving a 60 k load was achieved. With the illustrated load inductor L1 and switching frequency, the peak drain current was about 2.5 A (limited by the magnetic saturation of the inductor) and the flyback voltage was about 750 V.

Atlhough this current exceeds the continuous 2.0 A drain current rating of the device, it is well within the 7.0 A pulsed current rating. But, of even greater interest, since the FET has no second breakdown limitations — as do bipolars — it can sustain simultaneous high switching voltages and currents. Thus, the 750 V, 2.5 A load line is well within the SOA rating.

To produce even higher output power levels, two parallel connected power MOSFETs can be driven, as illustrated in Figure 8-10b. Using a larger inductor L2, the circuit was capable of easily producing an 800 V output into a 30 k load. The total peak drain current was 3.5 A with each driver sharing current inversely proportional to its $r_{DS(on)}$: i.e., matched on-resistance of 5.0 Ω produced about equal values of I_D of 1.75 A, unmatched 5.0 and 8.0 Ω, about 2.1 A and 1.4 A respectively. Reducing the load resistance even further, resulted in greater power output, with the individual device drain current being well within spec limits, as shown in Table 3:

TABLE 3

R_L	V_{DD}	V_O	Total $I_{D(pk)}$	P_o
30 k	28 V	800 V	3.6 A	21.3 W
25 k	31 V	800 V	3.8 A	25.6 W
21 k	34 V	800 V	4.2 A	30.5 W

And finally, to make a direct comparison between the two devices, the loads and the stored energy inductor should be the same. Since the bipolar originally was tested with the larger inductor and a 30 k load to produce as great as a 700 V output from a peak collector current of 3.2 A, the single TMOS was also tested to these conditions. Not only did the power MOSFET reach this energy level, it also reached 800 V at 3.6 A. To achieve the required inductor stored energy and power output for this application, the switching frequency was about 1.7 kHz. Even at this low frequency, the relatively high static losses [$V_{DS(on)} = r_{DS(on)} I_D$ = 8.0 Ω (max) (3.2 A) ≈ 25 V] contributed little to the total device loss.

Admittedly, power MOSFETs are still more expensive than a comparably die sized bipolar, but, as progression along the learning curve is achieved, the FET will become more cost competitive. Nevertheless, it has been shown that the single power FET circuit is much simpler and cost effective to drive in this example than the bipolar and offers the second breakdown free rectangular SOA curve that allows full $V_{(BR)DSS}$, I_D switching capabilities.

SWITCHMODE Power Supply (SMPS) Configurations

The implementation of switching power supplies by the non-specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback Switching Power Supplies: 50 W to 250 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{max} = -0.4$
- Maximum MOSFET working current:

$$I_W = \frac{2.0\ P_{out}}{\eta \cdot \delta_{max} \cdot \sqrt{V_{in(min)}} \cdot \sqrt{2.0}} = \frac{5.5\ P_{out}}{V_{in}}$$

- Maximum FET working voltage: $V_{DSW} = 2.0 \cdot V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geq 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

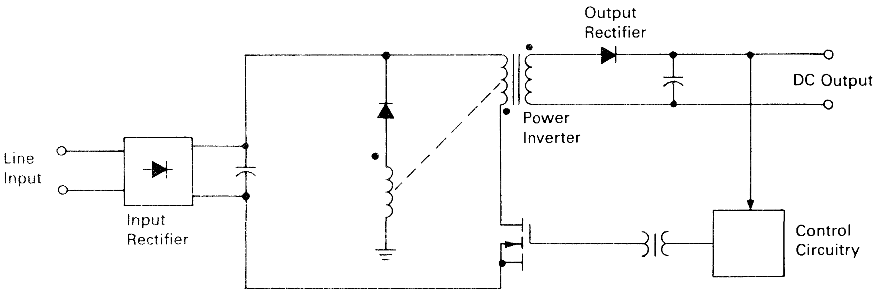


FIGURE 8-12 — BASIC FLYBACK CONFIGURATION

TABLE 4 — Flyback Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage, V_{in}	120 V	220 V or 240 V	120 V	220 V or 240 V	120 V	220 V or 240 V	120 V
MOSFET Requirements							
Max Working Current, I_W	2.25 A	1.2 A	4.0 A	2.5 A	8.0 A	4.4 A	11.4 A
Max Working Voltage, V_{DSW}	380 V	750 V	380 V	750 V	380 V	750 V	380 V
Power MOSFETs Recommended							
Metal (TO-204AA) (TO-3)	MTM4N45	MTM2N90	MTM4N45	MTM2N90	MTM7N45	MTM4N90	MTM15N45
Plastic (TO-220AB)	MTP4N45	MTP2N90	MTP4N45	MTP2N90	—	—	—
Plastic (TO-218AC)	—	—	—	—	MTH7N45	—	—
Input Rectifiers							
Max Working Current, I_{DC}	0.4 A	0.25 A	0.4 A	0.5 A	2.35 A	1.25 A	4.6 A
Recommended Types	MDA104A	MDA106A	MDA206	MDA210	MDA970	MDA210	MDA3506
Output Rectifiers							
Recommended types for							
Output Voltage of: 5.0 V	MBR3035PT		MBR3035PT		MBR12035CT		MBR20035CT
10 V	MUR3010PT		MUR3010PT		MUR10010CT		MUR10010CT
20 V	MUR1615CT		MUR1615CT		MUR3015PT		MUR10015CT
50 V	MUR1615CT		MUR1615CT		MUR1615CT		MUR3015PT
100 V	MUR440, MUR840A		MUR840A		MUR840A		MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494; Inverter Control Circuit MC3423, MC3424; Overvoltage Detector Error Amplifier: SINGLE TL431; DUAL-MC3438, LM358; QUAD — MC3403, LM324, LM2902						

Push-Pull Switching Power Supplies: 100 W to 500 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: δ_{max} = 0.8
- Maximum MOSFET working current:
  $I_W = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{1.4\,P_{out}}{V_{in}}$
- Maximum FET working voltage:
  $V_{DSW} = 2.0 \cdot V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage:
  $V_{DS} \geqslant 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

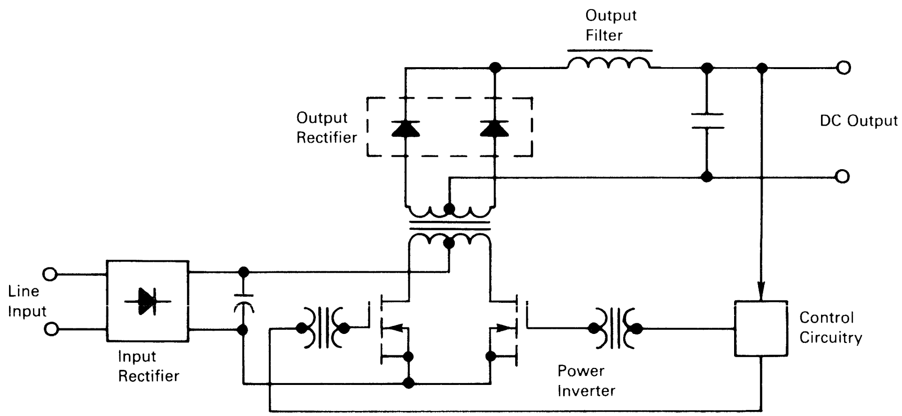


FIGURE 8-13 — BASIC PUSH-PULL CONFIGURATION

TABLE 5 — Push-Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_W Max Working Voltage, V_{DSW}	 1.2 A 380 V	 0.6 A 750 V	 2.9 A 380 V	 1.6 A 750 V	 5.7 A 380 V	 3.1 A 750 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM2N50 MTP2N45 —	 MTM2N90 MTP2N90 —	 MTM4N45 MTP4N45 —	 MTM2N90 MTP2N94 —	 MTM7N45 — MTH7N45	 MTM4N90 — —
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.35 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	See Table 4					

Half-Bridge Switching Power Supplies: 100 W to 500 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{max} = 0.8$
- Maximum MOSFET working current:
  $$I_W = \frac{2.0\ P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{2.8\ P_{out}}{V_{in}}$$
- Maximum FET working voltage: $V_{DSW} = V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geqslant 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

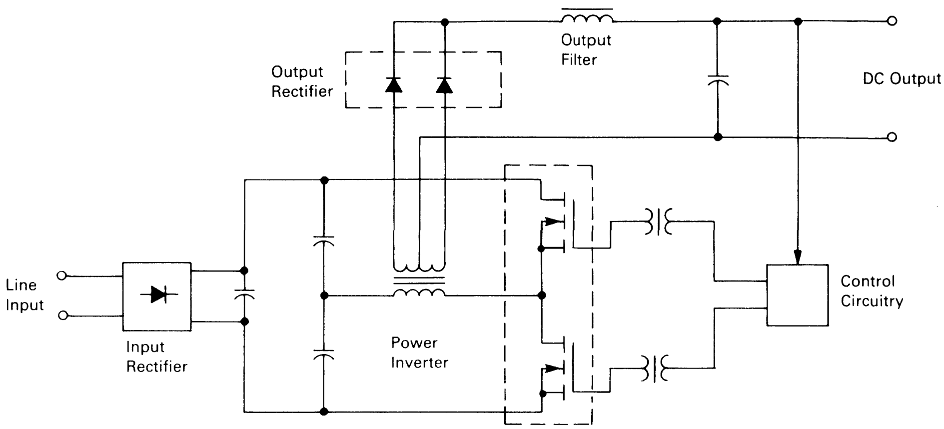


FIGURE 8-14 — BASIC HALF-BRIDGE CONFIGURATION

TABLE 6 — Half-Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_W Max Working Voltage, V_{DSW}	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM5N35 MTP3N40 —	 MTM2N45 MTP2N45 —	 MTM8N40 — MTH8N40	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970-5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	See Table 4					

Full-Bridge Switching Power Supplies: 500 W to 1000 W

- Input line variation: V_{in} + 10%, − 20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{max} = 0.8$
- Maximum MOSFET working current: $I_W = \frac{P_{out}}{\eta \cdot \delta_{max} \cdot V_{in(min)} \cdot \sqrt{2.0}} = \frac{1.4\ P_{out}}{V_{in}}$
- Maximum MOSFET working voltage: $V_{DSW} = V_{in(max)} \cdot \sqrt{2.0}$
- Minimum FET drain-source voltage: $V_{DS} \geqslant 1.2 \cdot V_{DSW}$
- Working frequency: f = 20 to 200 kHz

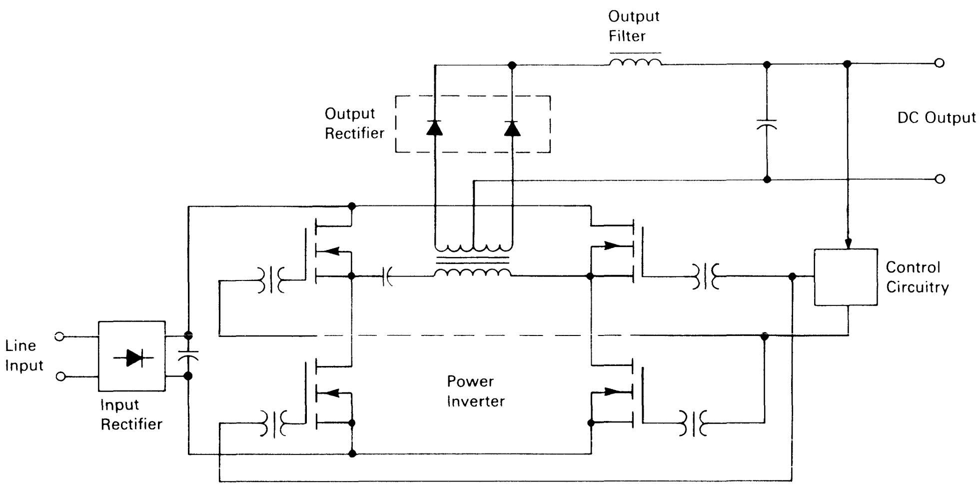


FIGURE 8-15 — BASIC FULL-BRIDGE CONFIGURATION

TABLE 7 — Full Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage, V_{in}	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements Max Working Current, I_W Max Working Voltage, V_{DSW}	 5.7 A 190 V	 3.1 A 380 V	 8.6 A 190 V	 4.7 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended Metal (TO-204AA) (TO-3) Plastic (TO-220AB) Plastic (TO-218AC)	 MTM8N20 MTP8N20 —	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 MTP4N45 MTH7N45	 MTM15N20 MTP12N20 MTH15N20	 MTM7N45 — MTH7N45
Input Rectifiers Max Working Current, I_{DC} Recommended Types	 4.6 A MDA3506	 2.5 A MDA3510	 7.0 A	 3.8 A	 9.25 A	 5.0 A
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		 MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT*		 MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	See Table 4					

*More than one device per leg, matched.

Motor Controls

Power MOSFETs are interesting devices for motor drive applications. The advantages and disadvantages are similar to those discussed for switching power supplies. With motor drives, however, there is more of a distinction. Whereas FETs are not yet a match for bipolar Darlingtons in off-line multiple horsepower drives, they are an excellent choice for fractional horsepower drives and drives that are operated off busses less than 100 V.

Three examples are illustrated. They include a stepping motor drive, a high efficiency H bridge, and a one-transistor PM motor speed control.

Using Power MOSFETs in Stepping Motor Control

Stepping motors are used extensively in electromechanical positioning systems. Applications range from printers to tape drivers, floppy disk drives, numerically controlled machinery and other digitally controlled positioning systems. The task of the stepping motor controller is to drive the rotation generating sequential current flows in the field winding of the motor on command from an external device.

The use of TMOS Power MOSFETs and CMOS logic simplifies the drive circuitry while allowing considerable flexibility of control. This section describes several types of stepping motor control circuits including an 88.0% efficient switching drive. Stepping motor logic sequencing, power requirements and dynamics are briefly examined.

DRIVE TECHNIQUES

Stepping Motor Characteristics

A basic understanding of stepping motors is desirable. A permanent magnet stepping motor consists of a series of permanent magnets distributed radially on a rotor shaft surrounded by electromagnets attached to the stationary housing. Energizing the electromagnets with the proper polarities generates a magnetic field pattern to which the motor magnets try to align producing torque. A simplified representation of a stepping motor is shown in Figure 8-16. Initially, Poles A and B are both energized with north up, drawing the rotor's south pole to the up position. Reversing the polarity of Pole A draws the rotor 90° clockwise to its final position; this is known as a full step. If pole A had been turned off instead of reversed, the rotor would have rotated only 45° clockwise to line up with the field created by Pole B; this is known as a half step. Stepping motors obtain small angle step increments by using large numbers of poles. Stator pole reversal can be accomplished by reversing the current flow direction in the winding or by using alternate halves of a center-tapped winding.

An external block diagram of a center-tapped stepping motor plus control switches, inductive clamp diodes, resistive current limiting and power supply is shown in Figure 8-17. Pole A, for instance, can be energized to one polarity by turning Switch 1 on and Switch 2 off; the opposite polarity is generated by turning Switch 1 off and Switch 2 on.

It follows that the proper magnetic polarity sequence for stepping can be generated by controlling Switches 1–4. Clamp diodes prevent the voltage across the inductive winding from flying up and destroying the switches as they are turned off. The required switching sequences for full and half step operation are shown in Figure 8-18. Reversing the sequences of Figure 8-18 will reverse the direction of motor rotation.

Rapid stepping requires high di/dt in the motor windings. Since di/dt is a function of supply voltage, a high supply voltage is desirable. The average winding current is limited by the motor manufacturer's specification. As an example, Superior Electric's SLO-SYN model M093-FC07 has a current rating of 3.5 amps/winding with 1.23 Ω/winding resistance and 7.94 mH/winding inductance. The recommended power supply is 24 volts; currents are limited to the maximum rating by a 6.5 Ω, 100 W resistor/winding. This yields a dc current of about 3.0 A and an L/R time constant of 1.0 ms. Higher supply voltages and

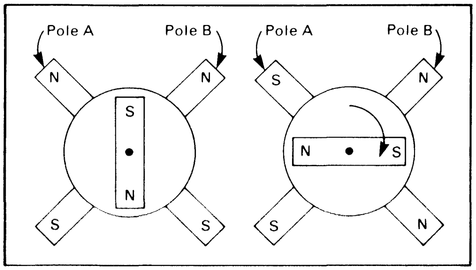
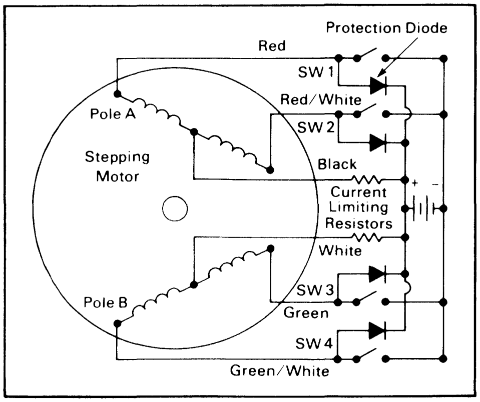


FIGURE 8-16 — SIMPLIFIED STEPPING MOTOR



*Colors are for Superior Electric SLO-SYN dc Stepping Motors

FIGURE 8-17 — SIMPLIFIED STEPPING MOTOR AND CONTROL BLOCK DIAGRAM* the resulting larger current limiting resistor will decrease L/R and increase the obtainable stepping rate.

Depending on rotor inertia, torque requirements and winding currents, a stepping motor may exhibit oscillatory behavior including vibration, lost steps and/or stalling near self-resonant stepping frequencies. Oscillatory behavior may be lessened or eliminated by adjusting winding currents, by adjusting interial and/or torque loading or by the use of mechanical dampers.

A Full Step Center-Tapped Drive

Figure 8-19 illustrates a full step center-tapped stepping motor controller using one CMOS 4-bit presettable shift register to drive four N-Channel TMOS Power FETs. Examining the full-step sequence of Figure 8-18, shows that the sequences for the various gate signals are the same except for a phase shift. Therefore, the desired control sequence of two on-time periods followed by two off-time periods may be preset into the 4-bit shift register (MC14194) of Figure 8-19. The required phasings are obtained by tapping the appropriate shift register outputs.

Clockwise stepping is obtained by right shifting the MC14194; left shifting yields counterclockwise stepping. Control signals S0 and S1 plus a clock line control stepping. On power-up, the MC14194 requires a preset obtained by setting S0, S1 = 1,1 and supplying a leading edge clock; this puts the logic in a known state. The remainder of the control functions are illustrated in the control table of Figure 8-19; stepping occurs in a leading edge clock. Diodes 1–4 prevent the inductive turn-off spike from avalanching the TMOS Power FETs. Resistor R3 creates a back voltage which halts winding current rapidly on turn-off. R3 is selected to limit the voltage spike to the TMOS S-D voltage rating. TMOS power FETs switch extremely fast, and the turn-on delay of the diodes may not be short enough to prevent S-D avalanche. A small capacitor (0.01 to 0.1 μF) placed across the motor winding will usually lower dv/dt sufficiently to prevent S-D avalanche. Resistors R1 and R2 limit motor winding currents.

A Full or Half Step Center-Tapped Drive

Figure 8-20 illustrates a full or half step controller. As in the full step sequence, the gate control signals for the half step sequence are identical except for a phase shift. Similarly, the desired pattern of three on-time periods followed by five off-time periods can be preset on a leading edge clock into an eight-bit shift register formed by two MC14194's. The full step sequence can be generated by setting the half step line high and performing a preset. Right shifting and left shifting control the motor shaft's direction of rotation as before. A full step will be executed for every two rising clock pulses independent of stepping sequence. Diodes D1–D4 and resistor R3 form the over-voltage protection for the TMOS Power FETs. R1 and R2 limit motor winding currents.

Push-Pull Drive

Figure 8-21 illustrates a complementary push-pull drive for a non-center tapped stepping motor driven from a 24 volt motor supply and a 15 volt logic supply. One of two winding drive sections plus the complete control logic is shown in Figure 8-21. The total drive consists of four N-Channel and four P-Channel TMOS Power FETs arranged in two push-pull drives per winding (the M093-FC07 center tap leads were floated, inductance/full winding = 31.76 μH, resistance/full winding = 2.46 Ω and rated current = 2.0 amps/winding).

Phasing signals are obtained with the shift register technique described earlier. The circuit of Figure 8-21 will provide a full or half step sequence as clocked into the two CMOS shift registers during a preset (a full step only controller can be implemented with one 4-bit CMOS shift register). Gate signals for the N-Channel FETs are taken directly from the CMOS registers. Gate signals for the P-Channel FETs are translated and referenced to the motor power rail through Q9–Q10.

Sufficient capacitance across the sources of the bridge FETs must be used to limit P-Channel gate-source voltage transients to below the pass frequency of the collector resistor and the P-Channel gate capacitance. During switching transients, it is possible that both FETs in a given complementary pair could briefly be on at once. This condition could short power to ground through the complementary pair. To avoid exceeding peak drain current rating, the gate-drive on the P-Channel FET is restricted to 10 V.

TMOS Power FETs are constructed with internal source-to-drain diodes. The circuit of Figure 8-21 uses these diodes to shunt turn-off transient currents from the ground plane to the power rail; thus, a given FET is protected from winding turn-off energy by the source-drain diode of its complement. The source-drain diode, how-

Full-Step Sequence

STEP	SW1	SW2	SW3	SW4
1	OFF	ON	OFF	ON
2	OFF	ON	ON	OFF
3	ON	OFF	ON	OFF
4	ON	OFF	OFF	ON
1	OFF	ON	OFF	ON

Half-Step Sequence

STEP	SW1	SW2	SW3	SW4
1	OFF	ON	OFF	ON
2	OFF	ON	OFF	OFF
3	OFF	ON	ON	OFF
4	OFF	OFF	ON	OFF
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	OFF
7	ON	OFF	OFF	ON
8	OFF	OFF	OFF	ON
1	OFF	ON	OFF	ON

FIGURE 8-18 — STEPPING SEQUENCES**

**Clockwise Rotation as Viewed from the Nameplate End of the Motor ever, requires about 300 ns of turn-on time. A 0.1 μF capacitor is placed across each winding so that the windings dv/dt is low enough to allow for diode turn-on without avalanching the FETs. Winding currents are limited by the 9.0 ohm 5.0 watt resistors.

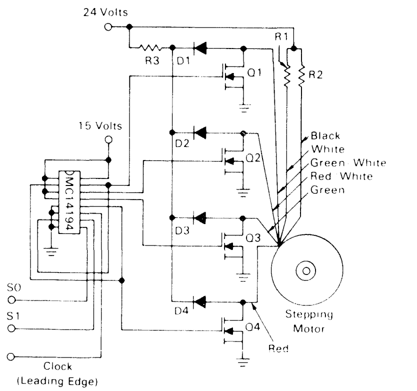
Switched Current Limiting

The circuit of Figure 8-21 uses resistive current limiting. With 2.0 amps flowing in each winding, 4.0 amps will be drawn off of the 24 volt supply yielding 96 watts of draw with only 25% of that power being delivered to the motor. Some form of switched current limiting is clearly desirable. Figure 8-22 illustrates a simple switching scheme.

Starting with zero current flow, let the desired current flow be left to right through the motor winding. Let the referenced voltage V_{ref} be 0.2 volts. Assuming $R_H >> R_{ref}$, the positive comparator inputs will be approximately 0.2 volts. With no current flow, the sense resistors will have no voltage across them and the comparators will have high outputs; this enables the C1 and C2 inputs to drive the P-Channel Power FETs. The proper C1, C2 input for left to right current flow is 1,0. This turns the upper left P-Channel and the lower right N-Channel on placing the full power supply across the motor winding. Current I1 increases with di/dt = V/L. When I1 increases to 2.0 amps, the voltage across the lower right 0.1 sensing resistor will be 0.2 volts, and the lower right comparator will go low after a short filter delay shutting off the upper left P-Channel FET. The current through the motor winding begins to decay around the I2 current path.

When the comparator went low, it shifted its positive input reference down by about 70 mV. I2 decays until the voltage across the 0.1 sense resistor falls below the hysteresis determined level; at that point, the comparator will go high turning on the upper left P-Channel FET and recharging the winding current along the I1 current path. The winding current within the C1, C2 control envelope increases to the reference level and oscillates around that level at a value set by RH, R_{ref} and the logic supply voltage. The frequency of oscillation is set by V/L, the hysteresis value and the current path resistances.

The circuit of Figure 8-22 places a negative voltage on



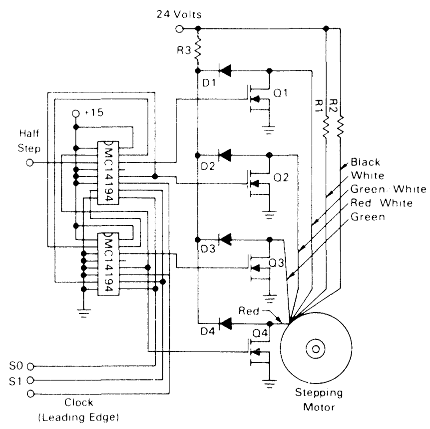
Control Signals

S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Logic Levels are Standard
15 V, CMOS
MC14194 is a Standard 16 Pin DIP.

Parts:
1. Example Motor is M093-FC07 Manufactured By Superior Electric
2. Diodes, D1-D4, 1N4002
3. R3, 10 Ω 10 W
4. R1, R2, 6.5 Ω 100 W
5. Integrated Circuit, MC14194 (CMOS)
6. Q1-Q4, MTM12N08 or MTP12N08

FIGURE 8-19 — CENTER-TAPPED STEPPING MOTOR DRIVE



Control Signals

S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

PARTS:
1. Example Motor is Superior Electric's Model M093-FC07
2. Diodes, D1-D4, 1N4002 or Equivalent
3. R3, 10 Ω 10 W
4. R1, R2, 6.5 Ω 100 W
5. Integrated Circuits, MC14194 (2 Required)
6. Q1-Q4, MTM12N08 or MTP12N08

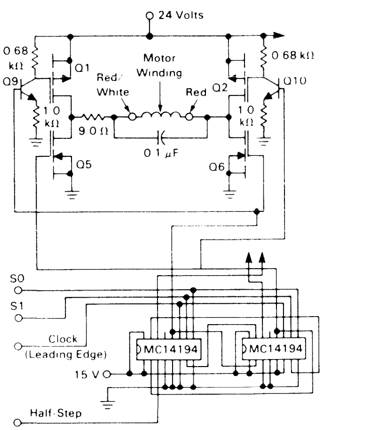
FIGURE 8-20 — HALF- OR FULL-STEP DRIVE FOR CENTER-TAPPED STEPPING MOTORS

the negative input terminal of the comparators during the I2 current path. This is not detrimental to the comparator provided that the terminal current doesn't exceed a few milliamps.

The complete logic circuit plus one of two required winding drive sections for a push-pull stepping motor with switched current limiting is shown in Figure 8-23. Figure 8-24 is the corresponding parts list for the complete circuit. The circuit of Figure 8-23 is limited to 8.0 amps continuous with a motor power supply voltage of about 70 volts by the specified P-Channel TMOS Power FETs. Thus, the controller can handle up to 560 watts delivered to each winding. Changes in RH, R_{ref} and the sensing resistor may be desirable for motors other than the example motor. For low inductance motors driven from high voltage supplies with low levels of hysteresis, faster components in the switched feedback loop may be required.

Utilizing Synchronous Rectification

The circuit of Figure 8-23 required 26.4 watts to maintain 2.0 amps/winding with 78.8% of the drawn power



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Parts:

1. 2 × MC14194 (CMOS)
2. Q1–Q4, 4 × MTP8P08 or MTM8P08 (TMOS Power FETs)
3. Q5–Q8, 4 × MTP12N08 or MTM12N08 (TMOS Power FETs)
4. Q9–Q12, 4 × MPS8099 (NPN Small Signal)
5. 2 × 9 Ohm 50 Watt Resistors
6. 4 × 0.68 kΩ 1/4 W Resistors
7. 4 × 1.0 kΩ 1/4 W Resistors

Example Motor: Superior Electric SLO-SYN Model M093-F007

FIGURE 8-21 — HALF- OR FULL-STEP RESISTIVE CURRENT LIMITED DRIVE FOR STEPPING MOTORS WITHOUT CENTER-TAP

delivered to the M093-FC07. Calculations indicated that greater than 50.0% of the control circuit power consumption was due to the S-D diode drop during the I2 current loop (Figure 8-22). This drop could be lowered by operating the lower N-Channel Power FETs as synchronous rectifiers. The additional logic required for synchronous rectification amounts to three CMOS integrated circuits. A complete logic circuit plus one of the two required winding drive sections is shown in Figure 8-25. Essentially, the lower N-Channel is turned on when the upper complementary P-Channel is turned off by the comparator or when the N-Channel control signal is high. The circuit of Figure 8-25 yielded 88.4% efficiency at 2.0 amps/winding.

Further Possibilities

Shaping of the applied current waveform is often desirable. If a large stepping torque followed by a low holding torque is desired, the required current waveform can be applied to the positive comparator input. Within the comparator hysteresis and the circuit's current response speed, the current in the motor will follow the comparator reference. The di/dt circuit response is limited by approximately $V_{motor\ supply}/L_{motor}$, provided that the series resistance drops only a few percent of the supply voltage. If current is allowed to decay without applying a reverse supply voltage, current decay time will be set by the L_{motor}/R_{decay} loop time constant.

In summary, the switching circuit of Figure 8-23 yields 79.0% efficiency at 2.0 amps/winding with faster current response than the 25.0% efficient resistive current limited circuit of Figure 8-20. Adding three CMOS integrated circuits to the circuit of Figure 8-23 yields the 88.0% efficient circuit of Figure 8-25. The use of TMOS Power FETs and CMOS logic in the designs of Figures 8-23 and 8-25 allowed high efficiency and considerable control flexibility to be achieved without excessive parts count or undue complexity.

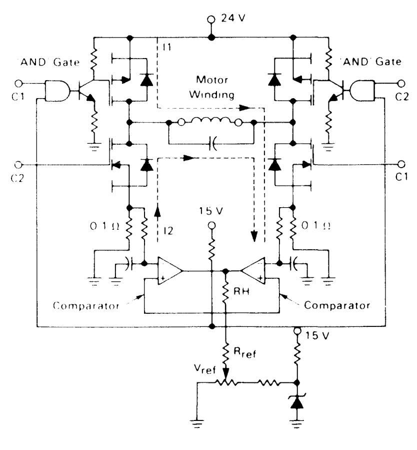
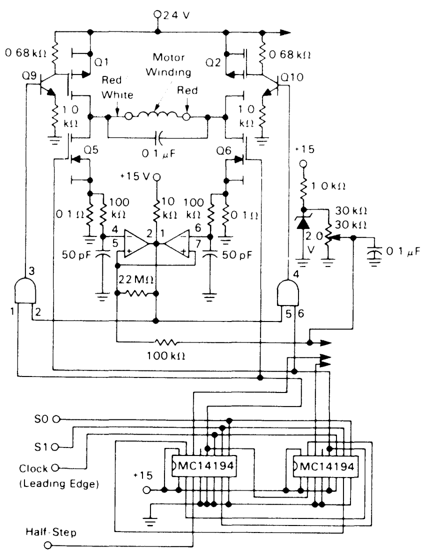


FIGURE 8-22 — COMPARATOR SWITCHED CURRENT LIMITING



S0, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

FIGURE 8-23 — HALF- OR FULL-STEP SWITCHED CURRENT DRIVE FOR STEPPING MOTORS WITHOUT CENTER-TAP

Integrated Circuits
1. 2 × MC14194B, CMOS 4-Bit Shift Register
2. 1 × MC14081B, CMOS Quad "AND" Gate
3. 1 × LM339N, Quad Comparator

TMOS Power FETs
1. Q1–Q4, 4 × MTP8P08 or MTM8P08, P-Channel Power FET
2. Q5–Q8, 4 × MTP12N08 or MTM12N08, N-Channel Power FET

Transistors
1. Q9–Q12, 4 × MPS8099, NPN Small Signal Transistors

Resistors
1. 4 × 0.1 Ω 2.0 W
2. 4 × 680 Ω 1/4 W
3. 5 × 1.0 kΩ 1/4 W
4. 2 × 10 kΩ 1/4 W
5. 1 × 30 kΩ 1/4 W
6. 1 × 30 kΩ Adjustable, 1/4 W
7. 6 × 100 kΩ 1/4 W
8. 2 × 22 MΩ 1/8 W

Zener Diode
1. 1 × IN, 2 V Reference

Capacitors
1. 3 × 0.1 μF 100 V
2. 4 × 50 pF 50 V

FIGURE 8-24 — PARTS LIST FOR CIRCUIT OF FIGURE 8-23

H Bridge Performance Comparisons

Power MOSFETs are excellent candidates for low voltage H Bridges. In this example, MOSFETs are compared with two other popular alternatives, bipolar discretes and bipolar Darlingtons. Circuits were designed for all three types of output power devices. Each circuit design is optimized for the output device used.

General "H" Switch Design Considerations:

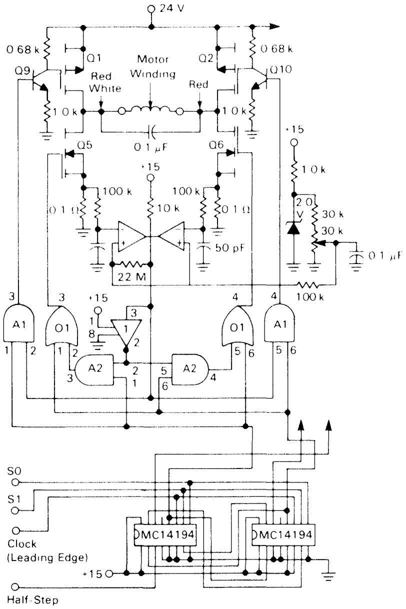
- P.M. DC Motor, 2.0 A run, 15 A stall/start.
- 12 V protected bus, 32 V max peak, 14 V nominal.
- "H" switch input, 2.0 mA max sink requirement.
- Discrete driver stages (for comparison of designs).
- Maximum ambient temperature of 100°C, maximum junction temperature = 150°C.
- Off the shelf type output power devices using maximum data sheet limits to calculate drive requirements and forward "on" voltage levels. The power output devices were chosen such that die sizes for the three types are approximately equal.

Discrete Bipolar "H" Switch

TIP35 and TIP36 power transistors were selected for their low cost and high current capacity. The high current-gain specification for these units results in base drive requirement of 1.5 amperes to switch a 15-ampere load current. It may be that base drive can be reduced by 30 percent if the units are screened for high-current h_{fe}, but for this design comparison, only "off-the-shelf" standard devices with the regular data-sheet specifications are under consideration.

The bipolar "H" switch design requires medium size driver transistors and large-wattage voltage-dropping resistors in the base-drive circuit. A buffer stage is also required. The control lines are shown tied to a SPDT center off switch. In an actual circuit, this switch would be a logic array or a microcontroller output network. A protective counter-EMF voltage clamp is provided by the back-to-back Zener rectifiers. The Darlington and TMOS units have built-in clamp diodes and for many applications would not require the zeners. Capacitor and resistor snubbing networks may be required with all three types output devices.

As indicated in the performance table, the bipolar design is not very practical because of the large base drive requirement. Of the three power devices, it is the least efficient by a wide margin. In most situations, FETs or Darlingtons are a better choice.



SO, S1	Result
0, 0	Hold
0, 1	Shift Right
1, 0	Shift Left
1, 1	Preset

Parts in Addition to Figure 8, 1 × MC14049UB, 1 × MC14081B, 1 × MC14071B

FIGURE 8-25 — HALF- OR FULL-STEP SWITCHED CURRENT DRIVE WITH SYNCHRONOUS RECTIFICATION

$V_{CE(sat)} = 1.8\ V\ @\ 15\ A,\ I_B = 1.5\ A$
$V_{CE(sat)} = 0.4\ V\ @\ 2.0\ A,\ I_B = 1.5\ A$
Base Drive $P_D = 14\ V \times 1.5\ A = 21\ W$
MTR $P_D = 10.4\ V \times 15\ A = 156\ W$
MTR $P_D = 13.2\ V \times 2.0\ A = 26.4\ W$

$$EFF = \frac{156}{75 + 156},\ 75 = \text{SW } P_D + \text{Base Drive } P_D$$
$= 67.5\%$ at stall condition

$$EFF = \frac{26.4}{22.6 + 26.4}$$
$= 53.8\%$ at nominal run condition

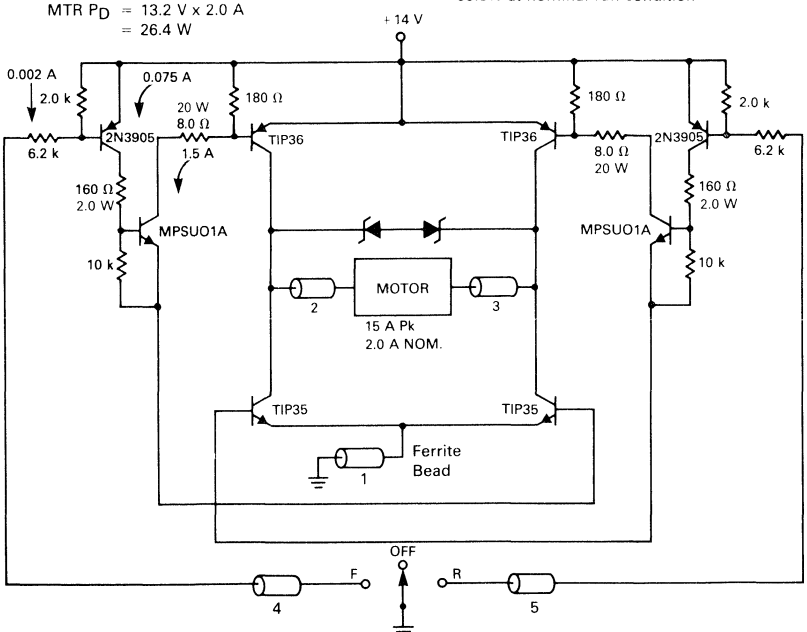


FIGURE 8-26 — "H" SWITCH BIPOLAR CONTROL CIRCUIT

Discrete Darlington "H" Switch

Motorola MJ4030 and MJ4033 power TO-204 (TO-3) Darlingtons were chosen for the Darlington version of the H bridge. As the chart shows, the drive-power requirements are substantially reduced from the bipolar power design. The tradeoff is that the forward "on" voltage is raised to such a high level that this particular motor will no longer be within its terminal voltage specification during stall or start-up. Also, the Darlington's dissipation will require a larger heat sink than the bipolar design. The Darlington does provide internal clamp diodes.

The Darlington "H" switch design works best in high-voltage, low-current load control circuits where the Darlington's high saturation power loss is not significant.

Power TMOS "H" Switch

An MTP25N05 Power FET was chosen for this design. Since the die size falls somewhat shy of the bipolar and Darlington device die sizes, an adjustment was made in the conduction loss calculation. Actual $V_{DS(on)}$ measurements were scaled according to the area ratio in order to arrive at the numbers presented here. As the comparison chart reveals, the TMOS design is clearly superior to the bipolar and Darlington designs. Its only technical drawback is the 34 volt bias supply requirement. This supply only has to source approximately 200 microamperes for this dc control, and can be derived from a single voltage pump-up circuit using TMOS gates and voltage doubling networks.

Test Measurement Calculations

The following equations were used to determine the circuit performance values for this example.

1. MOTOR POWER CONSUMPTION — The applied voltage across the motor load-terminals multiplied times the normal motor current.

   $P_{D(MTR)} = 1.0 \times (V_{BATT} - 2.0 \times V_{F(on)})$

   I = 2.0 AMPS RUN MODE I = 15 AMPS STALL MODE

   $V_{F(on)} = V_{CE(sat)}$ or V_{DS} per data sheet

2. OUTPUT DEVICE POWER DISSIPATION

   $P_{D(sw)} = (I \times V_{F(on)}) \times 2.0$

3. "H" SWITCH CONTROL EFFICIENCY

   $EFF = \dfrac{\text{Power Out}}{\text{Power In}}$

   Power Out = $P_{D(MTR)}$

   Power In = $P_{D(sw)} + P_{D(MTR)}$

$V_{CE(sat)} = 3.0$ V @ 15 A, $I_B = 0.08$ A
$V_{CE(sat)} = 1.1$ V @ 2.0 A, $I_B = 0.08$ A
Base Drive $P_D = 1.12$ W
MTR P_D = 8.0 V x 15 A = 120 W
MTR P_D = 11.8 V x 2.0 A = 23.6 W

$EFF = \dfrac{120}{91.1 + 120}$ = 57% stall mode

$EFF = \dfrac{23.6}{5.3 + 23.6}$ = 81% run mode

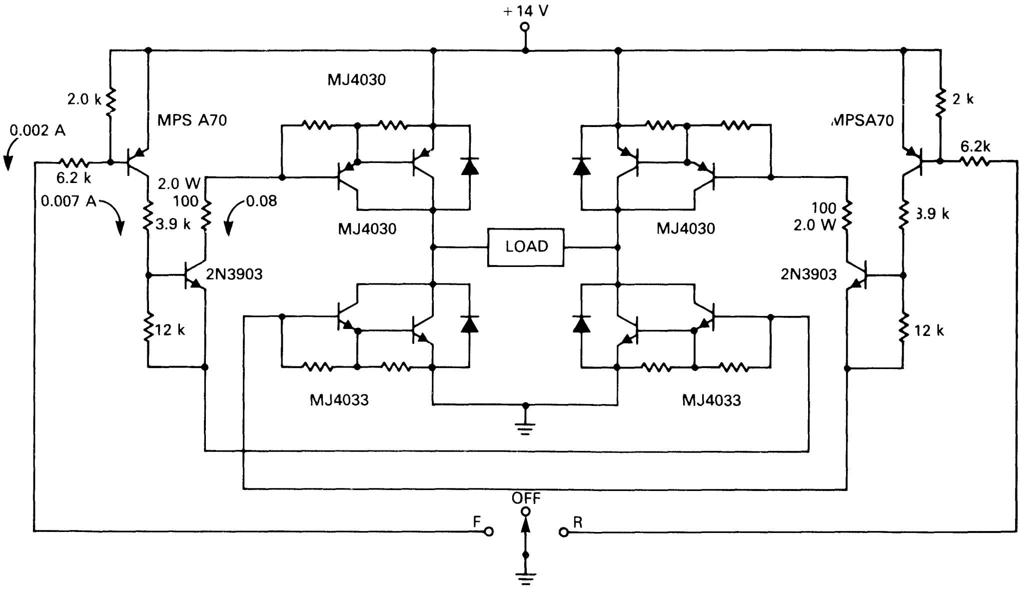


FIGURE 8-27 — "H" SWITCH DARLINGTON CIRCUIT

$V_{DS(on)} = 0.9\ V\ @\ 15\ A,\ V_{GS} = 20\ V$
$V_{DS(on)} = 0.12\ V\ @\ 2.0\ A,\ V_{GS} = 20\ V$
BIAS CIRCUIT $P_D = 0.01$ W MAX
MTR $P_D = 12.2,\ 2.0\ V \times 15\ A$
$= 183$ W
MTR $P_D = 13.76\ V \times 2.0\ A$
$= 27.5$ W

$$EFF = \frac{183}{27 + 183}$$
$= 87\%$ STALL MODE

$$EFF = \frac{27.5}{0.48 + 27.5}$$
$= 98\%$ RUN MODE

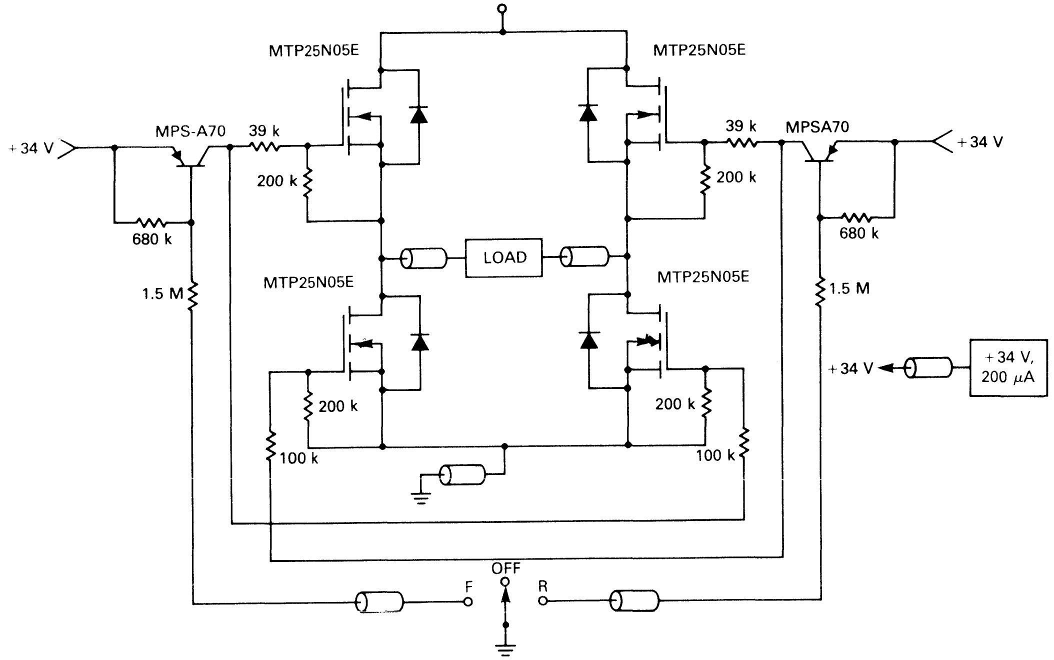


FIGURE 8-28 — "H" SWITCH POWER TMOS CIRCUITS

"H" SWITCH DESIGN COMPARISON CHART FOR AUTOMOTIVE MOTOR LOAD

	Die Size Area (Sq. Mils)	Max Forward Voltage (Off State)	Max Cont. Current	Forward Voltage Drop @ 2.0 Amp	Forward Voltage Drop @ 15 Amp	Driver Circuit Power Consumption	Switch Power Consumption @ 2.0 Amp	Switch Power Consumption @ 15 Amp	"H" Switch Total Efficiency @ 2.0 Amp	"H" Switch Total Efficiency @ 15 Amp	Motor Voltage @ 2.0 Amps with "H" Switch	Motor Voltage @ 15 Amps with "H" Switch	Comments
Bipolar	192	40 V	25 A	0.4 V	1.8 V	21 W	1.6 W	54 W	54%	68%	13.2 V	10.4 V	High base current required
Darlington	200	60 V	16 A	1.1 V	3.0 V	1.1 W	4.2 W	90 W	81%	57%	11.8 V	8.0 V	Large forward voltage drop
TMOS	176	40 V	20 A	0.12 V	0.9 V	0.01 W	0.48 W	27 W	98%	87%	13.8 V	12.2 V	34 V 200 μA Bias supply required

NOTES:
1) Bipolar devices are TIP35 and TIP36 TO-218 plastic NPN and PNP
2) Darlington devices are MJ4030 and MJ4033 TO-204 (TO-3) metal NPN and PNP.
3) TMOS devices are MTP25N05.
4) Figures shown above are the worst case data sheet condition for the parameter calculated.

Bidirectional Control of Fractional Horsepower Motors

By using power MOSFETs in Figure 8-29b's circuit, fractional-horsepower motors can be driven bidirectionally with only a small percentage of the base-drive power that bipolars require. Moreover, by sensing the motor's back EMF and delaying drive-voltage reversal, the circuit reduces the peak currents encountered during motor reversal. This feature allows the use of lower current MOSFETs than an instantaneous-reversal method would dictate.

A basic H switch, Figure 8-29a reverses the motor's supply voltage for bidirectional control. In Figure 8-29b's circuit, two pairs of N-channel MOSFETs serve as the CW (clockwise) and CCW (counterclockwise) switches. A flyback-type dc/dc inverter, composed of a CMOS hex inverter and a small signal MOSFET, drives the FET switches. The 3-inverter oscillator operates at 240 kHz; the three remaining inverter's average output tracks the power-supply input, ensuring adequate gate-bias voltage even for input-supply voltages as low as 6.0 V.

The Darlington transistors sense the motor's counter EMF (via the 20 V snubber zeners that become forward biased when the motor's back EMF appears) and shunt the drive-reversal signal to ground until the back EMF decays. The transistors will hold the gate-drive line low until the counter EMF drops below the base-to-emitter threshold voltage. This action causes the circuit to wait until the motor nearly stops rotating before applying reverse voltage. If faster response times are needed, the Darlingtons can be eliminated while connecting the 1.0 MΩ base resistors to ground — this change, however, would necessitate higher current MOSFETs because of the large peak-reversal currents that would ensue.

Figure 8-30 shows the dramatic difference in the peak currents that occur with and without the back-EMF-sensing feature. With the sensing circuit disabled (a), the currents exceed 50 A; the resulting MOSFET dissipation is approximately 140 W. Enabling the circuit (b) reduces the currents to approximately 30 A and the MOSFETs' dissipation to about 14 W. A 16 V zener diode limits the input voltage to the flyback inverter in case the supply

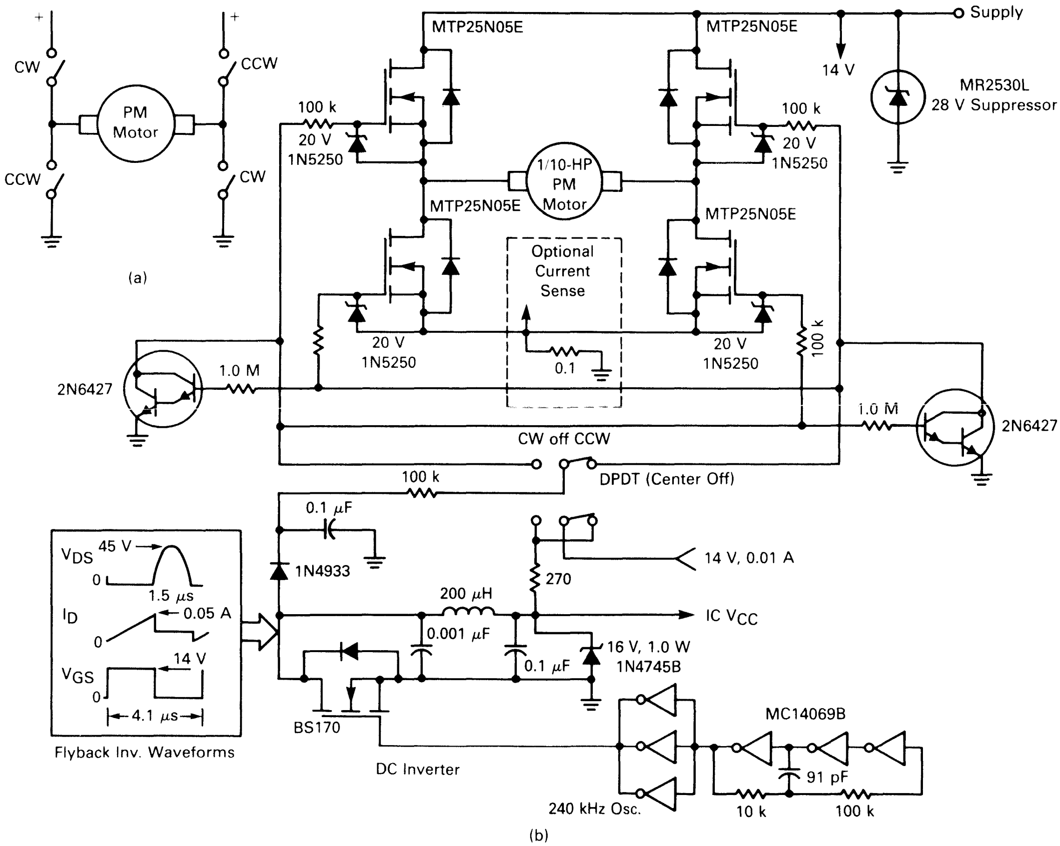


FIGURE 8-29 — DRIVE FRACTIONAL-HORSEPOWER MOTORS EFFICIENTLY WITH THIS POWER-MOSFET H-BRIDGE CIRCUIT. IT DISSIPATES MUCH LESS POWER THAN A BIPOLAR-TRANSISTOR DRIVER — MOREOVER, IT ALLOWS THE USE OF LOW-CURRENT MOSFETs BY DELAYING REVERSAL VOLTAGE UNTIL THE MOTOR COASTS TO A STOP.

rises higher than 16 V; the transient suppressor protects the MOSFETs from supply spikes greater than 28 V.

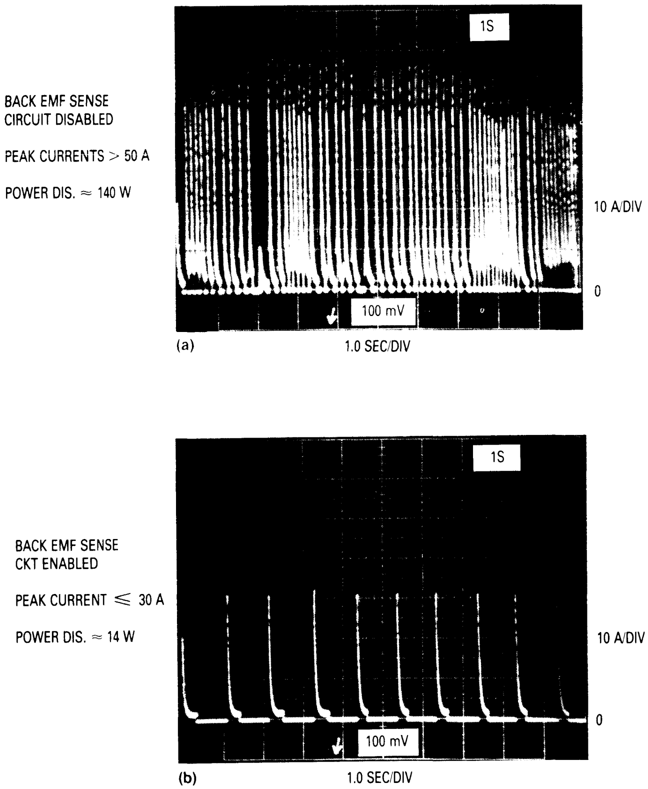
In this design, the MOSFETs require heat sinking to keep their junction temperatures less than 150°C in worst-case conditions (that could occur, for example, with a 16 V supply, 100°C ambient temperature and a stalled motor). As an option, a current-sensing circuit can be added to gate-off the power FETs after detecting a stall condition.

PWM Motor Speed Control

FETs can be used to considerable advantage for simplifying permanent-magnet motor speed control. The circuit shown in Figure 8-31 provides efficient pulse-width modulated control with a minimum number of components. The key feature is direct drive of the power FET from a CMOS control IC. The result is a control system with minimized parts count.

The control system is based upon the MC14528B dual monostable multivibrator. One-half of the monostable is connected in an astable mode, producing a pulse oscillator. The remaining half is then used as a one-shot, with its adjustable pulse-width determining the duty cycle and, therefore, motor speed.

In addition to its simplicity, the circuit of Figure 8-31 is notable for its low standby power drain. The combination CMOS control and TMOS power gives a very low quiescent current drain that is desirable in battery operated applications.



VERTICAL	HORIZONTAL
10 A/DIV	1.0 SEC/DIV

FIGURE 8-30 — COMPARISON OF "H" SWITCH PEAK CURRENTS DURING MAXIMUM FORWARD TO REVERSE SWITCHING WITH MANUAL TOGGLE SWITCH

Horizontal Deflection Circuits

Power MOSFETs can be a good alternative to bipolars in high resolution CRT sweep circuits. The most obvious advantage is simplicity. However, MOSFET horizontal outputs also offer significant benefits in terms of increased reliability and faster switching times.

Drive simplification with the MOSFET is even more significant than in the preceeding switching power supply examples. In most cases, a base-drive transformer is eliminated, as well as di/dt wave shaping networks.

The reliability issue is a little more complex, and relates to differences in SOA characteristics. It is normal design practice to exceed bipolar collector-emitter breakdown ratings during the retrace pulse transition. This is permissible if the base-emitter voltage is held negative during the retrace period. If, however, a positive noise pulse occurs during the retrace period, the bipolar base-emitter junction can become forward biased when collector-emitter voltage is greater than $V_{CEO(sus)}$. The bipolar's safe operating area is then violated, creating a substantial risk of failure. MOSFETs, on the other hand, will handle this type of stress quite readily, since their FBSOA capability extends beyond peak retrace voltage. Therefore, increased reliability with the MOSFET horizontal output is directly related to the probability of noise occurring in the drive circuitry.

Speed is also an important issue. At a 30 kHz scan rate, 1.0 μs of bipolar storage-time delay represents 3% of the horizontal line period, or a loss of 30 lines of data in a field of 1024 lines. In addition, bipolar storage time is not a fixed constant, but changes from device to device and with temperature. A horizontal phase locked loop can be added to compensate for the storage-time delays in the horizontal output stage. The active video data time may also be cut back, accordingly, to allow for internal horizontal timing delay.

Based upon these considerations, effective use of the bipolar transistor at high scan frequencies requires a complex base drive circuit, custom selection of the bipolar device for minimum storage-time variation, and an accurate phase locked loop to compensate for saturation time delays. Power MOSFETs, on the other hand, can be driven from a CMOS IC, do not require critical parameter screening, exhibit minimal turn-off delay, and do not require a phase locked loop for correcting device-induced timing errors.

Design Example

The power MOSFET, until recently, could not handle much current at voltages above 500 V. Recent technology developments have pushed this limit up to the 1000 V range with increased current ratings. Therefore, a power MOSFET can now be selected for computer CRT display systems with power supply requirements ranging from 12 V to 75 V.

The standard horizontal raster scan system is used in this design. That is, the horizontal yoke and flyback transformer are both switched by one output device. It should be pointed out that the power MOSFET has been switched up to 120 kHz scan rates, but due to other device constraints, the CRT anode high voltage network's performance is very marginal at this high frequency rate. Even a scan frequency of 30 kHz is pushing the limits of the high-voltage rectifier and associated components.

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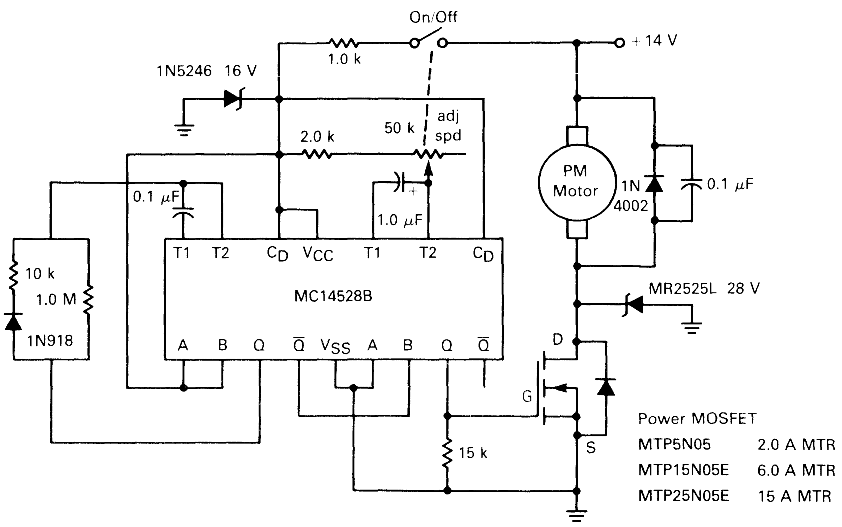

FIGURE 8-31 — POWER MOSFET MOTOR SPEED CONTROL CIRCUIT

The design concept is shown in the block diagram of Figure 8-32. The horizontal drive signal can be supplied by a free running synchronous clocked oscillator or by external computer logic. The safest method is to use a free running synchronous oscillator to insure the horizontal frequency is held within safe limits. There are several horizontal processor linear integrated circuits containing a phase detector, oscillator and predriver available. A partial list includes SGS TDA1180 and Motorola MC1391. None of these devices are presently designed to drive a MOSFET power unit directly, so some type of an interface or buffer circuit is required. Three power MOSFET drive circuits are shown in Figure 8-33. These circuits perform adequately in the horizontal system described here.

Circuit Description

The design presented in Figure 8-34 eliminates the driver transformer, driver transistor, and associated passive components that would normally be found in a bipolar design. A MLM311 comparator is used to invert and level-shift the incoming positive going synchronous pulse. The comparator output is ac coupled to the MC1391 horizontal processor which consists of a phase comparator and voltage controlled oscillator with adjustable duty cycle. The phase comparator of the MC1391 is connected to the incoming conditioned horizontal synchronous pulse and the output of the MC1391's internal oscillator. An error voltage is applied to the oscillator timing control voltage to lock in the external synchronous pulse and the oscillator. The duty cycle of the MC1391 oscillator output is set to provide a 63% "ON" time to the power MOSFET gate.

Essentially, the prime requirement for driving the power MOSFET for this horizontal scan output design is to insure sufficient gate on-voltage and low enough impedance for a fast turn-off transition. Since the power MOSFET has a high gate input impedance, the gate voltage requirement is easily met, with little wasted power. The off transition requires that the power MOSFET's internal 1000 pF gate capacitance be discharged very quickly. This is accomplished by using a single hex inverter IC, with all the gates wired in parallel. As mentioned before, other devices can be used to drive the MOSFET. The CMOS inverter was chosen to show that CMOS technology is sufficient to drive the MOSFET.

The system described above provides excellent performance. The gate-drive voltage of the power MOSFET was purposely pulsed during the peak retrace drain voltage pulse to simulate destructive transients due to anomalies such as arcing.

It was found that a controlled drain-to-source current occurred, with no catastrophic failures, as long as the total power dissipation was held within the limits of the power FET's safe operating area ratings. Figure 8-34 shows the waveforms associated with the retrace pulse test. Since the MOSFET is a high input impedance device, it is important to insure the gate of the power MOSFET is at a low impedance during the retrace period. The gate should not be driven negative, to minimize the possibility of voltage spikes causing gate avalanche. The gate cannot withstand an avalanche condition of any measurable current intensity and survive. Since the power MOSFET device selected for this design exhibits at least a 2.0 volt threshold, a negative gate-drive is not important.

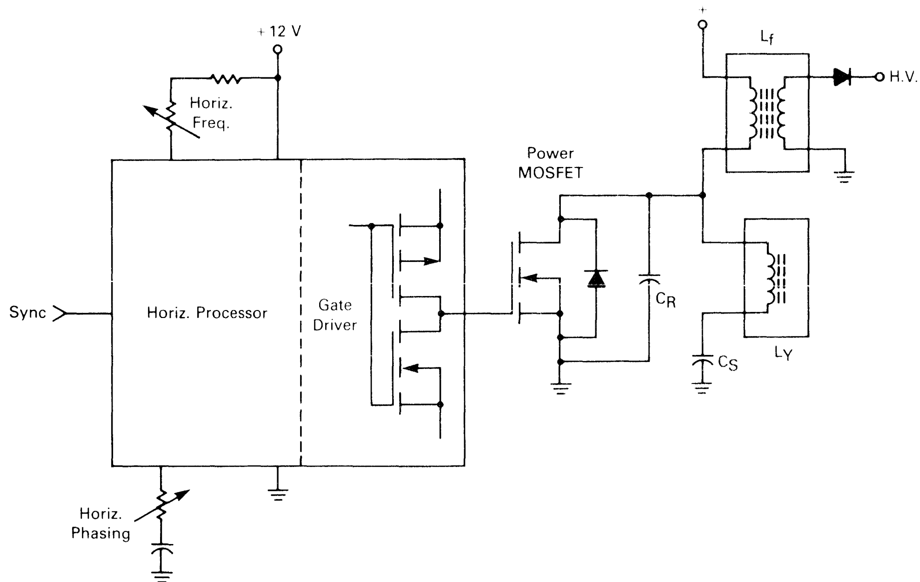

FIGURE 8-32 — POWER MOSFET HORIZONTAL OUTPUT SYSTEM

Figure 8-35 shows a comparison of the key horizontal output circuit waveform patterns between a bipolar and MOSFET design. Note the large reduction in the horizontal output drive power and lack of storage time in the MOSFET design.

Fast High-Current MOSFET Driver

A totem-pole MOSFET driver circuit shines when high-current, fast-transition pulses must be generated from low-voltage sources. Its MOSFETs sidestep a number of problems that their bipolar counterparts present in the same circuit.

High-speed transistors and high-current transistors intended for PWM applications have created a need for high-current, fast-drive circuits. Transistors that demand 20 to 35 A of reverse base current for rapid turn-off and can be driven by as little as 5.0 V of off-voltage are a common requirement. Bipolar devices switch in nanoseconds but are limited to 5.0 to 10 A when driven from low-voltage collector supplies. With higher current capability, such transistors require power transistors as drivers and, when driven by a low-voltage source, sacrifice switching speed.

Yet a third possible solution — paralleling fast, low-current transistors — presents two problems: current sharing and physical layout.

The MOSFET driver circuit in Figure 8-36 uses two N-channel devices with positive and negative polarities. Fast transitions are possible, even when a low-voltage source is used. The circuit returns to 0 V between pulses, an important feature when driving high-power Darlington transistors with base-bias resistors and speed-up diodes. In this case, excessive heating would otherwise occur during the off-time interval.

Small size, simple configuration, and minimum component count join with ease of operation to make this driver circuit very useful for applications in variable-frequency switched-mode power supplies, and inverters.

In operation, a single-polarity, negative-going pulse from a pulse generator is applied to the input. The pulse, whose width can vary anywhere from 5.0 μs to 3.0 ms, turns on PNP predriver transistors Q2 for the positive-polarity output.

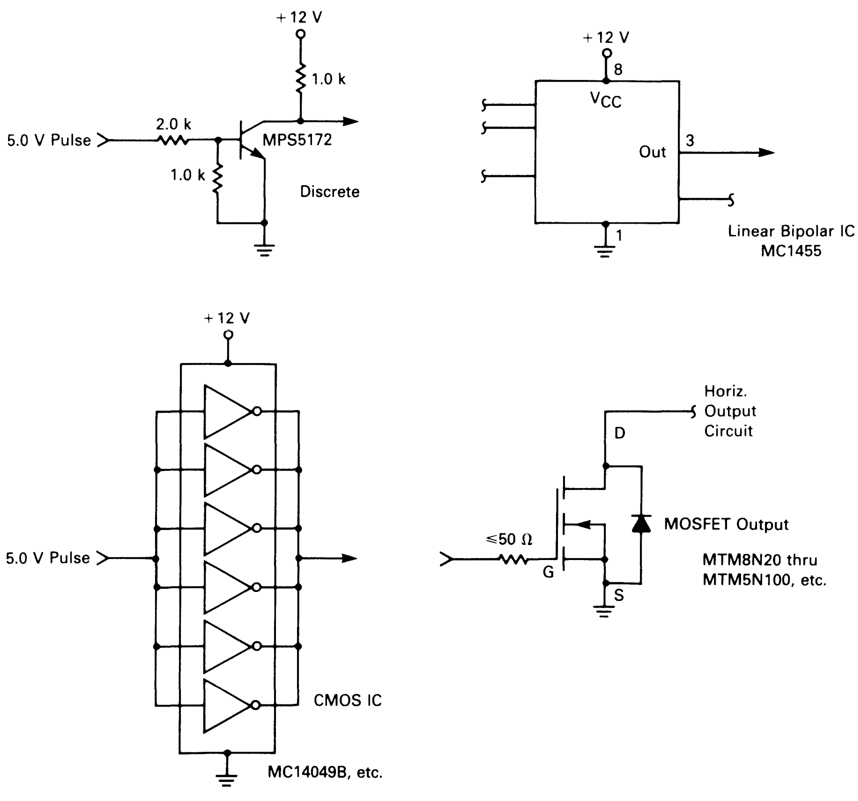

FIGURE 8-33 — MOSFET DRIVE CIRCUITS

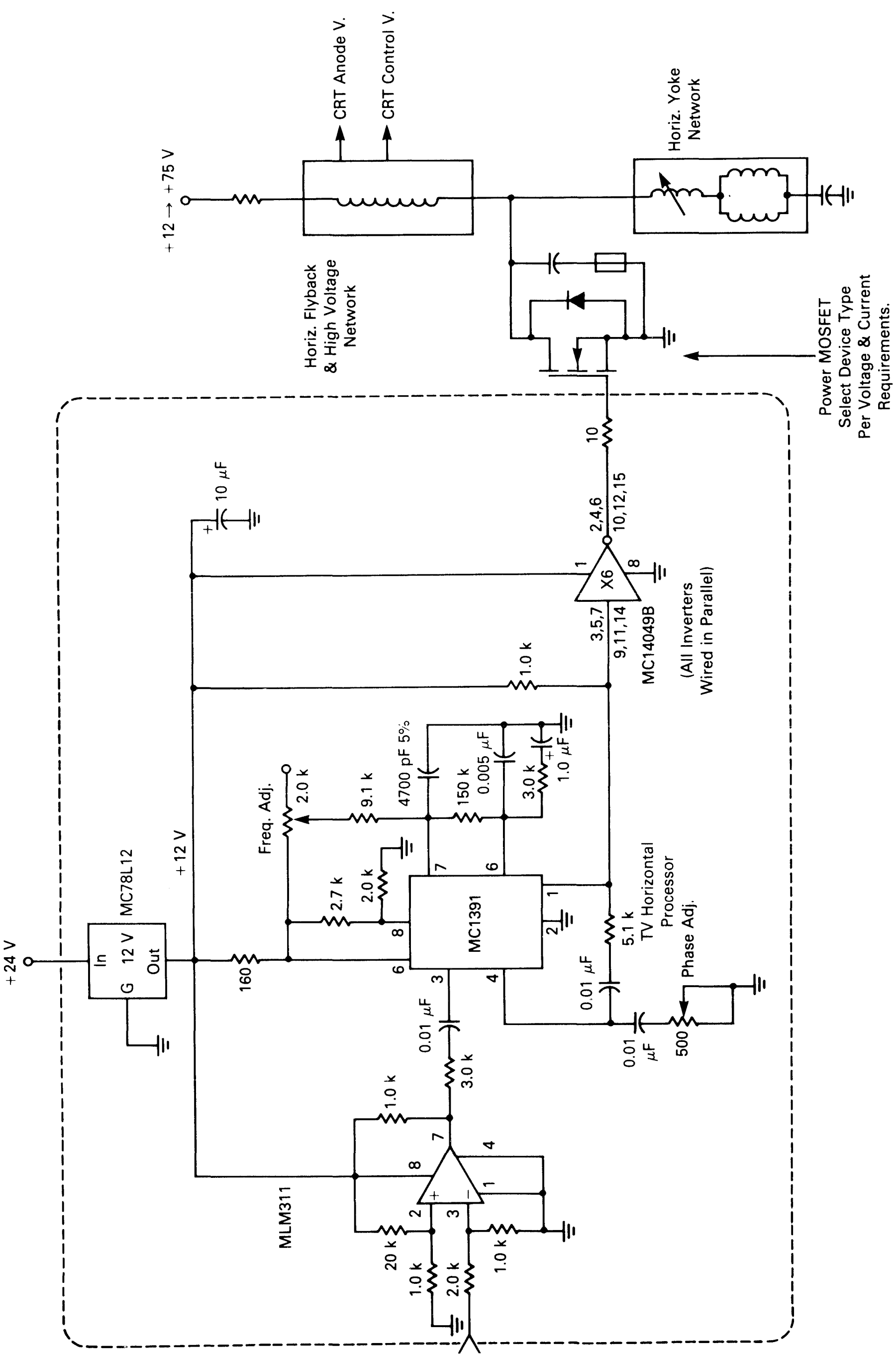

FIGURE 8-34 — POWER MOSFET HORIZONTAL SWEEP DESIGN

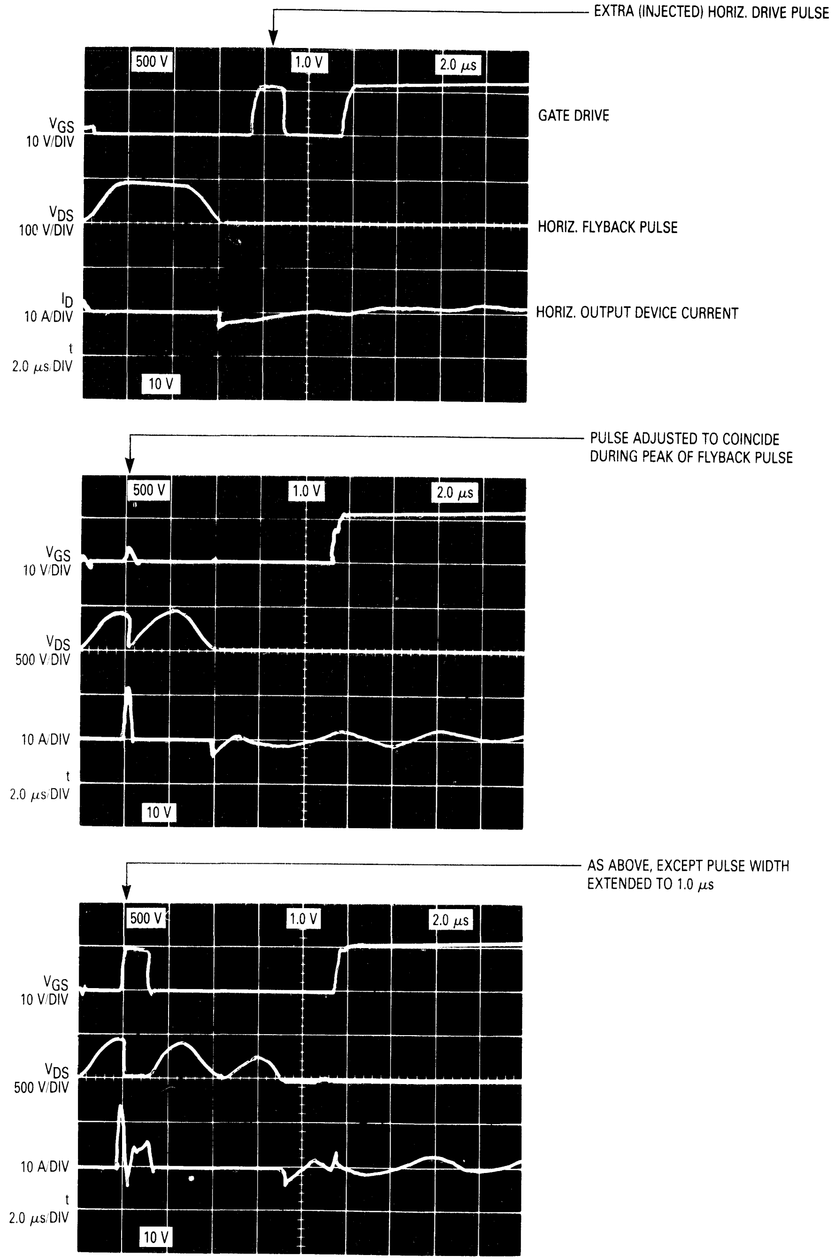

FIGURE 8-35 — HORIZONTAL DEFLECTION RETRACE PULSE TEST WAVEFORMS

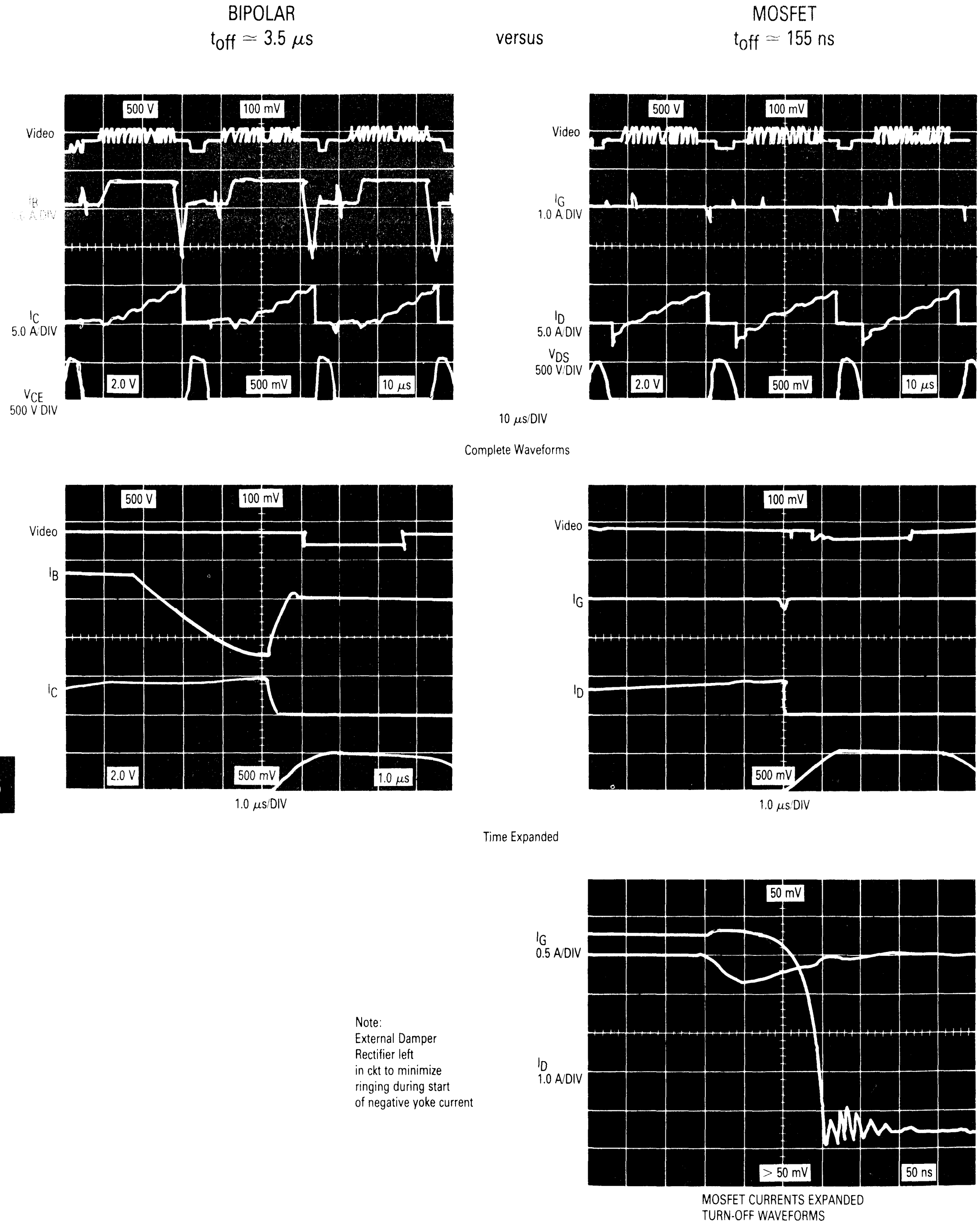

FIGURE 8-36 — BIPOLAR versus MOSFET

Resistor R_b, inserted in series with the drain lead of Q2 and the supply, sets the positive drive level. The resistor should be selected for a drive of 10 V or greater as well as the amount of desired current.

After the required on-time of the positive output current, the pulse generator returns to zero. Then, the RC differentiator network applies a positive voltage to the gate of MOSFET Q3, which supplies the negative polarity output. The values shown can be changed to lengthen the duration of the negative drive. The negative voltage remains for about 10 μs and then returns to zero, completing a single cycle.

The circuit can be used with FETs by replacing R_b with a short and the positive and negative voltages applied to the devices' gates. For controlled gate-impedance drive, resistors can be inserted in series with the gates. Similarly, a resistor added in series with the base of the bipolar transistor results in controlled base-current drive.

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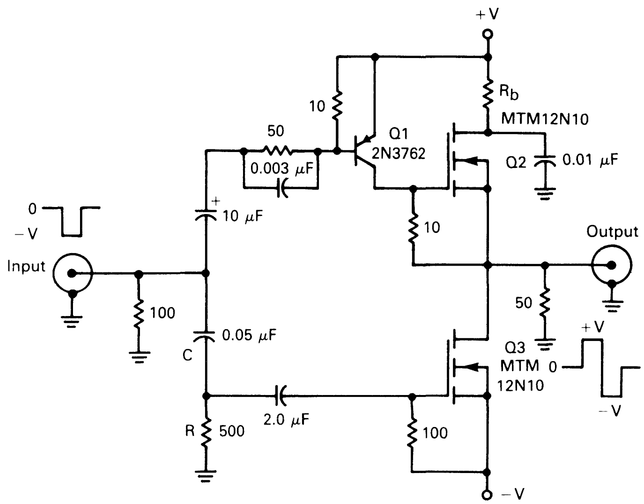

FIGURE 8-37 — MOSFET DRIVER CIRCUIT

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Chapter 9: Spin-Off Technologies of TMOS

SENSEFETs™

Some of the more exciting developments in discrete power semiconductors are arising from power IC concepts. Integrated circuit design engineers, with fine geometries and ratioing techniques as standard tools of the trade, are applying these concepts to discrete power semiconductor design with great success. One notable example is SENSEFETs.

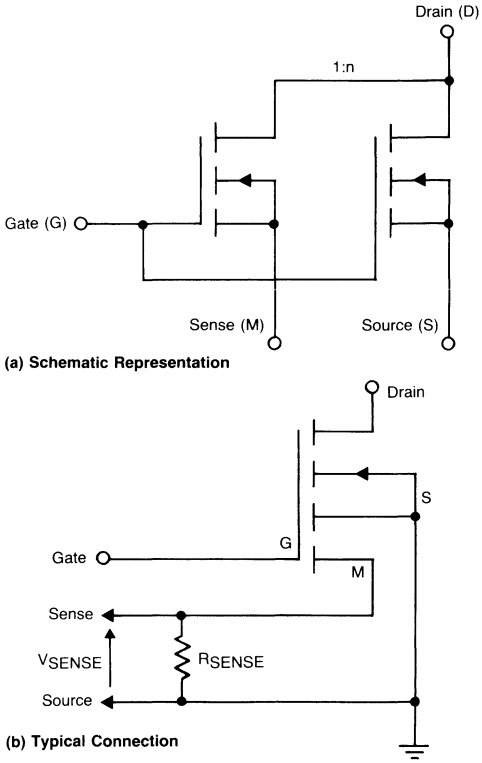
By splitting drain current into power and sense components, these new devices feature a "lossless" current sensing technique for discrete designs. The intention of this chapter is to explore the concept, device characteristics, and the state-of-the-art performance that SENSEFETs can provide.

Lossless Current Sensing

"Lossless" current sensing is a technique that arises from integrated circuit ratioing concepts. It is based upon the tendency of individual source cells in a monolithic power MOSFET to match. Therefore, if one or two out of several thousand cells are returned to a separate sense or mirror connection, a ratio between load current and sense current is developed.

This concept is illustrated in Figure 9-1a, where sense current and load current are related by the ratio 1:n, provided that the sense terminal and the source terminal are returned to the same potential. When a sense resistor is placed between these two terminals, the ratio is disturbed somewhat, but remains quite predictable for low values of R_{SENSE}. A shorthand symbol for the SENSEFET, and a connection for R_{SENSE} are shown in Figure 9-1b.

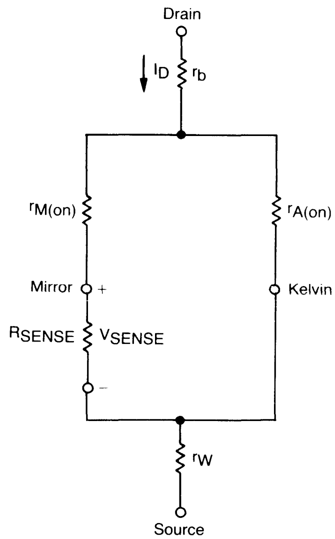
The circuit model and equations shown in Figure 9-2 describe SENSEFET behavior during fully switched on operation. From the equations, one can easily calculate the sense resistance required for a given sense voltage. Although any value of sense resistance can be used, two considerations are worth noting: (1) as R_{SENSE} increases, V_{SENSE} asymptotically approaches a maximum voltage magnitude equal to $I_D \cdot r_{A(on)}$, and (2) sense voltage accuracy over the operating temperature range severely degrades with increasing sense resistance. From a practical point of view, relatively good accuracy is maintained when $R_{SENSE} < r_{M(on)}/2$.



(a) Schematic Representation

(b) Typical Connection

FIGURE 9-1 — FUNCTIONAL REPRESENTATION



$r_b \triangleq$ bulk resistance
$r_{A(on)} \triangleq$ source cells on-resistance
$r_{M(on)} \triangleq$ sense cells on-resistance
$r_W \triangleq$ source wire bond resistance
$R_{SENSE} \triangleq$ external sense resistance
(1) $r_{M(on)} = n\, r_{A(on)}$ where $n \triangleq$ geometric current mirror ratio
(2) $V_{SENSE} = I_D \cdot r_{A(on)} \cdot R_{SENSE} / [R_{SENSE} + r_{M(on)}]$
(3) $R_{SENSE} = V_{SENSE} \cdot r_{M(on)} / [I_D \cdot r_{A(on)} - V_{SENSE}]$
(4) $I_D = V_{SENSE} \cdot (R_{SENSE} + r_{M(on)}) / r_{A(on)} \cdot R_{SENSE}$

FIGURE 9-2 — SENSEFET ON-RESISTANCE MODEL AND ASSOCIATED EQUATIONS

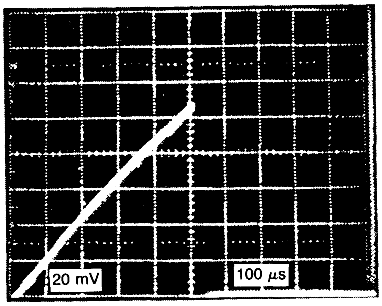
In linear operation, R_{SENSE} is in series with a current source, and does not directly attenuate sense current. Instead it is likely to have a first order influence on gate-source bias voltage. Since sense voltage subtracts from the sense cell's gate source voltage, sense cell current is reduced with respect to current in power section cells. Therefore, there is a debiasing effect which alters the 1:n sense ratio as a function of R_{SENSE}. Similar to switch-mode operation, moderate values of sense resistance alter the sense ratio in a predictable way, resulting in a useful measurement.

Accuracy

Accuracy for a current sensing technique can be looked at in a number of different ways. Of most concern in switching applications are the linearity, temperature coefficient, and unit to unit variations that occur when the power device is fully switched on. These parameters are illustrated for the MTP10N10M, a 10 A/100 V SENSEFET.

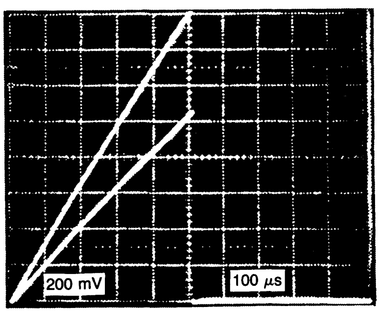
LINEARITY: At any given drain current, a corresponding sense voltage can be chosen by scaling R_{SENSE}. As drain current, I_D, changes from this baseline, linearity measures the accuracy with which the V_{SENSE}/I_D ratio holds at other currents. For example, at 10 A a 20 Ω sense resistor typically sets V_{SENSE} at 116 mV for the MTP10N10M. A linear response would suggest a reading of 58 mV at 5 A, which corresponds very nicely to a measured value of 58 mV. On the other hand, if R_{SENSE} is increased to 2 kΩ the results turn out somewhat different. At 10 A V_{SENSE} measures 1420 mV, implying a 5 A reading of 710 mV. However, measuring sense voltage at 5 A results in a 618 mV data point. The difference amounts to 15%, and points to a more accurate measurement with lower values of R_{SENSE}.

Sense Voltage @ 20 mV/div



(a) R_{SENSE} = 20 Ω — T_C = 25°C Upper Trace, T_C = 125°C Lower Trace, Peak Drain Current = 10 A

Sense Voltage @ 500 mV/div



(b) R_{SENSE} = 2 kΩ — T_C = 25°C Lower Trace, T_C = 125°C Upper Trace, Peak Drain Current = 10 A

FIGURE 9-3 — TEMPERATURE STABILITY

TEMPERATURE COEFFICIENT: A graphic representation of temperature stability is shown in Figure 9-3. For this figure drain current is ramped from 0 to 10 A. The photos are double exposures with one shot taken at 25°C and the other at 125°C. As with linearity, the best results are obtained with a sense resistor that is small with respect to the sense cell's on resistance, $r_{DM(on)}$. With 20 Ω, temperature tracking is essentially within a trace width, and the two values diverge by only 4% at 10 A. As R_{SENSE} is increased, temperature coefficient becomes less dependent upon matching and more a function of the power device's on voltage. In the limit where R_{SENSE} is very large, sense voltage approximates the power device's $V_{DS(on)}$ and tracks its temperature coefficient. This tendency is quite evident in Figure 9-3b, where at R_{SENSE} = 2 k the two measurements diverge by 45% for a 100°C change in temperature.

TOLERANCE: The parameter that describes tolerance for a SENSEFET is the cell ratio, n. It is defined for R_{SENSE} = 0 and measures the ratio of source current to sense current without the attenuation of a sense resistor. First generation specifications guarantee that n will fall within a ±10% window.

As sense resistance is increased from zero, the apparent cell ratio increases by approximately the ratio of R_{SENSE} to the sense cell's on-resistance, $r_{DM(on)}$. Tolerance also increases with increasing values of R_{SENSE}, as sense current becomes increasingly dependent upon $V_{DS(on)}$ and less upon ratioing. In the limit, large values of R_{SENSE} produce an initial tolerance which varies directly with $V_{DS(on)}$. In this situation tolerance degrades from better than 10% with $R_{SENSE} \ll r_{DS(on)}$ to roughly ±20% with $R_{SENSE} \gg r_{DM(on)}$.

Adding these factors to linearity considerations and temperature performance it is quite evident that SENSEFET accuracy improves as R_{SENSE} is minimized. However, signal level is also reduced, and an optimum design has to balance SENSEFET accuracy and signal level. In general this will result in values of R_{SENSE} which range from 10% to 100% of $r_{DM(on)}$

Subtle Considerations

There are a number of subtle considerations that can make or break a SENSEFET motor drive. Discussion begins with double pulse suppression and touches briefly on several other important design issues.

DOUBLE PULSE SUPPRESSION: In linear circuits where the current limiting control function is a compensated loop, application of the lossless current sensing technique is relatively straightforward from a circuit topology point of view. In PWM circuits, however, circuit topology is a critical issue. In particular, it is important to include double pulse suppression in the PWM drive loop. In other words, once the current limit trip point is reached, it is important to disable the power device for the remainder of the clock interval.

If the current limit loop is allowed to oscillate at its natural frequency, the primary objective of protecting the power transistor can be jeopardized. Without double pulse suppression, the loop will often oscillate faster than gate drive will switch the power device with reasonable switching losses. When this happens it is very easy for power dissipation to rapidly exceed acceptable levels and for an otherwise foolproof protection scheme to fail from over dissipation.

DIODE CLEARING: In bi-directional and brushless motor drives where freewheeling diodes are commutated, diode recovery currents can be an issue. For example, suppose that a P-channel MOSFET in the top half of a bridge has motor current flowing through its freewheeling diode. If a SENSEFET on the bottom half of this leg is then turned on rapidly there will be a substantial current spike. This spike consists of the motor current plus the freewheeling diode's reverse recovery current, and can easily be three or four times maximum run current.

SENSEFETs are high-speed devices that easily transmit a corresponding peak sense voltage to the drive's current limiting circuitry. Therefore, it may be necessary to keep switching peaks from inadvertently tripping current limit circuitry.

There are several relatively straightforward methods for doing this. In SMARTMOS circuits, for example, a low value of R_{SENSE} is generally used in combination with a sense amplifier. The sense amplifier does a good job responding to the PWM repetition rate but, due to its rolloff characteristics, largely ignores switching spikes. Similarly, a low pass filter between R_{SENSE} and the drive's current limit input will do the same job. Approaching the problem from a different angle, digital techniques can also be used to blank the current limit loop during reverse recovery time.

COMMUTATING ERROR: If a PWM signal is instead applied to the upper half of the same bridge, a more difficult situation is created. In this case, suppose that motor current is flowing through the SENSEFET's freewheeling diode when the upper switch turns on rapidly. This time it is the SENSEFET's drain source diode that gets cleared, and this clearing process produces a high level error signal. In other words, during reverse recovery time, the SENSEFET's output can easily exceed its steady state maximum value by more than an order of magnitude. This voltage is in the right direction to trip current limit circuitry, and is large enough to be difficult to filter out. For this reason, circuit topologies which avoid pulse width modulating both upper and lower halves of the bridge are usually preferred. Where this constraint is not desirable, digital blanking of current limit circuitry during reverse recovery time can be used.

SENSE AMP SATURATION: When a sense amplifier is used to boost a low level SENSEFET signal for further processing it is necessary to pay close attention to the amplifier's saturation voltage specification. For example, in CMOS systems the MC14574 quad comparator does a good job of working directly with SENSEFET signals. If instead the companion MC14573 operational amplifier is chosen to boost signal level, its output voltage range can pose a serious limitation. With the operational amplifier, there will be a dead zone that corresponds to its specified 1.05 volt minimum output voltage. In this dead zone the SENSEFET's output voltage does not affect the amplified output voltage until the latter exceeds 1.05 volts.

For this reason, minimum output voltage is a key specification for SENSEFET interfacing, assuming that single supply operation is desired. The MC34074 is an excellent choice in this regard, with a typical minimum output voltage of 100 mV, and specified maximum of 200 mV.

GROUND LOOPS: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop error in this kind of a situation is a first order design consideration. In particular, current flowing from the SENSEFET's source into a non-zero ground impedance can easily create voltage drops which are significant with respect to a 100 mV measurement.

For this reason, a Kelvin source connection is provided. Its use is relatively straightforward, and illustrated in Figure 9-4. The key consideration is to tie the current limit circuitry's voltage reference to the SENSEFET's Kelvin terminal. This connection eliminates the errors that can be developed by high currents flowing in power ground.

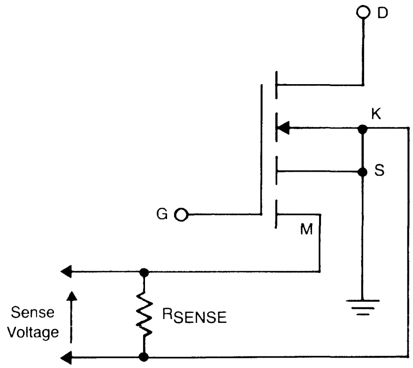


FIGURE 9-4 — KELVIN CONNECTION

Motor Drive Application Example

An example of how SENSEFETs fit into a PWM motor drive is illustrated in Figure 9-5. This is a CMOS/Power MOS system based upon the MC14574 quad comparator, MC14027B dual J-K flip flop, MC14049UB inverter buffer, and MTP10N10M SENSEFET.

This system establishes a 2.5 V reference with a TL431, and uses this voltage to limit the peak of a 2.5 V ramp. This ramp is generated by charging timing capacitor C_T until its voltage reaches 2.5 V, then tripping an R-S latch and turning on a small MOSFET until it has been discharged to approximately 250 mV. At this point the latch is reset, the BS170 MOSFET is turned off, and the cycle repeats. The MC14027B J-K in this case is configured as

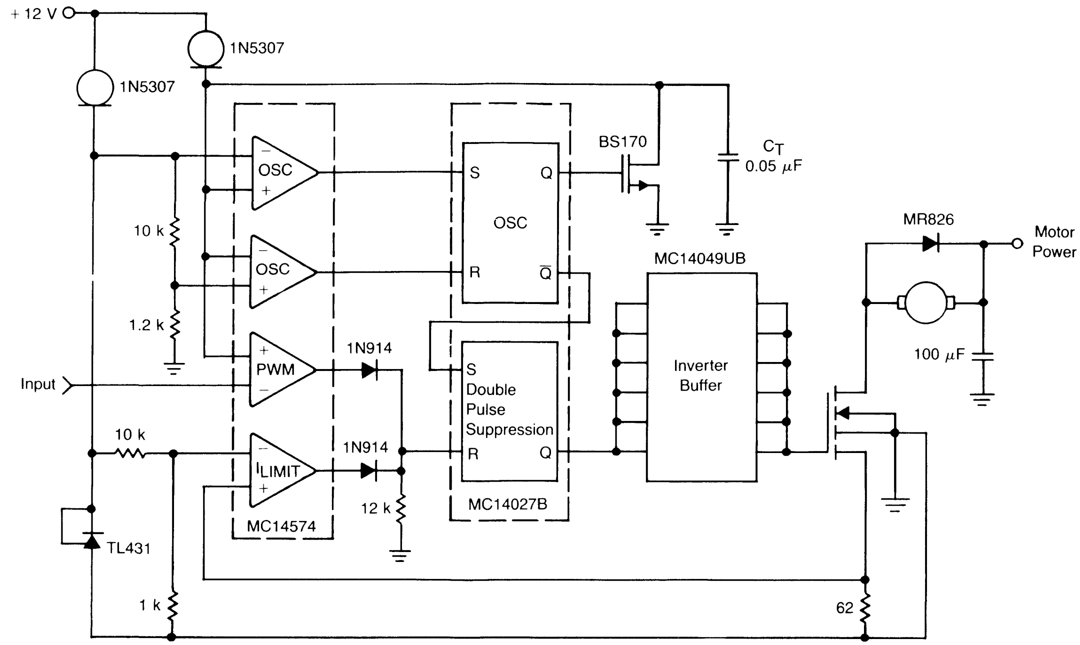


FIGURE 9-5 — CMOS/SENSEFET MOTOR DRIVE

an R-S latch. Clock and set terminals are tied together forming the S connection. The reset terminal is used as the R connection, and the J/K inputs are tied high and low respectively. The ramp is then fed into a PWM comparator, where a zero to 2.5 V input signal applied to its inverting input yields a zero to 100% duty cycle PWM output signal.

This signal is diode OR'd with the output of a current limit comparator and fed to the reset input of a double pulse suppression flip flop. The current limit comparator compares a 225 mV level that is derived from the reference with the SENSEFET's output voltage. Whenever either the PWM signal or the current limit comparator go high, this second flip flop is reset, thereby turning off the SENSEFET. The SENSEFET then remains off until the flip flop is set at the beginning of the next clock cycle.

This time the MC14027B J-K is configured as a reset dominant R-S latch. The connections are straightforward. The clock terminal serves as the "S" input and the reset terminal for the "R" connection. K and set terminals are grounded, J is tied high.

With the values shown, clock frequency is approximately 20 kHz and peak motor current is limited to 9 A. The MC14049 is quite adequate for providing gate drive at this frequency. Rise and fall times for the MTP10N10M are under 100 ns.

At lower PWM frequencies it is advisable to insert some resistance in series with the SENSEFET's gate in order to reduce switching noise. A 470 Ω series resistor produced the relatively clean waveforms in Figure 9-6, where the PWM rep rate has been set to approximately 1 kHz.

In this figure the ramp waveform at C_T is shown in the upper trace, SENSEFET drain current in the lower trace, and drain source voltage in the middle. Beginning with the second horizontal division a 2.5 V step function has been applied to the drive's input. The waveforms show an orderly startup, operating a 1/2 HP motor from an 80 V bus. The double pulse suppression technique syncs current limiting to the oscillator and provides for a safe, well controlled startup. When the double pulse suppression feature is removed, the MTP10N10M will fail almost instantaneously under the same starting conditions.

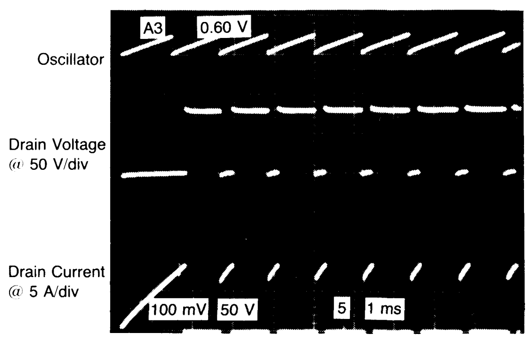


FIGURE 9-6 — STARTUP WAVEFORMS

Switching Power Supply Application Example

In order to work well with SENSEFETs, current-mode control circuitry has to accept relatively low values of sense voltage. First generation current-mode control IC's will accept the SENSEFETs output voltage during regulation but often are found lacking under short circuit conditions where current limit thresholds can be a volt or more for the most popular types.

A new current-mode control IC, the MC34129, has an architecture which works quite well with SENSEFET output voltages, and provides a number of other second generation features. An illustration of the circuit and a timing diagram are provided in Figure 9-7.

In terms of interfacing with SENSEFETs, there are three key features. First, the error amplifier and soft start buffer are open collector types. This configuration permits adjustment of the current limit threshold within the SENSEFET's operating range. Second, a 200 mV offset is provided in the PWM comparator. Functionally it appears as a voltage source that is inserted between the SENSEFET's output and the PWM comparator's noninverting input. This 275 mV gives the SENSEFET's output enough boost to overcome the error amplifier's saturation voltage.

In doing so, compensation is also provided for an opto isolator's saturation voltage, simplifying operation in isolated systems. The MC34129 also has both power and sense grounds, which enables optimum use of the SENSEFET's Kelvin source connection. As the application example in Figure 9-4 shows, the signal ground can be connected to the Kelvin terminal while the power ground is connected to the SENSEFET's source. This arrangement minimizes the noise problems that could otherwise occur working with small signal levels.

In terms of other second generation improvements, the SENSEFET's inherent efficiency advantages are complemented by the MC34129's unusually low supply current requirement. Even driving 500 pF of gate capacitance at 25 kHz it typically draws only 1.5 mA from the V_{CC} line. One of the secrets is an SCR which is used for off-drive. Compared to the usual bipolar transistor, the SCR can discharge a power MOSFET's gate capacitance with considerably less bias current. For off-line applications, the second generation architecture includes a start-run output that simplifies switching from start-up bias to an operating bias that is supplied by an auxiliary bootstrap winding. While the soft start capacitor is charging, the start/run output is high, enabling line bias from an NPN transistor to provide power for startup. An example is shown in Figure 9-8. When the soft start capacitor charges to a level of 2 V, the start/run output goes low, turning off this bias to allow for more efficient operation from a low voltage winding. Another unusual aspect of the topology is an internal fault timer that is part of the soft start network. Under conditions of prolonged output short-circuit, the fault timer will discharge the soft start capacitor and produce a skip cycle operation, thereby reducing stress on the power switching components. Last but not least, the MC34129 also includes a sync/inhibit input which allows synchronization of the oscillator to an external signal.

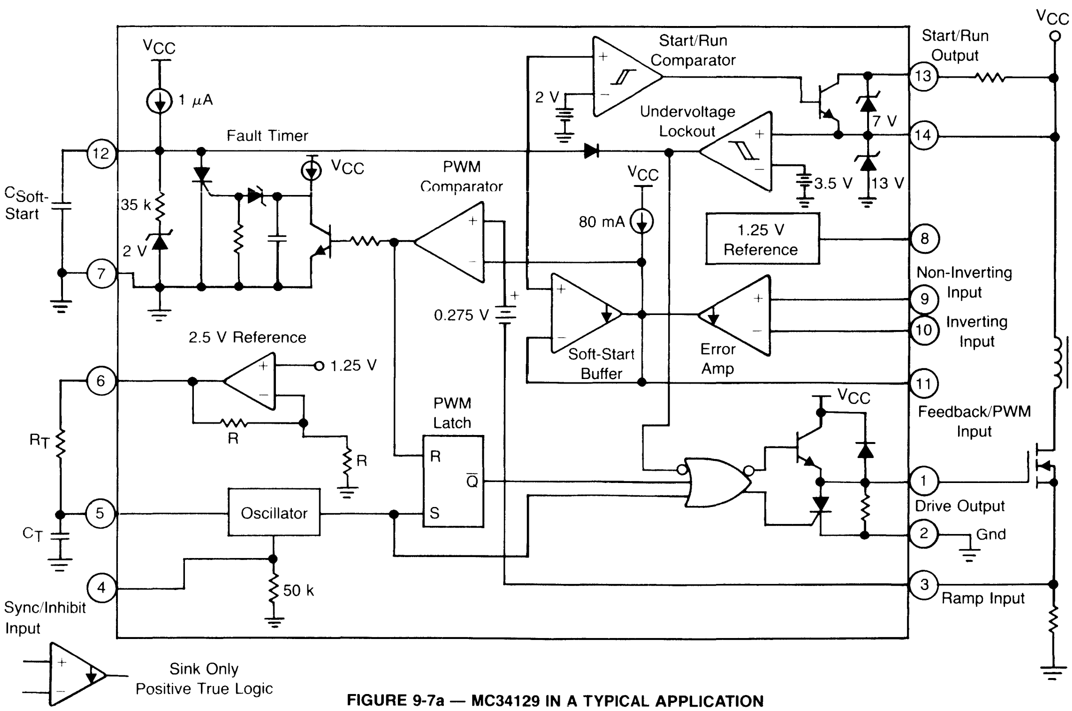


FIGURE 9-7a — MC34129 IN A TYPICAL APPLICATION

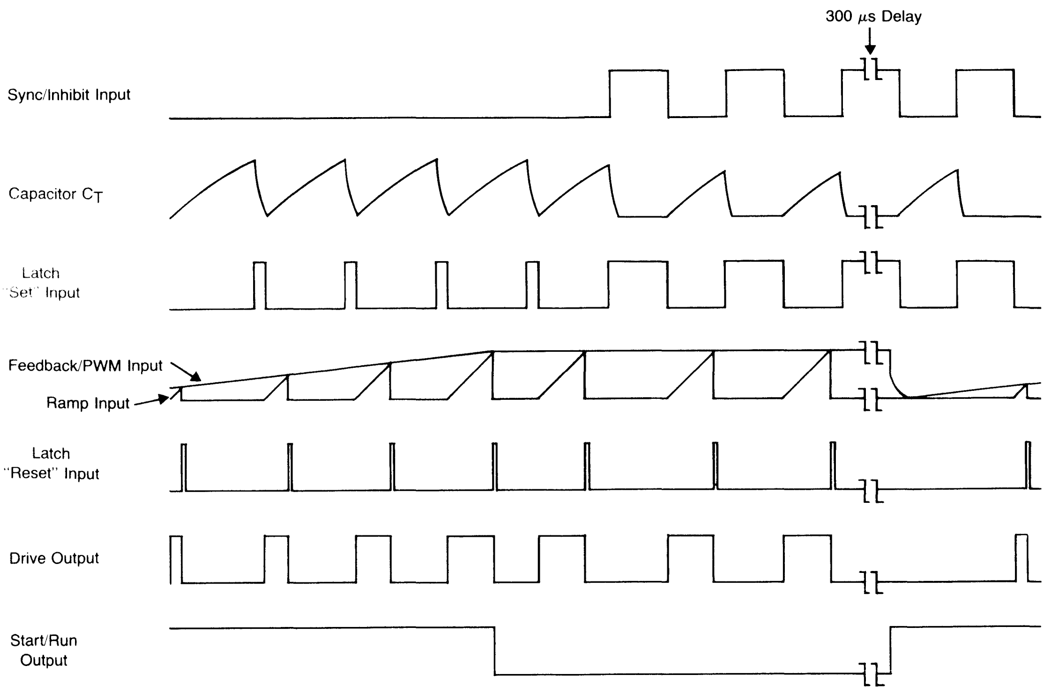


FIGURE 9-7b — TIMING DIAGRAM

FIGURE 9-7 — MC34129

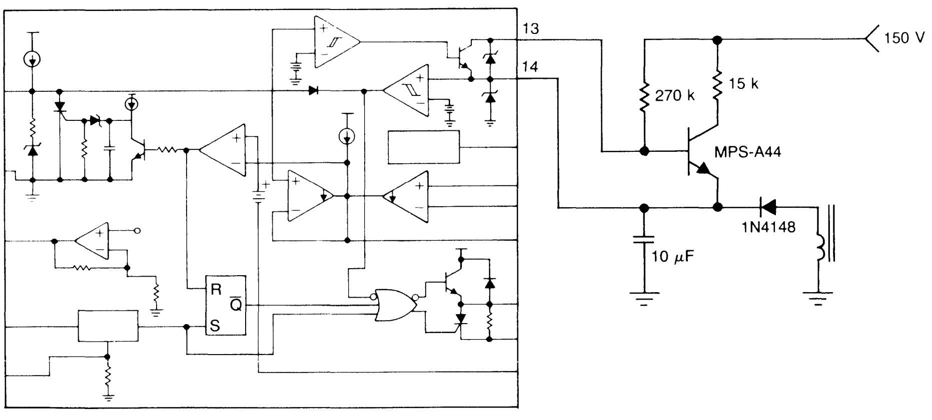


FIGURE 9-8 — BOOTSTRAP BIAS

An example which illustrates how the MC34129 and SENSEFETs are used appears in Figure 9-9. This figure describes an isolated 12 V to 5 V current mode supply and is a convenient vehicle for describing how to use both parts.

Starting with the oscillator, R_T and C_T are selected for operating frequency and dead time. Timing capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V, and discharged to ground by an internal current sink. During the discharge of C_T, the oscillator generates a clock pulse that sets the latch and holds one input of the NOR gate high. This causes the drive output to be held low, thus producing output dead time and limiting the output duty cycle.

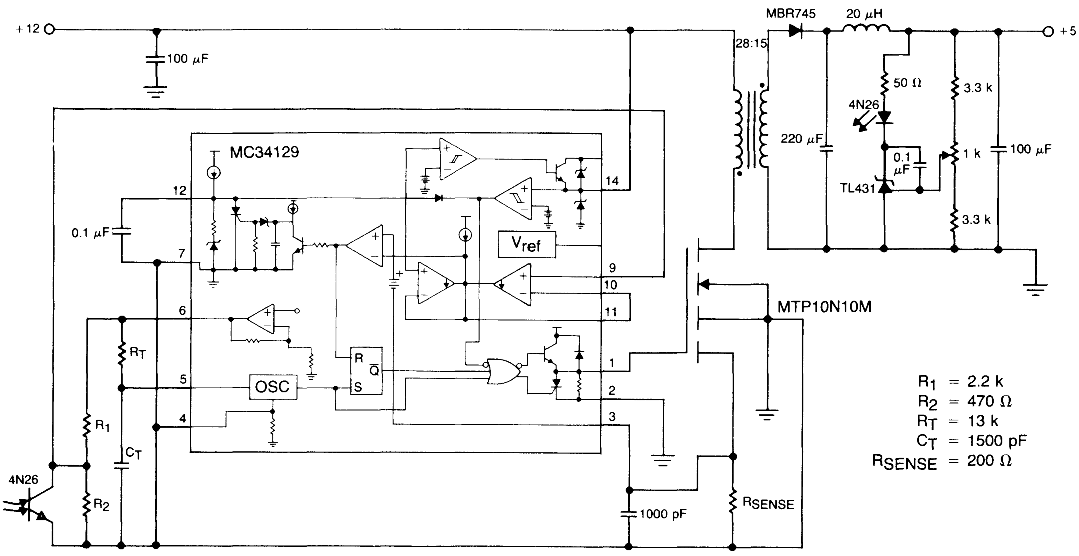


FIGURE 9-9 — MC34129/SENSEFET POWER SUPPLY

The amount of dead time can be programmed by values chosen for R_T and C_T. Note that many combinations of R_T and C_T will give the same oscillator frequency, however, only one combination will yield a specific dead time at a given frequency. The values shown produce an operating frequency of 28 kHz and a maximum on-time slightly less than 50%.

The ramp voltage, V_{Ramp}, is generated by R_{SENSE} and fed into the PWM comparator's noninverting input at pin 3. The ramp's magnitude is determined by the value of R_{SENSE} and the amount of primary current that is switched. As a first order approximation:

$$V_{Ramp} \cong \frac{R_{SENSE} \cdot I_P \cdot r_{DS(on)}}{r_{DM(on)} + R_{SENSE}},$$

where I_P represents primary current, $r_{DS(on)}$ is the SENSEFET's drain-source on resistance, $r_{DM(on)}$ is the sense section's on resistance, and R_{SENSE} is identified in Figure 9-9. As a general rule of thumb, best results are obtained when R_{SENSE} is chosen to produce at least a 100 mV signal at normal operating currents and also be no larger than $r_{DM(on)}$. Knowing the relationship between V_{SENSE} and I_P, maximum short circuit current can be set with voltage divider R1, R2. The output voltage from this divider is coupled through a unity gain follower to set the upper trip point on the PWM comparator. To calculate the trip point, 275 mV of offset is added to the SENSEFET's output voltage.

The regulation loop may be closed with an opto isolator which pulls down the voltage at pin 9, thereby reducing maximum primary current and also duty cycle. This configuration is advantageous in that it saves components. R1 and R2 are used to both limit peak current and provide a connection for the opto isolator.

Soft start is provided in a rather straightforward manner by connecting a capacitor between pins 12 and 7. A 1 μA internal current source charges this capacitor, producing a voltage ramp on pin 12 during startup. The output is held low until the voltage at pin 12 exceeds the PWM comparator's 200 mV offset. As the soft start capacitor is charged further, maximum allowable duty cycle ramps up with the capacitor voltage until the limit imposed by R1 and R2 takes over.

For the example in Figure 9-9, the MTP10N10M SENSEFET has nominal values of $r_{DM(on)}$ and $r_{DS(on)}$ which are 288 Ω and 160 mΩ, respectively. Sense voltage with 288 Ω of R_{SENSE} is therefore approximately 60 mV per amp of primary current. With R1 and R2 setting the upper trip point at 470 mV, peak current is limited to something just shy of 3 A, given the 275 mV offset. At startup, the 0.1 μF capacitor holds the output off for 20 ms, and allows full duty cycle after approximately 40 ms.

TMOS II, III and IV

Recent advances in low voltage power MOSFET technology are rapidly altering the power transistor market. These developments, which are highlighted by a dramatic reduction in the on-resistance for a given die size, render meaningless many of the previous performance and cost comparisons between MOSFETs and other technologies.

The differences between old and new device design philosophies and process techniques are resulting in MOSFETs with characteristics that differ from those of their predecessors in some key aspects. Consequently, in order to best utilize these advances, designers need to acquaint themselves with current development trends.

The intent here is to aid the circuit design engineer in such a study. The topics covered include:

1. The extent of the performance gains of the new generations of MOSFETs
2. A discussion of why these recent device improvements affect low voltage devices (<200 V) to a greater extent than they do high voltage devices
3. The special design considerations necessary to ensure optimum performance.

But first, a brief survey of power MOSFET history will help the reader understand why such remarkable performance improvements are possible.

A Brief History of Power MOSFETs

The history of power MOSFET development began less than a decade ago when device engineers started moving away from the conventional small-signal MOSFET structure, i.e., devices with all contacts on the surface of the die, long channel lengths and high on-resistance. Their inefficiency mandated the use of large die, which made the devices too expensive to compete with the bipolar transistor.

Lateral DMOS structures were the first devices that could reasonably be referred to as power MOSFETs. However, long channel lengths and poor silicon utilization still kept on-resistances and prices high. Other approaches soon followed.

A second breakthrough came with the advent of vertical current conduction. The first structures that allowed current to flow from the back of the die (the drain) to the source metallization on the top surface of the die were the V-groove devices, sometimes referred to as VMOS transistors. Although their development was an important step toward more efficient use of silicon, process and performance problems associated with the V-groove itself foretold its early demise. Most of the major manufacturers, including Motorola, once pursued this technology but have since abandoned it and have opted for the latest step in the progression toward more efficient silicon utilization.

By 1981, most manufacturers were persuaded that the Vertical DMOS technology was the most promising option. Its planar structure signaled simpler wafer processing, and its relatively short channel lengths promised low on-resistances. Each company coined trademarks to refer to their special cell geometry and processing techniques. For example, International Rectifier developed the "HEXFET," Siemens introduced the "SIPMOS" transistor, and Motorola preferred the name "TMOS" for its line of Vertical DMOS transistors. Even though some of the cell shapes were quite different, i.e., there were square and hexagonal cells and even long bar geometries, a cross section of each die revealed the same geometric patterns characteristic of all Vertical DMOS devices.

For a couple of years, the major manufacturers squabbled over which geometry provided the lowest on-resistance for a given die area. Somehow the cell geometry of each manufacturer was always quoted to be about 10% more efficient than all others. What was overlooked in these comparisons is the relative insignificance of squares versus hexagonal cells or other configurations and the great importance of optimizing the cell spacing, the dimensions of the various elements that constitute the cell itself, and wafer processing techniques.

1984 proved to be the year in which advances in power MOSFET technology have been so significant and have occurred so rapidly that even those closest to the developments have been surprised. Early in the year Motorola introduced their second generation devices, calling them "TMOS II." These devices offered on-resistances up to 30% lower than those of first generation MOSFETs of similar die size. Low voltage devices were the benefactors of most of the improvements. Adjustments to improve cell spacing, cell size, and in some cases cell geometry, were the features that distinguished TMOS II from TMOS I.

The final salvo of 1984 was fired in the fall when Motorola introduced the TMOS III line. Again a product introduction swept away preconceived notions of the limitations of power MOSFETs by making available devices with the lowest per unit area on-resistance in the industry. In an extension of the TMOS II design philosophy, cell packing densities rose from about 600K to 1 M for TMOS III. Diffusion profiles were optimized as was the resistivity of the silicon wafers used to build the devices. The combination of the increased packing density and the "short channel process" netted devices with on-resistances of about 1/4 that of the original TMOS.

There is an industry-wide trend toward smaller, more efficient, and less costly power MOSFET die. This foreshadows the rapid extinction of all the original low voltage chip designs. Such pervasive change makes mandatory a familiarization with the benefits and limitations of the newest devices.

In the span of just a few months, the performance standards of power MOSFETs have been revised to the point that the difference between the old and new is almost difficult to appreciate. This raises the two questions, "How were such dramatic improvements possible?" and "Why are the improvements limited to low voltage devices?" Their answers can be found with the aid of Figure 9-10, which shows the components of $r_{DS(on)}$ within a low or high voltage cell. In high voltage devices the resistivity of the n-epi layer must be large to stand off a maximum drain-to-source rating of 400 V, for example. Based on the percentage of the total on-resistance that each component claims, the resistance of the n-epi is by far the most costly in terms of on-state efficiency. To significantly improve the conductivity of high voltage devices, therefore, the resistance of the drain, r_D, must be reduced. (This is exactly the thrust of the GEMFET technology.)

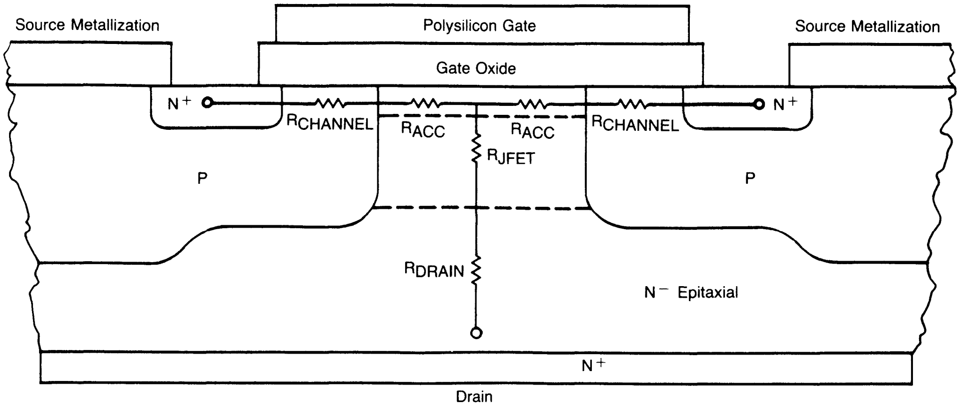


FIGURE 9-10 — THE COMPONENTS OF ON-RESISTANCE IN A HIGH- OR LOW-VOLTAGE MOSFET ARE CHANNEL RESISTANCE ($R_{CHANNEL}$), DRAIN RESISTANCE (R_{DRAIN}), JFET RESISTANCE (R_{JFET}), AND RESISTANCE OF THE ACCUMULATION REGION (R_{ACC}). LOWER ON -RESISTANCE VALUES ARE EASIER TO ACHIEVE IN LOW-VOLTAGE DEVICES, WHERE CHANNEL RESISTANCE MAKES UP ABOUT 70% OF THE TOTAL RESISTANCE IN A POWER-MOSFET CELL.

The lower maximum V_{DS} rating of low voltage devices allows using an n-epi with a much lower resistivity. Although there is no clear definition of what constitutes a "high" or "low" voltage device, at a maximum V_{DS} rating of about 200 volts, the significance of the drain resistance begins to dwindle and the importance of the channel resistance, the resistance of the accumulation region, and the JFET resistance begins to dominate. Especially for MOSFETs with voltage ratings less than 100 V, efforts directed at reducing these resistances pay big dividends.

These dramatic changes in the silicon area necessary to provide a given on-resistance are a bonanza for power MOSFET users. Designers now have the pleasant task of deciding how to use the device improvements. They may, for instance, choose to greatly minimize on-state losses by replacing first or second generation devices with second or third generation units that have the same die size. With the conductivity of a given chip size increasing nearly fourfold in some cases, designers can drastically reduce heat-sinking requirements and greatly improve system efficiency.

The second option open to the designer is to select replacements on the basis of their on-resistance or current ratings. This entails using a device with a much smaller die. Since much of the cost of a power transistor is associated with processing of silicon wafers, the use of smaller chips means lower component cost.

Comparison of On-Resistance

In 1986, TMOS IV was introduced with a series of products called E-FETs. This product had all the advantages of TMOS III products but ruggedness was added.

Much has already been said about greater conductivity per unit area of silicon being the strength of the newest generation of power MOSFETs. But an appreciation of just how far device designers have furthered their art in this respect comes only after a review of some of the $r_{DS(on)}$ versus die size data.

One very enlightening illustration (Figure 9-11) allows easy comparison of the typical on-resistance associated with a TMOS I, II, III and IV chip. The original TMOS MTP15N05 requires 150 x 150 mil^2 of silicon to yield a typical 135 MΩ on-resistance. With TMOS II technology, on-resistances are pushed down to 125 mΩ, with only 115 x 115 mil^2, about a 40% savings in silicon. Even with a 60% reduction in the original TMOS die area, TMOS III technology makes possible the added bonus of a 30% drop in $r_{DS(on)}$.

Almost as impressive as the performance gains is the rapid pace at which these changes are occurring. At the beginning of 1984, few realized that such dramatic improvements were possible, and virtually no one predicted the introduction of radically superior devices. Since each new generation delivered much greater perfor-

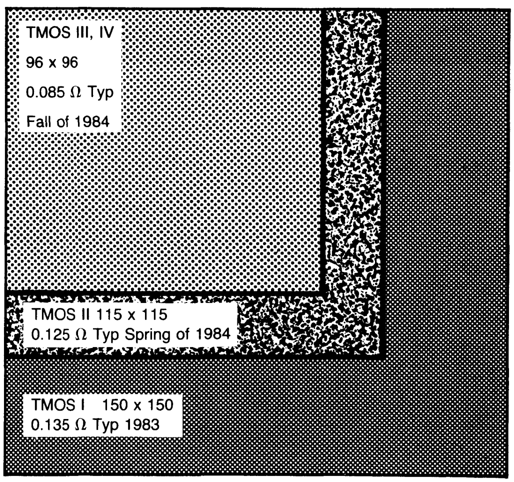


FIGURE 9-11 — FOR A GIVEN DIE SIZE, ON-RESISTANCE HAS FALLEN DRAMATICALLY DURING 1984

mance, the year was marked with the need for an almost continuous re-evaluation of the utility of low voltage power MOSFETs.

A second way to demonstrate the greater efficiency of the latest chip designs is to monitor case temperature rise in a typical application. This type of empirical evaluation is useful because it automatically includes the effect of practical considerations such as the influence that T_J has on $r_{DS(on)}$ (Figure 9-12). Since the intent of this exercise is to compare on-state losses in a typical application, a good test vehicle is a resistive load switched at a relatively low frequency (4 kHz). Table 1 lists die size information, typical $r_{DS(on)}$ values at 25°C, and steady state temperature readings during the 10 A, 14% duty cycle load test. The purpose of the table is not only to show that the case temperature rise predictably tracks the on-resistance data, but also to illustrate that even though the TMOS III die is much smaller, its power consumption is very moderate compared to the other devices. Advances of that proportion are normally restricted to the discovery of entirely new technologies and are not usually associated with improvements in existing techniques.

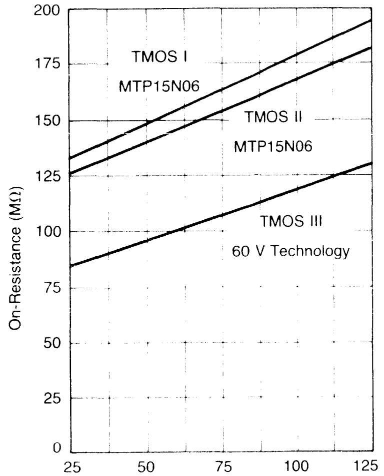


FIGURE 9-12 — THIRD GENERATION MOSFETs ALSO HAVE LOWER ON-RESISTANCE AT ELEVATED JUNCTION TEMPERATURES

TABLE 1 — ON-RESISTANCE COMPARISON OF FIRST, SECOND AND THIRD GENERATION MOSFETs

	TMOS I MTP15N06	TMOS II MTP15N06	TMOS III MTP14N06A
Die Area ($kmil^2$)	22.5	12.5	9.2
Typical $r_{DS(on)}$ @ 10 A, T_J = 25°C	135 MΩ	125 MΩ	85 MΩ
Case Temperature During 10 A Test	74°C	71°C	66°C
Normalized $r_{DS(on)}$ Die Area = 22.5 $kmil^2$	1.0	0.54	0.26

The last row of Table 1 offers another means of comparing device technologies. Those entries show the on-resistance of each device with all die sizes normalized to that of the TMOS I chip. Note that the third generation on-resistance is less than one third that of the first generation devices.

A final comparison involving one of the TMOS III devices and its bipolar namesake underscores the newly found strength of the low voltage MOSFET. The very popular MJE3055T (a 10 A, 60 V, 100 x 100 mil^2 bipolar) and the MTP3055A (a 12 A, 60 V, 96 x 96 mil^2 MOSFET) are the representatives of their respective technologies. (The MTP3055A is a one time deviation from Motorola's standard identification procedures. All other TMOS III units follow the standard numbering system but include an "A" suffix, e.g., MTP16N05A is a 16 A, 50 V device.) The first difference, one that may be surprising to some, is the lower on-voltage specification of the MOSFET. At a load current of 10 A, the MOSFET's maximum on-voltage rating is 1.5 V, and at a T_J of 125°C, the specification is 2.3 V. In comparison, the collector-emitter saturation voltage rating of the MJE3055T is 3 V, which is specified with a base drive of 3.3 A.

The other advantages of the MOSFET are numerous and familiar to most. They are greater speed, more extensive forward biased and switching safe operating areas, simpler and much more efficient drive, higher pulsed current rating, and greater ease of paralleling.

Several other parameters of power MOSFETs vary from generation to generation. Most notable are lower overall capacitance and junction-to-case thermal impedance. Because a change in either can alter circuit operation, performance comparisons between MOSFETs of different generations should address the effect of both these characteristics on design practices.

An added bonus; faster switching

Switching speeds, gate-charge requirements, and input capacitance — all closely related parameters — are improving. Although the switching-speed comparison is not quite as straightforward as the on-resistance comparison, the end result is good news for those concerned about switching losses and gate-drive efficiencies. For example, the switching speed of the MTP14N05A, a TMOS III device, is about 35% faster than that of the TMOS I version of the MTP15N05.

Changes in device design actually increase parasitic capacitance per unit of silicon area — about 35% for the same die size from TMOS I to TMOS III. However, because input capacitance (C_{iss}) is directly proportional to die size, die-size reductions of as much as 75% more than offset the effect of the greater parasitic capacitance per unit of area. Clearly then, the capacitance, switching speeds, and gate charge for a given current rating are much improved. Of the three parameters, the gate-charge requirements tend to be the spec that most clearly defines the device's switching speed, for it is independent of gate-drive impedance.

It's difficult to predict switching speeds using values of input capacitance (specified at a V_{DS} of 25 V) or curves that relate capacitance to V_{DS} or V_{GD}. The results could also be wrong. The simplest and most accurate way to compare potential switching speeds is to use gate-charge waveforms. If the gate drive is a constant-current source, you can use the expression Q = It to relate charge to switching time.

Figure 9-13 shows the gate charge waveforms of the MTP14N06A and the similarly rated TMOS I and II MTP15N06. Properly interpreted, the curves contain much information regarding potential switching speeds and input capacitances. The curves can be divided into three regions, each of which corresponds to a specific interval of the turn-on transition. The first interval consists of the initial ramp of the gate-to-source voltage. During this period the input capacitance is charging, but there are no significant changes in the drain current or drain-to-source voltage. Since I_G is constant in gate charge test circuits, the slope of the curve is inversely proportional to C_{iss} ($i = C\ dv/dt$). Note that the slope of the TMOS III curve in this region is the steepest, indicating relative ease of charging and lowest input capacitance.

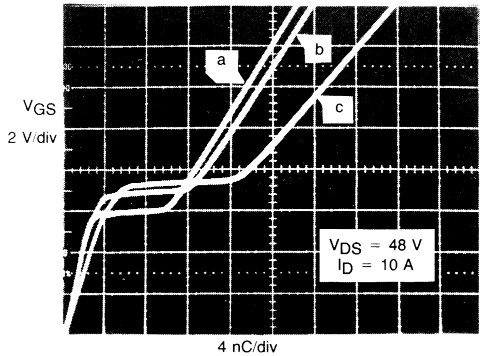


FIGURE 9-13 — GATE CHARGE REQUIREMENTS OF THE TMOS III MTP14N06A (a) AND THE TMOS II MTP15N06 (b) ARE MUCH IMPROVED OVER THAT OF THE TMOS I VERSION OF THE MTP15N06 (c)

During the second interval, the one in which the rise of the V_{GS} waveform falters and is stalled at a plateau, the drain voltage falls from the supply voltage to $V_{DS(on)}$. Such a large change in V_{DS} brings a large swing in V_{GD} and requires substantial charging of C_{rss} (or C_{gd}, the Miller capacitance). Therefore, the amount of time spent, or the amount of charge required, when moving through this region depends on the magnitudes of C_{rss} and the supply voltage. Here again, the TMOS III device delivers the best performance, needing only about 7 nC of gate charge compared to 8 and 11 nC for the TMOS II and I units.

Although switching is completed in Region 2, C_{iss} continues charging until the gate-to-source voltage reaches the desired $V_{GS(on)}$. As in the first region, the slope of the waveform in this third region indicates the size of the input capacitance. Interestingly, all waveforms are now rising more gradually than they did in the first region. The magnitude of C_{iss}, which is a function of the gate-to-drain voltage, is much higher now that the device is in the on-state, V_{DS} is relatively low and V_{GD} is positive.

Since the concept of required gate charge is based on a constant current gate drive, it applies directly to only those few gate drive topologies that can be modeled as constant current sources. Nevertheless, gate charge information does allow easy prediction of relative switching speeds, regardless of the type of gate drive.

As an example, consider driving a power MOSFET directly from a standard CMOS logic gate. The CMOS-MOSFET combination is especially important due to its simplicity and reduced parts cost. Based on the gate charge data in Figure 9-13, the drain voltage fall time of the MTP14N06A should be about 60% of that of the MTP15N06 — its TMOS I counterpart. That is indeed the case as shown in the turn-on and turn-off waveforms in Figures 9-14 a and b. The marked difference in transition times is directly attributable to the variation in gate charge requirements. The fact that TMOS III devices switch almost twice as fast as earlier units makes the use of a standard CMOS gate as a MOSFET driver more feasible.

This near doubling of switching speeds renews the possibility of using a standard CMOS gate as a MOSFET driver. Of course, although direct drive approaches are enticing, their associated switching losses limit operating frequency. A couple of assumptions and some recommendations from CMOS applications engineers allow a rough calculation of the operating frequency limits.

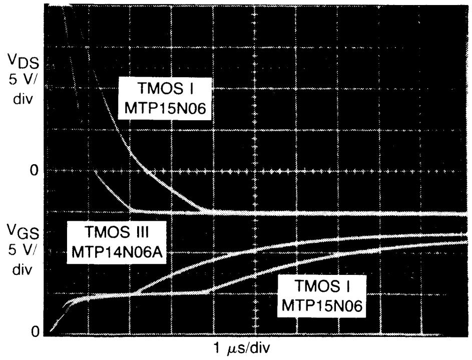


FIGURE 9-14a — GATE VOLTAGE RISE AND DRAIN-TO-SOURCE VOLTAGE FALL DURING TURN-ON.

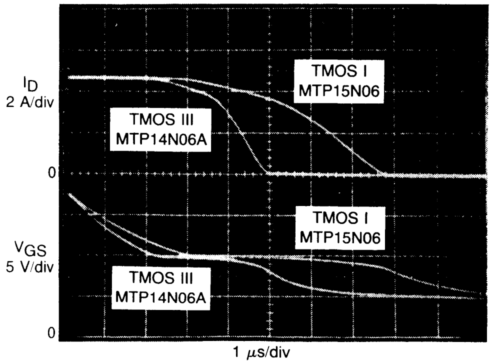


FIGURE 9-14b — GATE VOLTAGE FALL AND DRAIN CURRENT FALL DURING TURN-OFF.

FIGURE 9-14 — IN A COMPARISON OF FIRST AND THIRD GENERATION MOSFETs OF SIMILAR CURRENT RATINGS, TMOS III OUTCLASSES ITS PREDECESSOR BY SWITCHING NEARLY TWICE AS FAST WHEN DRIVEN BY A SINGLE CMOS GATE. IN THIS CASE A 1.5 kΩ SERIES GATE RESISTOR HOLDS PEAK GATE CHARGING CURRENT TO LESS THAN 10 mA.

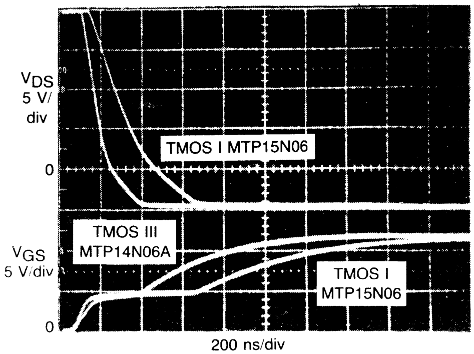


FIGURE 9-15a — GATE VOLTAGE RISE AND DRAIN-TO-SOURCE VOLTAGE FALL DURING TURN-ON.

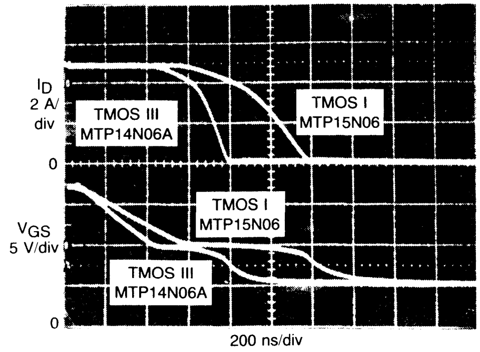


FIGURE 9-15b — GATE VOLTAGE FALL AND DRAIN CURRENT FALL DURING TURN-OFF.

FIGURE 9-15 — THE NEWEST MOSFETs, BECAUSE OF THEIR REDUCED GATE CHARGE REQUIREMENTS, CAN OPERATE AT HIGHER FREQUENCIES WHEN GATE DRIVE CURRENT IS LIMITED. HERE THREE PARALLELED CMOS INVERTERS ARE DRIVING THE MOSFET GATE THROUGH A SERIES RESISTANCE OF 100 Ω. EVEN AT FREQUENCIES APPROACHING 20 kHz, TOTAL TMOS III SWITCHING TIME IS ONLY 1% OF THE ENTIRE PERIOD.

To a large extent, switching speeds are strongly dependent on how hard one is willing to push the capabilities of the CMOS gate. The recommended maximum continuous output current is 10 mA per pin. Since these devices are not designed to drive highly capacitive loads such as a MOSFET gate, their pulsed current ratings are not specified.

Rigid adherence to the continuous specification results in the switching speeds shown in Figure 9-14. In this case, the TMOS I and TMOS III devices are driven from a single inverter of an MC14572, a hex gate IC. A 1.5 k series resistance between the output of the IC and the gate of the MOSFET limits peak charging and discharging to less than the 10 mA specification. Since the RMS value of the TMOS III gate current at 20 kHz is less than one milliampere, decreasing the magnitude of the series gate resistance is tempting.

Either paralleling CMOS gates, which must be from the same chip to guarantee good current sharing, or decreasing the value of the series gate resistance improves switching times. Figures 9-15 a and b illustrate the effect of both of these adjustments. With three inverters in parallel and a 100 Ω series resistance, transition times fall well below the 1 μs. Peak gate current rises to 40 mA, or about 13 mA per gate. This brief excursion beyond the 10 mA specification is harmless because of its short duration (<300 ns).

Translating these current and voltage fall times and the associated switching losses into an upper limit of operating frequency is a subjective exercise. Many factors, including available heatsinking, current and voltage magnitudes, on-state losses and duty cycle, dictate the amount of acceptable switching losses.

One rule of thumb is to limit the sum of the turn-on and turn-off transition times to less than 1% of the period. Using this criterion, the TMOS I device driven from a single CMOS inverter is limited to 1.3 kHz and the TMOS III equivalent is bounded by 2.4 kHz. With the three gates in parallel, 9 and 17 kHz are the upper limits.

Although faster switching and lower gate charge are normally desirable traits, they can be a mixed blessing. Since switching speeds may be almost twice as fast, the possibility of excessive voltage transients must be reconsidered. The design of all power MOSFET circuits should include rigorous monitoring of the drain-to-source voltage to preclude the possibility of excessive voltage transients during the turn-off transition. With the faster TMOS III devices this concern becomes more critical. Speeding the response time of the overvoltage protection circuitry may be needed if the device is switched more rapidly. When greater speeds are unnecessary, a higher gate drive impedance in the form of a resistance in series with the gate slows the switching transitions and simplifies the design of overvoltage protection circuitry.

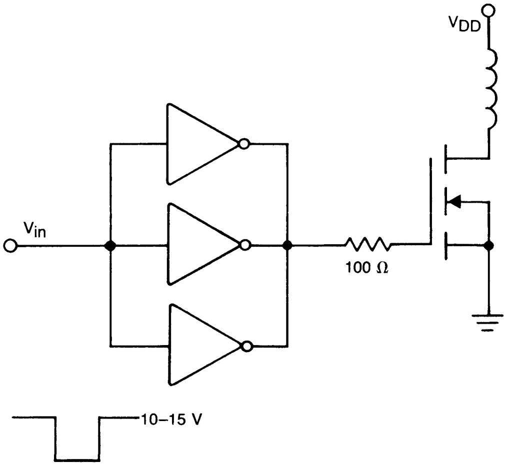


FIGURE 9-15c — THREE STANDARD CMOS INVERTERS OF AN MC14572 DRIVING A MOSFET GATE WITHOUT THE AID OF A BUFFER STAGE.

Thermal considerations are important

It's also important that you understand the thermal implications of the smaller die sizes of third-generation MOSFETs. A lower $r_{DS(on)}$ value per unit area increases the power-handling capability of a given die size, but the ability to dissipate power is still tied to the thermal resistance of the device. The newer, smaller devices — sometimes less than a third the size of their predecessors — have less area in contact with their cases, which increases their thermal resistance and decreases the power they can dissipate. It's therefore not a good idea to select replacements for first-generation MOSFETs solely on the basis of on-resistance and drain-to-source breakdown voltage.

Because junction temperatures directly affect long-term reliability, the T_J value is an important indicator of a transistor's exposure to stress. Where junction temperature is such a major concern, the junction-to-case thermal impedance also becomes critical. In fact, when it comes to minimizing junction temperature, the magnitude of the thermal impedance is almost as important as the value of on-resistance. The following example shows why.

Assume that Device A is a first generation MOSFET that is being replaced with Device B, a third generation unit. With the RMS value of the drain current held constant in each instance, a requirement of Device B is that its operating junction temperature must be less than or equal to that of Device A.

$$\text{If } T_{J1} = T_{J2}$$

$$\text{then } P_{D1}(R_{\theta JC1} + R_{\theta CA}) = P_{D2}(R_{\theta JC2} + R_{\theta CA})$$

$$\text{or } I_{RMS}{}^2 r_{DS(on)1}(R_{\theta JC1} + R_{\theta CA}) = I_{RMS}{}^2 r_{DS(on)2}(R_{\theta JC2} + R_{\theta CA})$$

If, for a moment, $R_{\theta CA}$ is assumed to be zero, the equation simplifies to:

$$(r_{DS(on)} \times R_{\theta JC})_1 = (r_{DS(on)} \times R_{\theta JC})_2$$

This equation states that if the case temperatures are held constant, which is assured when $R_{\theta CA} = 0$ (infinite heat sink); then equating the product of the thermal resistance and the on-resistance guarantees that the junction temperatures will be the same. Therefore, this product, referred to as the "resistance product," is a useful tool for comparing devices from different technologies or manufacturers.

The best way to elaborate on the concept of the resistance product is with a numerical example. Table 2 contains the ratings of Motorola's IRF531 and the MTP14N06A. On the basis of their similar resistance products, they might be considered to be direct replacements.

TABLE 2 — CHARACTERISTICS OF DEVICES WITH SIMILAR RESISTANCE PRODUCT RATINGS

	Device A	Device B
Device Type	IRF531	MTP14N06A
Technology	TMOS I	TMOS III
$r_{DS(on)}$	0.18 Ω	0.10 Ω
$R_{\theta JC}$	1.67°C/W	3.12°C/W
$P_{D(max)}$	75 W	40 W
Resistance Product	0.30°C/A²	0.31°C/A²

Let $I_{RMS} = 10$ A and $R_{\theta CA} = 3°C/W$

Then $P_{D1} = (100\ A^2 \times 0.18\ \Omega) = 18$ W $\qquad P_{D2} = (100\ A^2 \times 0.10\ \Omega) = 10$ W

$$\Delta T_{JC1} = P_{D1}R_{\theta JC1} = 18\text{ W} \times 1.67°\text{C/W} = 30°\text{C} \qquad \Delta T_{JC2} = P_{D2}R_{\theta JC2} = 10\text{ W} \times 3.12°\text{C/W} = 31°\text{C}$$

As expected, the junction to case temperature rise in each instance is nearly the same because the resistance products are so closely matched. But here the similarity ends due to the greater efficiency of the smaller chip. Depending on the magnitude of the case to ambient thermal resistance, the case to ambient temperature differential, T_{CA}, might vary considerably. When $R_{\theta CA} = 3.0°C/W$, then

$$\Delta T_{CA1} = 3.0°\text{C/W} \times 18\text{ W} = 54°\text{C} \quad \text{and} \quad \Delta T_{CA2} = 3.0°\text{C/W} \times 10\text{ W} = 30°\text{C}$$

For $T_A = 25°C$,

$$T_{J1} = \Delta T_{JC1} + \Delta T_{CA1} + T_A = 30 + 54 + 25°\text{C} = 109°\text{C} \quad \text{and} \quad T_{J2} = \Delta T_{JC2} + \Delta T_{CA2} + T_A = 31 + 30 + 25°\text{C} = 86°\text{C}$$

As the numbers illustrate, a constant resistance product does not always guarantee identical junction temperatures — it only forces the same ΔT_{JC}. In fact, if the case to ambient thermal resistance is high, junction temperatures may be quite different. However, the product can still be used as a comfort factor when designing in the newer power MOSFET generations. If the resistance product is held constant, the on-resistance of the more efficient device must be lower even though its junction to case thermal impedance is higher. Therefore, the newer device will dissipate less power for a given load current by virtue of its lower on-resistance. The lower power dissipation then results in a smaller case to ambient temperature differential and a lower junction temperature.

The preceding analysis ignores how T_J affects on-resistance, a very important consideration. The interdependence of the magnitude of $r_{DS(on)}$, T_J and power dissipation makes the resistance product an inexact tool. Also, the concept of the resistance product is based on the steady state thermal resistance and is, therefore, not appropriate for transient analysis. In spite of these inadequacies, the concept is useful for first order approximations, and it does illuminate some of the considerations that must be thought through to safely utilize the advantages of the new technology. For a more detailed thermal analysis, Motorola's AN569, "Transient Thermal Resistance — General Data and Its Use" is an excellent guide.

Fortunately for the designer, die size, steady state and transient thermal impedance, on-resistance, maximum allowable junction temperature and package limitations are all factored in when a device's maximum pulsed and continuous current ratings are assigned. Consequently, the MTP16N05A (which is a 16 A, 50 V device of the TMOS III vintage) is almost always a drop in replacement for any other 16 A, 50 V power MOSFET. The lower maximum on-resistance specification compensates for the smaller die and increased junction-to-case thermal impedance. Linear applications are an exception to this rule since the main concern in those circuits is power dissipation capability. Die area and thermal impedance must remain unchanged in those cases since improvements in on-resistance often do not reduce power dissipation.

Expanding Range of Applications

Already the expansion of the MOSFET into the power transistor market is outpacing the predictions of many. But the steady expansion is likely to turn into an explosion when the potential of the latest MOSFETs are fully appreciated. The new efficiency and economy of the low voltage MOSFETs foreshadows their dominance of that section of the power transistor market.

The automotive industry is among those likely to welcome a means of cost effectively controlling large continuous and pulsed currents. Specific applications involve the control of the many small motors found under the dash and hood and in the doors, the replacement of mechanical relays, and the switching of many lamps and solenoids. Interestingly, automakers often have little use for the MOSFET's most proclaimed attribute, its tremendous switching speed. Instead, they are impressed by its low on-voltages, extensive SOA, and modest gate drive requirements.

The use of MOSFETs for synchronous rectification is an example of an application that deserves reconsideration. Previously, MOSFETs had trouble competing with Schottky diodes, for example, because the MOSFET required much more silicon area to deliver the same performance. With the precipitous drop in per unit area on-resistance, the MOSFET is now much more competitive (Figure 9-16).

Several other applications come to mind, for example, solid state relays, hammer drivers for printers, telecommunications equipment, and output stages for programmable controllers. But the application primed for the introduction of such a switch is the brushless DC motor controller. As the cost of the semiconductor control circuitry continues to fall, the benefits of the electronically commutated motor — high efficiencies, linear speed/torque characteristics, long service life, the potential for speed control, etc. — will become more affordable.

Figure 9-17 illustrates one such control circuit. The design is tailored for a blower motor, so it is limited to single speed, unidirectional operation. After processing the signals from the three Hall effect sensors, the MC14028B (a binary to decimal decoder) and the six OR gates provide the proper logic sequence to control the output transistors. The relatively low commutation frequency is strictly a function of the motor speed, because the Hall effect sensors ultimately determine the firing sequence.

For simplicity, a P-channel MOSFET, an MTP5P20, was used as the power switch in the upper legs of the bridge. With a few drive circuit modifications, a PNP bipolar or even an NPN Darlington could also fill that socket. The most qualified candidate to serve as the low side switch is one of the third generation MOSFETs, again a 96 x 96 mil^2 chip. This device has a drain-to-source voltage rating of 200 V and a typical $r_{DS(on)}$ of only 0.3 Ω. A continuous motor load current of about 2 A causes negligible power dissipation in this device.

In the open loop system shown in Figure 9-17, motor speed is unregulated and is a function of the motor characteristics, the type of load and the magnitude of the DC supply voltage. Changing the supply voltage or using pulse width modulation allows regulation of motor speed. In this case, the best place for a speed control network is between the OR gates and the hex buffer.

There are three ways to control the effective motor voltage with pulse width modulation. The designer may PWM only the bottom three transistors, or only the top devices. The third option, pulse width modulation of both the upper and lower devices, also controls motor speed. The simplest approach is to pulse width modulate MOSFETs in the lower legs of the bridge. In that position, the MOSFET shows off several of its most advantageous attributes. It is fast, cost effective, efficient and very easy to drive.

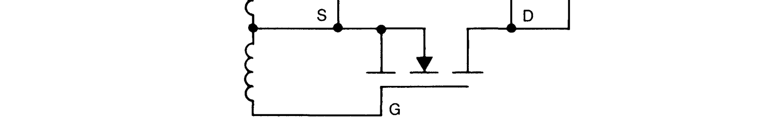


FIGURE 9-16 — USING POWER MOSFETs AS "SYNCHRONOUS RECTIFIERS" IN THE OUTPUT STAGE OF A SMPS CAN REDUCE RECTIFICATION LOSSES. WHEREAS MOSFETs ONCE REQUIRED TOO MUCH SILICON TO RIVAL THE SCHOTTKY DIODE NORMALLY USED, THE NEWEST MOSFETs ARE MUCH MORE COMPETITIVE.

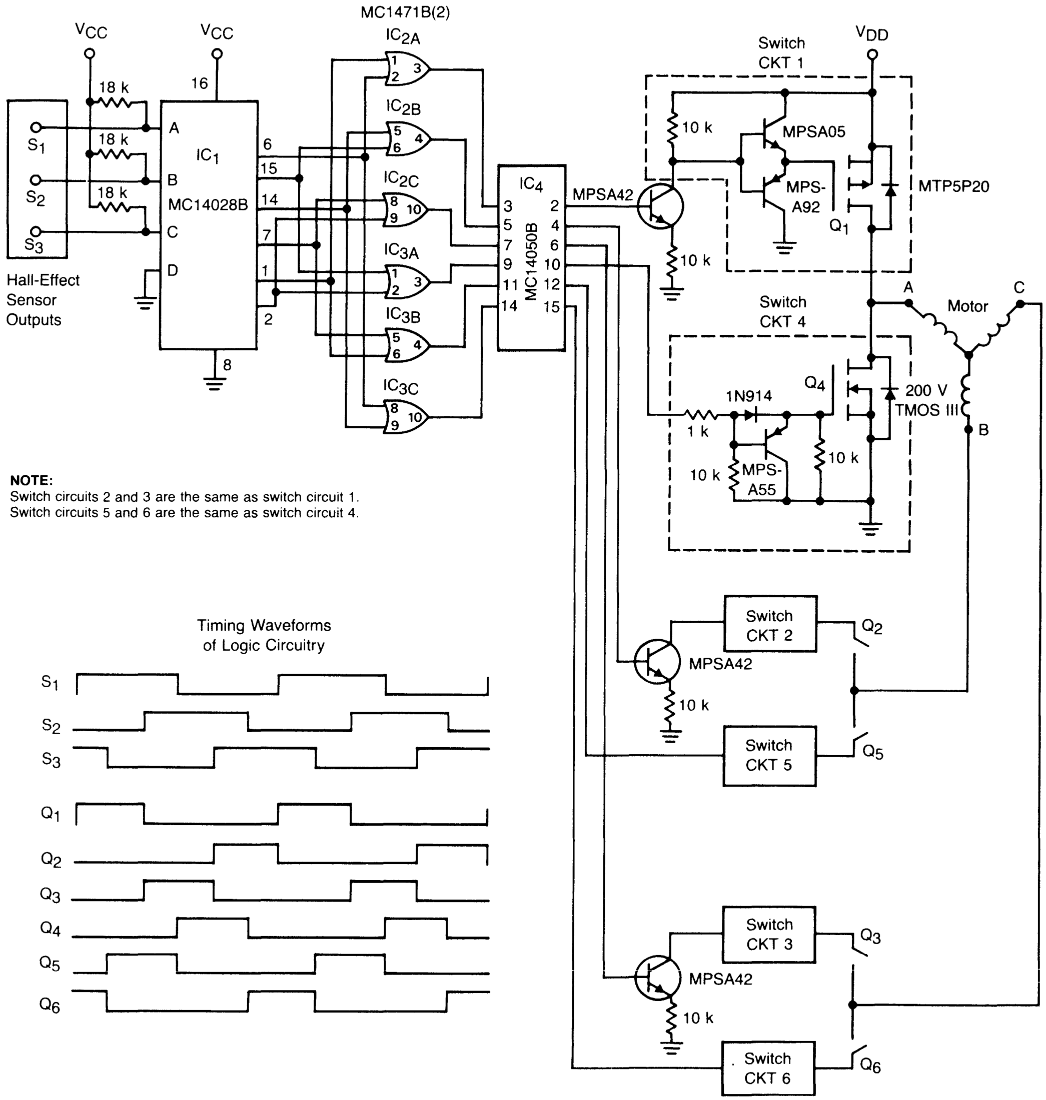


FIGURE 9-17 — TO SIMPLIFY THE DESIGN OF THIS BLOWER-MOTOR CONTROL CIRCUIT, THE UPPER LEGS OF THE BRIDGE EMPLOY A P-CHANNEL MOSFET FOR THE POWER SWITCH

Pulse width modulation of only the lower devices also circumvents one other potential problem. Even in these third generation devices, the MOSFET's diode is still sensitive to high dv/dt's (in the range of 1 volt per nanosecond) during its reverse recovery time. Use of a bipolar, in parallel with a discrete diode, is a tidy solution. The discrete diode doesn't mind the commutation stresses imposed by the fast switching MOSFETs. Also, rapid turn-on of the bipolars is unnecessary because their switching frequency, which is tied to the motor speed, is much lower. Therefore, the MOSFET's intrinsic diode need not endure the rigors of very high dv/dt.

Even Greater Expectations

Although recent performance improvements have been startling, they are only one point on a continuum of advances. Soon TMOS III will be superseded by an even more efficient version of the third generation product. The logical extension of certain changes in design philosophy from TMOS I to III suggest that even lower on-resistances are within reach. Photolithographic tools and techniques will also continue to improve, allowing yet finer cell geometries and even greater packing densities.

Another forthcoming change is the introduction of new packaging to compliment the greater current handling capability of the newest devices. Even now, moderately sized 50 and 60 V chips can cause excessive I^2R losses and high temperatures in the leads of the popular TO-220, TO-3 and TO-218 packages. Since the problems with the present packaging are associated with undesirable lead resistance and not insufficient power dissipation ratings, the solution entails enlarging the leads of the popular package types.

At the other end of the spectrum, smaller packaging will become more important. The trend toward surface mount technology and the development of small MOSFET die with low on-resistance meld together quite conveniently. The new chips are so efficient that packages such as the D-pack will have unconventionally high current capabilities for surface mount devices. In the surface mountable D-pack the 96 x 96 mil^2 TMOS III die can easily conduct 2.5 A of continuous drain current with less than one watt of power dissipation. Drain currents can reach at least 10 A under pulsed conditions.

The GEMFET — A New Option for Power Control

The world of power switching is constantly searching for the ideal switch. Such a switch would have infinite resistance in the off-state, zero resistance in the on-state, instantaneous switching times, and require zero input power to operate. In a real switching application, one must choose the device that most closely approximates the ideal switch for that particular application. The choice involves considerations such as voltage, current, switching frequency, drive circuitry, inductive loads, temperature effects, etc. Every switching device has its strong points and weak points and the designer is always forced to make trade-offs to find the best switch for a given situation.

For a solid state switch, the three characteristics that are most desirable are fast switching speeds, simple drive requirements and low on-state losses. In low voltage applications, the new generations of power MOSFETs have very low on-resistance and closely model the ideal switch. But in high voltage devices, comparatively high on-resistance still limits the MOSFETs efficiency. Furthermore, future advances in decreasing $r_{DS(on)}$ will become more difficult as on-resistances fall closer to the theoretical minimum, which is determined by the optimum cell geometry and the resistivity of the N-epi layer. Therefore, subsequent large reductions in $r_{DS(on)}$ of high voltage MOSFETs will require new technologies.

The GEMFET (Gain Enhanced MOSFET), also called an insulated gate bipolar transistor (IGBT), is the result of one such technological advance. It is a relatively new high voltage power semiconductor device with a combination of characteristics previously unavailable to the designer of power circuitry. Closely related to the power MOSFET in structure, this new device has forward voltage drop comparable to bipolars while maintaining the high input impedance and fast turn-on associated with the isolated gate of the MOSFET. Although turn-on speeds are very fast, current fall times of approximately 4.0 μs are quite slow, and may restrict the use of at least the first generation of these devices to lower frequency applications.

At switching frequencies below about 10 kHz, however, the GEMFET is an attractive alternative to the more traditional bipolars, power MOSFETs and thyristors. Compared to a standard thyristor, the GEMFET is faster and has a higher input impedance, better dv/dt immunity and, above all, gate turn-off capability. While some thyristors, e.g. GTOs, can be turned off at the gate, this requires substantial reverse gate-drive current, whereas, turning off the GEMFET requires only that the gate capacitance be discharged. On the other hand, thyristors generally have a slightly lower forward drop and a higher surge current rating than a comparable GEMFET.

In a comparison of drive requirements, the GEMFET clearly outperforms bipolar transistors. In a 10 A application, for instance, the bipolar requires 2.0 A of base drive (assuming a beta of 5.0) while the GEMFET requires only nanoamperes of gate current to remain in the "on" state. Without the large base-drive current required by the bipolar, the GEMFET gate-drive circuit can be much simpler and more efficient. Darlingtons also simplify drive requirements, but on-voltage is compromised in doing so.

Sometimes MOSFETs are used in low frequency applications because of their simple gate-drive requirements. In many low frequency, high voltage circuits, replacement of the MOSFET with a GEMFET improves efficiency or reduces the cost of the switch. Because their structures and gate-drive considerations are so similar, the change usually entails no significant circuit modifications. Substitution of a GEMFET with approximately the same die area dramatically improves on-state efficiency and current ratings.

If cost is a major concern, another option is to replace the power MOSFET with a GEMFET that has a smaller die area. The result can be a device with a similar current rating and comparable on-state losses. Except at higher frequencies, the cost/performance tradeoffs are substantially in favor of the GEMFET.

The GEMFET is suitable for high current, high voltage, low frequency applications because of its low forward drop and relatively long turn-off time. Appropriate applications for the GEMFET include motor drive circuits, automotive switches, programmable controllers, robotics, home appliances, machine tools, etc.

Device Structure

The GEMFET is very similar to the double-diffused power MOSFET. Simply by varying starting materials and by altering certain process steps, a GEMFET may be produced from a power MOSFET mask set. Figure 9-18 illustrates that the two structures are identical except for the P+ layer adjacent to the drain metalization. Additional current carriers in the form of holes are injected from the P+ substrate into the normally high resistivity N-epi layer and markedly reduce the on-voltage. The resulting four layer structure (P-N-P-N) allows current densities much greater than those attainable in power MOSFETs and comparable to those of bipolars.

Like the power MOSFET, the gate of the GEMFET is electrically isolated from the rest of the chip by a thin layer of SiO_2. Accordingly, the GEMFET is also a high input impedance device and exhibits the associated advantages of modest gate-drive requirements and excellent gate-drive efficiencies. The uniqueness of the GEMFET is that low on-voltages as well as high input impedances are now available in high voltage power semiconductors.

The symbols and equivalent circuits of the GEMFET and MOSFET are shown in Figure 9-19. Because of its four layer structure, the GEMFET lacks the parasitic drain-source diode common to nearly all power MOSFETs.

Device Characteristics

Output Characteristics

In the forward conduction mode, the GEMFET closely resembles a power MOSFET. The equivalent circuit is best modeled as shown in Figure 9-19 in which a low voltage, low $r_{DS(on)}$, N-Channel MOSFET is driving a PNP transistor in a compound configuration. The PNP device not only helps lower the effective $r_{DS(on)}$, but also enhances the device gain (transconductance) at high drain currents. Except at excessive drain currents or junction temperatures, the NPN device is considered to be a parasitic and does not influence circuit operation.

The output characteristics of a popular power MOSFET (MTP4N50) and a GEMFET (MGP20N50) of identical die dimensions and similar breakdown voltages are shown in Figures 9-20a and 9-20b. The two major differences between the curves are:

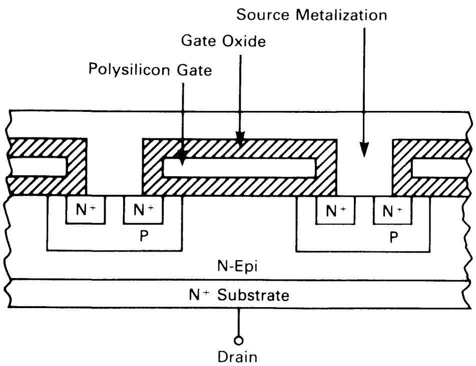


FIGURE 9-18a — CROSS SECTION OF TMOS CELL

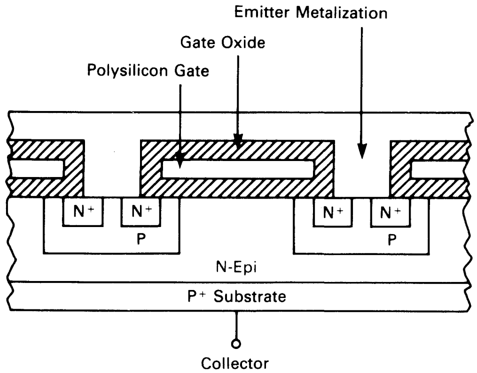


FIGURE 9-18b — CROSS SECTION OF GEMFET CELL

1 — The GEMFET has a much lower on-resistance at currents greater than 2.0 A.

2 — Before the GEMFET can conduct current, the P-N junction formed by the P+ substrate and the N-epi layer must be forward biased. Consequently, the GEMFET curves are offset from the origin by a diode drop, similar to SCRs or Darlingtons.

Figure 9-21 indicates that at 25°C the 20 A, 500 V MGP20N50 gives no hint of a propensity to latch at currents up to 62 A, which is much larger than the pulsed current rating of the MOSFET.

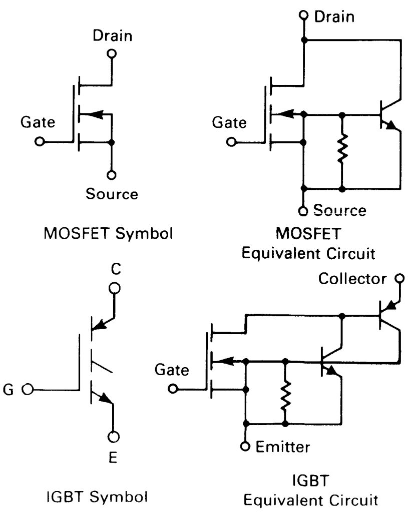


FIGURE 9-19 — MOSFET AND GEMFET SYMBOLS AND EQUIVALENT CIRCUITS

Switching Speeds

Presently, the feature that limits the GEMFET from serving a very wide range of applications is its relatively slow turn-off speed. While turn-on is fairly rapid, current fall times at turn-off can exceed 4.0 μs.

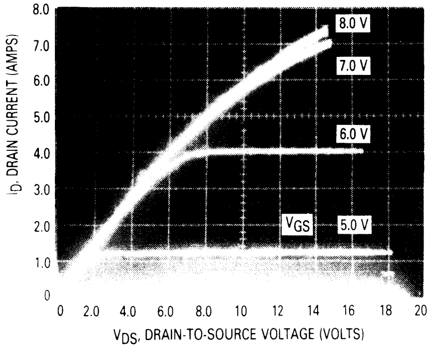


FIGURE 9-20a — OUTPUT CHARACTERISTICS OF POWER MOSFET (MTP4N50)

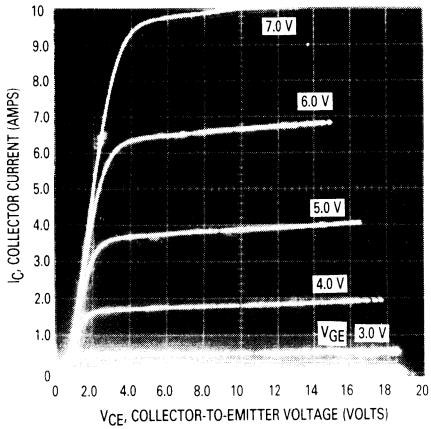


FIGURE 9-20b — OUTPUT CHARACTERISTICS OF GEMFET (MGP20N50)

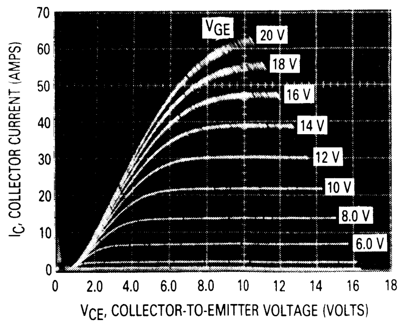


FIGURE 9-21 — OUTPUT CHARACTERISTICS OF GEMFET AT HIGH DRAIN CURRENTS

The turn-off of the GEMFET is rather slow because many minority carriers are stored in the N-epi region. When the gate is initially brought below threshold, the N-epi contains a very large concentration of electrons, consequently, there will be significant electron injection into the P^+ substrate and a corresponding hole current into N-epi.

As the electron concentration in the N-region decreases, the electron injection decreases, leaving the rest of the holes and electrons to recombine. The turn-off of the GEMFET should then have two phases: the injection phase where the drain current falls very quickly; and a recombination phase where the drain current decreases more slowly. Figure 9-22 shows the clamped inductive turn-off waveforms of the MGP20N50.

Although turn-off speeds are not impressive, this is the first generation of these devices and improvements in switching speeds can be expected. For GEMFETs, there is an $r_{CE(on)}$ — switching speed trade-off. Theoretically, turn-off times can be decreased without large increases in $r_{DS(on)}$ by controlling carrier lifetimes or by other proprietary methods.

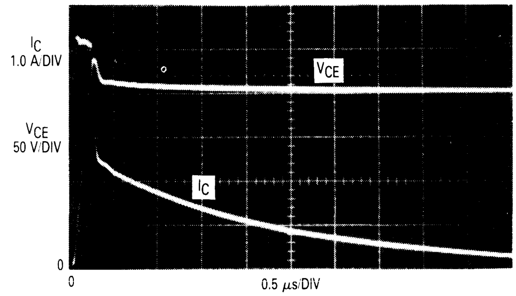


FIGURE 9-22 — CLAMPED INDUCTIVE TURN-OFF OF GEMFET

Even though MOSFETs are championed for their simple gate-drive requirements, at high operating frequencies sizable peak gate currents must be supplied to ensure rapid switching. Since this first generation GEMFET is, by comparison, much slower, the gate drive-impedance can be fairly high without affecting turn-off speeds. In the circuit shown in Figure 9-23, R_G was varied from 0 to 1.0 kΩ, but the current fall time essentially remained constant at 3.75 μs (Table 3).

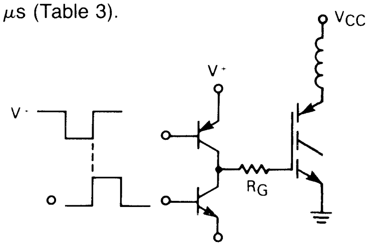


FIGURE 9-23 — CIRCUIT TO TEST VARIATIONS IN CURRENT FALL TIMES WITH CHANGES IN GATE DRIVE IMPEDANCE

TABLE 3 — Effect of Series Gate Resistance on Turn-off Speeds

Series Gate Resistance	0 Ω	50 Ω	100 Ω	200 Ω	500 Ω	1000 Ω
Collector Voltage Rise Time	140 ns	140 ns	150 ns	180 ns	350 ns	810 ns
Collector Current Fall Time	3.75 μs	3.75 μs	3.75 μs	3.75 μs	3.75 μs	3.75 μs

Comparison of On-State Losses

The most pronounced advantage of the GEMFET over the power MOSFET is its lower on-resistance. The $V_{DS(on)}$ of a high voltage MOSFET is fairly large and rises with increasing junction temperature and drain current. Conversely, the $V_{CE(on)}$ of a GEMFET decreases with increasing T_J and is not greatly affected by I_C. Figure 9-24 compares the on-voltages of the two technologies at various drain currents and at a T_J of 25°C and 100°C. Since the MOSFET does not have the GEMFET's offset voltage in its output characteristics, at low currents the MOSFET on-voltage is slightly lower. However, as the illustration suggests, at high currents and temperatures the difference is dramatic. For comparison, a bipolar transistor was also included in Figure 9-24. Its on-voltage is

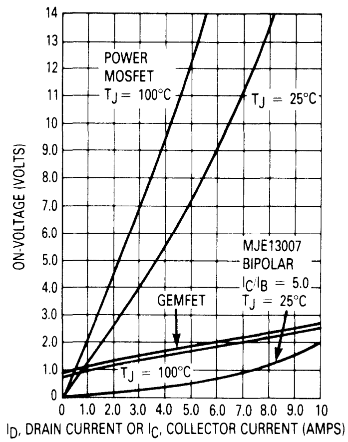


FIGURE 9-24 — ON-VOLTAGE versus DRAIN OR COLLECTOR CURRENT FOR A GEMFET, MOSFET AND BIPOLAR OF EQUIVALENT DIE SIZE

a function of the transistor's high current beta and the magnitude of the base current.

On-state efficiencies are not solely determined by on-voltages. Gate or base-drive currents are also contributing factors. Its high input impedance allows the GEMFET to rival the on-state efficiency of the bipolar transistor, even though its on-voltages are comparable to those of SCRs (one diode drop in addition to a bipolar saturation voltage). The bipolar device chosen for this comparison had a forced beta so low (about 5) at the desired collector current that the base current losses were important.

To illustrate the variation in the on-state efficiencies of each technology, a bipolar transistor, MOSFET and GEMFET were used as the switching element in an open loop PWM dc motor control circuit. The bipolar (MJE13007) was a 156 x 156 mil chip rated at 8.0 A, 400 volts. The 20 A, 500 volt GEMFET (MGM20N50) and the 4.0 A, 500 volt MOSFET (MTP4N50) had areas equivalent to a die size of 150 x 150 mil. To keep switching losses to a minimum, the frequency was held constant at about 90 Hz as the duty cycle was varied from 9% to 71%. Since

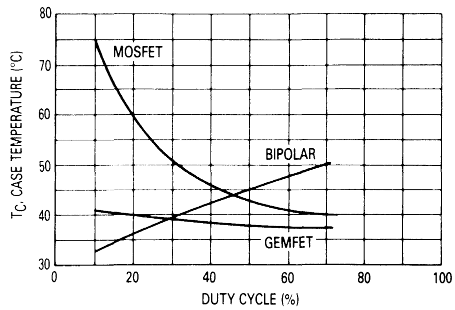


FIGURE 9-25 — ON-STATE EFFICIENCY COMPARISON — PULSE WIDTH MODULATION OF DC MOTOR

TABLE 4 — On-State Efficiency Testing: Pulse Width Modulation of DC Motor

	Pulse Width (ms)	Duty Cycle %	I_C(max) or I_D(max) (A)	Case Temp (°C)	Power Dissipation (W)	On Voltage (Volts)	V_{DS} or $V_{CE(pk)}$ (Volts)	Relative Power Out (Speed)	Relative Power In
GEMFET (MTM20N50)									
	8.0	71	0.75	37.2	0.69	1.0	1.75	78	2.0
	6.0	54	1.0	37.4	0.70	1.1	2.0	77	2.0
	4.0	36	1.6	38.5	0.75	1.1	2.5	73	2.0
	2.0	18	2.75	39	0.79	1.5	4.0	64	2.0
	1.0	9.0	4.50	40.9	0.86	2.0	6.5	49	2.0
TMOS (MTP4N50)									
	8.0	71	0.75	38.6	0.76	1.0	1.75	78	2.0
	6.0	54	0.80	42.1	0.91	1.3	2.25	77	2.0
	4.0	36	1.25	49.4	1.22	2.0	3.25	70	2.0
	2.0	18	2.25	62	1.77	4.5	6.50	48	2.0
	1.0	9.0	3.50	77.4	2.44	7.5	11.00	18	2.0
BIPOLAR (MJE13007)									
	8.0	71	0.80	49.7	1.24	0.1	0.8	82	140
	6.0	54	1.1	45.7	1.06	0.2	1.0	81	104
	4.0	36	1.5	40.7	0.85	0.2	1.5	78	72
	2.0	18	2.75	34.8	0.59	0.3	3.0	70	36
	1.0	9.0	4.5	32.6	0.50	0.5	5.0	59	20

T = 11.2 ms T_A = 21.2°C   f ≈ 90 Hz V_{DD} ≈ 14 V $R_{\theta HS}$ = 23°C/W a motor is a nonlinear load and conditions such as motor speed and back EMF change with pulse width, the results of the comparison (Table 4 and Figure 9-25) should be carefully interpreted.

The "relative power out" referred to in Table 4 is simply a measurement proportional to the motor speed and is inversely related to the saturation voltage. If the on-voltage is high, the potential across the motor is diminished and the speed is decreased. The "relative power in," a measure of forward base (or gate) current, is useful for comparing the required base or gate power necessary to control a five ampere load.

The following generalizations can be drawn from Table 4 and Figure 9-25:

1. Even though its on-voltage is very low, the bipolar is not the most efficient device at high duty cycles. The power consumed by the device due to its large base current is great enough to be reflected in an increase in case temperature. Because of the bipolar's low beta, the case temperature and power dissipation closely track the relative power in.
2. The bipolar invariably results in the highest motor speed for a given pulse width because its saturation voltage is always lowest.
3. For the MOSFET, high on-resistance, especially at higher currents and temperatures, influences the performance. As the duty cycle decreases, the motor speed and back EMF also decline. With the lower back EMF, the effective motor voltage is higher, allowing higher currents. The increasing current and on-resistance combine to elevate the case temperature at low duty cycles.
4. The case temperature of the GEMFET remains almost unchanged as conditions vary. Unlike the bipolar, its input power is very small and does not significantly affect the power dissipation at high duty cycles. At lower duty cycles and higher currents, the GEMFET on-voltage is much lower than the MOSFET's. Again, the result is cooler case temperatures.

While the GEMFET looks quite respectable in this comparison, the peak current chosen influences the relative efficiencies. If the motor supply voltage had been increased to obtain larger peak currents, the comparison would have been even more in favor of the GEMFET. The MOSFET would have performed more poorly due to its I_D-$r_{DS(on)}$ relationship, and the bipolar's base drive losses, due to forced betas' less than 5.0, would further reduce its efficiencies at large pulse widths.

Switching Losses

The present maximum operating frequency of the GEMFET is limited by its turn-off speed. Defining a specific upper limit could be misleading because the frequency limitation depends on heat sinking, drain current, drain supply voltage, gate-drive impedance, and drain-source flyback voltage. To set a benchmark for a specific set of conditions, the following test circuit and procedure was developed to compare the switching efficiencies of a GEMFET (MGP20N50), MOSFET (MTP4N50), and bipolar (MJE13007).

In the test procedure, the independent variable was switching frequency, which was varied by changing the timing capacitor C1 in the test circuit shown in Figure 9-26. By adjusting potentiometer R1 and by properly sizing the inductive load, the load current waveform was fixed to a 25% duty cycle and a peak of 5.0 A.

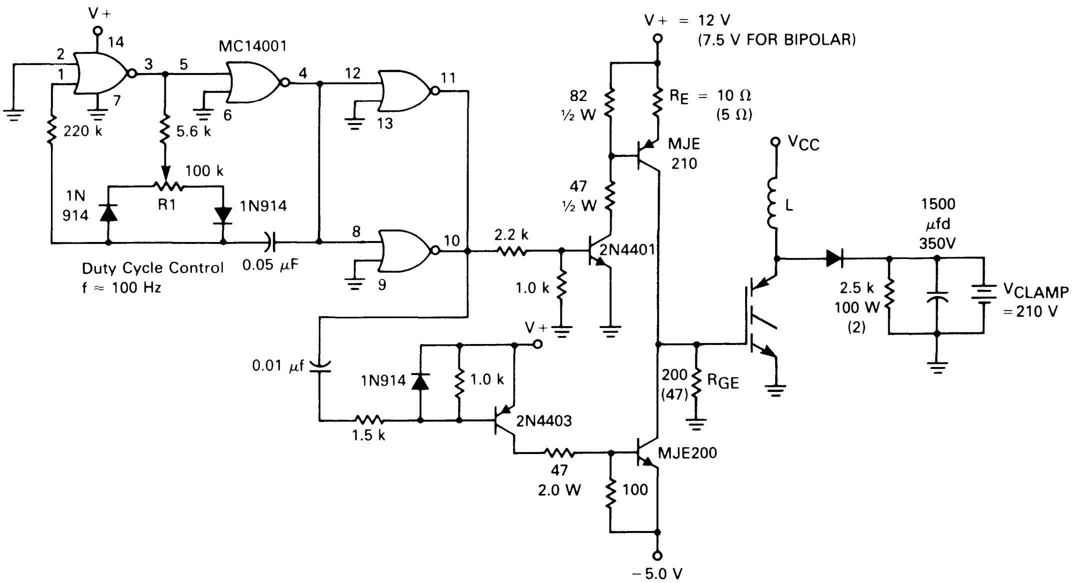


FIGURE 9-26 — CIRCUIT TO COMPARE SWITCHING EFFICIENCIES OF GEMFET, MOSFET AND BIPOLAR

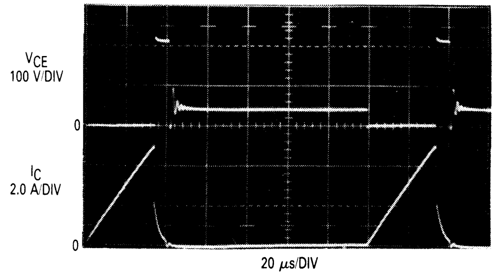


FIGURE 9-27a — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — GEMFET

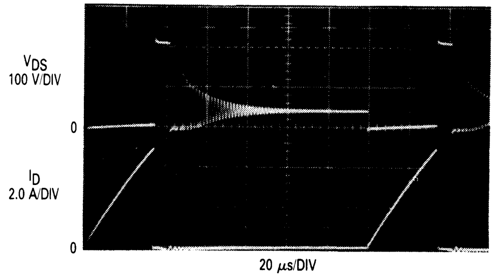


FIGURE 9-27b — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — MOSFET

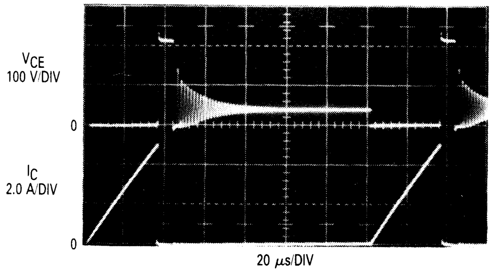


FIGURE 9-27c — CLAMPED INDUCTIVE SWITCHING WAVEFORMS AT 7.0 kHz — BIPOLAR

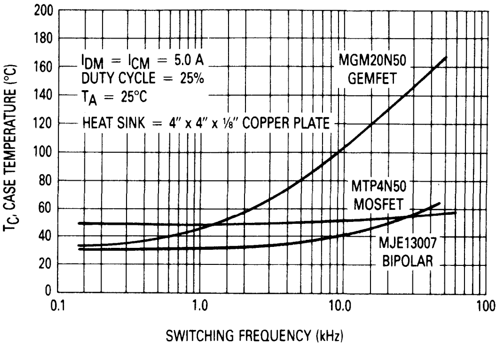


FIGURE 9-28 — COMPARISON OF CASE TEMPERATURE versus FREQUENCY FOR A GEMFET, MOSFET AND BIPOLAR

For the MJE13007, the forced beta of 5.0 required a base current of 1.0 A. Turn-off of all three types of devices was initiated by clamping the base (or gate) to −5.0 volts. The oscillograms in Figure 9-27 show the drain (or collector) current and drain-source (or collector-emitter) voltage of each device at 7.0 kHz.

Again, the test results were quite predictable, and the case temperature versus frequency for this specific case is plotted in Figure 9-28. The efficiency of the heat sink, in this instance a 4½″ x 4½″ x ⅛″ copper plate ($R_{\theta CA}$ = 5°C/W), markedly influences the temperature rise results. A larger or smaller heat sink would have decreased, or increased, the noted temperature differences. The testing was restricted to lower frequencies because above 40 kHz secondary effects began to influence and distort the comparison.

The GEMFET switching losses rose rapidly with frequency, illustrating its high-frequency limitations. By comparison, the bipolar's case temperature increased only slightly while the MOSFET proved its high frequency capability with virtually no case temperature rise.

Thermal Resistance, $R_{\theta JC}$

As expected, GEMFETs and power MOSFETs produced from the same mask set have very similar junction-to-case thermal resistances. $R_{\theta JC}$ of a power MOSFET can be determined by testing for variations in one of the following temperature sensitive parameters, or TSPs:

1. Drain-source diode on-voltage
2. Gate-source threshold voltage
3. Drain-source on-resistance

All previous thermal resistance testing of the TMOS power MOSFET was based on the temperature dependence of the on-voltage of its drain-source diode. For the MTP4N50, the results were typically about 0.79°C/W. Because the GEMFET has no parasitic diode, this method was inappropriate for the MGP20N50. Instead, $R_{\theta JC}$ of the GEMFET was determined by using a second circuit that detects variations in the gate-source threshold voltage due to changes in T_J. Before testing the GEMFET, correlation between the two test methods was obtained by comparing the results of testing the MOSFET in each circuit. By testing for variations in threshold voltage, the $R_{\theta JC}$ of the MTP4N50 and the MGP20N50 were both typically 0.67°C/W. This suggests that the two methods are in fairly close agreement and that the thermal resistances of a MOSFET and GEMFET of equal die area are essentially the same.

Safe Operating Areas

Important ratings of any solid state switching element are its Safe Operating Areas. For the GEMFET, these include its Forward Biased SOA, or FBSOA, and Reverse Biased SOA, or RBSOA. Since non-destructive fixtures were used to determine both of these SOA limitations, an entire curve could be drawn with each device tested. With this capability, device trends readily became apparent.

Figure 9-29 shows the dc FBSOA limits of an MTP5N40 and an MGP20N50. Even though the curves are quite similar, at either end there are significant differences. At

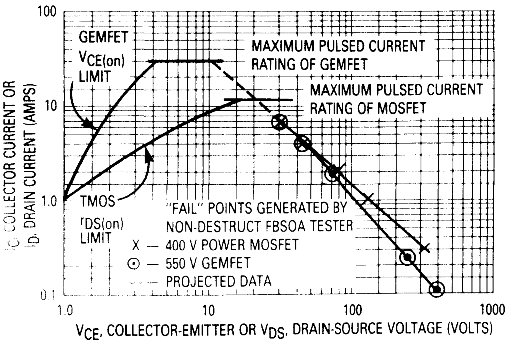


FIGURE 9-29 — COMPARISON OF FBSOA CURVES OF A 400 V MOSFET AND 550 V GEMFET OF EQUAL DIE AREA

high voltages and low currents, the GEMFET's curve begins to roll off somewhat like the curve of a bipolar that is approaching a second breakdown limitation. This is not surprising since the parasitic PNP bipolar is instrumental in sustaining its unique mode of current conduction.

At the low voltage, high current portion of the FBSOA curve, the effect of on-resistance is evidenced in two different ways. First, at very low voltages, on-resistance can limit the current. This is simply a manifestation of Ohm's Law and does not indicate a stress-related limit. As Figure 9-29 suggests, the wide difference in on-resistances between MOSFET and GEMFET is reflected in the on-resistance limit of their respective FBSOA curves. Second, a lower on-resistance also increases a device's peak-current rating by virtue of its more efficient current conduction. This limit is stress related and also is illustrated for both devices in Figure 9-29.

An RBSOA rating details the maximum drain-current and drain-source voltage stress allowable during clamped inductive turn-off. If a device undergoes second breakdown at some combination of V_{DS} and I_D that is within its pulsed power dissipation capability, an RBSOA derating curve is in order. In essence, an RBSOA derating indicates that a device may fail due to localized hotspotting even though its average junction temperature is within its $T_{J(max)}$ rating. Second breakdown of the MOSFET only occurs when its maximum junction temperature is exceeded. Therefore, operation of the MOSFET is only limited by its $T_{J(max)}$, I_{DM} and V_{DSS} ratings.

As for the GEMFET, special RBSOA considerations are necessary to ensure optimum reliability. Junction temperature and turn-off speed are especially noteworthy parameters since they can dramatically alter the GEMFET RBSOA capability. With all other conditions fixed, an increase in T_J can lessen the reverse-biased safe operating area if the drain current is high. At turnoff, lower gate-drive impedances are also more stressful, as explained below.

Figures 9-30 and 9-31 outline the operating limits of typical MGM20N50 (20 A, 500 V GEMFET in a TO-204 Package). The figures are typical of the devices used in this evaluation and do not represent a guaranteed RBSOA rating. A more thorough evaluation is being conducted to provide guaranteed curves for the data sheet. The gate-drive circuit used (Figure 9-32) allows adjustment of the gate-drive output impedance at turn-off simply by varying R_{GE}.

To generate each "fail" point, a resistor, collector current and temperature were selected, then the magnitude of the clamp voltage was increased until the device either dissipated the coil's energy in avalanche or entered second breakdown. If the test device experienced a rapid collapse of its collector-emitter voltage (which is charac-

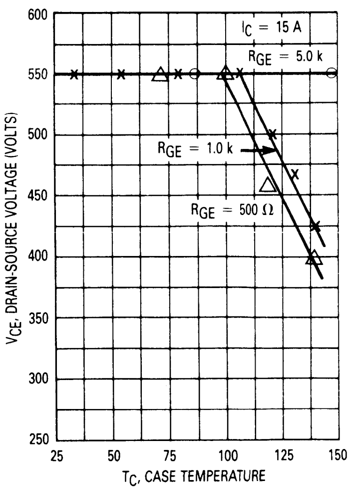


FIGURE 9-30 — EFFECT OF GATE DRIVE IMPEDANCE AND CASE TEMPERATURE ON GEMFET RBSOA

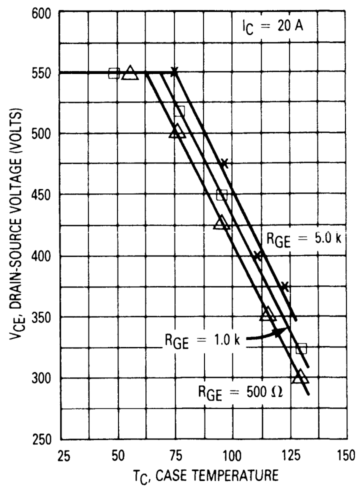


FIGURE 9-31 — EFFECT OF GATE DRIVE IMPEDANCE AND CASE TEMPERATURE ON GEMFET RBSOA

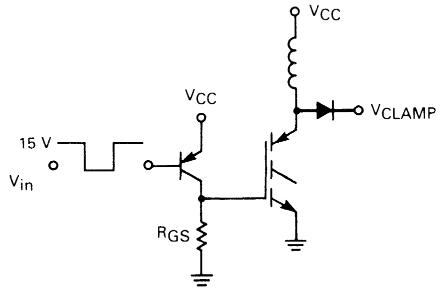


FIGURE 9-32 — GEMFET RBSOA GATE DRIVE CIRCUIT

teristic of second breakdown), the non-destruct fixture rapidly (150 ns) removed energy from the DUT before its die suffered damage.

Interestingly, the failure mechanism is not simply power related, i.e., slower switching speeds and greater crossover times tend to increase its RBSOA. This is clearly shown in the turn-off waveforms of Figures 9-33a and 9-33b. Even though the device enjoys lower switching losses with an R_{GE} of 51 Ω, its RBSOA is lessened. This phenomena may be due to a very rapid MOSFET turn-off that places a dv/dt stress on the PNP bipolar.

If the GEMFET is turned off more slowly, the MOSFET carries a greater portion of the load current and lessens the strain on the bipolar during this critical portion of the switching cycle.

The GEMFET is poised to alter the options available to power circuit designers. While its slow turn-off speeds limit its potential applications at this point, the GEMFET's low $r_{CE(on)}$ and high input impedance make it the technology of choice for many applications requiring low frequency switching.

An Application of the GEMFET

An ideal example of a GEMFET application would highlight its three strongest features. It would require a switch with high blocking voltage capability, a large current rating and simple drive requirements. The switching element in an automotive electronic ignition control system is one of many such applications in which the GEMFET deserves consideration as an alternative to the switches currently in use.

Presently, high voltage Darlingtons are the most commonly used switch in automotive ignition systems. The advantage of using a GEMFET as its replacement is the elimination of the Darlington's base drive circuitry. Since the required switching frequency is below 1.0 kHz, the GEMFET's high input impedance and low drive requirements make it ideally suited to be driven directly from CMOS logic.

When the transistor — whether it be a Darlington, GEMFET, or Power MOSFET — turns on, the primary current ramps up to 3.0 to 7.0 A (6.0 A peak for this exercise). At turn-off, the inductive kick, or flyback voltage, is allowed to rise as high as practical to produce the very high transformer secondary voltages (20 kV) required to generate a spark. In the present systems that employ high voltage Darlingtons, voltage is often clamped to about 400 V by a zener placed from collector to base. As soon as the collector-base voltage exceeds the nominal zener voltage, the zener supplies the base current to the Darlington, turning it on and thus clamping V_{CE} to V_Z. In this mode the zener carries only a small fraction of the load current and its power dissipation rating can be sized accordingly (a collector-emitter zener must carry the full peak primary current). On the other hand, the transistor is acting as its own voltage clamp and must dissipate the energy contained in the inductive kick.

When a GEMFET is used in place of a Darlington, the same clamping scheme can be used. If the zener is placed across the drain and gate terminals, any zener avalanche current soon charges the GEMFET's input capacitance and initiates turn-on. With this clamping method, the GEMFET experiences the same high power dissipation interval as the Darlington. One additional component is needed in the GEMFET version of the clamp. A diode in series with the zener is needed to block any current that would otherwise flow if the gate were more positive than the collector [high V_{GE}, low V_{CE}].

Since the GEMFET performed very well in this evaluation, the question arises as to the applicability of the power MOSFET in this same circuit. Again the comparison is of the MGM20N50 and the MTM4N50, which are a GEMFET and a MOSFET of identical die size. The first consideration is that a peak drain current of 6.0 A exceeds the MOSFET's 4.0 A continuous rating. This in itself is not a problem, but thermal limitations are possible at higher duty cycles and elevated case temperatures.

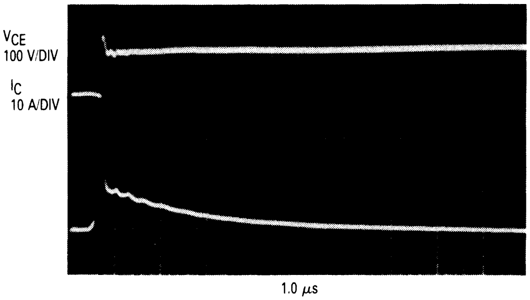


FIGURE 9-33a — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF MGM20N50 – R_{GE} = 51 Ω

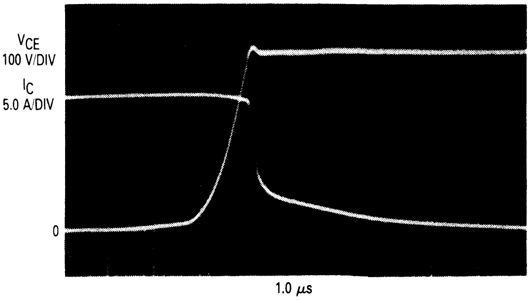


FIGURE 9-33b — CLAMPED INDUCTIVE TURN-OFF WAVEFORMS OF MGM20N50 – R_{GE} = 510 Ω

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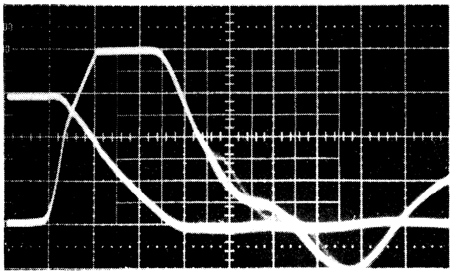

FIGURE 9-34 — AN AUTOMOTIVE ELECTRONIC IGNITION SYSTEM IS AN APPLICATION FOR WHICH THE GEMFET SHOWS GREAT PROMISE. THE SIMPLE GATE DRIVE CIRCUITRY (b) IS ONE OF THE MAJOR ADVANTAGES IN THIS SYSTEM. BECAUSE OF THE COLLECTOR-TO-GATE ZENER, CURRENT FALL TIME IS DICTATED BY THE AMOUNT OF ENERGY STORED IN THE INDUCTIVE KICK.

Although the greatest stress on the switch occurs during the clamping of the inductive kick and generation of the spark, that clamping interval does not necessarily contribute more to the average power dissipation than does the interval in which the switch is on and current ramps up in the primary. This is especially true of the power MOSFET due to its high $r_{DS(on)}$.

The difference between the on-resistance of the MOSFET and the GEMFET becomes evident during the monitoring of the case temperatures. Under the same conditions (using a Thermalloy heat sink #6016B), the GEMFET's T_C is 37°C, while the MOSFET's is 59°C, representing a 2.5 W difference in power dissipation.

A second problem, again related to the MOSFET's higher $r_{DS(on)}$, also complicates its use in an electronic ignition control system. Due to the limited battery potential, especially during engine startup in very cold weather, the $r_{DS(on)}$ of the switch must remain low so as not to limit the peak current in the primary of the ignition coil. Therefore, the 1.5 Ω maximum specification for the MTM4N50 is probably too high for this application. In this test the "battery" voltage must be increased by about 30% to achieve the same primary current that the GEMFET conducted.

In addition to its higher on-state efficiency, the GEMFET can also offer a cost advantage over the power MOSFET. A large portion of a power transistor's cost is associated with its die area. Since the GEMFET can operate at current densities at least five times that of a high voltage MOSFET, significant savings can result from using a GEMFET with a smaller die size.

Chapter 10: Relative Efficiencies of TMOS and Other Semiconductor Power Switches

The prime requisite of a power switch (semiconductor or mechanical) is to transfer the maximum power to the load. A comparison of the relative efficiencies of various power semiconductor switches will be demonstrated with three different switching loads: resistive, inductive and a dc motor.

There are four factors that contribute to the system losses: input or driving power losses due to the input current and/or voltage required to turn on the device; saturation or static losses when the device is ON (a product of the on-voltage and current); switching or dynamic losses that result from the transition times when the device is turned ON and OFF; and off losses due to the product of leakage current and the power supply voltage. Generally off losses are by far the least significant since modern semiconductors have low leakage currents and can be ignored in system loss calculations.

The variation of input power losses can be substantial for the various semiconductors. As an example, a high voltage switching transistor would have relatively low current gain and, consequently, requires relatively high input base current to turn it fully on whereas a MOSFET, with its extremely high static input impedance, would require very little input power to turn it on.

The output power losses are illustrated in Figure 10-1. It is apparent that the switching losses, depending on the switching frequency and transition times, can contribute a large share of the total system losses. Thus, for high frequency applications, where switching losses predominate, fast switching devices should be used. Conversely, for low switching frequency applications, low on or saturation losses are more important.

Power MOSFETs are recognized as being extremely fast switching devices, but are they more efficient than bipolars in all or many switching applications? The answer is — it depends. Efficiency is a measure of dissipation,

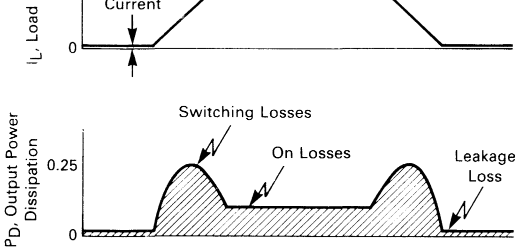

FIGURE 10-1 — NORMALIZED SWITCHING WAVEFORMS FOR A RESISTIVE LOAD

which, in switchmode circuits, consists primarily of switching losses, both turn-off and turn-on, and saturation losses. Since switching losses are a function of the switching frequency and saturation losses are relatively constant, a point is reached in the frequency spectrum where one loss predominates over the other. Thus, in low frequency applications, devices with low saturation or on-voltage would show lower losses as measured by the device case temperature, and at high frequencies, the fast switchers would run cooler. This applies to all types of semiconductors, be they power MOSFETs, Bipolars, Darlingtons, GTO (Gate Turn Off) SCRs or a GEMFET (Gain Enhanced MOSFET) (A standard SCR can also be used wiith commutating circuitry; however, it is not included in this evaluation due to the additional circuit requirements and associated costs.)

Temperature Testing High Voltage Devices TMOS versus Bipolar Switchmode I and III

A simple way of measuring the relative efficiencies of the DUTs, one that measures the total device losses, is by measuring the case temperature. This is accomplished by attaching a thermocouple to the mounting flange of a TO-204 (TO-3) package or tab of a plastic (TO-220) package. The first evaluation was to compare the switching efficiency of three high voltage switching transistors — the 2N6545, one of the first transistors characterized for switchmode applications, called Switchmode I, (SMI); the MJ16004, a state-of-the-art Switchmode III transistor (SMIII) designed for higher frequencies; and the power MOSFET MTM5N40. All these devices are of similar die size and have similar ratings (Table 1). All were tested with nearly identical loads and were driven by the same test circuit, except that the forward input current (I_{B1}) and input resistance were scaled for the particular DUT). Reverse current or turn-off current was derived from the same input clamp transistor switch and the magnitude of this current (I_{B2}) was dictated by the stored charge of the device under test (DUT).

Since the input drive for both turn-on and turn-off can be chosen to optimize the swıtching speed, the drives selected were those generally shown on the data sheet; i.e., forced gains of 5.0 and 7.0, respectively, for the 2N6545 and the MJ16004; off-bias voltages of −5.0 V and −2.0 V for the above; and a gate-drive of greater than 10 V for the MTM5N40.

Resistive loads were chosen for the temperature rise-versus-frequency test since the load current could be maintained at a constant 2.5 A as the frequency was varied. Recognizing that the "real world" load is usually inductive and that inductive turn-off switching losses are greater than turn-on due to the rectangular load line, a single frequency (75 kHz) inductive test was also run. Due to the different on-voltages and turn-off times for bipolar and MOSFET devices, the load inductances had to be slightly different to achieve the same peak collector (drain)

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TABLE 1 — Specifications of DUTs

	SMI 2N6545	SMIII MJ16004	TMOS MTM5N40
Die Size (Area)	160x160 mil (25600 mil²)	157x175 mil (24649 mil²)	126x182 mil (22932 mil²)
I_C, I_D	8.0 A	5.0 A	5.0 A
V_{CEO}, V_{DSS}	400 V	450 V	400 V
$V_{CE(sat)max}$, $V_{DS(sat)max}$	1.5 V @ 5.0 A	2.5 V @ 3.0 A	2.5 V @ 2.5 A, $r_{DS(on)}$ max = 1.0 Ω
$V_{CE(sat)typ}$, $V_{DS(sat)typ}$	0.3 V	0.3 V	2.2 V @ 0.9 Ω
$h_{FE(min)}$, $g_{fs(min)}$	7.0 @ 5.0 A	7.0 @ 5.0 A	2.0 mhos @ 2.5 A

currents for a normalized test. For the 75 kHz test, the peak ramp current of about 3.0 A peak was achieved with inductances of 32 μH and 27 μH respectively when V_{CC} and V_{DD} were +16 V.

The temperature rise test fixture (Figure 10-2) consists of a clocked, three-phase counter sequentially driving the three respective switching circuits; thus, each device under test is driven at a 33% duty cycle. However, at high frequencies (low on times), DUTs with greater storage times will effectively be powered for longer duty cycles and therefore have greater saturation losses contributing to the device temperature rise. As an example, at 150 kHz (period of 6.7 μs) the 33% dc drive on-time of about 2.2 μs would result in about 48% power on-time with only 1.0 μs of storage time.

The clocks for this system, one for the resistive load case and the other for the inductive load, consist of two CMOS gate configured RC astable multivibrators. Switchable timing capacitors set the frequencies for the resistive load at 5.0, 25, 75 and 150 kHz respectively; the inductive load clock is set at a fixed frequency of 75 kHz. The output of these MV's clock the MC14002 Octal Counter Divider connected as a three-phase ring counter whose respective emitter-follower, positive-going outputs control the three virtually identical drivers.

Forward base current for the bipolar transistors is set by turning on the NPN transistors Q2 and Q7 and the following PNP transistors Q3 and Q8. To minimize storage time, Q3 and Q8 are fashioned as constant-current generators, supplying the base currents to the 2N6545

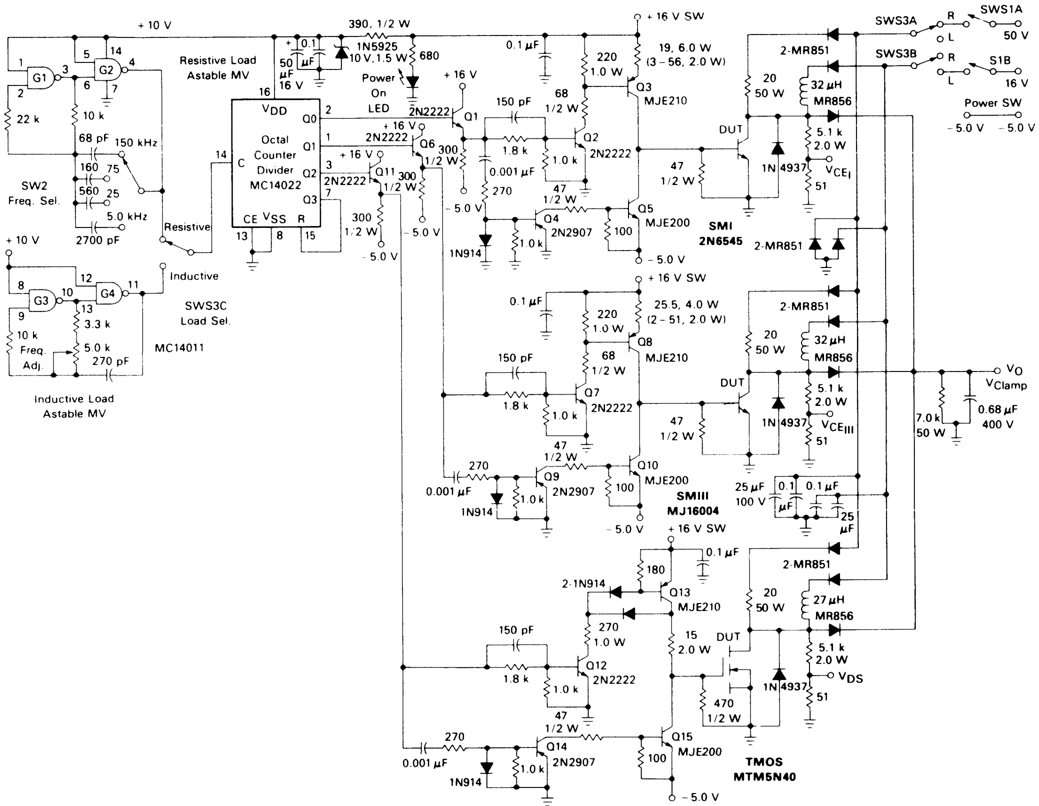

FIGURE 10-2 — TEMPERATURE RISE FIXTURE SWITCHMODE I, SWITCHMODE III, TMOS

($\beta_F = 5.0$, $I_{B1} = 600$ mA) and MJ16004 ($\beta_F = 7.0$, $I_{B1} = 430$ mA) for the inductive load current of 3.0 A peak. Forward gate voltage for the power MOSFET is generated by turning on PNP transistor Q13 (Baker clamped to minimize t_s) and thereby applying nearly the full 15 V rail voltage to the gate. The 15 ohm current limiting resistor provides the low source impedance for quickly charging (and thus switching) the MOSFET input capacitance C_{iss}.

Reverse bias voltage $V_{BE(off)}$ or $V_{GS(off)}$ for rapidly turning off the DUTs, are derived by differentiating the input pulse with the resistor-capacitor networks in the base circuits of Q4, Q9 and Q14. The resulting negative going pulses, which are coincident with the trailing edge of the input pulse, then turns on the following respective PNP transistors Q4, Q8 and Q13 for about 3.0 μs. These transistors then turn on NPN transistors Q5, Q10 and Q15 whose emitters are referenced to a negative power supply; thus, the reverse bias voltages and resulting reverse bias currents (I_{B2} for bipolars) are applied to the DUT for the 3.0 μs immediately following the turn-on pulse. This reverse bias voltage can then be varied to determine its effect on switching speeds, power dissipation and case temperature rise. For the following described temperature tests the bias voltages were set for -2.0 V and -5.0 V respectively, the presumed optimum values that are listed in the respective data sheets.

The resistive loads, being somewhat inductive wire-wound resistors, have turn-on switching current rise times limited by the L/R time constant (Figure 10-3) and thus independent of input drive. However, the turn-off voltage and current switching times are affected by off-bias (Figure 10-4); thus at optimum bias voltage, the switching losses and therefore case temperature can be minimized. This is quite evident in the curves of Figure 10-5 showing temperature rise versus frequency at two off-bias voltages. All three devices showed slightly lower case temperatures (1.0 to 3.0°C) when the optimum off-bias was used at the higher frequencies where switching losses predominate.

The power MOSFET also runs cooler at higher off-bias voltage. This is due to the charged input capacitance C_{iss} being discharged more quickly when clamped to a greater negative voltage; thus the turn-off switching speeds are improved.

As expected at low frequencies, where on losses predominate both the 2N6545 (SMI) and the MJ16004 (SMIII) have temperature rises proportional to $V_{CE(sat)}$, both being about 0.3 V at 2.5 A. The power MOS transistor (TMOS), with a typical on-resistance $r_{DS(on)}$ of about 0.9 ohm [1.0 ohm(max)] has an on-voltage of about 2.2 V at

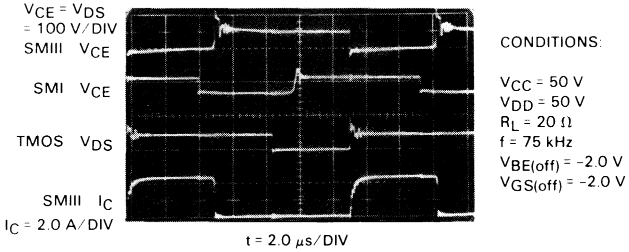

FIGURE 10-3 — RESISTIVE LOAD SWITCHING OF DUTs AT 75 kHz

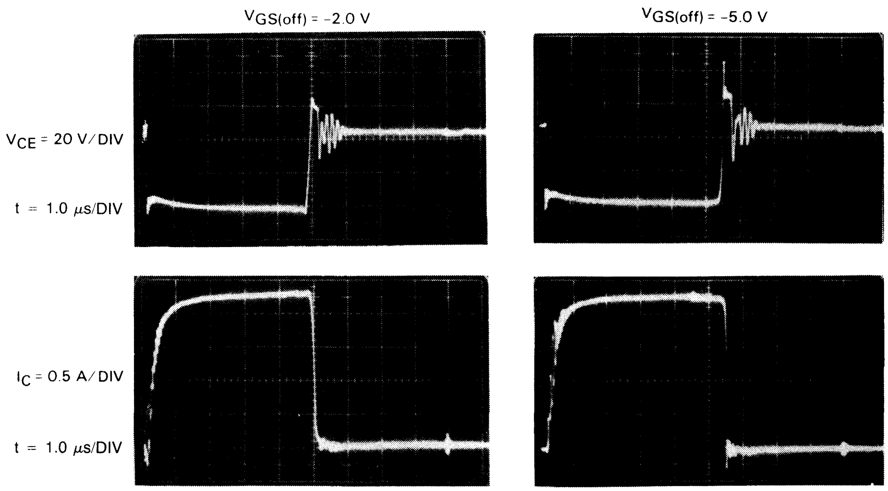

FIGURE 10-4 — RESISTIVE LOAD SWITCHING OF SWITCHMODE III MJ16004 AT TWO OFF-BIAS VOLTAGES

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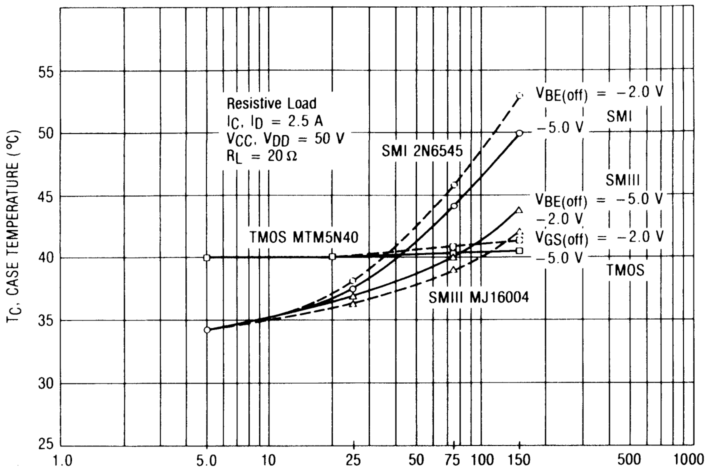

FIGURE 10-5 — TEMPERATURE RISE OF SWITCHMODE DEVICES AS A FUNCTION OF FREQUENCY

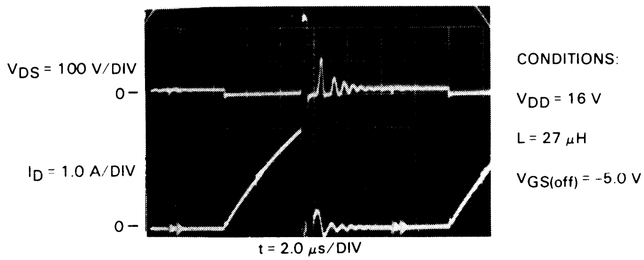

FIGURE 10-6 — CLAMPED INDUCTIVE LOAD SWITCHING WAVEFORMS OF TMOS MTM5N40

2.5 A, resulting in the higher case temperature. As the frequency is increased, the extremely fast switching MOSFET introduces little additional switching losses, resulting in a relatively constant case temperature.

The first generation SMI transistor shows the expected increasing temperature rise with increasing frequencies due to its relatively slow switching speed (the device was designed for 20 kHz applications). By contrast, the Switchmode III transistor, MJ16004, which was designed for improved operation at higher frequencies with improved reverse bias safe operating area, shows a much lower case temperature rise; in fact, it typically operated cooler than the power MOSFET up to the 75-100 kHz range.

The illustrated temperature rise curves were derived with typical devices. Testing of about ten sets of devices produced similar results, although in some cases the effects of off-bias were not as pronounced due to slight differences in device processing, temperature measurement repeatability and accuracy, particularly where small differences in temperature had to be determined.

Although the curves show defined temperatures, the magnitude of the rise is only relative as it is obviously a function of the size and efficiency of the heat sink chosen. For this exercise, small heat sinks were chosen to raise the case temperature for higher differential temperature measurements. Secondly, the heat sinks (both the small ones for the DUTs and the large ones for the resistive and inductive loads) were thermally isolated from each other to minimize mutual thermal coupling effects; (the DUT heat sinks were mounted on ceramic standoffs and the load sinks on plastic washers to reduce thermal conduction to the chassis and hence to each device).

The vertical temperature axis of Figure 10-5 could have been labeled Power Dissipation (P_D), knowing the thermal resistance of the heat sink ($R_{\theta SA}$) used and the relationship between case temperature and thermal resistance ($P_D = \frac{T_C - T_A}{R_{\theta CS} + R_{\theta SA}}$). However, for relative efficiency considerations, measuring the device case temperature will suffice.

For clamped inductive loads, the greatest switching dissipation generally occurs during turn-off where the device, due to the rectangular load line, can be stressed simultaneously with both high current and voltage. The illustrated inductive loads simulate a flyback switching regu-

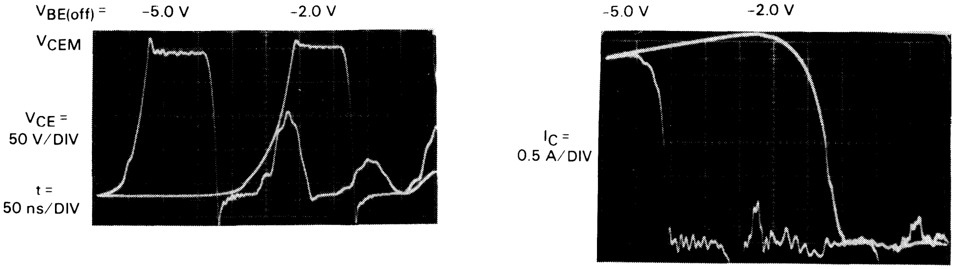

FIGURE 10-7 — CLAMPED INDUCTIVE LOAD TURN-OFF TIMES OF SWITCHMODE I 2N6545 WITH TWO OFF-BIAS VOLTAGES

lator where the energies stored in the inductors when the DUTs are turned on are transferred via their respective clamp diodes to the resistor-capacitor load during turn-off time. By proper selection of this load, the resulting clamp voltage was set for about 250 Vdc. The actual peak collector-to-emitter voltage V_{CEM} overshoot can be somewhat higher, being dependent on the rate of collector current fall time t_{fi}, the forward recovery time of the clamp diode and the degree of proper RF layout (Figure 9-7). It is not uncommon for this overshoot to exceed the clamp supply voltage by 100 Volts.

An example of how reverse bias affects the switching speed, and thus efficiency, of the 2N6545 is shown in the photos of Figure 10-7. Note the difference in t_s, t_{fi}, V_{CEM} and collector-emitter voltage rise time t_{rv}. At the optimum bias of about -5.0 V, the device turns off faster, there is less energy to be dissipated and a lower case temperature results. This is also true of the other two DUTs.

Although there is no "storage time" associated with FETs, there is a turn-off delay time $t_{d(off)}$ due to device capacitances having to be discharged. The photos of Figure 10-8 describe the turn-off times when the off-bias is varied from 0 V, -2.0 V and -5.0 V respectively. As mentioned previously, the greater off-bias results in the lowest turn-off times.

The average temperature rise measurements of the three DUTs for the inductive load case (Table 2) illustrates the effect of off-bias on device efficiency.

A direct point-by-point comparison between the inductive load and resistive load tests at 75 kHz can't be made since the respective load currents, and thus power dissipation are not the same. However, the trends can be compared; i.e., for the inductive load test, a greater temperature differential resulted between the optimum off-bias voltage and the second tested voltage, being as high as about 15°C for SMI. By comparison, the resistive load test showed only a few degrees difference. This is due to the change in turn-off switching time having a greater effect on the more energy stressful inductive load switching than on the resistive load.

In addition to driving the bipolar devices with the recommended forced beta, β_F of about 5.0 and 7.0 respec-

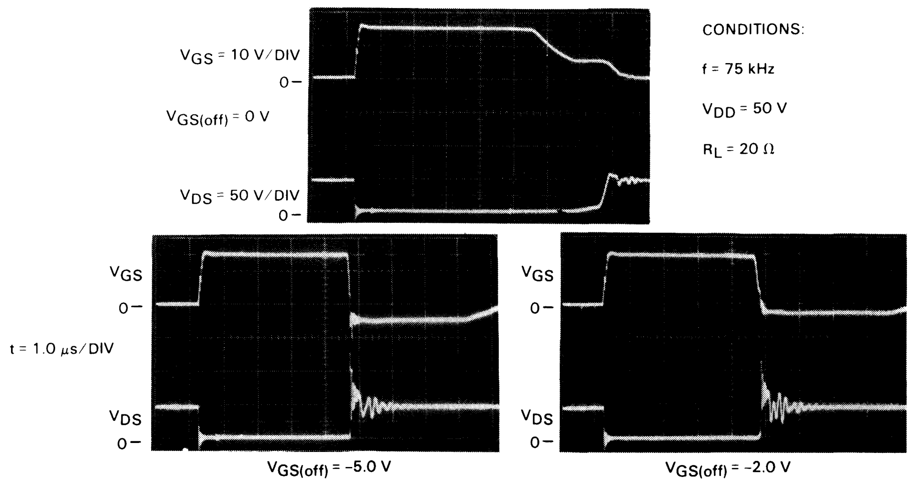

FIGURE 10-8 — THE EFFECT OF OFF-BIAS VOLTAGE $V_{GS(off)}$ ON TURN-OFF TIMES OF TMOS MTM5N40, RESISTIVE LOAD

TABLE 2
Temperature Rise of an Inductive Load
f = 75 kHz, I_{CM} = 3.0 A, V_{CEM} ≅ 250 V

Off-Bias Voltage	Case Temperature		
	SMI	SMIII	TMOS
2.0 V	58°C	34°C	42°C
5.0 V	43°C	39°C	38°C

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tively for the 2N6545 and MJ16004, a brief test was conducted by reversing β_F (7.0 and 5.0 respectively). Although the dynamic saturation characteristic of the bipolars changed subtly due to different base drive, and the turn-off switching time (even with off-bias) changed by only a second order, the change in power dissipation was minimal, if any. Within measurement repeatability, the resultant case temperatures were about the same, suggesting no great requirement of maintaining a defined β_F.

Examination of the above test results, the resistive temperature curves and the photos of the switching waveforms lead to the following conclusions about the switching efficiency of the test devices:

- The temperature rise results are a measure of total device dissipation, including the input drive loss.
- The fast switching speeds of TMOS coupled with the low drive power requirements and relatively simple drive circuitry make the MOSFET an attractive high frequency device.
- Power MOSFETs become more efficient at frequencies beyond about 100 kHz when compared to the new generation of switchmode bipolar transistors.
- Power MOSFETs have lower $t_{d(off)}$ when sufficiently reverse biased than bipolar t_s, thus allowing a higher operating frequency.
- At low frequencies, ON (static) losses predominate; thus bipolars are presently more efficient than comparably sized first generation power MOSFETs. Technology advancements of Motorola power MOSFETs have been made to significantly reduce the on-resistance, $r_{DS(on)}$ to make these devices competitive with the bipolars.
- Switchmode III MJ16004 compares favorably to power MOSFET MTM5N40 at 75 kHz with an off-bias of −5.0 V and generally runs cooler at the optimum bias of −2.0 V (relative to −5.0 V for TMOS). Although not described in this text, the SOA of SMI & SMIII is not as large as TMOS.
- For "real world" inductive loads, where the turn-off switching losses predominate, insufficient off-bias can produce higher case temperature rise for SMI transistors due to slower turn-off switching speeds (e.g., @ 75 kHz T_C = 58°C for $V_{BE(off)}$ = −2.0 V compared with 43°C for −5.0 V).
- Optimum off-bias will reduce turn-off switching times and thus switching losses for the bipolars and FET, but does not necessarily minimize the storage time (e.g., for SMIII $t_{fi(min)}$ and $t_{s(min)}$ occur at about −2.0 V and −5.0 respectively.
- Under optimum off-bias voltage condition, the t_f of SMIII approaches that of the very fast TMOS, however, drive power is high.
- Switchmode I 2N6545 can be comparably operated to 75 kHz when there is sufficient off-bias voltage (or reverse base current), approximately −5.0 V.
- Storage time, when it is not compensated for by circuit feedback techniques, somewhat affects efficiency at high frequencies due to increased ON losses.
- Specified force beta β_F of the bipolars are not too critical for efficiency considerations as the turn-on times are partially dictated by the load. Off-bias tends to minimize the storage time effects as β_F is varied; however, excessive overdrive can cause I_C tail lifts during turn-off which may contribute to larger temperature rise.

Low Voltage Devices: TMOS versus Bipolar, Darlington and GTO Devices

PWM DC Motor Controller Test

The load used in this test is a dc motor whose speed is controlled by PWM. Consequently, when narrow pulse widths are applied — low speed — the back emf is low and the load current (collector, drain or anode current) is high, about 11 A. To ensure device saturation under this worst case condition, adequate input current must be applied. For the devices tested, the forward input current for the bipolar, Darlington, TMOS and GTO were about 700 mA, 100 mA, 1.0 mA, and 120 mA, respectively.

Due to the motor time constant, the switching frequency was set for about 100 Hz and the min/max duty cycles were about 8% and 70% respectively. At this low frequency, the use of off-bias for the bipolar, Darlington and TMOS produces negligible improvement in efficiency as the decrease in turn-off time is extremely small for the time frame involved. However, the GTO does require off-bias which for this test circuit and DUT was as much as 2.2 A lasting for about 10 μs. This turn-off power should be considered in the efficiency calculations. At low frequencies, it is relatively small, but as frequency increases, it can become substantial (refer to Figure 10-10 for drive circuits and input power equations).

The bipolar, Darlington, and TMOS are turned on by the input pulse whose width is a function of the required motor speed, whereas the GTO is turned on by a relatively narrow, positive gate current pulse and turned off by a narrow, negative gate current pulse. As the frequency is increased it is apparent that the GTO input power increases and will reach a point where its input power is greater than that of the bipolar or Darlington. This crossover frequency is a function of the power supplies used and the particular duty cycle chosen. As an example, for a 50% duty cycle with the illustrated power supplies, this crossover point between the Darlington and GTO would be about 2.0 kHz.

Test Circuit Analysis

The test circuit, shown in Figure 10-9, consists of a two gate CMOS, astable multivibrator (MV) clocking a CMOS configured monostable multivibrator (MV) to produce the approximate 100 Hz, variable pulse width output. Darlington transistor Q1 furnishes the buffered output to drive the two channels of the power amplifier, with transistors Q2 and Q3 supplying the positive input current to the DUT and Q4 and Q5 the negative current. When the DUT Selector Switch S1 is in positions 1, 2, or 3, the full pulse width will be applied to the DUTs as differentiating capacitor C1 is shorted out. Thus, positive input current is generated by the direct coupled pulse turning on the NPN transistor Q2 and the following PNP transistor Q3 connected, in positions 1, 2, and 4, as a constant current source. The respective emitter resistors set the current I_{B1} or I_{GT} for the DUTs. Negative current is derived by differentiating the input pulse with C2, R2 and using the negative going, trailing edge pulse for turning on the following PNP transistors Q4 and NPN clamp transistor Q5. Thus, an off-bias voltage (clamped by diodes D1 and D2) is supplied to the selected DUT. If required, the off-bias can be removed by the Negative Bias Switch S2.

The GTO requires only a relatively narrow positive gate current pulse to turn it on. This pulse is derived from the differentiating network C1, R1 (switch S1A open), with the positive going, leading edge pulse turning on Q2 and Q3. For the component values shown, a turn-on, positive drive current pulse I_{GT} of about 120 mA in amplitude and 40

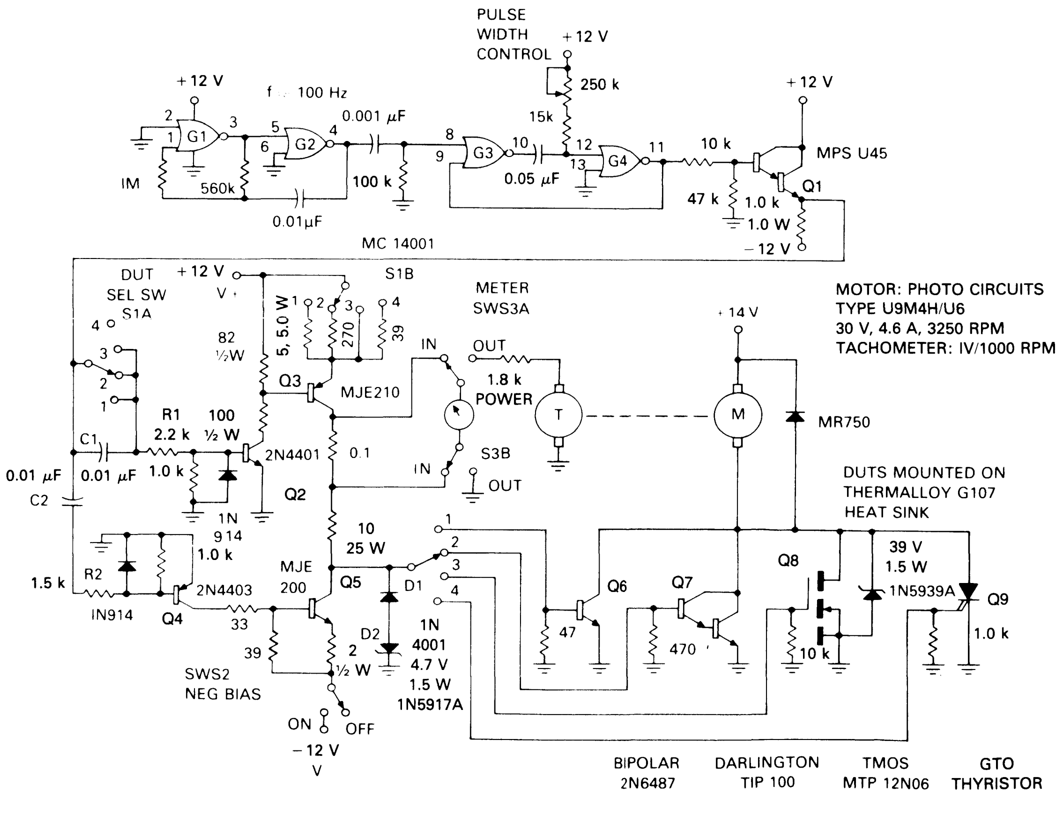


FIGURE 10-9 — TEST CIRCUIT FOR MEASURING RELATIVE EFFICIENCY OF DUT

μs wide is generated, followed by an approximate −6.0 V, 35 μs wide turn-off voltage pulse that is coincident with the trailing edge of the input pulse. This voltage pulse produces a reverse current I_{GR} of about 2.2 A for 10 μs (anode current of about 11 A) when the stored charge is depleted. Obviously, if no reverse bias is applied (Switch S2 open), the GTO will lose control, always being on, and the motor will run at its maximum speed.

Relative Efficiency Measurement of DUTs

In order to measure the relative efficiencies of the DUTs, both input power and output power are recorded. This is simply done by switching in a current meter to measure the average input current, or a voltmeter to measure output RPM by means of a tachometer coupled to the motor. The output voltmeter, in effect, measures the relative saturation loss of the DUT since this voltage is subtracted from the applied motor voltage and, consequently, the motor speed will be indicative of this loss. Only the relative positive input current is measured as the reverse currents at this low frequency contribute very little additional drive power. However, as the power equations note in Figure 10-10, with increased operating frequency, this off-bias power can be substantial.

The relative efficiency measurements for the four DUTs are listed in Table 3. Of interest, in regard to efficiency, are the measured input currents (both pulsed and relative average), and tachometer outputs, on-voltages and case

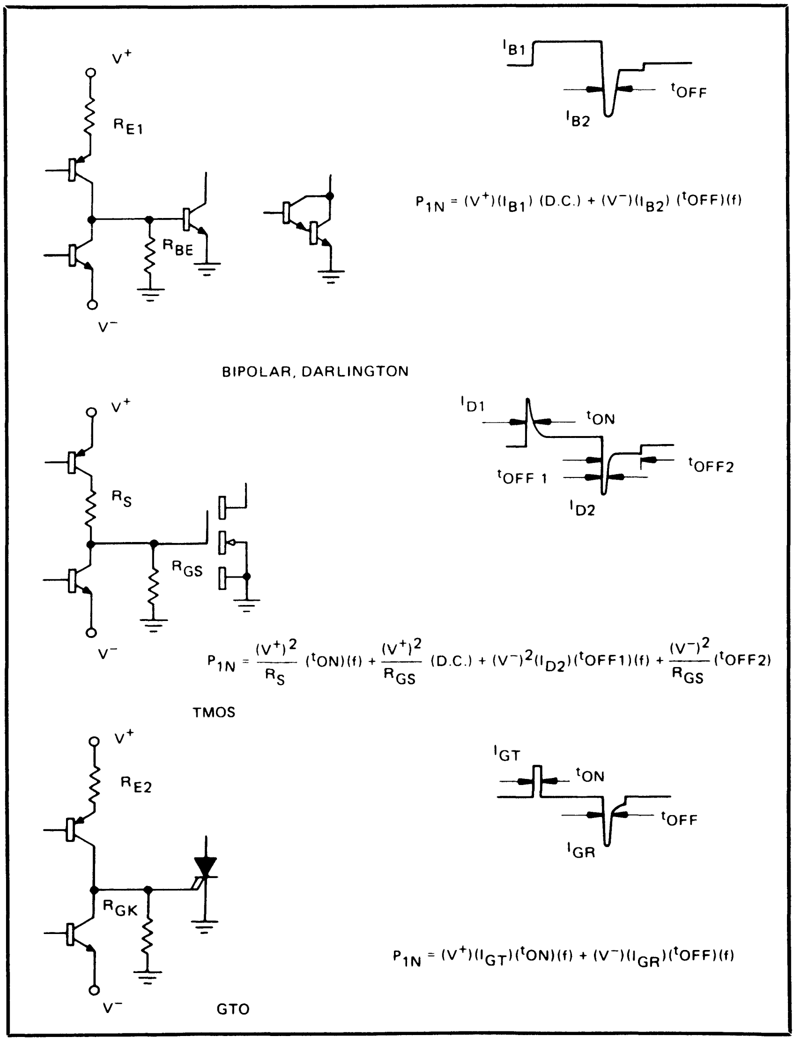


FIGURE 10-10 — DUT DRIVE AND INPUT POWER CALCULATION

temperatures. Within measurement repeatability, the DUTs with the highest on-voltage had the lowest relative output power due to reduced motor voltage and the case temperature rise correlated with the total power dissipation (input plus output). These readings generally confirmed what was expected:

TABLE 3 — Relative Efficiency Measurement of DUTs

DUT	Bipolar 2N6487			Darlington TIP 100			TMOS** MTP12N06			GTO Thyristor		
Die Size (MIL)	110 x 130			120^2			120^2			180^2		
Voltage Rating	60 V			60 V			60 V			300 V		
Current Rating	15 A			8.0 A			12 A			10 A		
Switching Speeds (Relative)	Medium			Medium			Fast			Slow		
Input Current, (Forward/(P.W.)	700 mA			100 mA			1.0 mA			120 mA (40 μs)		
Input Current, Reverse/(P.W.)	1.0 A @ I_{MAX} (0.2 μs)			0.4 A @ I_{MAX} (0.1 μs)			0.2 @ I_{MAX} (0.1 μs)			2.2 @ I_{MAX} (10 μs)		
Duty Cycle	8%	12%	56%*	8%	12%	81%*	8%	12%	74%*	8%	12%	68%*
Load Current, Peak	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A	11 A	5.0 A	0.9 A
Power In (Relative)	5.0	13	75	3.0	4.0	11	1.0	2.0	2.0	1.0	2.0	2.0
Power Out (Relative)	20	59	85	16	57	84	17	59	87	17	55	84
$V_{(on)IN}$	1.9 V	1.3 V	1.0 V	2.8 V	2.0 V	1.6 V	12 V	12 V	12 V	1.4 V	1.2 V	0.85 V
$V_{(on)OUT}$	1.2 V	0.4 V	0.12 V	2.1 V	1.3 V	0.78 V	1.7 V	0.9 V	0.15 V	2.0 V	1.5 V	1.0 V
Case Temp	36.6°C	32.9°C	38.3°C	43.6°C	41.3°C	40.4°C	42.3°C	36.0°C	29.5°C	39.5°C	41.1°C	38.2°C

*Clock varied with temperature
**Data was taken on first generation TMOS devices. Later device designs give a dramatic improvement in on-state efficiency of low voltage devices.

TMOS MTP12N06
At low frequency and low motor current, the TMOS is the most efficient device. Its input drive power is extremely low and its On voltage, due to the zero offset, relatively linear $r_{DS(on)}$ is low.

BIPOLAR 2N6487
The bipolar, with its low $V_{CE(sat)}$, has low output dissipation but its input power is the highest to satisfy high collector current — forced β conditions.
At medium and high load currents, the bipolar has the lowest On voltage followed by the TMOS with the Darlington and GTO being about equal in third place.

DARLINGTON TIP100
Total device dissipation and thus case temperature rise is due to input and output dissipation. The Darlington, with its high $V_{CE(sat)}$, can still have lower case temperature than the bipolar at some peak collector currents, due to its low drive power.

GTO THYRISTOR (Experimental)
The GTO is extremely efficient at low frequencies from a drive point of view since it requires only narrow turn-on and turn-off current pulses, but becomes less efficient as the frequency increases due to the higher duty cycles involved.

Efficiency as a Function of Frequency Tests

The PMW Motor Control Circuit was tested at a constant, low frequency, so the relative efficiencies measured were primarily due to static (saturation) losses. To determine the effect of the dynamic (switching) losses, which increase with increasing frequencies, the four different devices were tested with a resistive load, using a variable frequency, constant duty cycle (50%) input signal. The load current was set for about 4.0 A (V_{CC} = 28 V, R1≈7.0 Ω) and the same basic test circuit shown in Figure 9-9 was used. Most of the modifications were in the reverse bias circuit, with the off-bias voltage being either 0 V or −5.0 V for the bipolar, Darlington and TMOS tests and −12 V for the GTO.

Transistor Q4 emitter resistor (2.0 Ω) was shorted out to form an off-bias voltage source; Q3 emitter was tied to the +12 V bus to furnish drive to Q4 when $V_{BE(off)}$ was 0 V; and differentiating capacitor C2 was increased to 0.02 μF to allow greater turn-off time for the GTO. Also, the bipolar forward base current was set fo 600 mA, resulting in a β_F of about 7.0.

Test Results

The results of this efficiency versus frequency test, as measured by the case temperature rise using a small heatsink, are shown in Figure 10-11.

TMOS MTP12N06

As expected, the TMOS device ran the coolest at higher frequencies, being very constant in temperatures up to about 10 kHz and then rising slightly thereafter. At low frequencies, where static losses predominate, the TMOS MTP12N06 case temperature was only about 2°C warmer than the bipolar 2N6487, due to the respective saturation voltages of about 0.6 V ($r_{DS(on)}$ Typ = 0.15 Ω) and 0.4 V. Although not shown, increasing the off-bias voltage ($V_{GS(off)}$) from 0 V to −5.0 V showed only about a 2°C improvement at 33 kHz, due to slightly faster turn-off time; otherwise, at lower frequencies, the difference in turn-off time had little effect in case temperature.

Bipolar 2N6487

The bipolar transistor 2N6487 showed marked improve-

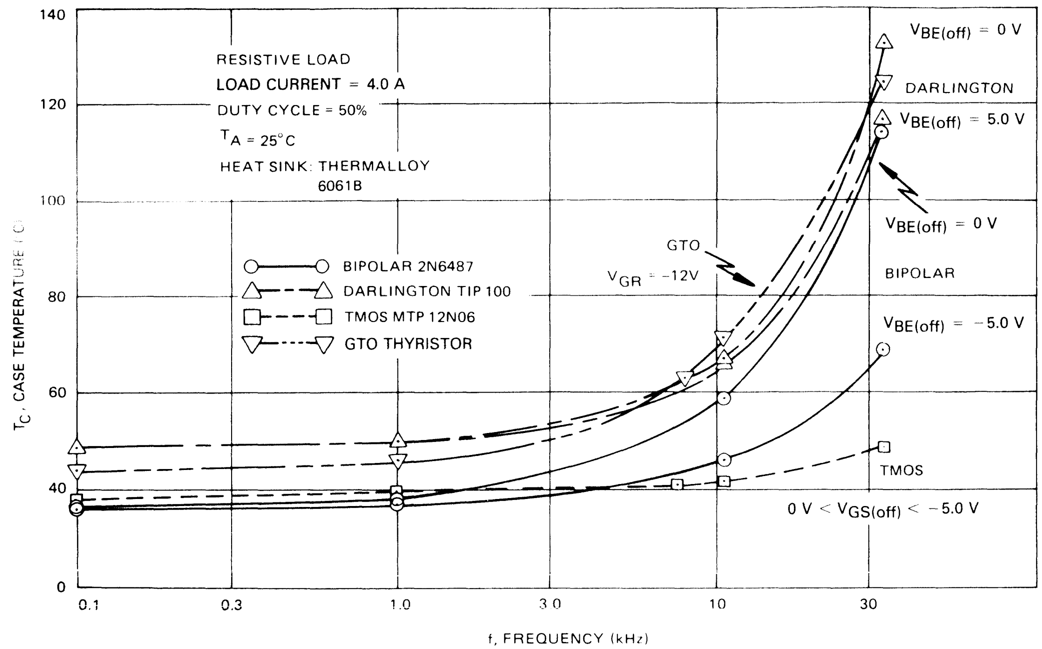


FIGURE 10-11 — TEMPERATURE RISE OF POWER SEMICONDUCTOR AS A FUNCTION OF FREQUENCY

ments in efficiency at the higher frequencies when the $V_{BE(off)}$ was increased from 0 V (base-emitter clamp) to −5.0 V. Without off-bias, the case temperature approached 115°C at 33 kHz, whereas, with −5.0 V, it was only about 70°C.

Darlington TIP100

The low voltage TIP100 Darlington does not have a speed-up diode across its input emitter-base resistor and thus the stored charge of the output transistor cannot be efficiently removed. Consequently, there is no improvement in case temperature at low or nominal frequencies and only some moderate improvement at 33 kHz (117°C relative to 133°C) when the off-bias was increased to −5.0 V.

The Darlington, with the highest saturation voltage of the four devices, not surprisingly, had the highest case temperature at low frequencies and, beyond 5.0 kHz, was about as inefficient as the GTO.

GTO (Experimental)

The experimental GTO exhibited static losses somewhere between the bipolar and the Darlington due to its on-voltage of about 1.2 V at 4.0 A. The device did perform at 33 kHz, however, its case temperature rose to about 125°C. This was due to its relatively slower switching times, as shown by the oscillograms in Figure 10-12. Figure 10-12 (a), (b) and (c) show the 33 kHz waveforms of anode current, anode-cathode voltage and gate current, respectively, relative to the TMOS drain current (Figure 10-12d) and drain-source voltage (Figure 10-12e). Note that the load current rise time is limited by the inductance of the wire-wound load resistor and that the TMOS switches much faster. Second, to ensure turn-off of the GTO at elevated temperatures, the peak reverse gate current with V_{GR} of −12 V was about 6.0 A with a pulse width of about 1.0 μs at the 50% point.

THE GEMFET versus THE MOSFET AND BIPOLAR

The GEMFET (Gain Enhanced MOSFET) is a new power semiconductor device with a combination of characteristics that were previously unavailable to the designer of power circuitry. Closely related to the power MOSFET in structure, this device has a forward voltage drop comparable to bipolars while maintaining the high input impedance and fast turn-on of its isolated gate. While turn-on speeds are very fast, turn-off is presently relatively slow and will restrict the use of at least the first generation of these devices to lower frequency applications.

The most pronounced advantage of the GEMFET over the power MOSFET is its lower on-resistance. The $r_{DS(on)}$ of a high voltage MOSFET is fairly large and rises with increasing junction temperature and drain current. Conversely, the $r_{CE(on)}$ of a GEMFET decreases with increasing T_J and is not greatly affected by I_C. Since the MOSFET does not have the GEMFET's offset voltage in its output transfer characteristics, at low currents the MOSFET on-resistance is slightly lower. However, at high currents and temperatures, the difference is dramatically in favor of the GEMFET.

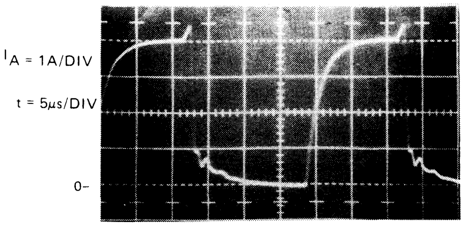


FIGURE 10-12a — GTO ANODE CURRENT

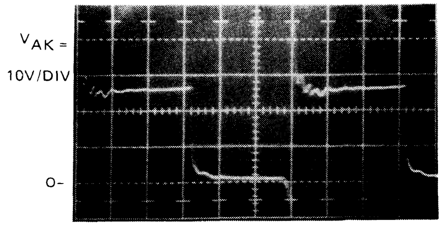


FIGURE 10-12b — GTO ANODE-CATHODE VOLTAGE

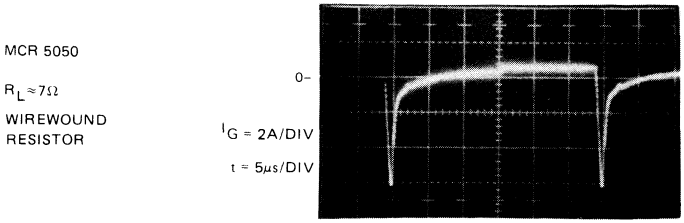


FIGURE 10-12c — GTO GATE CURRENT

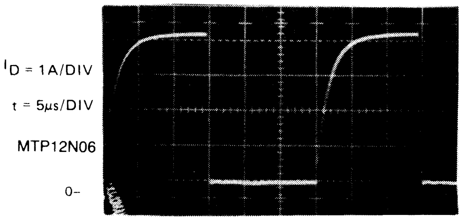


FIGURE 10-12d — TMOS DRAIN CURRENT

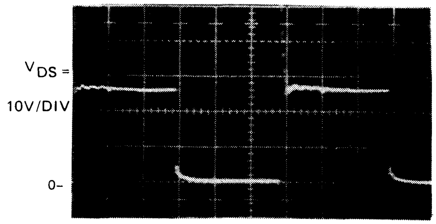


FIGURE 10-12e — TMOS DRAIN-SOURCE VOLTAGE

FIGURE 10-12 — COMPARATIVE SWITCHING OF A GTO AND TMOS AT 33 kHz

To illustrate the relative efficiencies of these two TO-220 devices — MGP20N50 GEMFET and MTP4N50 MOSFET — with that of a comparable die size, TO-220, high voltage Switchmode bipolar MJE13007, the low frequency, PWM motor controller test described in the previous section was performed. The results of a duty cycle versus case temperature rise test is shown in Figure 10-13. Note that at his low frequency test, where saturation losses predominate, the GEMFET is much more efficient than the MOSFET at low duty cycles (high motor armature currents), and even runs cooler than the bipolar device as the pulse width increases (motor current decreases).

The second test, comparing the three devices with an inductive load at several frequencies (the inductances were changed to maintain the same peak currents for all frequencies) is illustrated in Figure 10-14. Now, at the higher frequencies, the GEMFET runs the hottest — due to its slow turn-off switching time — and the MOSFET becomes more efficient than the bipolar at about 25 kHz.

For more information on the GEMFET, please refer to Chapter 9, the Spin-off Technologies of TMOS.

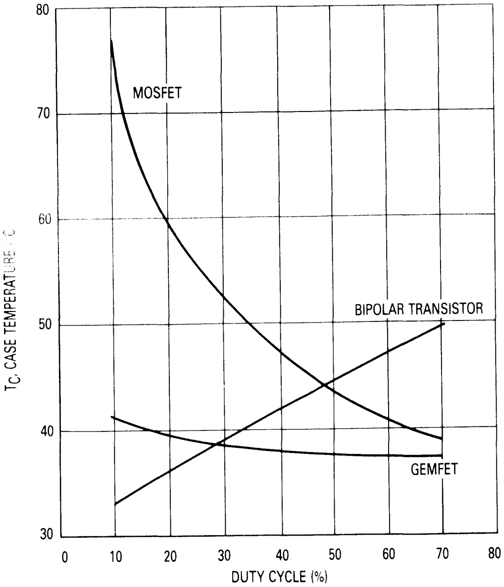


FIGURE 10-13 — ON-STATE EFFICIENCY COMPARISON — PWM OF DC MOTOR

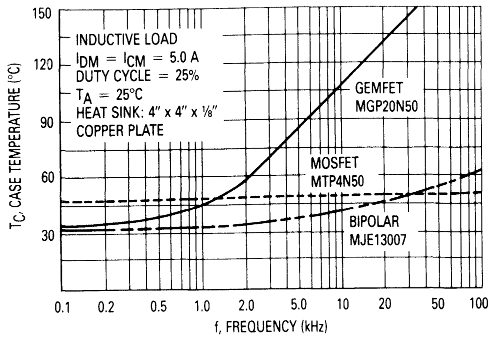


FIGURE 10-14 — COMPARISON OF CASE TEMPERATURE versus FREQUENCY FOR A GEMFET, MOSFET AND BIPOLAR TRANSISTOR

Chapter 11: TMOS Die for Hybrid Packaging

Using TMOS Die for Hybrid Assembly

Substantial savings in weight and volume can be achieved by hybrid packaging techniques. Selected Motorola TMOS packaged devices are available in die form for custom hybrid assembly. The same advanced MOS processing techniques and silicon-gate structure available in packaged form is available in die form. The unique TMOS design utilizes thousands of source sites, interconnected in parallel, on a single die. This structure minimizes on-state voltage drop. The TMOS processing techniques result in an extremely reliable device which is highly reproducible in various die sizes.

Die Characteristics

Several die sizes are available with voltages ranging from 50 to 500 volts. All die are individually probed, at room temperature, to the dc electrical specifications of their equivalent packaged device.

Due to limitations when probing in wafer form, some of the specifications of the equivalent packaged device cannot be tested and guaranteed in die form. These parameters are safe-operating area (SOA), thermal resistance ($R_{\theta JC}$), and on-voltage at full rated current. The above parameters depend on the assembly techniques of the individual user.

Visual Inspection of Die

All Motorola TMOS dice meet the visual inspection criteria of Mil-Standard 750B, Method 2072, with the exception of specific criteria listed below. All TMOS dice are visually screened to a 0.1% AQL level.

Die Backing

All standard TMOS dice come with Titanium-Nickel-Silver drain metallization. This metallization is suitable for solder pre-form mounting with solders such as 95/5 PbSn or 92.5/5.0/2.5 PbInAg. Commonly used header or substrate materials such as copper, nickel plated copper, gold plated molybdenum, beryllia and alumina are acceptable. The substrate material must be free of all oxides prior to assembly. Mounting is generally accomplished in a profiled belt furnace (hydrogen atmosphere is recommended). The use of solder fluxes is not recommended.

Wire Bonding

Electrical connection to the gate and source bond pads can be accomplished by ultrasonic wire bonding, using AlMg* wire having an elongation of 10%. Caution should be exercised during wire bonding to insure that the bonding footprint remains within the bonding pad area. Wire bond settings should be optimized and a wire pull test performed (see Method 2037, Mil Standard 750B) to monitor wire bond strength uniformity. Destructive sample testing and 100% non-destructive testing is recommended.

*Wire sizes of 15 mils and greater are pure Al.

Encapsulation

Before encapsulation, the assembly must be kept in a moisture free environment. I_{GSS} and $V_{GS(th)}$ are sensitive to surface moisture. For a non-hermetic package, a high grade electronic coating such as Dow Corning RTV3140 should be applied (coating is optional with a hermetic package). Before encapsulation, a 150°C two-hour bake should be performed to remove any surface moisture and any capping of hermetic packages must be performed in a dry, nitrogen atmosphere.

Handling and Shipping

TMOS Dice are available packaged several ways:

1. Anti-static MultiPak — Waffle type carrier with individual die package.
2. Scribed and Broken Wafers — Wafer on Mylar and vacuum sealed in plastic, with rejects inked.
3. Wafer Pak — Whole wafers, with rejects inked.
4. Circle Pak — Whole wafer is placed on sticky film before being sawed and broken. Special equipment is needed to remove die from sticky film, with rejects inked.

Upon opening the plastic container, dice should be stored in a nitrogen atmosphere to prevent oxidation of bond areas prior to assembly. All dice should be handled with teflon tipped probes to prevent any mechanical damage and the probe needles should be dipped in a conductive solution as teflon can cause ESD problems.

2

2-11

Chapter 12: Characterization and Measurements

FBSOA Testing of Power MOSFETs

Power MOSFETs are essentially free of second breakdown; at least in the sense that second breakdown is defined for bipolar transistors. If second breakdown is defined as a region in which total allowable power dissipation decreases as drain-source voltage increases, the power MOSFETs do exhibit a second breakdown behavior. However, this phenomena occurs at power levels in excess of the device rating. In terms of measured safe-area capabilities, power FETs commonly show higher power dissipation capability at lower voltages than they do at voltages approaching $V_{(BR)DSS}$.

The phenomena which causes apparent second breakdown in FETs is similar to bipolar second breakdown in that increasing drain-source voltage widens depletion regions, allowing less of the silicon area to be used for current conduction. In FETs, higher voltages constrict the vertical channel somewhat, reducing the total area for current conduction and the maximum power dissipation capacity. Unlike bipolar transistors, there is no regenerative action associated with the current constriction. Its effects, therefore, are much less severe; so much so that FETs are generally regarded as being free of second breakdown. In general, consideration of the thermal ratings is all that is required when devices are operated within their current and voltage ratings.

To ensure that the power MOSFETs do not exhibit any limitation within the thermally limited portion of the FBSOA curve (the theoretical locus of constant power based on the thermal resistance), the DUTs were subjected to energy levels beyond the curve. As in turn-off switching SOA, a non-destruct tester would be advantageous, allowing one DUT to be used to generate a complete curve.

An important advantage of a non-destruct fixture is that it can give individual device trends and, from that, clues to the actual failure mechanism. Some have indicated that a steepening of the SOA slope at high-voltage, low-current indicates breakdown due to negative resistance effects (43,44).

The non-destruct fixture is also safer and is easier on larger power supplies. If a destructive tester were to short out a device, there is nothing to limit the current flow until the device heats to the point of opening up. This non-destruct fixture turns off the power supply and harmlessly dissipates the energy in the circuit.

Basic Theory

When a power MOSFET is operated just outside its SOA, the drain current, I_D, will suddenly increase very rapidly as the device breaks down. Unless the energy can be removed very quickly, the device will be destroyed. The basic idea of the non-destruct fixture is to sense this current surge and divert the energy from the Device Under Test as rapidly as possible. The fixture reacts within approximately 100 ns and usually saves the device.

Circuit Description

The circuit performs three main functions. First, it controls the desired drain-source voltage, V_{DS}, drain current, I_D, and pulse width in order to provide a defined energy to the DUT. Second, it protects the device just as it starts to fail; and third, once an overstress is detected, it removes power from the system.

The N-channel circuit is shown in Figure 12-1 and will be described. (The P-channel circuit is virtually identical except for inversion of power supplies, logic outputs and complementary transistors.) Controlled drain current is applied to the common source connected power MOSFET by means of the feedback loop around its gate-source with op-amp U1 being the error amplifier. The loop will force the source voltage (developed across the drain current sense-resistor R1) to be equal to the reference voltage that is applied to the non-inverting input of U1. The gate-source voltage will automatically assume that value required to produce the required drain current. Thus, by varying the reference voltage by means of the I_D Adjust control, a defined, accurate drain current can be chosen.

Drain-source voltage is applied to the DUT through a current-limiting inductor L1 (to reduce short-circuit current) and a series-connected Darlington NPN switch, Q9. Thus the drain voltage is approximately equal to the V_{DD} power supply (neglecting the $V_{CE(sat)}$ of Q9).

The series Darlington, configured as an emitter-follower, is controlled by level translating NPN high voltage transistor, Q7, and the following PNP high voltage transistor, Q8. Transistors Q8 and Q9 are in effect a compound Darlington and Q7 acts as a current source to minimize drive variations when V_{DD} is varied. System operation begins by applying a positive-going pulse by means of an external pulse generator to the base of Q7, thus turning on the switched drain supply. The gate is also turned on, but is slightly delayed by the R3C1 base integrating circuit of the unclamped transistor Q1 to minimize turn-on stress on the DUT.

A fast video amplifier, U2, also monitors the DUT source, looking for a current spike. This amplifier, connected to produce a voltage gain of 200 with a bandwidth of 40 MHz, will quickly detect the advent of the destructive current spike and amplify it to a level to trigger a fast discrete R/S flip-flop.

To "lock-out" false signals that may occur due to device turn-on, an N-channel FET series switch, Q2, is connected between the video amp and the flip-flop. This FET is controlled by PNP driver, Q10, NAND Gate, G3, and input-pulse-triggered monostable multivibrator G1 and G2. Thus, by varying the Pulse Width Adjust, R4, the first 5.0 to 50 ms of the switched drain current can be blanked to prevent false triggering of the circuit.

A "true" trigger will turn on PNP transistor Q3 of the flip-flop whose output is buffered by NPN transistor Q5. The positive-going signal will then turn on the fast crowbar power MOSFET Q6, thus quickly diverting the energy from the DUT. The high level flip-flop output from Q3 will also turn on the LED — indicating a crowbar occurrence — and clamp off the input pulse generator by means of turned on transistor Q11. Consequently, Darlington Q9 is

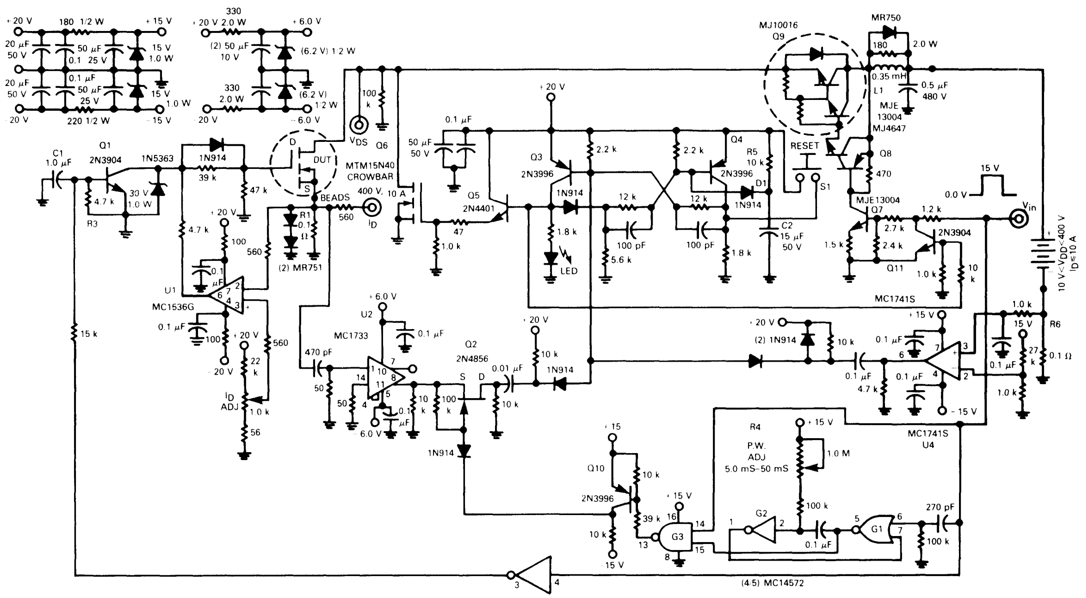


FIGURE 12-1 — N-CHANNEL POWER MOSFET NON-DESTRUCT FBSOA TESTER

also turned off. To protect the crowbar FET and Q9, which are both on for about 30 μs due to propagation delays, current limiting inductor L1 is placed in series with the power loop.

The system is reset by depressing push-button S1, thus placing the flip-flop in the proper state. The resistor R5, capacitor C2 and diode D1 network in the base circuit of Q4 ensure that the flip-flop will be in the proper state when power is first applied.

The circuit also has over-current protection. A second current sensing resistor R6 in the return bus of the V_{DD} supply monitors the input current and activates the flip-flop if more than 10 A is sensed. This is accomplished by comparator U4 and its associated pulse steering circuitry.

The P-channel fixture shown in Figure 12-2 is nearly identical to the N-channel except that it contains its own pulse generator and its supplies and transistors are inverted. The pulse generator uses a quad, two input NOR gate to produce the required astable multivibrator (A1 and A2) that clocks the following monostable multi-vibrator (A3 and A4).

Testing Mechanics

The intended use of the FBSOA test fixture is to ensure that device operation is limited only by its specified power rating based on a measured $R_{\theta JC}$ and not a second breakdown of the parasitic bipolar transistor or any other phenomena.

To determine if the device was actually facing failure when the fixture crowbarred, V_{DS} was held constant and I_D was gradually increased with successive pulses until the fixture crowbarred. Then the crowbar was disabled and the device was pulsed again. The device would fail indicating that the crowbar was only being activated when the device was beginning to fail.

Normally, a one second pulse was used, but other pulse durations were investigated. Time was allowed between pulses for cooling. A two second pulse did not significantly change the FBSOA curve. The device would handle about 20.0% more power during a 0.1 second pulse and the slope of the FBSOA curve remained the same (Figure 12-3).

During a 10 ms pulse, the device handled another 20.0% more power before failing. Since the blanking period lasts at least the first 5.0 ms of the 10 ms pulse, the fixture had difficulty saving units at this high energy level. The implication of this test is that the mechanism causing crowbarring is energy (time) dependent, tracking somewhat the thermal response of the device. Presumably, the junction temperature when the fixture crowbars is about the same for all pulse width variations.

Careful testing, i.e., slowly increasing the energy level, can ensure multiple crowbar activations of the DUT. One N-channel device went through 30 crowbars with no degradation in $r_{DS(on)}$, leakage current or drain-source breakdown voltage. Parts were either saved without degradation or destroyed, usually shorted from drain-to-source.

The case temperature of the TO-220 MTP5N20 ($R_{\theta JC}$ = 1.67°C/W), using a large finned, air cooled heat sink, rose to about 120°C when the DUT activated the crowbar. The applied power of 150 W thus produced a calculated junction temperature of about 370°C. At first glance, the Motorola parts appear to be rated with a fair amount of guardband. The actual FBSOA guardband is even larger since the rated curve assumes a case temperature of

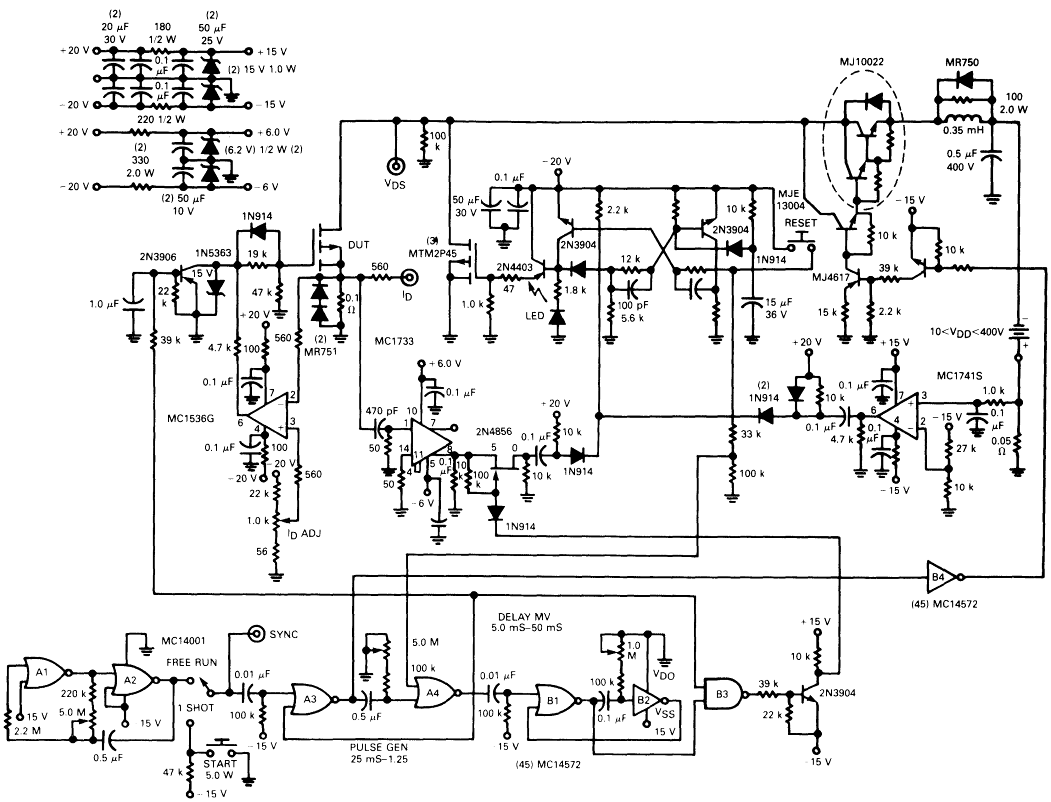


FIGURE 12-2 — P-CHANNEL POWER MOSFET NON-DESTRUCT FBSOA TESTER

25°C and the measured curve was derived at an elevated case temperature. Nevertheless, to ensure reliability, the user must operate the power MOSFET within the specified thermally limited curve.

Results of Testing One Part Along the Entire Curve

Many of the N-channel curves turned out to be very linear when plotted on log-log paper (Figures 12-3, 12-4). Within the same product line, the slope was very similar from device to device and always steeper than the −1.0 slope of the constant power dissipation curve. The plots from product line to product line also tended to be tightly clustered, with slopes varying from about −1.2 to −1.5 over the eight different lines tested.

Some have reported a steepening of the SOA curve at higher voltage and that this is due to a negative resistance phenomena. This occurs when avalanche breakdown takes place in the drain junction which increases I_D. Because of the finite resistance of the substrate, the increase in I_D causes an increase in the potential in the substrate. If I_D and the substrate resistance are large enough, the source junction can become forward biased, which would intensify the avalanche multiplication. N-channel devices with short channels are susceptible to this phenomena, but the problem can be alleviated by decreasing the substrate resistance or increasing the channel length. This negative resistance effect on SOA is illustrated in Figure 12-5. The intent is to compare slopes and not to compare power handling capabilities of equivalent die sizes (43,44,45).

Testing indicates that the Motorola Power MOSFETs are not influenced by the negative resistance effect even though they utilize very short channels to decrease on-resistance. This is because of the additional P+ plug that is diffused beneath the source contact. When the device goes into avalanche breakdown, as illustrated in Figure 12-6b, the preferred avalanche current path is from N substrate through the P+ plug and into the source. This keeps the forward voltage drop of the source junction low, or below turn on. This avalanche current is quite possibly the current surge that the FBSOA tester detects when the fixture activates the crowbar.

At still higher power levels current may flow, as in Figure 12-6c, increasing the voltage in the P region. The forward voltage drop across the source junction may rise to above turn-on, establishing the negative resistance phenomena. This produces a positive feedback mechanism because the source is now injecting electrons into the substrate and thus intensifying the avalanching, effectively turning on the parasitic transistor. Such an avalanche injection would most likely destroy the device.

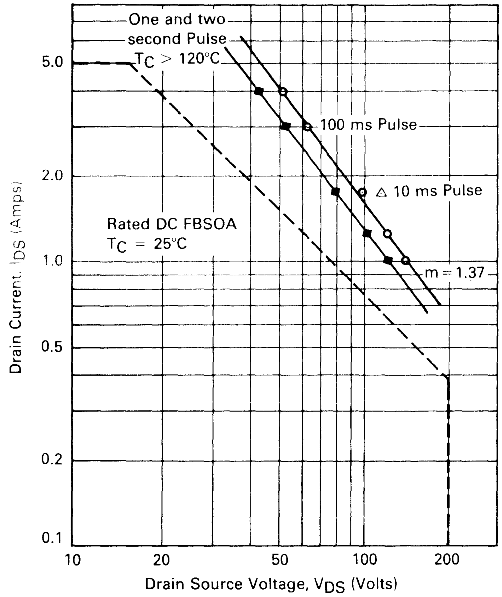


FIGURE 12-3 — DC FBSOA OF MTM5N20

The questions "Why does the empirical FBSOA slope deviate from the −1.0 slope of constant power?" and "What is the significance of the slope on the SOA curves?" still remain. Since thermal resistance of bipolars decreases with increasing current at a constant power level, it was thought that the same may be true for power MOSFETs and that this could steepen the SOA slope (46). If $R_{\theta JC}$ increases with voltage (decreasing current), the device would not be able to dissipate as much power at the high voltage, low current end of the curve.

To investigate this premise, many thermal resistance measurements were taken on the DUTs, all at a constant power level, but varying I_D and V_{DS} ($V_{DS1}\ I_{D1} = V_{DS2}\ I_{D2}$, etc.). A thermal resistance fixture that used a switching technique to measure the voltage drop across the parasitic drain-to-source diode was used initially. The inherent measurement error in this method tended to suppress any trends in the variation of $R_{\theta JC}$ with I_D.

A second method that measures the junction temperature of a decapped device with an infrared microradiometer proved to be more accurate. The instrument read out an average temperature of about 10.0% of the die area that was located in the center or the hottest part of the chip. Again, I_D and V_{DS} were varied while P_D was held constant. As shown in Figure 12-7, $R_{\theta JC}$ does decrease with increasing I_D at a constant P_D, like bipolars, but the 10.0% change in $R_{\theta JC}$ is not enough to account for the approximate 30.0% change in power handling capabilities (m = 1.4). Although $R_{\theta JC}$ varies and does steepen the FBSOA slope, it has only a partial effect under these test conditions. These results must be qualified because the equipment did not allow the measurement of $R_{\theta JC}$ at a power level near the FBSOA limits where the change in $R_{\theta JC}$ could be more or less significant.

The failure mechanism and thus the slope of the curves obtained from the FBSOA test fixture, is a function of junction temperature, V_{DS}, I_D and a variable thermal resistance. Because the junction temperature rose so high, the device could be going into avalanche breakdown which would be a strong function of V_{DS}, as the curves indicate. This temperature at failure is above $T_{J(max)}$ ratings and demonstrates why users must not exceed published SOA curves.

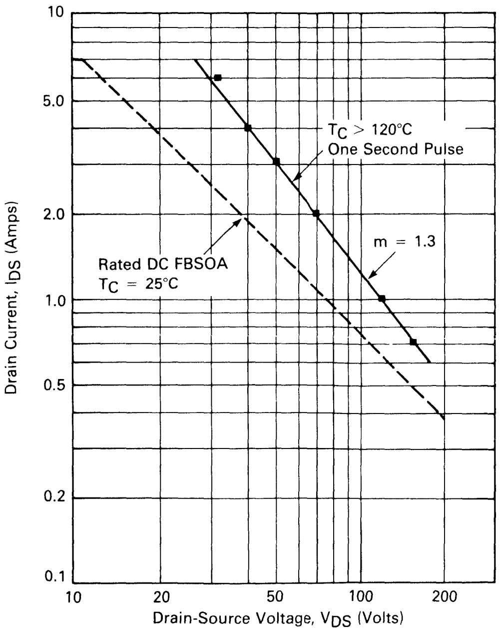


FIGURE 12-4 — DC FBSOA TEST ON MTP7N20

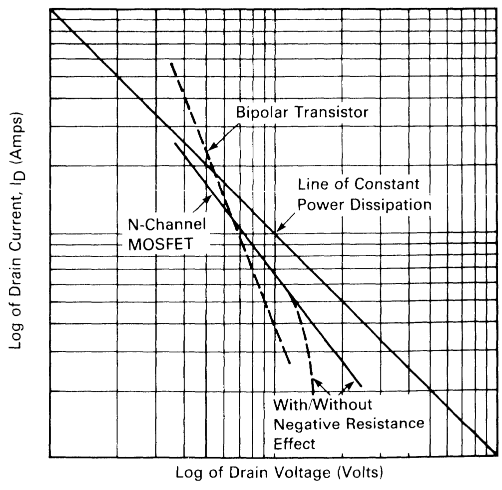


FIGURE 12-5 — COMPARISON OF TYPICAL FBSOA SLOPES

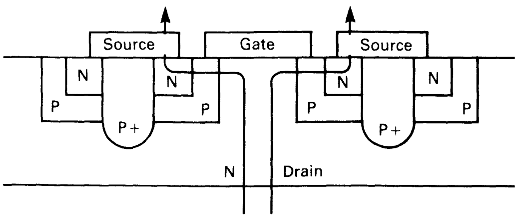


FIGURE 12-6a — TYPICAL CURRENT FLOW IN TMOS POWER MOSFET

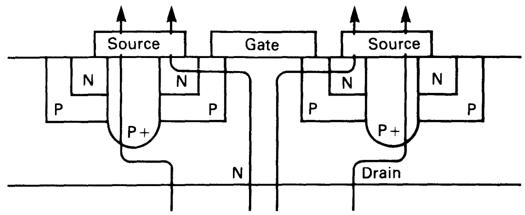


FIGURE 12-6b — CURRENT FLOW DURING AVALANCHE

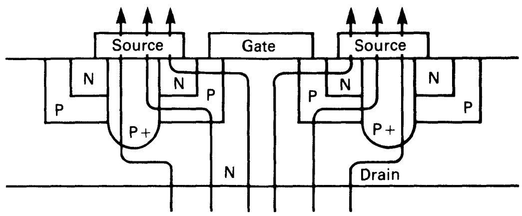


FIGURE 12-6c — CURRENT FLOW DURING NEGATIVE RESISTANCE BREAKDOWN

Since power MOSFETs or, for that matter, bipolar transistors, do change their thermal resistance as operating conditions vary, this could warrant a change in the published SOA curves. The thermally limited portion of the curve is presently based on one thermal resistance reading taken at a single operating condition. If this is a worst case reading (taken at low current, high voltage), this could significantly underrate the device at the high-current, low-voltage portion of the curve. Conversely, if the reading is taken at the high-current end, this could overrate the device at the low-current end. Further study needs to be done to determine if the change in $R_{\theta JC}$ is significant enough to alter the way manufacturers derive published SOA curves.

The significance of the slope greater than minus one, as accurately derived from the non-destruct FBSOA tester, is that a simple power limit of, say, 75 W may not be appropriate because it could overrate a device under certain conditions and underrate the same device at the same power level but lower voltage and higher current. Motorola establishes conservative derating of $R_{\theta JC}$ to ensure reliable operation under all bias conditions.

Switching Safe Operating Area (SSOA)

TURN-OFF SWITCHING SOA OF POWER MOSFETS

One of the advantages of power MOSFETs over bipolars is its superior reverse bias safe operating area (RBSOA) performance. Power MOSFET RBSOA curves are generally "square" at $I_{D(max)}$ and $V_{(BR)DSS}$, (Figure 12-8) indicating that performance is bounded only by maximum voltage and maximum pulsed current ratings. In other words, MOSFETs are not generally RBSOA limited. There are possible exceptions to this rule, however. As noted in the dv/dt section outlined earlier in Chapter 4, rapid changes in drain-source voltages can limit the RBSOA (turn-off switching SOA) capability of the MOSFET due to the injected current into the C_{rss} capacitance inadvertently biasing-on the MOSFET.

Many practical power loads are inductive which can cause severe stress on the power switching device during turn-off. Due to the nature of an inductive load line, the switch, be it a power MOSFET or bipolar transistor, can simultaneously experience a high current and high voltage. Depending on whether the switch is unclamped (Figure 12-9a) or protected with a clamp circuit (Figure 12-9b) will determine the two energy limitations during

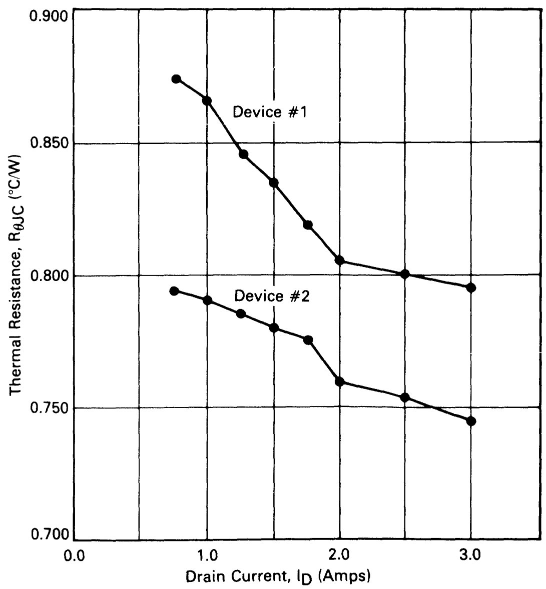


FIGURE 12-7 — THERMAL RESISTANCE OF MTM12N10 versus DRAIN CURRENT AT P_D = 50 W

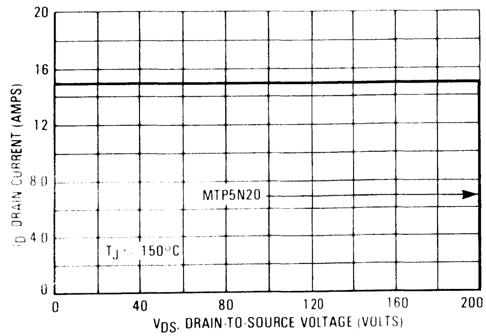


FIGURE 12-8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

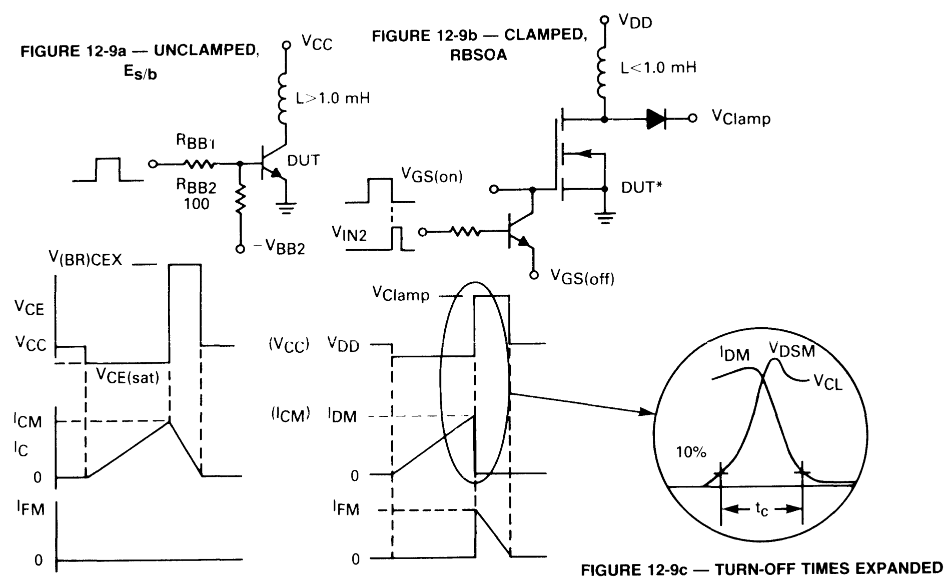
inductive turn-off: Second Breakdown Energy ($E_{s/b}$) and RBSOA.

Second Breakdown Energy ($E_{s/b}$)

Power transistors were originally characterized with an unclamped inductive load (Figure 12-9a). The Device Under Test (DUT), typically a low voltage, extremely rugged transistor, is turned on by applying a positive pulse to its base through a resistive network terminated in a reverse bias voltage V_{BB2}. Collector current then ramps up at a rate dictated by the time-constant of the relatively large inductance in the collector circuit. When the DUT turns off, the energy stored in the inductor ($E = 1/2LI_{CM}^2$) has to be dissipated in the transistor since there is no external circuit, or clamp, to "catch" this energy as the current ramps down. Also, immediately at turn-off, the collector-emitter voltage flies back up due to the "inductive kick" ($v = L\ di/dt$). If the stored energy is great enough and the transistor turn-off time fast enough, this voltage will fly back to the breakdown voltage of the device ($V_{(BR)CEX}$), causing the transistor to avalanche. The transistor thus has to dissipate the energy due to this unclamped operation by sustaining its breakdown voltage until the collector current falls to zero and the inductor discharges. The maximum energy that the device can sustain, defined as Second Breakdown Energy ($E_{s/b}$), is determined by increasing the collector current until the device fails. Usually this current is below the nominal operating current of the device since the transistor has to absorb the relatively high inductor energy and generally cannot sustain its maximum specified current. Theory and practice have shown that most low-voltage transistors have decreasing $E_{s/b}$ capability with increasing reverse-bias voltage due to current crowding.

The unclamped inductive loads stress the power MOSFET in a similar manner. Now, the falling drain current will cause the flyback voltage to avalanche the drain-source of the MOSFET ($V_{(BR)DSS}$).

The problem with this $E_{s/b}$ rating is that the derived energy is only related to that particular inductance and is highly dependent on its Q (quality factor, i.e., series re-



*Waveforms shown for MOSFET DUT.
Bipolar Terms in Parentheses.

FIGURE 12-9 — INDUCTIVE LOAD SWITCHING

sistance). Additionally, the inductance specified to achieve $E_{s/b}$ is generally quite large, 10 mH or greater, and does not represent the real world inductance seen in Switch-mode applications. Finally, and most important, most applications use some form of clamping to prevent drain-voltage breakdowns. For this reason, most high voltage switching transistors are specified with a clamped inductive load.

RBSOA

A more precise and definitive inductive turn-off rating is the clamped inductive turn-off rating labeled RBSOA. In the simplified test circuit of Figure 12-9b, the DUT is subjected to a real world clamped condition. The inductance need be only large enough to ensure that the flyback time is greater than the drain current fall time, generally resulting in inductances from 100 μH to 1.0 mH. These values also more accurately represent the leakage inductances encountered in switching applications.

To subject the device to the greatest stress during turn-off, the inductance should be of high Q to ensure that the peak drain current, I_{DM}, and flyback voltage, V_{DSM}, are simultaneously presented to the DUT, Figure 12-9c, resulting in a turn-off load line that approximates a rectangle. Under these conditions, I_D will start to fall when V_{DS} forward biases the clamp diode, at which time the stored inductor energy (current) will be transferred to the external diode circuit.

To determine the RBSOA capability of the device, I_{DM} is set to a typical operating current and the clamp voltage is increased until the transistor goes into second breakdown. Then other current levels are tested until the complete RBSOA curve is established. These second breakdown points relate to the energy dissipated in the device during turn-off, specifically the crossover time t_c, (Figure 12-9c) and represents the energy encountered in inductive switching applications, (whereas, the lower I_{DM} for the unclamped $E_{s/b}$ mode does not). Reverse biasing in this example is provided by a transistor clamp from the gate of the N-Channel MOSFET to either a negative voltage or ground.

Switching Safe Operating Area (SSOA)

The term Switching Safe Operating Area is the generalized SOA limitation during turn-on and turn-off of the power MOSFET. Turn-off switching SOA is equivalent to RBSOA for bipolar devices and will henceforth be used to describe this characteristic.

The straightforward method of determining the turn-off switching SOA is through destructively testing the power MOSFET in the clamped inductive turn-off circuit. This is accomplished by setting the drain current to a specified value by either adjusting the applied input pulse width (t_{PW}) or the drain supply voltage V_{DD} since $I_D \cong \frac{V_{DD}\, t_{PW}}{L}$. Then the clamp supply voltage is gradually increased until one of two conditions occurs. If the specified I_D is less than the I_{DM} rating, the clamp voltage can be increased until the device avalanches and begins dissipating the inductor's energy. Since the MOSFET is operating in an $E_{s/b}$ mode at this point, failures may occur.

At drain currents greater than I_{DM}, the device is operating outside its current ratings and the MOSFET may fail at clamp voltages less than $V_{(BR)DSS}$. In short, the MOSFET's SSOA curves guarantee that the locus of failures is outside the I_{DM} — $V_{(BR)DSS}$ boundaries. The SSOA curve shown in Figure 12-8 is applicable for both turn-on and turn-off of devices with switching times less than one microsecond.

Normally a destructive fixture is used to ensure that the fail points lie outside the turn-off SOA boundaries. This requires testing of many devices and device trends are difficult to determine. The use of a non-destructive fixture greatly simplifies establishing the SSOA ratings since usually only one DUT can be used to generate a complete turn-off switching SOA curve.

N-Channel Non-Destruct Turn-Off Switching SOA Test Fixture

In order to save the DUT from the normally destructive second breakdown energy, the stored inductive energy must be quickly diverted from the transistor to an external crowbar circuit. A test fixture, based on the work done at the United States National Bureau of Standards,[31] was designed to have the capability of crowbarring as much as 50 A and blocking as much as 1000 V. The 10 A crowbarred propagation delay was about 70 ns and the current rise time was about 40 ns. Triggering of the crowbar was accomplished by detecting the fast rate of change of the collapsing drain-source voltage once the device went into second breakdown. Using this test fixture, a complete SOA curve can often be formed using only one DUT; consequently, the DUT must sustain as many as 30 or 40 crowbars (second breakdowns) to establish the curve. Not all devices will survive so many crowbars without degradation or failure, but a large percentage do, allowing a relatively simple and non-ambiguous curve to be generated. Degradation is measured by a relatively large change in drain leakage current, I_{DSS}, after testing. For this magnitude of leakage current change, subsequent retesting will usually show a decrease in device turn-off SOA capability.

The main elements of the non-destruct SOA test fixture are illustrated in the block diagram of Figure 12-10. Of these blocks the most important are the Drive Circuit consisting of the $V_{GS(on)}$ and $V_{GS(off)}$ Transistor Switches, the Detector/Crowbar and a Pulse Generator capable of being inhibited when crowbarring occurs. Of secondary importance are the V_{DD} Switch, and a Greater than 10% Duty Cycle Lockout circuit. Also required is an externally connected inductor, typically about 200 μH.

Referring to Figure 12-10, the circuit operates as follows: An input pulse, V_{in}, is applied to the input of the Drive Circuit controlling the three respective switches, $V_{GS(on)}$, $V_{GS(off)}$, and V_{DD}. The $V_{GS(on)}$ switch supplies the positive turn-on gate voltage and concurrent with its turn-off, the $V_{GS(off)}$ switch is turned on. The drain supply is also turned on (V_{DD} switch) when positive gate voltage is applied and, to ensure proper system operation, will remain on for several microseconds (due to drive transistor storage time) after removal of the input pulse. During this on-time, the collector current ramps-up and, upon

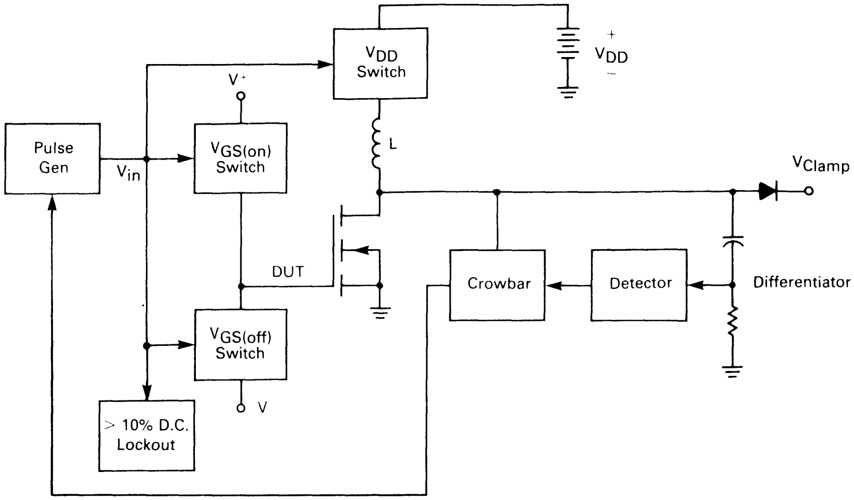


FIGURE 12-10 — BLOCK DIAGRAM OF THE N-CHANNEL NON-DESTRUCT TURN-OFF SWITCHING SOA TEST FIXTURE

turn-off, the drain voltage flies back. When the flyback voltage reaches the clamp voltage, the inductor current is transferred to the clamp circuit. The drain voltage will then fall at a relatively slow rate, typically a couple of hundred nanoseconds, as the energy stored in the inductor is completely discharged.

If, however, excessive energy is applied to the DUT during this switching time, the FET can go into second breakdown. Then the drain voltage falls very rapidly, possibly in less than 10 ns. When this occurs, the low R-C time-constant Differentiator detects this fast falling waveform — discriminating against the normal slow falling waveform — and produces a negative-going pulse which ultimately triggers the crowbar. The crowbar fires and the current in the DUT is quickly diverted to the crowbar, removing the turn-off energy stress from the transistor. The Pulse Generator is also disabled, preventing any successive pulses from being reapplied until the system is reset.

Drive Circuit

The drive circuit for the SOA test fixture is shown in Figure 12-11 and consists of the three aforementioned switches. A Darlington transistor, Q1, is used to buffer the CMOS-derived input pulse of 15 V from the drive circuit.

Positive gate voltage is generated by turning on the NPN transistor, Q2, with the positive going input pulse. This stage supplies drive to the PNP Baker-clamp-configured transistor, Q3, whose output feeds the gate of the DUT, turning it on.

Reverse bias is derived by differentiating the input pulse with the R1C1 network. The generated negative-going pulse, which is coincident with the trailing edge of the input pulse, then turns on PNP transistor, Q4, and the following NPN transistor, Q5.

This off-bias voltage pulse is set by R1C1 and, for the values chosen, is about 10 μs. Also, due to the trailing edge coincidence of the two pulses (plus approximately equal propagation delays through the two respective switches), the transition time between $V_{GS(on)}$ and $V_{GS(off)}$ can be relatively fast for some DUTs and operating conditions, approaching less than 200 ns.

The drain switch is used as a safety device, removing current from the inductor if the DUT were to fail short. This circuit utilizes two cascaded Baker-clamped monolithic Darlingtons (NPN Q6 and PNP Q7) to reach the 50 A capability of the fixture. The Baker-clamp diodes (D3, D4 and D5, D6) minimize the storage time of this switch after the DUT is turned off.

Once the DUT is turned off, the inductor-stored energy is dissipated through the two clamp diodes (D7 and D8 for high-voltage capability), the clamp supply and filter network, and Q7 clamp diode D9. Diodes D10 and D11 in the drain circuit of the DUT are used to prevent reverse drain currents from flowing and also to ensure that the crowbar saturation voltage is lower than the parasitic transistor second breakdown voltage, thus diverting the drain current.

Drain current can be monitored by the current loop as shown. Additionally, the current-sense resistor, R2, can be used to monitor I_D, but care must be taken in the layout to minimize ground loops which can distort this current replica. As in any high-speed, high-current switch, good RF techniques should be used in the layout.

Detector/Crowbar Circuit

As previously mentioned, an RC differentiator is used to discriminate between the normal V_{DS} fall time and second breakdown fall time; the components used are a 1.0 kV capacitor, C2, fixed resistor R3, and Sensitivity Control R4.

Originally, the output pulse from this network fired a 25 A

SCR as a crowbar, but the turn-on time of about 600 ns proved to be too long to save the DUT. What is required is a fast latching crowbar. This is now achieved by using a common-base-connected NPN transistor, Q10, as a level detector-pulse amplifier, triggering a fast, discrete monostable multivibrator (MV) consisting of PNP transistors Q11 and Q12. This 25 μs MV, which allows adequate time for the inductor stored energy to be dissipated, then drives the direct-coupled NPN transistor, Q13, and following PNP transistor, Q14, to a power level capable of turning on the crowbar. Diode D12 is used to block any noise pulses on the V_{DD} line from false triggering the monostable MV.

The crowbar consists of four parallel MJ10011 monolithic Darlington transistors (Q15–Q18) selected for V_{CEO} greater than 1000 V. This transistor, designed for horizontal deflection circuits, offers the best blocking voltage-switching speed tradeoff of the several different devices tested. By using fast, wide-band transistors throughout, propagation delay and rise time of 70 ns and 40 ns, respectively, were measured at an I_C of 10 A.

Diode D13 and resistor R5 prevent possible high dv/dt

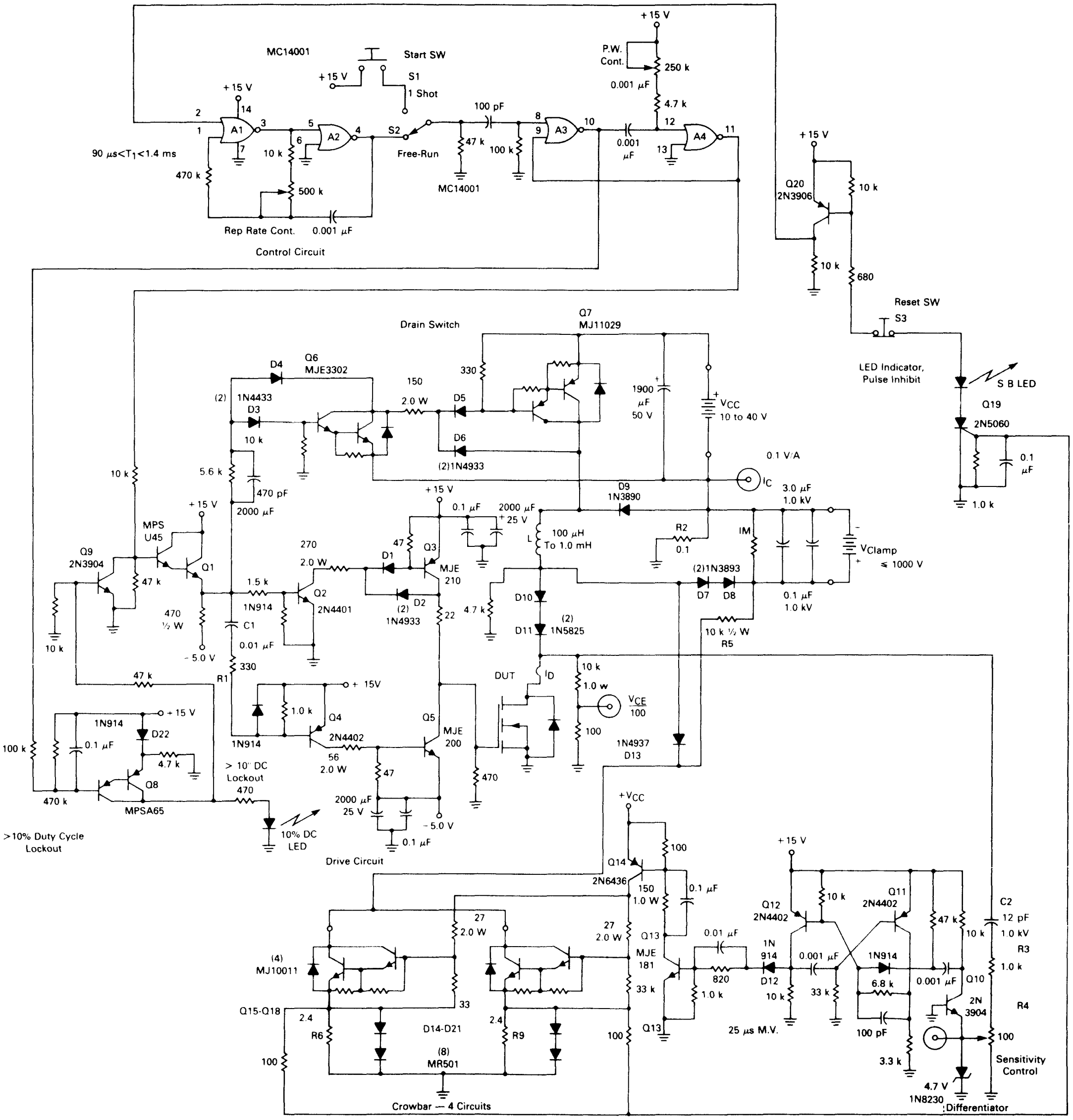


FIGURE 12-11 — N-CHANNEL POWER MOSFET NON-DESTRUCT TURN-OFF SWITCHING SOA TESTER 1000 V, 50 A

flyback voltages from falsely turning on the crowbar.

The resistor-diode networks (R6–9, D14–21) in the respective Darlington emitter circuits serve both as a ballasting-voltage clipping circuit and a crowbar indication source for the second breakdown LED indicator circuit.

Pulse Generator

The timing functions for the Non-Destruct Turn-off SOA Test Fixture are generated by a quad, 2-input NOR gate, MC14001. These gates are configured as an astable MV (gates A1 and A2) clocking a monostable MV (gates A3 and A4) for pulse-width generation. By setting the Rep-Rate Control and the Pulse-Width Control, periods of from 90 μs to 1.4 ms and pulse-widths of 4.0 μs to 180 μs are achievable.

The Control Circuit produces free running pulses whose duty cycle should be maintained at less than 10% (limited by the driver circuit resistor power ratings). One-shot operation can also be generated by simply setting switch S2 to the one shot position and depressing the pushbutton start switch S1, thus providing a trigger to the Pulse-Width Mono MV.

Complete N-Channel Non-Destruct SOA System

Included in Figure 11-11, the complete N-channel Non-Destruct Turn-off Switching Tester, are two other circuits not previously described. They are:

1. The Greater Than 10% Duty Cycle Lockout Circuit.
2. The LED Indicator/Pulse Inhibit Circuit.

The 10% Duty Cycle circuit integrates the input pulse train with an RC network in the base circuit of the small-signal PNP Darlington MPSA65 (Q8). The resultant dc base voltage is compared with the emitter reference voltage derived from a 1N914 diode (D20). At duty cycles greater than about 15–20%, the Darlington will turn-on, lighting a LED indicator and turning on the NPN 2N3904 (Q9) transistor clamp across the input of the MPSU45 emitter follower (Q1). This effectively limits the duty cycle and the power dissipated in the drive circuit.

The LED Indicator/Pulse Inhibit circuit is enabled when the crowbar fires. The control signal is derived from the emitters of the Darlington crowbars and fed to the gate of the second breakdown SCR (Q19), turning it on. Placed in the anode circuit of this SCR are the series-connected second breakdown LED, reset switch (S3) and base biasing resistors for the 2N3906 pulse inhibit transistor (Q20). Thus, when the SCR fires, the LED will turn on, indicating second breakdown. The inhibit transistor will also turn on, placing the input to astable MV (A1) high, thereby disabling the pulse train. The system is enabled by opening (depressing) the normally closed pushbutton reset switch, thus unlatching the SCR.

Characterizing Drain-To-Source Diodes of Power MOSFETs For Switchmode Applications

When turning off inductive loads with a semiconductor switch, some means must be used to suppress, limit or clamp the resulting "inductive kick" from exceeding the breakdown voltage of the switch. Various types of suppressors or "snubber" circuits such as Zeners, MOVs, RC networks and clamp or "free-wheeling" diodes are generally used. The energy stored in the inductor is diverted from the transistor at turn-off and is harmlessly dissipated in the snubber, thus protecting the transistor switch.

To protect single power MOSFET switches, the snubber can be placed across either the inductor or the MOSFET. A Zener diode or RC snubber circuit can protect the drain-source of the power MOSFET but a simple clamp diode across these terminals will not, as it will only come into operation if its reverse blocking voltage is exceeded. However, in the multitransistor configurations commonly used for switching regulators, inverters and motor controllers, clamp diodes across the semiconductor switches are frequently used (Figure 12-12). The diodes do not protect their respective FETs but rather the complementary FET. As an example, in the totem-pole configuration of Figure 12-12c, diode D2 protects Q1 and D1 protects Q2.

To illustrate this, assume Q2 is initially conducting, causing load current to flow up through the inductor from ground. When Q2 turns off, the inductive current will continue but now through D1, through the power supply V^+ and return to the ground side of the inductor. Consequently, the fly-back voltage will be clamped to V^+ (from V^-), resulting in an amplitude of 2.0 V^+ when V^+ equals V^-.

If the output power devices are power MOSFETs with D-S diodes, the question arises as to whether these diodes are capable of adequately clamping the turn-off inductive load current. In other words, do the diodes switch fast enough and can they take the commutated load current?

The following discussion characterizes the D-S diode of a number of power MOSFETs so that the circuit designer can make the performance/cost comparisons between using these internal diodes or discrete outboard ones.

Switching Characteristics

The important switching characteristics of clamp diodes in switchmode applications are reverse recovery time, t_{rr}, and turn-on time, t_{on}. Diodes with long t_{rr} times can cause excessive turn-on stress on the FET they should be protecting as both the diode and the FET will be conducting during this time interval. The result will be a feed through drain current spike which could exceed the forward bias SOA of the FET. If the diode has relatively slow t_{on} times or high overshoot voltage — modulation voltage $V_{FM(DYN)}$ — then, in a similar manner, the FET might not adequately be protected during inductive turn-off.

In the past, most semiconductor manufacturers would characterize and specify (if they did it at all) the internal diodes for switching, using the JEDEC suggested circuits of Figure 12-13a and 12-13b. There are several problems associated with these circuits; for one, they were originally developed for sine-wave rectifier applications. As such, the t_{rr} test circuit would produce a half sine-wave of controllable current amplitude, I_{FM}, and di/dt of the current fall time. However, since the current waveform was derived from a capacitor dump, tuned circuit, the resulting

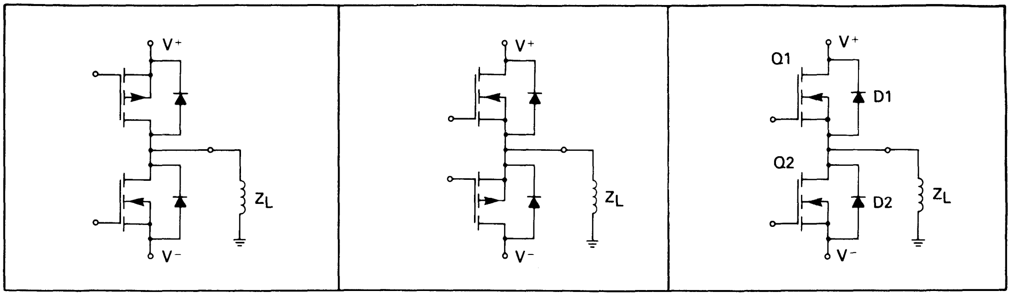


FIGURE 12-12a — COMMON SOURCE
FIGURE 12-12b — COMMON DRAIN D-S Complementary Push-Pull
FIGURE 12-12c — TOTEM-POLE

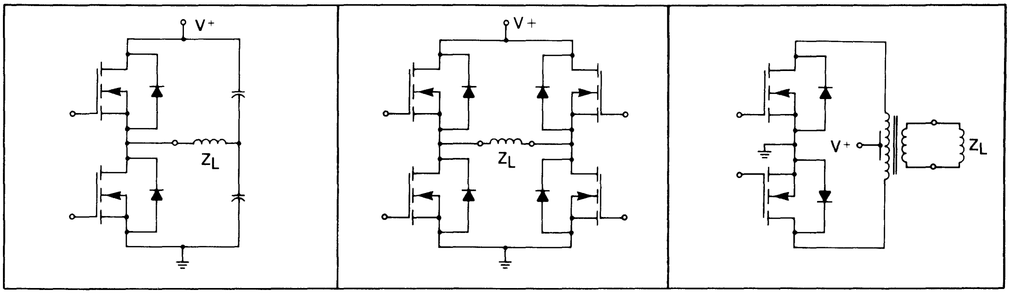


FIGURE 12-12d — 1/2 BRIDGE
FIGURE 12-12e — H BRIDGE
FIGURE 12-12f — TRANSFORMER PUSH-PULL

FIGURE 12-12 — MULTIPLE POWER FET DRIVE CONFIGURATIONS USING D-S DIODES

current duration t_p was dictated by I_{FM} and di/dt. Under some high di/dt conditions, t_p can become relatively short compared to the t_{rr} of the device under test (DUT) and consequently the diode is not fully turned on, thus producing inaccurate t_{rr} measurements. To ensure adequate DUT turn-on, t_p should exceed five times t_{rr}.

Second, since t_{rr} is dependent on I_{FM} and di/dt, what should these variables be set to? I_{FM} is obvious: it should be the diverted drain current, but di/dt could be anything, be it 25 A/μs or 100 A/μs, etc. In reality, this diode current turn-off time is controlled by the complementary FET turn-on time.

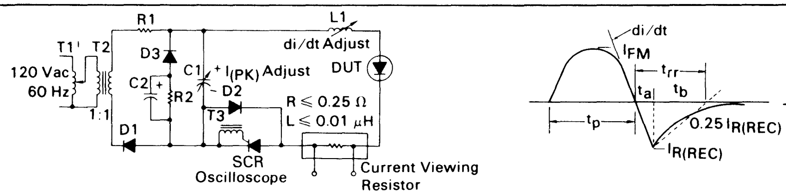


FIGURE 12-13a — REVERSE RECOVERY TEST CIRCUIT AND WAVEFORM

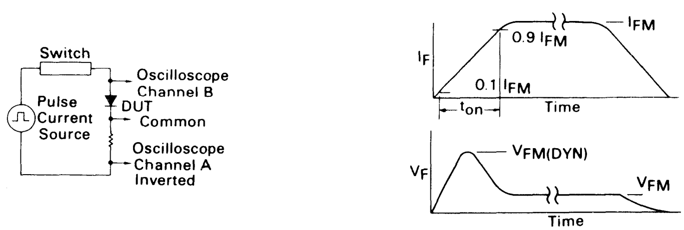


FIGURE 12-13b — DIODE TURN-ON TEST CIRCUIT AND WAVEFORMS

FIGURE 12-13 — JEDEC SUGGESTED DIODE SWITCHING TEST CIRCUITS

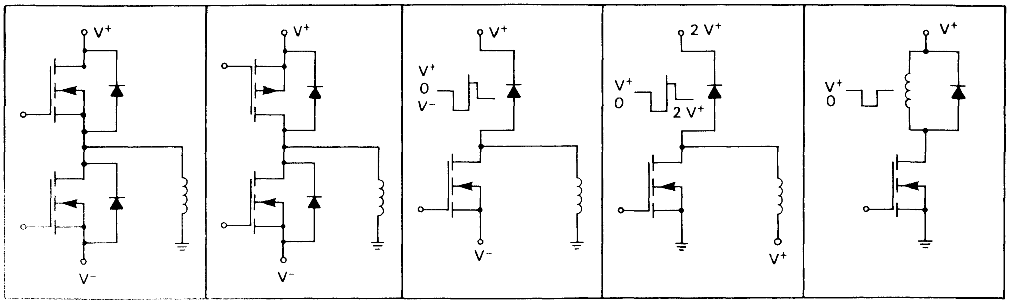


FIGURE 12-14a — TOTEM-POLE | FIGURE 12-14b — COMPLEMENTARY | FIGURE 12-14c — SIMPLIFIED CLAMP CIRCUIT | FIGURE 12-14d — LEVEL TRANSLATED | FIGURE 12-14e — TEST CIRCUIT

FIGURE 12-14 — EVOLUTION OF INDUCTIVE CLAMP TEST CIRCUIT

The problem with the t_{on} test circuit was the difficulty in defining and controlling the rise time of the current pulse applied to the DUT. Since this current pulse affects the measured $V_{FM(DYM)}$ and t_{on} of the DUT, its shape should be related to the real world conditions.

This is what the proposed test circuit does. Its configuration is derived from a typical two transistor Switchmode application, be it a totem-pole for characterizing N-channel D-S diodes or a complementary common source for characterizing P-channel D-S diodes (Figure 12-14). These configurations reduce to the simple, single-ended inductive clamp circuit (Figure 12-14e) whereby the clamp diode would be the D-S diode of either the N-channel FET (totem-pole) or the complementary P-channel FET.

The reverse recovery time is of greatest significance for continuous load currents common in switching inductive loads. Figure 12-15a describes the idealized current waveforms when a continuous inductive load current I_L is commutated between the FET (I_D) and clamp diode (I_F). Figure 12-15b shows the time expansion of both the leading and trailing edges of I_D and I_F. Note that the drain current fall time t_{fIC} controls the diode current rise time t_{fID} (or t_{on}) and in a similar manner, the dI_D/dt (or t_{rID}) of the drain current turn-on time dictates the dI_F/dt of the diode current turn-off time. Thus, the faster the FET switches, the greater is the di/dt applied to the diode. The diode di/dt then dictates the magnitude of the reverse recovery time t_{rr} and current $I_{RM(REC)}$. Since the current through the inductor is equal to I_D plus I_F the peak drain current I_{DM} at turn-on will consequently have the magnitude of I_{DM} impressed on it. This is illustrated in Figure 12-16 whereby the switching times of I_D and I_F are the mirror image of each other; the sum of the two waveforms would yield the inductor current, whose ripple magnitude is dependent on the switching frequency and load inductance.

An example of discontinuous and continuous load current waveforms are shown in Figures 12-17a and 12-17b respectively. Note that for the discontinuous case, where the inductor current I_L is allowed to completely discharge, the di/dt of I_F is extremely low, thus producing no I_{RM} or t_{rr}. For the continuous current case, the resultant di/dt produces significant I_{RM} and t_{rr}.

The size of the inductor used has little, if any, effect on the t_{rr} measurements as shown in Figures 12-18a and 12-18b; Figure 12-18a shows the full cycle and time expanded waveform of diode current for inductances of

FIGURE 12-15a — IDEALIZED CURRENT WAVEFORMS

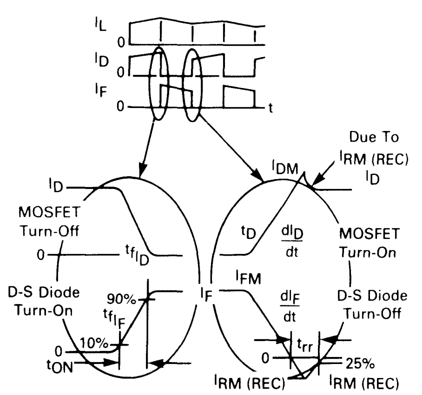


FIGURE 12-15b — WAVEFORMS TIME EXPANSION

FIGURE 12-15 — CONTINUOUS LOAD CURRENT SWITCHING WAVEFORMS

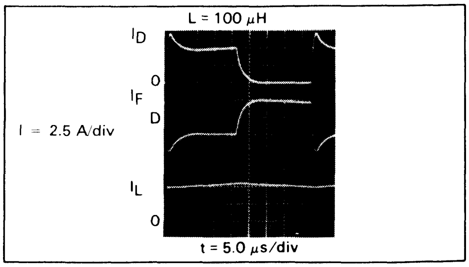


FIGURE 12-16 — SWITCHING CURRENTS OF A CLAMPED INDUCTIVE LOAD

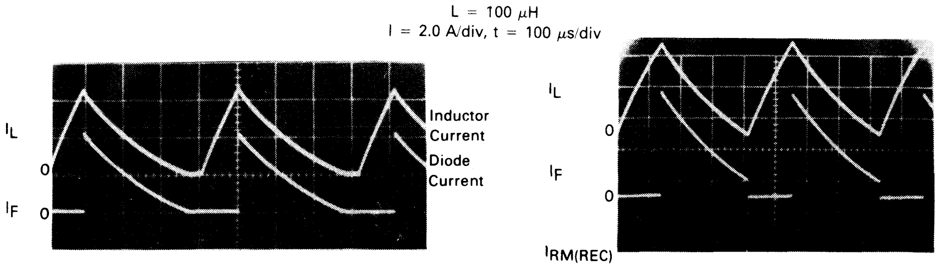


FIGURE 12-17a — DISCONTINUOUS LOAD CURRENT

FIGURE 12-17b — CONTINUOUS LOAD CURRENT

FIGURE 12-17 — THE EFFECT OF SWITCHING INDUCTIVE LOAD CURRENT ON t_{rr} AND $I_{RM(REC)}$ OF D-S DIODE

100 µH (air core) and Figure 12-18b for a 10 mH (iron core) inductor. The major difference is the magnitude of the ripple current, the larger inductor producing a more constant current source.

Test Circuit

The test circuit used for generating the diode switching characteristics, a translation of the "real world" circuit of Figure 12-14e, is shown in Figure 12-19. It consists of a CMOS, astable multivibrator (Gates G1 and G2) driving two parallel connected Gates 3 and 4 as a buffer. Potentiometer R1 varies the duty cycle of the approximately 25 kHz output which therefore sets the magnitude of the DUT current (along with V_{DD}). The positive-going output from the buffer is direct-coupled to turn on the NPN transistor Q1 and the following Baker-clamped PNP transistor Q2.

To produce an off-bias to the driver, which can shape its turn-off time and consequently the diode turn-on time, the negative going edge of the output pulse from the buffer is used. Capacitor C1 and resistor R2 form a differentiating circuit to produce the negative pulse for turning on PNP transistor Q3 and the following NPN transistor Q4. This transistor acts as the off-bias switch, applying to the driver a negative voltage pulse (approximately V−) coincident with the trailing edge of the input pulse and lasting as long as the R2C1 time constant, about 5.0 µs for the component values shown.

Switching Test Results

TMOS D-S diodes are usually tested at the rated continuous drain current. The supply voltage V_{DD} should be greater than 10 V to ensure that the DUT driver is operating with typical transconductance. Since the DUT current is a function of duty cycle and/or V_{DD}, reducing the input pulse width will allow a greater V_{DD} to be used, if so required.

Although it is not always possible to test the DUT with its real world supply voltage (i.e., high voltage devices with higher V_{DD}s than low voltage devices), the results would be more indicative if it were possible, since g_{fs} and switching speeds will vary somewhat with V_{DD}.

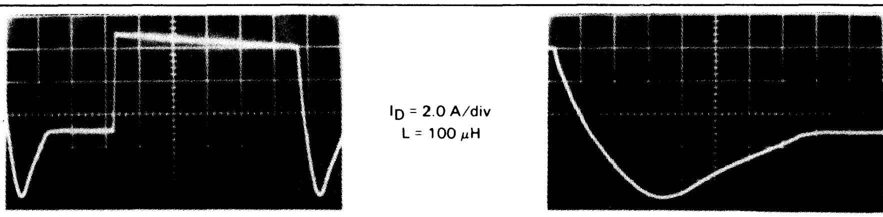


FIGURE 12-18a — 100 µH INDUCTOR

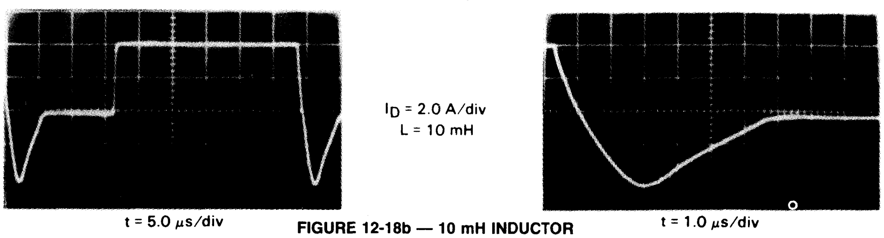
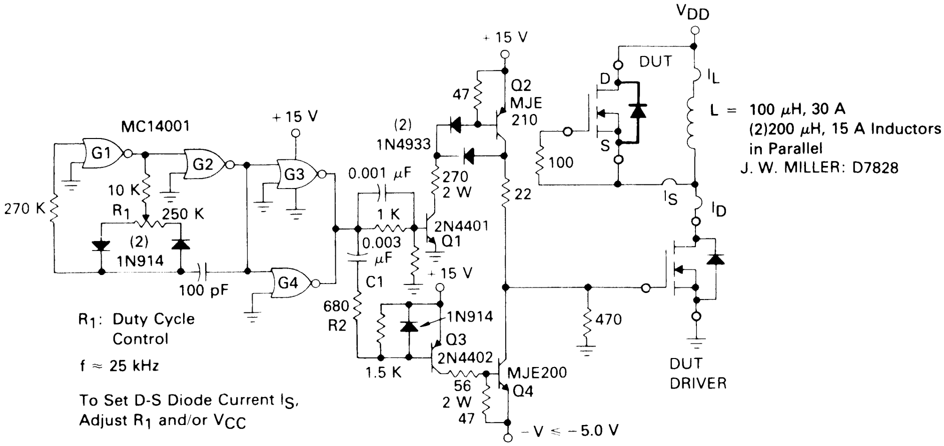


FIGURE 12-18b — 10 mH INDUCTOR

FIGURE 12-18 — THE EFFECTS OF LOAD INDUCTANCE ON D-S DIODE REVERSE RECOVERY CHARACTERISTICS



NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

FIGURE 12-19 — TMOS D-S DIODE SWITCHING TIME TESTER

Testing of several different FETs as a function of V_{DD} showed a second order variation in t_{rr} measurements. At any rate, to ensure measurement repeatability, V_{DD}, frequency, duty cycle and inductor specification should be listed. For most of the TMOS FETs tested, the inductor was either one 200 µH, 15 A rated air core or two in parallel (100 µH, 30 A). Whatever the conditions, the DUT driver and diode under test should be adequately heat sunk to minimize excessive case temperature rise.

The switching characteristics of an MTM15N15 as shown in Figure 12-20, and the complete switching results for the TMOS FETs tested are compiled in Table 1.

Also shown (Figure 12-21) for comparison, are switching photos of discrete rectifiers. Note that the fast recovery rectifier, as expected, had the lowest t_{rr} and that the standard rectifier, the largest t_{rr}. But of even more interest, the TMOS D-S diode had the lowest t_{rr} of all diodes tested (Table 1).

From this data, the circuit designer can now decide if the switching characteristics of the diode are adequate for his application.

Surge Characteristics

An equally important consideration is whether the diode can handle the commutated load current in which, under continuous load current, high duty cycle conditions, the energy can be quite high.

The TMOS D-S diode is the result of the parasitic NPN transistor across the FET and as such, actually has more die area available to conduct diode current than the FET has for drain current. For data sheet purposes, the drain-source diode current, labeled I_S, is made equal to the drain current I_D.

To verify these current ratings, the D-S diodes were subjected to two different pulse width surge tests, a one

MTM15N15
D-S Diode Current I_S (I_F)

FIGURE 12-20a — FULL CYCLE

I_S = 2.0 A/div
t = 5.0 µs/div

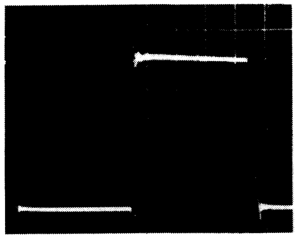


FIGURE 12-20b — D-S DIODE t_{rr}

I_S = 0.5 A/div
t = 100 ns/div

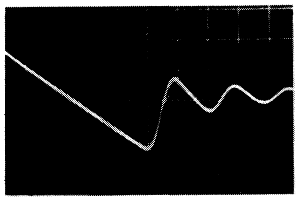


FIGURE 12-20c — D-S DIODE t_{on}

I_S = 2.0 A/div
t = 50 ns/div

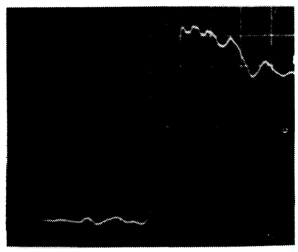


FIGURE 12-20 — SWITCHING CHARACTERISTICS OF A TMOS D-S DIODE

TABLE 1 — Switching and Surge Current Characteristics of TMOS D-S Diodes

			Switching					Surge Current	
Device	Type (Chan)	Spec I_D Cont (A)	I_{FM} (A)	di/dt (A/μs)	I_{RM} (A)	t_{rr} (μs)	t_{on} (μs)	300 μs 60 pps (A)	1.0 s 1 Shot (A)
MTM8N10	N	8.0	6.0	8.5	1.0	0.20	0.20	30	11
MTM15N06	N	15	10	9.0	1.0	0.24	0.29	80	24
MTM15N15	N	15	10	5.0	0.8	0.28	0.05	120	19
MTP1N60	N	1.0	1.0	10	0.3	2.0	0.03	25	6.0
MTP5N06	N	5.0	5.0	3.7	0.24	0.14	0.09	50	12
MTP25N06	N	25	25	10	1.0	0.20	1.0	140	35

second, one-shot pulse and a 300 μs, 1.8% duty cycle (60 Hz rep rate) pulse train. The one second test, which approximates a dc test, was run with the DUT bolted to a four inch square copper heat sink, initially water cooled and then in free air. The DUT forward current was then increased until the device was destroyed. The test results on one product line for the water cooled versus free air cooled were virtually identical so all subsequent tests were done in free air. The results of these tests are shown in the surge current sections of Table 1.

For power dissipation purposes and clamping efficiency determination, the typical forward characteristics of the diodes were also taken, as shown in Figure 12-22. These V_F-I_F curves were derived from a curve tracer using a 300 μs current pulse at 60 PPS; the low duty cycle ensured low case temperature readings. For comparison purposes, Figure 12-23 describes the forward characteristics of discrete diodes under the same test conditions. Knowing the voltage drop and current, the diode dissipation can be calculated. For any combination of power dissipation, the total diode and FET dissipations should not exceed the rating of the devices. After determining the switching characteristics and the power handling capability of the diodes, a cost/performance trade-off can be made. If the switcher is in the development phase, it is relatively simple to determine the effects of using the internal monolithic diode over a discrete, outboard diode, i.e. measuring case temperature rise, current and voltage waveforms, load lines to ensure safe SOA, device and system efficiency, etc.

Diode Current I_F = 0.5 A/div. t = 1.0 μS/div

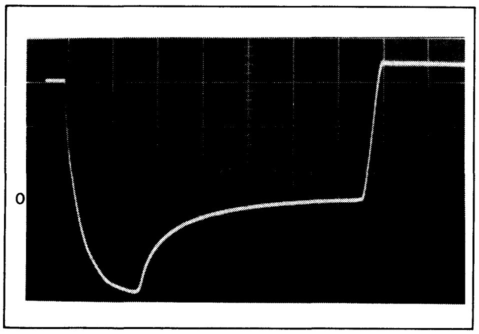


FIGURE 12-21a — 1N4001 STANDARD RECTIFIER

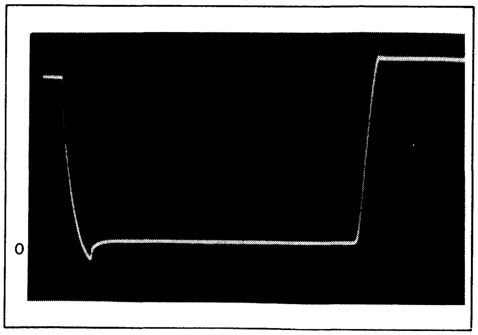


FIGURE 12-21b — 1N4935 FAST RECOVERY RECTIFIER

FIGURE 12-21 — COMPARISON OF WITH DISCRETE RECTIFIERS
FOR REVERSE RECOVERY CHARACTERISTICS

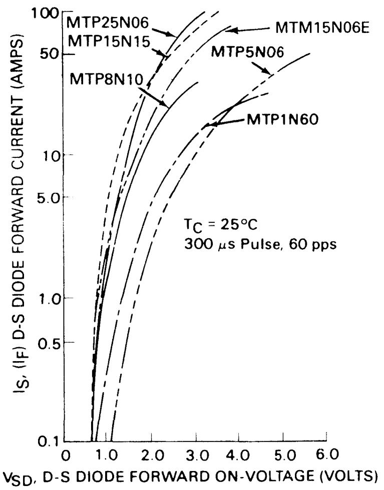


FIGURE 12-22 — FORWARD CHARACTERISTICS OF POWER MOSFETs D-S DIODES

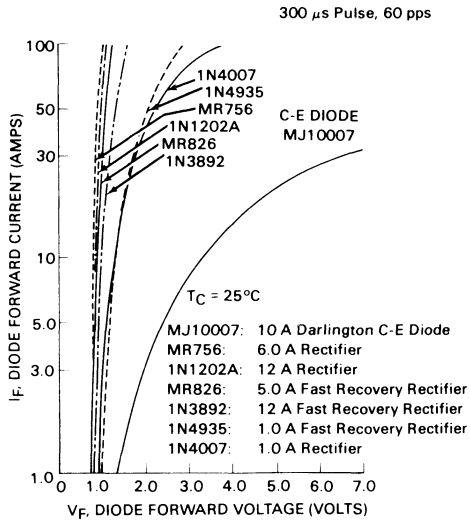


FIGURE 12-23 — FORWARD CHARACTERISTICS OF DISCRETE RECTIFIERS

Thermal Measurements

Steady State Thermal Resistance Measurements

It is a well known fact that, for reliable operation of a semiconductor, junction temperature is of great concern. All semiconductor die have a critical temperature which must not be exceeded or failure will occur. Also, semiconductor operating life can be either extended or shortened by its operating temperature.

The usual semiconductor die is enclosed in some type of package which prevents a direct temperature measurement. Due to the inaccessibility of the die, an indirect method must be used to determine the junction temperature. A common method is to use a temperature sensitive electrical parameter. The parameter used can vary, depending upon the type of semiconductor measured.

A basic block diagram for steady-state thermal resistance measurements for bipolar transistors is shown in Figure 12-24. The forward biased base-emitter-junction is used as the temperature sensitive parameter. This junction is calibrated at an elevated temperature in the forward direction, with a low calibration current (I_M), and should be in the linear region above the diode knee. Also, I_M should not contribute significantly to junction temperature nor turn-on the transistor; typical values are 2.0 to 10 mA.

The calibration procedure can be performed in a temperature chamber, with the temperature set for a normal operating temperature value for the semiconductor being measured. A typical temperature for a silicon die is around 100°C. The base-emitter forward voltage is measured and recorded at I_M and at the calibration temperature.

After calibration, a power switching fixture (Figure 12-24) is used to alternately apply and interrupt the power to the test device. The transistor is operated in the active region and power dissipation can be adjusted by varying I_E and/or V_{CE} until the junction is at the calibration temperature. This condition is known by monitoring the base-emitter voltage during the time when I_M only is flowing, with either an oscilloscope or a sample-and-hold circuit. When V_{BE} is equal to the value obtained in the calibration procedure, the junction temperature is known. The case temperature is noted at this time, as well as I_E and V_{CE}.

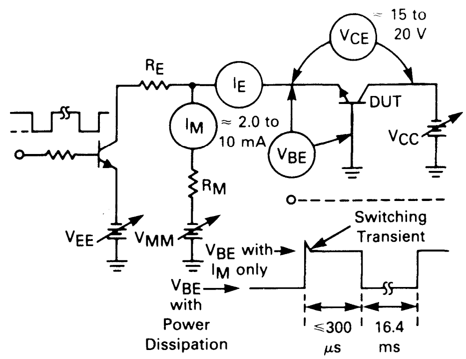


FIGURE 12-24 — BASIC BLOCK DIAGRAM OF STEADY STATE THERMAL RESISTANCE TEST CIRCUIT FOR BIPOLAR TRANSISTORS

The heating period is long, so the temperature of the transistor case is stabilized and the interval of power interruption short, usually 300 μs, so junction cooling will be minimal.

The steady state thermal resistance can be easily calculated from the information obtained in the calibration and power dissipation procedures. The simple formula is derived from the basic thermal resistance model (Figure 12-25) showing the thermal to electrical analogy for a semiconductor.

Steady state thermal resistance, junction-to-case, is as follows:

$$R_{\theta JC} = \frac{T_J - T_C}{V_{CE} \times I_E} \quad \text{or} \quad \frac{\Delta T}{P_D}$$

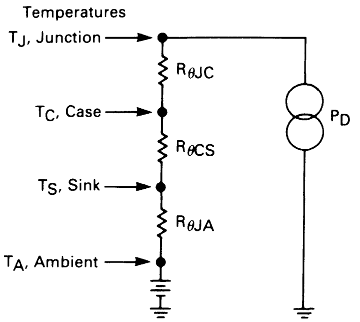


FIGURE 12-25 — BASIC THERMAL RESISTANCE MODEL SHOWING THERMAL TO ELECTRICAL ANALOGY FOR A SEMICONDUCTOR

For junction-to-case measurements, sufficient heat sinking should be provided to prevent excessive junction temperature. Measurement accuracy is improved with a large temperature delta between the junction and case. This delta can be achieved by using an efficient heat sink permitting a power dissipation (I_E V_{CE}) of sufficient magnitude to reach the calibration temperature.

Using Temperature Sensitive Parameters for Measuring Power MOSFETs Thermal Resistance

In order to determine the thermal resistance of any semiconductor device, an accurate and repeatable method of measuring the device temperature is required. The linear temperature dependence of the on-voltage of a forward biased semiconductor junction has proven to be a reliable parameter and is consequently used for bipolar transistors (emitter-base or collect-base junctions), rectifiers, zeners and thyristors. Because of their intrinsic D-S diode, this technique is also applicable to TMOS power MOSFETs.

When measuring the thermal resistance of power MOSFETs, the gate-source threshold voltage or the drain-source on-resistance $r_{DS(on)}$ can be used in addition to the on-voltages of the drain-source diode. Knowing the temperature characteristics of these parameters — by measuring the voltage or resistance variations with temperature in an oven, as an example — the device temperature, when powered, can be determined and the thermal resistance can be calculated.

These temperature sensitive parameters (TSP) of a power MOSFET with their approximate temperature coefficients are listed as follows:

Drain-Source Diode ≈ −2.0 mV/°C

Gate-Source Threshold Voltage ≈ −2.0 to −6.0 mV/°C

Drain-Source On-Resistance ≈ +7.0 mΩ/°C when $r_{DS(on)} = 1.0\ \Omega$

How these TSP can be measured is described in the simplified schematics of Figure 12-26, with Figure 12-26a using the D-S diode, Figure 12-26b, the $V_{GS(th)}$ and Figure 12-26c, the $r_{DS(on)}$.

D-S Diode TSP

Generally, the most often used circuit for measuring $R_{\theta JC}$ of power MOSFETs uses the D-S diode. When electronic switches S1 and S2 are in position 1, the FET is biased on and the heating power ($V_{DS}I_D$) is applied to the FET for a relatively long period. Then the switches are thrown to position 2 for a short period of time (sense time) so that the FET temperature will not change appreciably. Next, the FET is turned off and a constant current I_M (the same sense current at which the TSP was temperature calibrated) is applied to the forward biased D-S diode. By measuring the forward voltage drop of the diode and comparing it to the calibration curve, the FET junction temperature can be ascertained. Knowing the input power and the junction temperature, the thermal resistance can be calculated. In practice, the input power, either voltage or current, is varied until the D-S diode drop is equal to a calibration point, thus simplifying the test procedure by not having to generate a complete calibration curve.

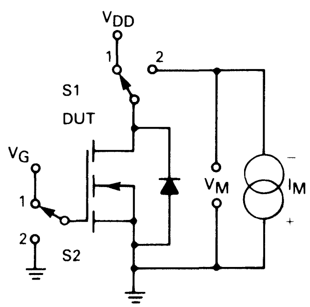


FIGURE 12-26a — DRAIN-SOURCE DIODE VOLTAGE

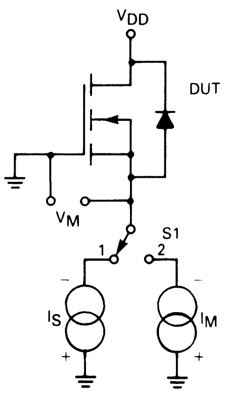


FIGURE 12-26b — GATE-SOURCE THRESHOLD VOLTAGE

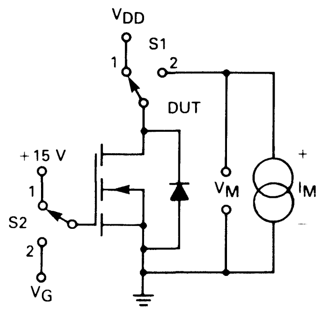


FIGURE 12-26c — DRAIN-SOURCE ON RESISTANCE

FIGURE 12-26 — CIRCUIT CONFIGURATIONS FOR MEASURING TSP

Gate-Source Threshold Voltage TSP

This thermal resistance test circuit is extremely useful for measuring $R_{\theta JC}$ of GEMFETs since this device has no parasitic diode. As in the D-S diode tester, heating power is applied to the DUT when switch S1 is in position 1. Then, switch S1 is briefly thrown to position 2, applying the sense current to the FET (I_D at $V_{GS(th)}$) and the gate-source threshold voltage is measured. Input power (V_{DS}-I_S) is varied to make $V_{GS(th)}$ equal to the elevated temperature, calibration reading resulting in a known junction temperature and thus $R_{\theta JC}$.

Drain-Source On-Resistance

This circuit is conceptually similar to the D-S diode tester. However, now when the switch is in position 2 (Sense Time), a positive constant current I_M and +15 V gate bias are applied to the device, turning it on. I_M should be of a value to produce about 0.5 V V_{DS}. The voltage V_{DS} measured (V_M) is related to $r_{DS(on)}$ by:

$$r_{DS(on)} = V_M/I_M$$

Thermal Test Fixtures

D-S Diode Thermal Fixture

$R_{\theta JC}$

The D-S diode Thermal Fixture, shown in Figure 12-27, is partially an implementation of the simplified circuit of Figure 12-26. It also contains circuitry for measuring transient thermal resistance r(t) and the analogue circuits for reading out the drain-source diode forward voltage and input power (V_{DS} and I_D). Thermal resistance is measured when the Mode Selector Switch S1 is in position 1, $R_{\theta JC}$. System timing is line synchronized and is derived from the Schmitt trigger (gates G1A and G1B) shaping circuit clocking the 300 μs Sense Time Monostable Multivibrator (gates G2A and G2B). Thus, the power MOSFET DUT is turned on via the Drain Switch circuit (cascade transistor Q1 and Q2) and unclamped gate transistor Q3 for 8.0 ms (full-wave rectified line rate minus 300 μs) and off for the 300 μs sense time. Drain current is set and readily controlled by I_D Control potentiometer R1 in the gate-source, closed loop, regulator circuit (op-amp U5).

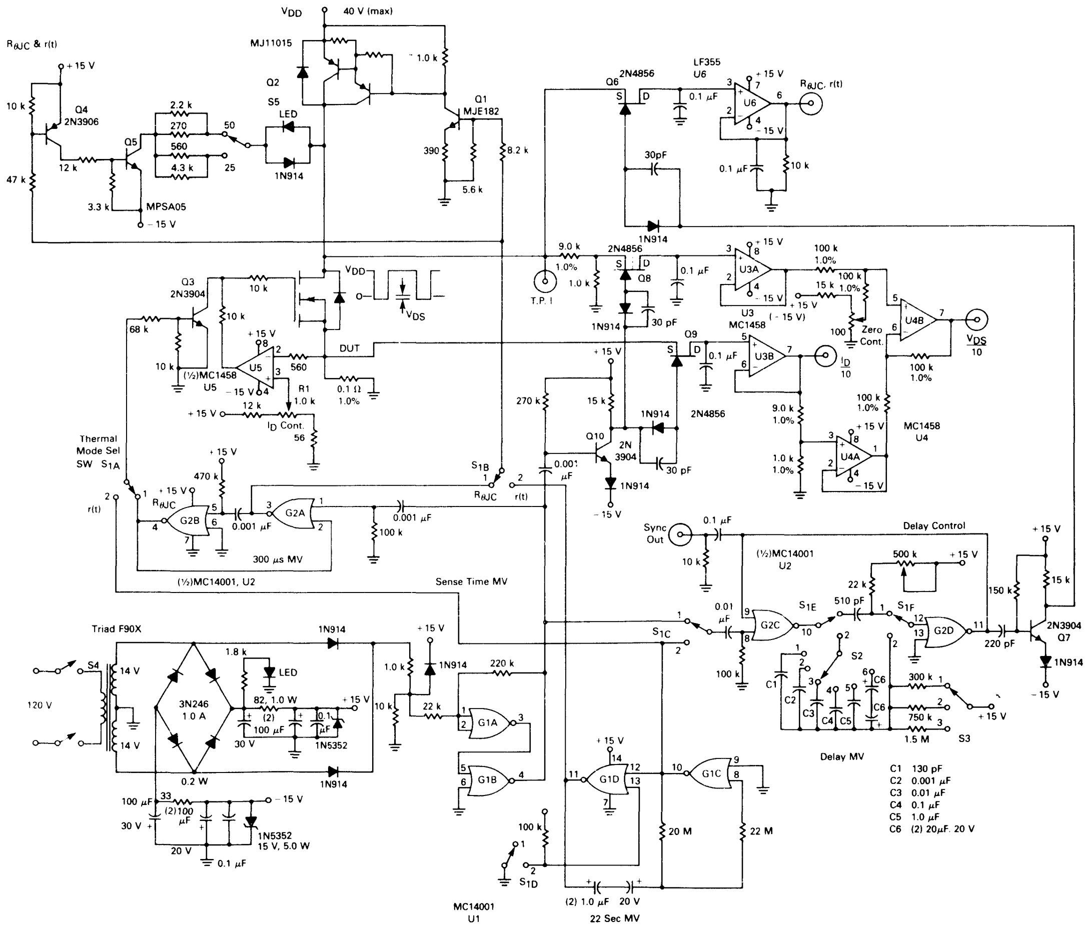


FIGURE 12-27 — POWER MOSFET D-S DIODE THERMAL FIXTURE

During the sense interval, DUT power is turned off (Q2 is off, Q3 is on) and the sense current I_S is applied to the now forward biased D-S diode by means of turned on transistors Q4 and Q5. The resultant D-S diode voltage can be observed by a scope or measured by the Sample and Hold circuit consisting of series FET switch Q6, buffer amp U6, sample driver Q7 and line synchronized, Delay Monostable MV gates G2C and G2D. The Delay Control of this MV allows the sample pulse to be positioned some time after the start of the Sense time so as to measure the settled voltage of the D-S diode, ignoring the possible thermal and/or electrical switching transients on the leading edge of the sense pulse. This delay time is typically 50 μs to 150 μs.

Using similar sample-and-hold circuitry, the applied power ($V_{DS/10}$ and $I_{D/10}$) can be measured. This is accomplished by the respective FETs Q8 and Q9, sample driver Q10, buffer U3A and U3B and difference connected op-amps U4A and U4B.

Transient Thermal Resistance r(t)

Transient thermal resistance, r(t), is measured when switch S1 is in position 2. Now the system timing is derived by the 22 second astable MV (gates G1C and G1D) which turns the DUT on and off for about 11 seconds each. During the off time, cooling cycle, the voltage of the D-S diode can be measured at any selected period of time. This is accomplished by selecting the various resistor-capacitor timing components of the Delay MV, thus positioning the sample pulse accordingly. The six switchable capacitors, by means of Selector Switch S2, will produce the six time decades of control (100 μs to 10 s) and the three resistors (switch S3), the multipliers within the decade, e.g., 0.2, 0.5 and 1.0.

Gate Threshold Voltage $V_{GS(th)}$ Thermal Fixture

The Gate-Source Threshold Voltage ($V_{GS(th)}$) Thermal Fixture, Figure 12-28, was specifically designed for measuring the thermal resistance of GEMFETs as this device does not have a D-S diode. Since it detects temperature

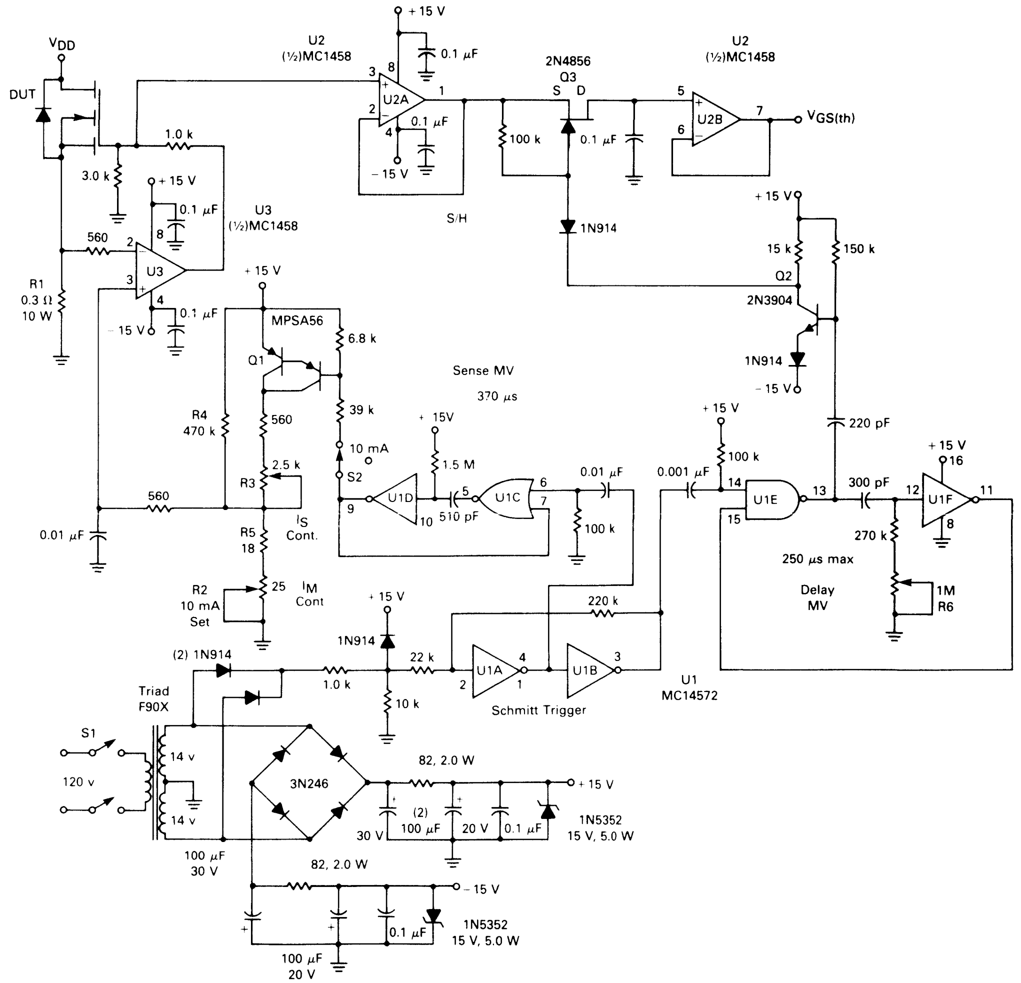


FIGURE 12-28 — POWER MOSFET $V_{GS(th)}$ THERMAL FIXTURE

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2-12

induced variations in the gate-source threshold voltage, it can also be used for power MOSFETs. Its line synchronization and current regulator loop around the gate and source make it very similar to D-S Diode Thermal Fixture. The major difference is the setting of the two different drain currents (or source currents), the power current, I_S, and sense current I_M. This is accomplished by switching two different reference voltages to the positive input of the loop regulator op-amp U3. As in any regulator loop of this type, the voltage at the negative input of the op-amp, as derived from the voltage drop across the source sense resistor R1, will be driven by the closed loop to a value equal to the reference input. Thus, if a heating current, I_S, of say 10 A is required, the reference voltage should be 3.0 V (10 A x 0.3 Ω). If a sense current I_M of 10 mA is specified, V_{REF} should be 3.0 mV.

Although most power MOSFETs are specified for a 1.0 mA drain current at $V_{GS(th)}$, the 10 mA level was chosen for measurement simplicity; in reality, there is negligible difference in the test results at either currents.

As in the D-S Diode Fixture, the system timing is line synchronized by Schmitt Trigger U1A and U1B, whose complementary outputs are used to clock the 370 μs sense MV (U1C and U1D), and the variable delay MV (U1E and U1F) for the sample pulse. This type of line synchronization offers several advantages: at high power heating drain currents, it simplifies the oscilloscope viewing, particularly when the external power supplies are not well regulated, and it is easily derived from one hex gate CMOS IC MC14572.

During the 370 μs sense time, the output of U1D is high; thus, PNP Darlington, Q1 is Off and the reference voltage is determined solely by the voltage divider R2 (the 10 mA Set Control), R4 and R5. To set R2, switch S2 is opened and the drain current is monitored for the required 10 mA.

When U1D goes low for the approximate 8.0 ms power cycle, Q1 is turned on, placing R3, the I_S control, into the reference voltage circuit. Consequently, the reference voltage will be switched from the 3.0 mV sense voltage to the I_S control voltage.

During the sense time the magnitude of the gate-source voltage, can be monitored with a scope or read out with the sample-and-hold circuit consisting of FET series switch Q3, buffer amps U2A and U2B, sample driver Q2 and delay MV U1E and U1F. Power to the DUT is then varied, either V_{DS} or I_D, to make $V_{GS(th)}$ equal to the calibrated value; thus, T_J and P_{IN} are known and $R_{\theta JC}$ can be calculated ($R_{\theta JC} = \frac{(T_J - T_C)}{P_{IN}}$).

Measuring Power MOSFET Capacitances

The internal capacitances of a power MOSFET are viewed from the outside world as the three device capacitances, C_{gs}, C_{gd} and C_{ds} (Figure 12-29).

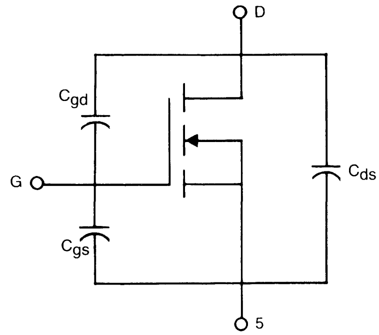


FIGURE 12-29 — DEVICE CAPACITANCES

For the Common Source configuration, the device capacitances are combined to reflect the capacitive reactances presented to the drive source and load. These composite capacitances are:

C_{rss} — Reverse Transfer Capacitance
C_{iss} — Common Source Input Capacitance
C_{oss} — Common Source Output Capacitance

C_{rss} is the capacitance between the drain and gate terminals with the source ac-guarded. C_{iss} is the capacitance between the gate and source with the drain ac-short-circuited to the source. C_{oss} is the capacitance between drain and source with the gate ac-short-circuited to the source. Table 2 summarizes the relation between the Common Source and device capacitances.

TABLE 2

COMMON SOURCE		DEVICE
C_{rss}	=	C_{gd}
C_{iss}	=	$C_{gd} + C_{gs}$
C_{oss}	=	$C_{gd} + C_{ds}$

C_{rss}, measured between gate and drain of the MOSFET, consists primarily of a MOS capacitance between the polysilicon gate and the accumulation section of the MOSFET's drain region. The major component of C_{gs} is between the polysilicon gate and the source metallization. An additional component of C_{gs} is a MOS capacitance between the gate structure and the "back-gate" regions (channel capacitance). C_{ds} is the PN junction capacitance between the drain and the "back-gate" regions. C_{gd} and C_{ds} (and, to a lesser extent, C_{gs}) are strongly voltage dependent.

Modern capacitance meters (e.g. Boonton 74BD, HP4275A) are "guarded" and have provisions for superimposing dc bias on the measurement loop to the component being tested.

Guarded meters are shielded and so configured that the displacement current (Im) detector circuitry is above ground (Figure 12-30). Any leakage current (or current through a three-terminal composite capacitor) is bypassed around the detector, thus only current through the capacitance under test is detected and measured. A more thorough discussion of guard circuitry can be found in (1-2).

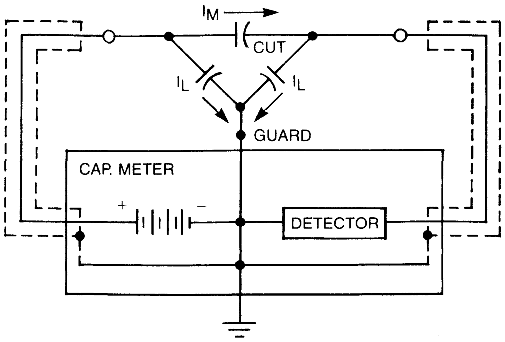


FIGURE 12-30 — "GUARDED" CAPACITANCE MEASUREMENT

A guarded arrangement is seen in Figure 12-31, the test configuration for C_{rss}. As shown, the measurement loop encloses only C_{gd}. Any displacement current through C_{gs} or C_{ds} is bypassed around the measurement loop; only C_{gd} displacement current enables the measurement circuitry. Dc bias voltage, however, may be placed in the "L" bus appearing between drain and source, and allowing measurement of C_{rss} at various voltages.

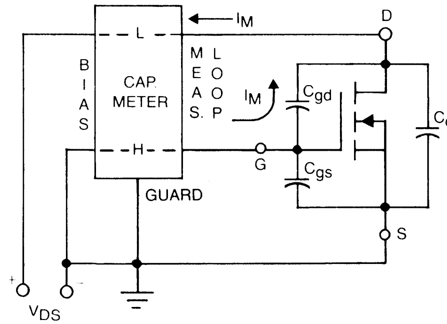


FIGURE 12-31 — C_{rss} TEST CONFIGURATION

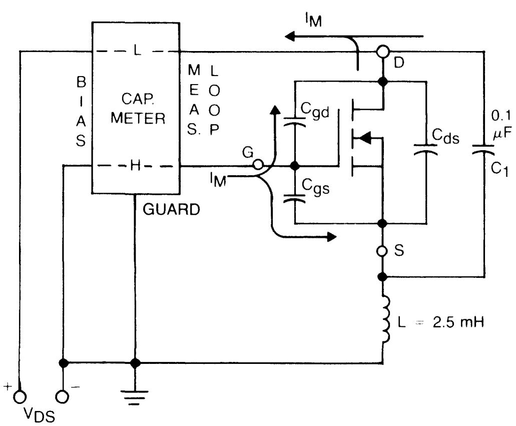


FIGURE 12-32 — C_{iss} TEST CONFIGURATION

To measure C_{iss}, the displacement current through C_{gs} must be included in the measurement loop. One easy way to accomplish this would be to "hard-wire" the source to the drain, however, such an arrangement would preclude measurement at any drain-source voltage other than zero. A better way is illustrated in Figure 12-32. In this arrangement the source is ac shorted to the drain by C_1, thus including C_{gs} in the measurement loop. RFC_1 provides a dc return from ground to the source, enabling measurement of C_{iss} versus V_{DS}.

Measurement of C_{oss} is similarly straightforward. The simplest way to include the C_{ds} displacement current in the C_{rss} measurement loop is to "hard-wire" the source to the gate (Figure 12-33). Such an arrangement still allows the desirable feature of measurement at various drain-source voltages.

An inspection of the measurement configurations of Figures 12-31, 12-32 and 12-33 shows that they differ only in termination of the device source terminal. Figure 12-34 embodies Figures 12-31, 12-32 and 12-33 in one test set-up. A two-pole, three position rotary switch connects the source terminal to the appropriate nodes for the three common-source capacitance measurements. The 50 kΩ resistor between gate and source insures proper termination of the MOSFET in case of capacitance meter failure. A pushbutton enables the drain-source bias voltages. P-Channel devices may be measured simply by inverting the connections of the biasing power supply.

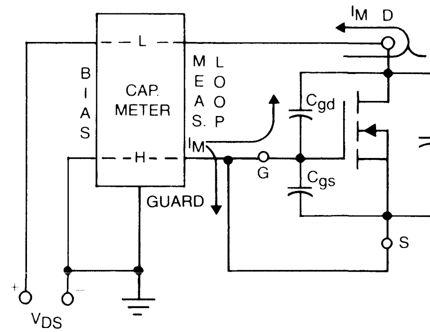


FIGURE 12-33 — C_{oss} TEST CONFIGURATION

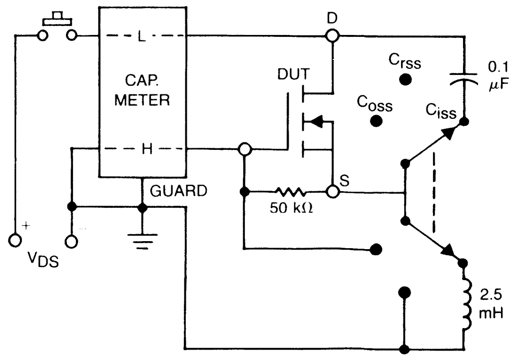


FIGURE 12-34 — COMMON SOURCE CAPACITANCE TEST SET-UP

Figure 12-35 shows a typical family of Common Source Capacitance curves derived with use of the test set-up of Figure 12-34.

For reasons detailed in Chapter 6, Figure 12-35 is not a complete picture of the variation of C_{rss} and C_{iss}. In brief, the missing data are the changes that occur as the device moves deep into the on-state. The circuit shown in Figure 12-36 provides a means of measuring the additional capacitance variation, which is shown to the left of zero in Figure 12-37.

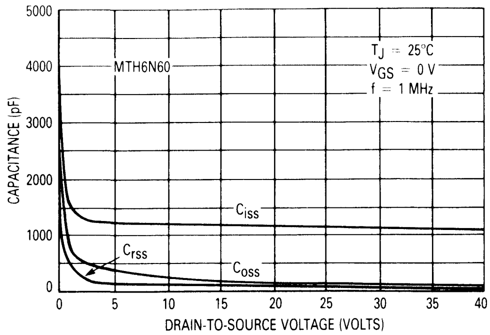


FIGURE 12-35 — C_{iss}, C_{rss} AND C_{oss} VARIATION OF THE MTH6N60

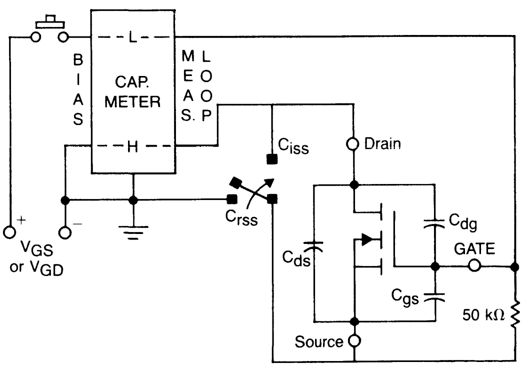


FIGURE 12-36 — CIRCUIT USED TO MEASURE C_{iss} AND C_{rss} OF A POWER MOSFET WHEN IT IS IN OR ENTERING INTO ITS ON-STATE

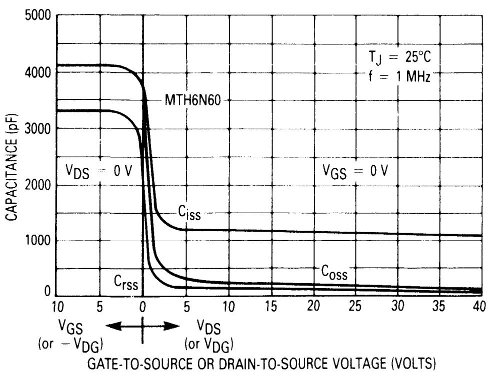


FIGURE 12-37 — COMPLETE REPRESENTATION OF CAPACITANCE VALUATION OF THE MTH6N60

CHARACTERIZING POWER MOSFETs FOR UNSPECIFIED PARAMETERS

Although many modern data sheets characterize power MOSFETs specifically for operation in power conversion equipment, it is not practical to guarantee operation for every conceivable set of operating conditions. Therefore, equipment design frequently requires the use of power MOSFETs in conditions for which they are not specified. To compensate for the unknowns, use of a relatively large design sample is common practice. A relatively large sample gives a feeling of statistical security. All too often, the sample comes from transistors purchased in a single group, with predictably unfortunate results. A common scenario goes something like this.

Design Scenario

The designer orders as many as 100 of each of the key components to try in this equipment. He may simply verify that the equipment performs satisfactorily, or he may attempt to do a worst case analysis based upon parametric variations. Either way, it is believed that the 100 pieces constitute a statistically conservative sample.

With performance and worst case analysis indicating satisfactory performance, the design is finalized. Preproduction begins with components from the initial 100 piece order. Except for routine debugging, all goes well. Hard tooling is committed. Initially, or months, or even years later, the equipment begins to fail as it comes off the production line. Perhaps with less fortune, the equipment fails in the field. The reason, which is at first elusive, boils down to the equipment requiring a combination of non-reproducible characteristics in one or more of the key components.

All too many people have been adversely affected by just this kind of scenario. Yet, minimizing the risks associated with component selection is considerably easier than might be expected. Guidelines for minimizing the risks, with respect to power MOSFETs, are presented here. In addition to general guidelines, a straightforward method for determining safe operating safety margin is highlighted. The discussion begins with statistical concepts.

Semiconductor components have three statistical populations which are relevant to the equipment designer. They are:

1) Wafer lot
2) Wafer
3) Individual component

A wafer lot is a group of wafers which are processed together. A typical example for switching power supply output transistors is fifty wafers per lot and 100 transistors per wafer, for a total of roughly 5,000 transistors per wafer lot. The statistical considerations arise from the way semiconductors are batch processed in wafer lots. The cookie analogy is a helpful illustration.

Suppose a baker has three groups of raw cookies. Each group is sufficiently large to fully use available space in the baking oven. The three groups are therefore baked sequentially. The first group is slightly overdone and relatively dark. The second group comes out slightly underdone and very light. The third group turns out medium.

Lightness or darkness of the individual cookies will vary somewhat within each group, but probably not by very much. Variations in color are much more dependent upon which group a cookie was baked in than which individual cookie was chosen from a given group. A sample of cookies chosen from any one group will poorly predict the variations expected from the baking process.

Semiconductor characteristics vary in much the same way. Many characteristics are far more dependent upon the wafer lot in which a device is processed than upon which individual device is chosen from a given wafer lot. An illustration is shown in Figure 12-38.

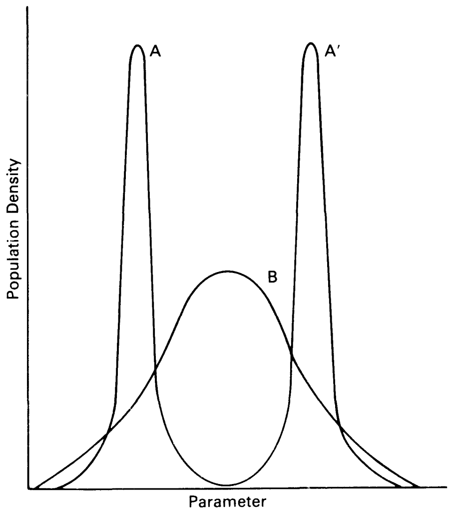


FIGURE 12-38 — EXAMPLE PROBABILITY DISTRIBUTIONS

Population densities for transistors in two different wafer lots, curves A and A′, are plotted on the same scale as the wafer lot distribution for the same parameter. It is clear that a sample selected from wafer lot A will poorly predict the performance expected from transistors in lot A′. These curves are typical of the way many transistor parameters vary. They are also descriptive of batch processed components in general.

From an equipment design point of view, these characteristics have serious implications. The validity of a 100 piece design sample becomes questionable, when the possibility that all 100 devices may be from the same wafer lot is considered. In fact, the validity of using 100 devices, which are purchased all in one group, is more than questionable. For those parameters which are highly wafer lot dependent, such a sample is, in effect, not a 100 piece sample, but a one piece sample, since there is a very high probability that only one wafer lot is represented.

The unfortunate circumstances in the opening scenario are a direct result of a one piece wafer lot sample. The one piece sample does not buy much statistical insurance. Surprises are likely, since a false sense of security is generated when it is believed that 100 physical units in a design sample represent a 100 piece statistical sample. The results are predictable and unpleasant for all concerned.

Design Samples

A key factor in top notch design work is obtaining statistically relevant samples of key components. With respect to power transistors, this means including a number of different wafer lots in the design sample. This task can be seemingly difficult since, in general, the number of wafer lots in a given sample is not known. However, the minimum number of wafer lots in a sample can be determined by assuming that each date code consists of separate wafer lots. There may be many wafer lots in a date code, but usually two date codes will not contain transistors from the same wafer lot.

Often, transistors have two date codes, one which corresponds to the time period in which they are tested and the other which denotes the time period in which they were assembled. The assembly date code is by far the more valuable of the two. As an example, Motorola TO-204 transistors have a three-digit assembly date code stamped on the ear. The first digit is coded to the year. The second and third digits correspond to workweek. A transistor built in the last workweek of 1987 would read 752.

Sample selection, then, hinges on being able to obtain transistors from a number of different date codes. Here are some suggestions.

1) Place several small orders sequentially in time.
2) Order from several different distributors, preferably in more than one geographic location. Five 20 piece shipments from five different distributors will cost more than a single shipment of 100 pieces, but the benefits dwarf the added expense.
3) Ask the manufacturer for assistance.

As a practical matter, it will generally be rather difficult to obtain a sample with more than four or five wafer lots represented. Since this is a relatively small sample, a working knowledge of parameter variations is very helpful. This is particularly true of Safe Operating Area (SOA) which is presented here as a special case.

Safe Operating Area

Safe Operating Area is probably the most troublesome of the unspecified parameters. Operation in unspecified regions is difficult to avoid since it is not practical to guarantee the transistor for all conditions in which it can be used. Usually, unspecified operation is related to the fact that SOA curves are drawn for given circuit configurations and bias conditions. Operation in conditions other than specified is not necessarily guaranteed. Therefore, it is often easy to operate fully within the boundaries of an SOA curve, yet be in an unspecified region because of differences in circuit configuration or bias.

At times like this, a straightforward test can be very effective. The steps are as follows:

1. Starting with the equipment in which the transistor will operate, or a suitable test circuit, raise the input bus voltage to 1.25 × its worst case value. Test the equipment for survivability. If any transistors in the design sample fail, there is not enough safety margin. Future trouble is almost guaranteed. If none fail, proceed to Step 2.
2. Raise the bus voltage to 1.33 × its worst case value. Repeat the testing. If more than 50% of the sample transistors survive, then SOA safety margin is probably more than adequate.

3. Recognize that worst case SOA stress, in switching power conversion systems, will often occur at conditions other than full load and high temperature. It is important to either choose conditions which maximize transistor stress, or cycle the equipment through its mini-max load and temperature ranges. Successful results will depend largely on attention to test conditions. An example is noteworthy.

   SOA stress is often maximized in the first or last switching cycle, when the equipment is turned-on or turned-off. Load lines for the first or last cycle often have larger excursions than steady-state full load operation. A single excursion to a high voltage is usually more hazardous than operating at a lower voltage on a continuous basis.

These steps are very effective at eliminating unwanted surprises, provided transistors from at least three wafer lots are included in the test. They form the same basic procedure that is used to generate data sheet SOA curves.

General Guidelines

It is often of interest to obtain reasonable limits for parameters other than SOA. A discussion of expected variations is a good place to start.

Variations within a given sample are obvious. Of interest here is the expected worst case variations over the life of a multi-year production run. Table 3 gives an indication of what can generally be expected for various parameters. Measured mean values come from data taken on transistors in the design sample. They are normalized to 1.0 for ease of comparison. It is important to note that Table 3 applies only if at least three wafer lots are included in the sample data.

TABLE 3

Parameter	Measured Mean Value	Expected Min	Expected Max
Leakage Currents	1.0	10^{-3}	10^{+3}
Breakdown Voltages	1.0	0.7	1.5
Gain	1.0	0.5	4.0
Turn-On Delay Time	1.0	0.7	1.5
Rise Time	1.0	0.5	2.0
Turn-Off Delay Time	1.0	0.5	2.0
Fall Time	1.0	0.5	2.0
Crossover Time	1.0	0.5	2.0
Gate Threshold Voltage	1.0	0.6	1.5
$r_{DS(on)}$	1.0	0.5	2.0
$V_{DS(on)}$	1.0	0.5	2.0
C_{iss}	1.0	0.7	1.5
C_{oss}	1.0	0.5	2.0
C_{rss}	1.0	0.6	1.6

Although some of the resulting tolerances may seem rather large, they are realistic when production runs spanning a number of years are considered. It is far better to face these numbers up front, than be surprised downstream with equipment failures.

Conclusion

The risk of equipment failure can be significantly reduced by straightforward improvements in the selection of design samples. Risks are further minimized with realistic estimation of worst case parameter variations, and the proper choice of test conditions for maximum stress.

Power MOSFET Measurement Techniques For The Curve Tracer

The curve tracer is an extremely useful tool in measuring the pertinent power MOSFET parameters. The techniques are not dissimilar to those used for measuring bipolar transistors. Table 4 lists the equivalent parameters between the two.

TABLE 4

Transistor	MOSFET
Collector	Drain
Emitter	Source
Base	Gate
$V_{(BR)CES}$	$V_{(BR)DSS}$
V_{CBO}	V_{DGR}
I_C	I_D
I_{CES}	I_{DSS}
I_{EBO}	I_{GSS}
$V_{BE(on)}$	$V_{GS(th)}$
$V_{CE(sat)}$	$V_{DS(on)}$
C_{ib}	C_{iss}
C_{ob}	C_{oss}
h_{FE}	g_{fs}
$R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$	$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$
V_{EC}	V_{SD}

No FET parameters are measured in an open gate condition. To prevent damage to the part, the gate should always be terminated with a resistor (typically $R_{GS} = 1.0\ M\Omega$) or a short for the appropriate test condition.

DEFINITIONS OF ELECTRICAL CHARACTERISTICS

Off Characteristics

$V_{(BR)DSS}$, Drain-Source Breakdown Voltage — Maximum sustaining voltage between the drain and source, measured at a specific drain current, I_D; Gate shorted to the source.

I_{DSS}, Drain-Current With Zero Gate Voltage — Drain leakage current at a specified drain-source voltage, V_{DSS}; Gate shorted to source.

I_{GSS}, Gate Body Leakage Current — Gate leakage current for a specified gate-source voltage; Drain shorted to source.

On Characteristics

$V_{GS(th)}$, Gate Threshold Voltage — Value of the gate voltage that must be applied to initiate conduction. It has a negative temperature coefficient of about -6.7 mV/°C.

$V_{DS(on)}$, Drain-Source On-Voltage — Voltage drop measured between the drain and source at a specified drain current and specified gate-source voltage.

$r_{DS(on)}$, Drain-Source On-Resistance — Value of the resistance measured between drain and source at a specified drain current and a specified gate-source voltage. It is defined as:

$$r_{DS(on)} = \frac{V_{DS(on)}}{I_D}$$

g_{fs}, Forward Transconductance — The MOSFET gain parameter. It is the ratio between the change in drain current, I_D, for a given change in gate-source voltage, at a specified drain-source voltage and specified drain curreNt. In algebraic fOrm:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

V_{SD}, Diode Forward On-Voltage — The forward voltage drop between the source and drain at a specified S-D diode current I_S.

Curve Tracer Measurements

The following explains how to measure the parameters listed above on a curve tracer. Although the set-up charts correspond to the Tektronic Type 576 Curve Tracer, the same measurements can be performed on a Tektronix Type 577 Curve Tracer.

Before applying power to MOSFETs on a curve tracer, the following precautions should be observed:

1 — Test stations should be protected from Electro-Static Discharge.

2 — When inserting parts into a curve tracer, voltage should not be applied until all terminals are solidly connected in the socket.

3 — A resistor of 100 Ω should be connected in series with the gate to damp spurious oscillations that can occur on the tracer.

4 — When switching from one test range to another, voltage settings should be reduced to zero to avoid generation of potentially destructive voltage surges during switching.

The test set-ups to follow are for the Motorola MTP12N10 Power MOSFET, which is a 12 Amp, 100 volt N-Channel device in the TO-220 package.

$V_{(BR)DSS}$ — Also known as BV_{DSS}. Specified at an I_D of 5.0 mA at T_C = 25°C.

Test set-up and Source Trace (See Figure 12-39).

1 — Set maximum peak volts on 350, Series Resistors on 3.0 k.

2 — Polarity to NPN, Mode to Norm.

3 — Vertical on 1.0 mA/Division, Display Offset on 0, Horizontal on 20 volts/Division.

4 — Step Generator is not used for this measurement.

5 — Emitter grounded; Base Term on short.

6 — With device in socket, adjust variable collector supply until trace breaks and reaches 5.0 mA.

I_{DSS} — Specified at 85% of rated $V_{(BR)DSS}$. Maximum allowable leakage is 250 μA at T_C = 25°C.

Test Set-Up

Set-up is the same as $V_{(BR)DSS}$/except:

1 — Set Mode Switch to Leakage.

2 — Set Vertical to 50 μA/Division

3 — Adjust variable collector supply to 85 volts and read leakage. If Leakage reads 0, adjust Vertical to desired level (This increases sensitivity on low leakage devices).

I_{GSS} — Specified at V_{GS} = ±20 volts, maximum allowable leakage is 500 nA at T_C – 25°C.

Test Set-Up

1 — Drain and gate connections on socket are reversed so drain is shorted to source.

2 — Set maximum peak volts to 75, and Series Resistors to 140 Ω.

3 — Polarity to NPN and Mode Switch to Leakage.

4 — Vertical on 50 nA/Division, Display Offset on 0, Horizontal on 2.0 Volts/Division.

5 — Step generator is not used for this measurement.

6 — Emitter grounded; Base Term on short.

7 — With device in socket, adjust variable collector supply to 20 volts and read Leakage. If leakage reads 0, adjust vertical to desired level.

$V_{GS(th)}$ — Specified at 1.0 mA with limits of 2.0 volts minimum and 4.5 volts maximum at T_C = 25°C.

(Figure 12-40)

1 — Set Maximum Peak Volts to 15, Series Resistors to 0.3 Ω.

2 — Polarity to NPN, Mode Switch on Normal.

3 — Vertical on 0.2 mA/Division, Display Offset on 0, Horizontal on 2.0 Volts/Division.

4 — Step Generator; number of steps = 1, Offset Mult on 0, Offset on Aid, Steps Button in, Step Family on Single, Rate on Norm, Step offset amplitude = 1.0 V.

5 — Emitter grounded; Base Term on Step Generator.

6 — With device in socket, adjust variable collector supply to 10 volts, then adjust Offset Mult until trace reaches 1.0 mA. Read $V_{GS(th)}$ directly from Offset Mult Control.

$V_{DS(on)}$ — Specified at V_{GS} = 10 volts and at one half rated I_D. $r_{DS(on)}$ is calculated from measured $V_{DS(on)}$ value.

(Figure 12-41)

1 — Set Maximum Peak Volts on 15, Series Resistors on 0.3 Ω.

2 — Polarity on NPN, Mode to Norm.

3 — Vertical on 1.0 A/Division, Display Offset on 0, Horizontal on 0.5 Volts/Division.

4 — Step Generator; number of steps — 10, Offset on zero, pulsed steps on 300 μs, Step Family on Rep, rate on Norm, Step Offset/Amplitude = 1.0 V.

5 — Emitter grounded; Base Term on Step Gen.

6 — With device in socket, adjust variable collector supply until the top left dot on trace reaches 6.0 Amps then read $V_{DS(on)}$ off horizontal scale.

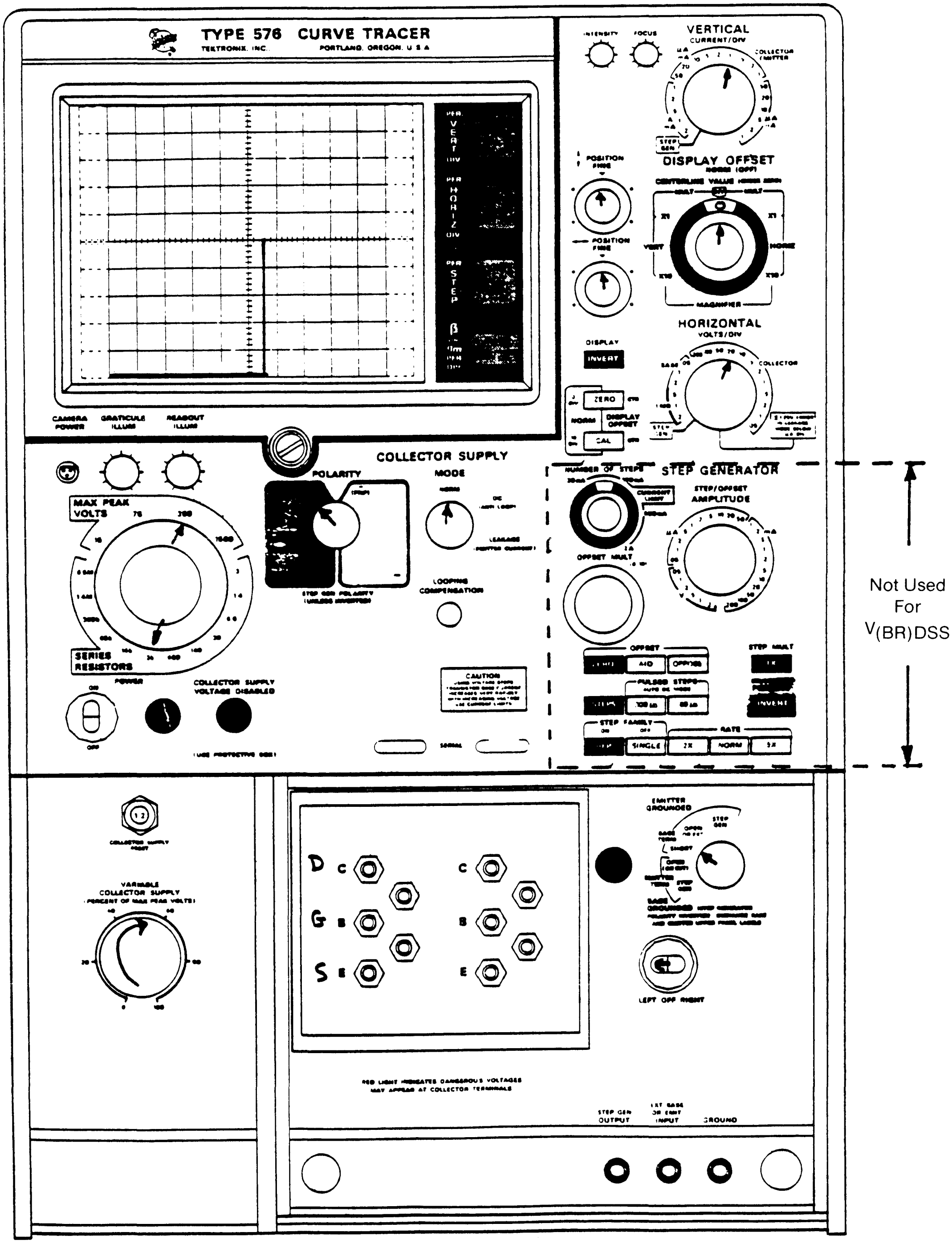


FIGURE 12-39 — TEST SET-UP CHART TYPE 576 FOR MEASURING POWER MOSFET PARAMETERS

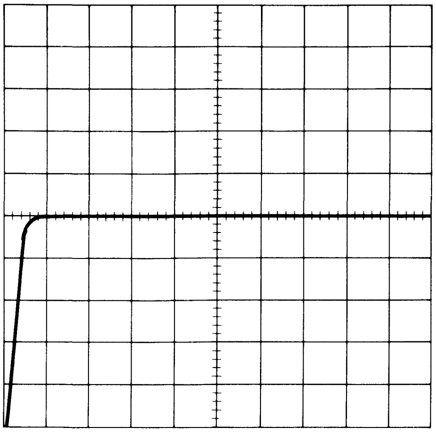


FIGURE 12-40 — CURVE TRACER PRESENTATION FOR $V_{GS(th)}$ — MTP12N10

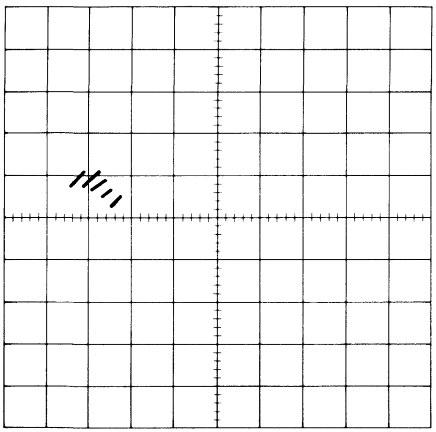


FIGURE 12-41 — CURVE TRACER PRESENTATION FOR $V_{DS(on)}$

g_{fs} — Specified at one half rated I_D at V_{DS} = 15 volts.
(Figure 12-42)

1 — Maximum Peak Volts on 15, Series Resistors on 0.3 Ω.
2 — Polarity on NPN, Mode to Norm.
3 — Vertical on 1.0 Amp/Division/Display Offset on zero, Horizontal on 2.0 Volts/Division.
4 — Step Generator; number of steps = 10, Offset on zero, Pulsed Steps on 300 μs, Step Family on Rep, rate on Norm, Step Offset Amplitude −1.0 V.
5 — Emitter grounded; Base Term on Step Gen.
6 — Readout illum turned fully clockwise.
7 — With device in socket, adjust variable collector supply until trace with steps closest to 6.0 Amps reaches 15 volts. g_{fs} is the number of divisions between those two steps, as designated by the right hand corner of the screen labeled g_m per Division.

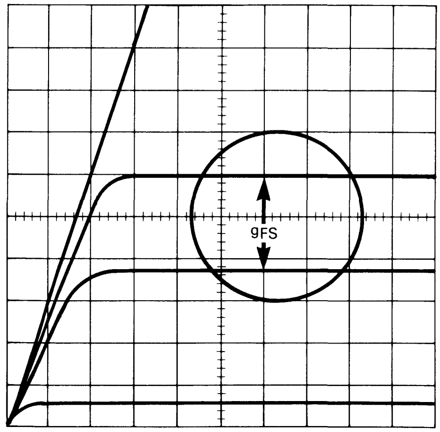


FIGURE 12-42 — CURVE TRACER FOR g_{fs}

V_{SD} — Specified at rated I_D with V_{GS} = 0.
(Figure 12-43)

1 — Set Maximum Peak Volts on 15 and Series Resistors on 0.3 Ω.
2 — Polarity on PNP, Mode on Norm.
3 — Vertical on 2.0 Amps/Division, Display Offset on 0, Horizontal on 0.5 Volts/Division.
4 — Push Display Invert in.
5 — Step Generator is not used for this measurement.
6 — With device in socket, adjust variable collector supply until trace reaches 12 Amps and read voltage.

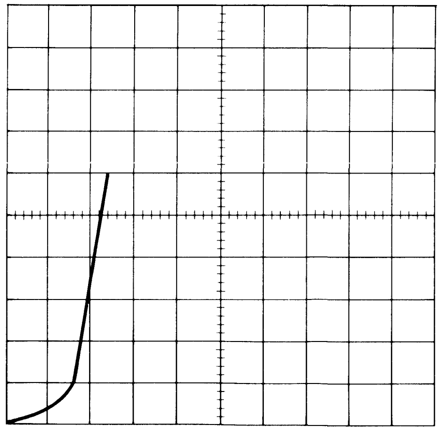


FIGURE 12-43 — CURVE TRACER PRESENTATION FOR V_{SD}

REFERENCES

1. Fink, *Electronic Engineers' Handbook,* 1 ed 1975, McGraw Hill, pp17–31 to 17–32.
2. Henny, *Radio Engineering Handbook,* 5 ed, 1959, McGraw Hill, pp14–36 to 14–37.

Additional Reference Material: Measurement Concepts From Tektronix.

2

2-12

Chapter 13: Reliability and Quality

Introduction

In today's semiconductor marketplace two important elements for the success of a company are product quality and reliability. Both are interrelated — reliability is the quality extended over the expected life of the product. For any manufacturer to remain in business, their products must meet and/or exceed the basic quality and reliability standards. Motorola, as a semiconductor supplier, has successfully achieved these standards by supplying product for the most strenuous applications to perform in the most adverse environments.

It is recognized that the best way to accomplish an assured quality performance is by moving away from the previous methods of "testing in" quality and embracing the newer concept of "building in" quality. At Motorola, we use a twofold approach toward reaching the ultimately achievable level of quality and reliability. First, we develop and implement a process that is inherently reliable. Then we exercise meticulous care in adhering to the specifications of the process every step of the way — from start to finish. This allows the development and application of inspections and procedures that will uncover potentially hidden failure modes. It is this dedication to long-term reliability that will ultimately lead to the manufacture of the "perfect product."

Motorola approaches the ideal in TMOS product reliability by instigating a four-step program of quality and reliability:

1. Stringent in-process controls and inspections.
2. Thoroughly evaluated designs and materials.
3. Process average testing, including 100% QA redundant testing.
4. Ongoing reliability verifications through audits and reliability studies.

These quality and reliability procedures, coupled with rigorous incoming inspections and outgoing quality control inspections add up to a product with quality built in — from raw silicon to delivered service.

Reliability Tests

Motorola TMOS products are subjected to a series of extensive reliability tests to verify conformance. These tests are designed to accelerate the failure mechanisms encountered in practical applications, thereby ensuring satisfactory reliable performance in "real world" applications.

The following describes the reliability tests that are routinely performed on Motorola's TMOS devices.

High Temperature Reverse Bias (HTRB) Per MIL-STD-750, Method 1039:

The HTRB test is designed to check the stability of the device under "reverse bias" conditions of the main blocking junction at high temperature, as a function of time.

The stability and leakage current over a period of time, for a given temperature and voltage applied across the junction, is indicative of junction surface stability. It is therefore a good indicator of device quality and reliability.

For TMOS devices, voltage is applied between the drain and source with the gate shorted to the source. I_{DSS}, $V_{(BR)DSS}$, I_{GSS}, $V_{GS(th)}$, and $V_{DS(on)}$ are the dc parameters monitored. A failure will occur when the leakage achieves such a high level that the power dissipation causes the devices to go into a thermal runaway. The leakage current of a stable device should remain relatively constant, only increasing slightly over the testing period.

Typical conditions:

V_{DS} = 100% of maximum V_{DS} rating
V_{GS} = 0 (shorted)
T_A = 150°C
Duration: 1000 hrs for qualification

High Temperature Gate Bias (HTGB): Per MIL-STD-750, Method 1039:

The HTGB test is designed to electrically stress the gate oxide at the maximum rated dc bias voltage at high temperature. The test is designed to detect for drift caused by random oxide defects and ionic oxide contamination.

For TMOS devices, voltage is applied between the gate and source with the drain shorted to the source. I_{GSS}, $V_{GS(th)}$, and $V_{DS(on)}$ are the dc parameters monitored. Any oxide defects will lead to early device failures.

Typical conditions:

$V_{GS} = \pm 20$ V
V_{DS} = 0 (shorted)
T_A = 150°C
Duration: 1000 hrs for qualification

High Temperature Storage Life (HTSL) Test: Per MIL-STD-750, Method 1032.

The HTSL test is designed to indicate the stability of the devices, their potential to withstand high temperatures and the internal manufacturing integrity of the package. Although devices are not exposed to such extreme high temperatures in the field, the purpose of this test is to accelerate any failure mechanisms that could occur during long periods at storage temperatures.

The test is performed by placing the devices in a mesh basket, then placed in a high temperature chamber at a controlled ambient temperature, as a function of time.

Typical conditions:

T_A = 150°C on Plastic package
Duration: 1000 hrs for qualification

High Humidity High Temperature Reverse Bias (H^3TRB) Test: Per MIL-STD-750, Method 1039.

The H^3TRB test is designed to determine the resistance of component parts and constituent materials to the combined deteriorative effects of prolonged operation in a high temperature/high humidity environment. This test only applies to nonhermetic devices.

Humidity has been a traditional enemy of semiconductors, particularly plastic packaged devices. Most moisture related degradations result, directly or indirectly, from penetration of moisture vapor through passivating materials, and from surface corrosion. At Motorola, this former problem has been effectively addressed and controlled through use of junction "passivation" process, die coating, and proper selection of package materials.

Typical conditions:
V_{DS} = 100% of maximum V_{DS} rating up to 200 V
V_{GS} = 0 (shorted)
T_A = 85°C
RH = 85%
Duration: 1000 hrs for qualification

2

Autoclave Test (Pressure Cooker).

The Autoclave Test is designed to determine the moisture resistance of devices by subjecting them to high steam pressure levels. This test is only performed on plastic/epoxy encapsulated devices and not on hermetic packages (i.e., metal can devices). Within the pressure cooker a wire mesh tray is constructed inside to keep the devices approximately two inches above the surface of deionized water and to prevent condensed water from collecting on them. After achieving the proper temperature and atmospheric pressure, these test conditions are maintained for a minimum of 24 hours. The devices are then removed and air dried. Parameters that are usually monitored are leakage currents and voltage.

Typical Conditions:
T_A = 121°C
P = 14.7 psi
RH = 100%
Duration: 72 hrs for qualification

Intermittent Operating Life:
(IOL or Power Cycling) Per MIL-STD-750,
Method 1037.

The purpose of the IOL test is to determine the integrity of the chip and/or package assembly by cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied) as is normally experienced in a "real world" environment.

DC power is applied to the device until the desired function temperature is reached. The power is then switched off, and forced air cooling applied until the junction temperature decreases to ambient temperature.

$$\Delta T_J = \Delta T_C + R_{\theta JC} Pd$$

$$\Delta T_J = 100°C$$

(typically, which is an accelerated condition)

$$\Delta T_C = T_{C\,HIGH} - T_{C\,LOW}$$

The sequence is repeated for the specified number of cycles. The temperature excursion is carefully maintained for repeatability of results.

The Intermittent Operating Life test indicates the degree of thermal fatigue of the die bond interface between the chip and the mounting surface and between the chip and the wire bond interface.

For TMOS devices, parameters used to monitor performance are thermal resistance, threshold voltage, on-resistance, gate-source leakage current and drain-source leakage current.

A failure occurs when thermal fatigue causes the thermal resistance or the on-resistance to increase beyond the maximum value specified by the manufacturer's data sheets.

Typical conditions:
$V_{DS} \geq 10$ V
ΔT_J = 100 °C
$R_{\theta JC}$ = Device dependent
T_{on}, $T_{off} \geq 30$ seconds
Duration: 15K cycles for qualification

TEMPERATURE CYCLE (TC) PER MIL-STD-750, METHOD 1051:

The purpose of the Temperature Cycle Test is to determine the resistance of the device to high and low temperature excursions in an air medium and the effects of cycling at these extremes.

The test is performed by placing the devices alternatively in separate chambers set for high and low temperatures. The air temperature of each chamber is evenly maintained by means of circulation. The chambers have sufficient thermal capacity so that the specified ambient is reached after the devices have been transferred to the chamber.

Each cycle consists of an exposure to one extreme temperature for 15 minutes minimum, then immediately transferred to the other extreme temperature for 15 minutes minimum; this completes one cycle. Note that it is an immediate transfer between temperature extremes and thereby stressing the device greater than non-immediate transfer.

Typical Extremes

−65/+150°C

The number of cycles can be correlated to the severity of the expected environment. It is commonly accepted in the industry that ten cycles is sufficient to determine the quality of the device.

Typical Cycles for Evaluations

TO-204 and TO-220 devices: Minimum 100 cycles

TO-204 and TO-220 devices: Maximum 1000 cycles

Temperature cycling identifies any excessive strains set up between materials within the device due to differences in coefficients of expansion.

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short".

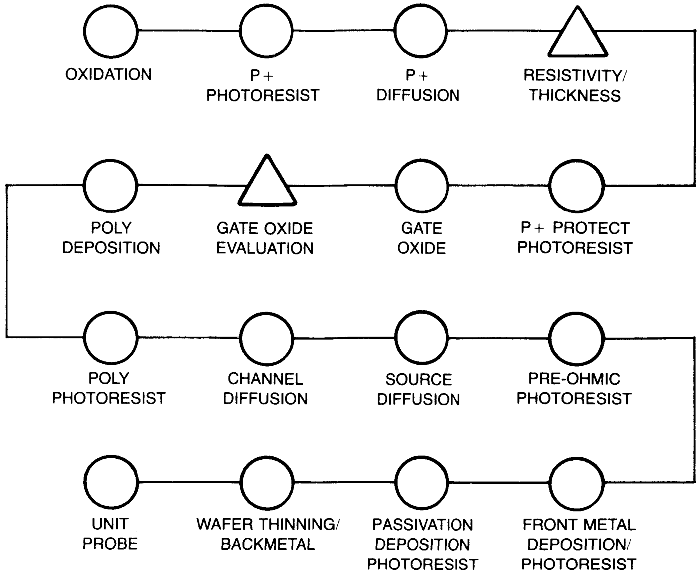
Thermal Shock (TC) Per MIL-STD-750, Method 1056:

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature.

The test is performed by placing the devices in a mesh basket, then alternatively immerse in baths of liquid (maintained at −55°C and +150°C). They are kept for thirty seconds in each bath and immediately transferred to the alternate bath.

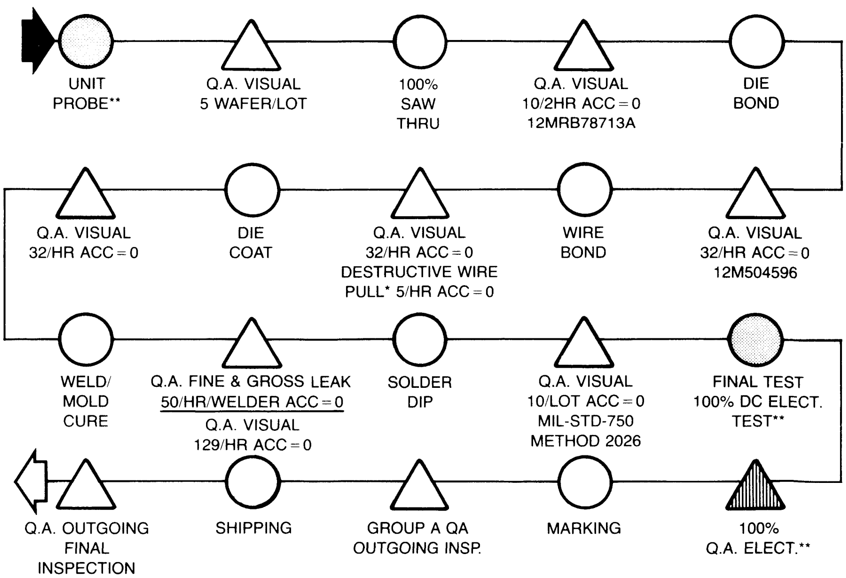
This test produces sudden heating and cooling of the device, and produces unusual stresses due to the short term temperature gradients that are set up. It is commonly accepted in the industry that five cycles is sufficient to determine the quality of the device.

A failure occurs when there is a change in the device's parameters beyond specified levels, or when a device checks electrically as "open" or "short".



Δ — DENOTES QA INSPECTION POINT
○ — DENOTES PROCESS STEP

TMOS WAFER FABRICATION



*100% NON-DESTRUCTIVE WIRE PULL AFTER WIRE BOND
**100% DC ELECTRICAL TESTING

Δ — DENOTES QA INSPECTION POINT
○ — DENOTES PROCESS STEP

ASSEMBLY PROCESS FLOW

Environmental Package Related Test Programs:

A. Physical Dimensions — Mil-Std-750, Method 2066. This test is performed to determine the conformance to device outline drawing specifications.

B. Visual and mechanical examination — Mil-Std-750, Method 2071. A test to determine the acceptability of product to certain cosmetic and functional criteria such as marking legibility, stains, etc.

C. Resistance to Solvents — Mil-Std-202, Method 2025.3. A test to determine the solderability of device terminals.

D. Terminal Strength — Mil-Std-750, Method 2036. This test is a lead bend test to check for lead strength.

E. Constant Acceleration — Mil-Std-750, Method 2006. The parts are accelerated to 20,000 G's and higher to check for defects that would show up in this environment.

F. Vibration Variable Frequency — Mil-Std-750, Method 2056. Parts are vibrated in different planes and at different frequencies to check for loose particles or ruptured wire or die bonds.

Every manufacturing process exhibits a quality and reliability distribution. This distribution must be controlled to assure a high mean value, a narrow range and a consistent shape. Through proper design and process control this can be accomplished, thereby reducing the task of screening programs which attempt to eliminate the lower tail of the distribution.

Accelerated Stress Testing

The nature of some tests in this report is such that they far exceed that which the devices would see in normal operating conditions. Thus, the test conditions "accelerate" the failure mechanisms in question and allow Motorola to predict failure rates in a much shorter amount of time than otherwise possible. Failure modes that are temperature dependent are characterized by the Arrhenius model.

$$AF = e^{\frac{EA}{K}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)}$$

AF = Acceleration Factor
EA = Activation Energy (ev)
K = Boltzman's Constant (8.62×10^{-5} ev/°K)
T_2 = Operating Temperature (°K)
T_1 = Test Temperature (°K)

Therefore, the equivalent device hours are equal to the acceleration factor (as determined by the Arrhenius Model) times the actual device hours.

With the following charts (13-1, 13-2), one can determine a temperature dependent failure rate for our power MOSFETs under reverse and gate bias conditions when establishing their design circuits. For example, if the established operating temperature is set at 50°C, the charts show the failure rates to be 1 and 680 fits for high temperature reverse bias and high temperature gate bias, respectively.

Review of Data

High Temperature Reverse Bias (HTRB) indicates the stability of leakage current, which is related to the field

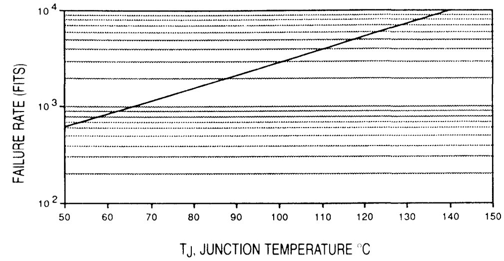


FIGURE 13-1 — HIGH TEMPERATURE REVERSE BIAS FAILURE RATE VERSUS JUNCTION TEMPERATURE

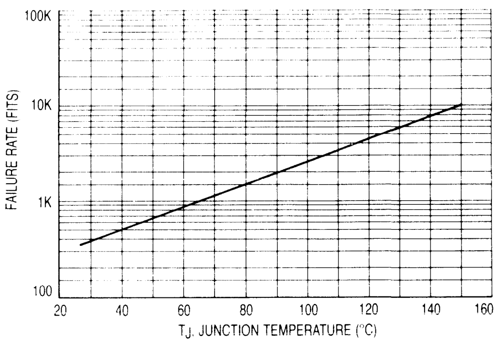


FIGURE 13-2 — HIGH TEMPERATURE GATE BIAS FAILURE RATE VERSUS JUNCTION TEMPERATURE

distortion of TMOS devices. HTRB enhances the failure mechanism by high temperature reverse bias testing, and therefore is a good indicator of device quality and reliability, along with verification that process controls are effective.

High Temperature Gate Bias (HTGB) checks the stability of the device under "gate bias" forward conditions at accelerated high temperature, as a function of time. This test is performed to electrically stress the gate oxide to detect for drift caused by random oxide defect. This failure mechanism appears in the infant and random zones of the reliability "bath tub curve" at a very low rate of defect.

Intermittent Operating Life (IOL) is an excellent accelerated stress test to determine the integrity of the chip and/or package assembly to cycling on (device thermally heated due to power dissipation) and cycling off (device thermally cooling due to removal of power applied). This test is perhaps the most important test of all, along with simulating what is normally experienced in a "real world" environment. IOL exercises die bond, wire bonds, turning on the device, turning off the device, relates the device performance, and verifying the thermal expansion of all materials are compatible. Motorola performs extensive

IOL testing as a continual process control monitor that best relates to the "device system**" as a whole. Motorola also performs extensive analysis and comparison of delta junction temperatures. Motorola has determined that to effectively stress the device a delta T_J of 100°C is necessary which far exceeds many customers' application and determines the reliability modeling of the device.

Temperature Cycling (TC) is also an excellent stress test to determine the resistance of the device to high and low temperature excursions in an air medium. Where IOL electrically stresses the "device system" from internally, temperature cycle stresses the "device system" thermally from external environment conditions.

High Temperature Storage Life (HTSL), High Humidity Temperature Reverse Bias (H^3TRB), Thermal Shock (TC) and "Pressure Cooker" (Autoclave) are routinely tested, however it is felt by Motorola Reliability Engineering that HTRB, HTGB, IOL and TC are of primary importance. Motorola has been in the semiconductor industry for many years and will remain there as a leader with continued reliability, quality and customer relations.

2

Test Results Summaries

TABLE 1
SUMMARY OF TIME DEPENDENT TESTS

Test Type	Test Conditions	Devices Failed	Device Hrs. (Actual)	Equivalent Device Hrs. @ 90°C	Failure Rate % Per 1000 Hrs.
HTRB	V_{DS} = 80% of Max. Rating* V_{GS} = 0 (Shorted) T_A = 150°C	43	7×10^6	6.51×10^8	.0068
HTGB	V_{GS} = ±20 V V_{DS} = 0 (Shorted) T_A = 150°C	24	3.11×10^6	1.21×10^9	.2063
HTSL	T_A = 150°C	1	8.9×10^5	8.3×10^7	0.0025
H^3TRB	T_A = 85°C R.H. = 85% V_{GS} = 0 (Shorted) V_{DS} = 80% of Max. Rating up to 200 V	0	3.2×10^5	—	0.28

Failure Unit (FIT):
Modern electronic system reliability utilizing today's semiconductor devices requires quite low component failure rates, and therefore requires a workable number. This number called a FIT (Failure Unit) is defined as: FIT = one failure on 10^9 device hours.

Mean Time Between Failures (MTBF):
The significant distribution properties of electronic system reliability is expressed as MTBF, which is defined as:

$t = 1/\lambda$
Where, t = time, hours
λ = failure rate

* (changed to 100% of max rating 2Q87)

TABLE 2
SUMMARY OF CYCLE DEPENDENT TESTS

Test Type	Test Conditions	Devices Failed	Device Cycles (Actual)	Equivalent Device Hrs. @ 90°C	Failure Rate % Per 1000 Cycles
I_{OL}	ΔT_J = 100°C $V_{DS} \geq$ 10 V $t_{on}, t_{off} \geq$ 30 s	9	4.3×10^7	—	.023
T_C	T_{low} = −65°C T_{high} = 150°C (Plastic) T_{high} = 200°C (Metal)	18	2.44×10^6	—	0.74

*Activation energy for HTRB, HTSL = 1 eV; for HTGB = 0.3 eV.

Reliability Audit Program

At Motorola reliability is assured through the rigid implementation of a reliability audit program. All TMOS products are grouped into generic families according to voltage ranges and package types. These families are sampled weekly from the raw stock at final test, then submitted for audit testing. The extreme stress testing, in real-time for each product run, may uncover process abnormalities that are detectable by the in-process controls. Typical reliability audit tests include high temperature reverse bias, high temperature gate bias, intermittent operating life, temperature cycling, and autoclave. To uncover any hidden failure modes, the reliability tests are designed to exceed the testing conditions of normal quality and reliability testing.

Audit failures which are detected are sent to the product analysis laboratory for real-time evaluations. This highly specialized area is equipped with a variety of analytical capabilities, including electrical characterizations, wet chemical and plasma techniques, metallurgical cross-sectioning, scanning electron microscope, dispersive x-ray, auger spectroscopy, and micro/macro photography. Together, these capabilities allow the prompt and accurate analysis of failure mechanisms — ensuring that the results of the evaluations can be translated into corrective actions and directed to the appropriate areas of responsibility.

The Motorola reliability audit program provides a powerful method for uncovering even the slightest hint of potential process anomalies in the TMOS product line. It is this stringent and continuing concern with the reliability audits that gives positive assurance that customer satisfaction will be achieved.

Power FET TMOS Reliability Audit Program

Test	Conditions	S/S	Frequency
HTRB	V_{DS} = 100% Max Rating V_{GS} = 0 T_A = 150°C Duration = 72 Hours (short), 1000 Hours (long)	50/Family	Weekly
HTGB	V_{GSS} = ± 20 V V_{DS} = 0 T_A = 150°C Duration = 72 Hours (short), 1000 Hours (long)	50/Family	Weekly
IOL	Metal Products	36/Family	Weekly
	ΔT_J = 100°C $V_{DS} \geq 10$ V Duration = 5000 Cycles (short), 15,000 cycles (long)	36/Family	Weekly
Solder Heat	1 Cycle @ 260°C for 10 seconds followed by:	25/Family	Weekly
Temperature Cycle	100 Cycles (short) 500 Cycles (long) −65 to + 150°C Dwell Time ≥ 15 minutes Requires Faraday Cages	25/Family	Weekly
Pressure Cooker	P = 15 psi, T = 121°C Duration = 48 Hours (short), 96 Hours (long) (Plastic Package Only)	25/Family	Weekly

AVERAGE OUTGOING QUALITY (AOQ)

AOQ refers to the number of devices per million that do not fall within specification limits at the time of shipment. By implementing the philosophy of building in quality and reliability, Motorola has continually improved its outgoing quality. This pursuit of quality has led to a vendor certification program which guarantees a specific level of quality for the customer which has in many cases reduced or eliminated the need for incoming inspections.

AVERAGE OUTGOING QUALITY (AOQ)

AOQ = Process Average x Probability of Acceptance x 10^6 (PPM)

- Process Average $= \dfrac{\text{Total Projected Reject Devices}}{\text{Total Number of Devices}}$
- Projected Reject Devices $= \dfrac{\text{Defects in Sample}}{\text{Sample Size}}$ x Lot Size
- Total Number of Devices = Sum of all the units in each submitted lot
- Probability of Acceptance $= 1 - \dfrac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$
- 10^6 = Conversion to Parts Per Million

Essentials of Reliability:

Paramount in the mind of every semiconductor user is the question of device performance versus time. After the applicability of a particular device has been established, its effectiveness depends on the length of trouble free service it can offer. The reliability of a device is exactly that — an expression of how well it will serve the customer. Reliability can be redefined as the probability of failure free performance, under a given manufacturer's specifications, for a given period of time. The failure rate of semiconductors in general, when plotted versus a long period of time, exhibit what has been called the "bath tub curve" (Figure 13-3).

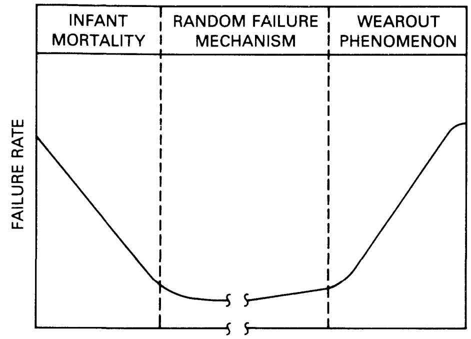


FIGURE 13-3 — FAILURE RATE OF SEMICONDUCTOR

Reliability Mechanics

Since reliability evaluations usually involve only samples of an entire population of devices, the concept of the central limit theorem applies and a failure rate is calculated using the λ^2 distribution through the equation:

$$\lambda \leq \frac{\lambda^2 (\alpha, 2r + 2)}{2\,nt}$$

λ^2 = chi squared distribution

where $\alpha = \dfrac{100 - cl}{100}$

λ = Failure rate

cl = Confidence limit in percent

r = Number of rejects

n = Number of devices

t = Duration of tests

The confidence limit is the degree of conservatism desired in the calculation. The central limit theorem states that the values of any sample of units out of a large population will produce a normal distribution. A 50% confidence limit is termed the best estimate, and is the mean of this distribution. A 90% confidence limit is a very conservative value and results in a higher λ which represents the point at which 90% of the area of the distribution is to the left of that value (Figure 13-4).

The term (2r + 2) is called the degrees of freedom and is an expression of the number of rejects in a form suitable to λ^2 tables. The number of rejects is a critical factor since

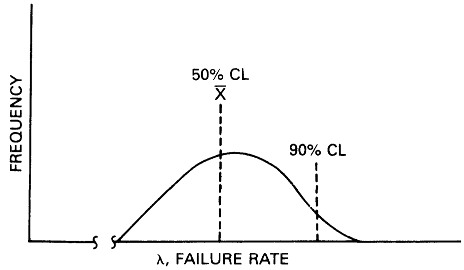


FIGURE 13-4 — CONFIDENCE LIMITS AND THE DISTRIBUTION OF SAMPLE FAILURE RATES

the definition of rejects often differs between manufacturers. Due to the increasing chance of a test not being representative of the entire population as sample size and test time are decreased, the λ^2 calculation produces surprisingly high values of λ for short test durations even though the true long term failure rate may be quite low. For this reason relatively large amounts of data must be gathered to demonstrate the real long term failure rate. Since this would require years of testing on thousands of devices, methods of accelerated testing have been developed.

Years of semiconductor device testing has shown that temperature will accelerate failures and that this behavior fits the form of the Arrhenius equation:

$$R(t) = R_o(t)e^{-\phi/KT}$$

Where $R(t)$ = reaction rate as a function of time and temperature

R_o = A constant

t = Time

T = Absolute temperature, °Kelvin (°C + 273°)

ϕ = Activation energy in electron volts (ev)

K = Boltzman's constant = 8.62×10^{-5} ev/°K

This equation can also be put in the form:

AF = Acceleration factor

T2 = User temperature

T1 = Actual test temperature

The Arrhenius equation states that reaction rate increases exponentially with the temperature. This produces a straight line when plotted on log-linear paper with a slope physically interpreted as the energy threshold of a particular reaction or failure mechanism.

Reliability Qualifications/Evaluations Outline:

Some of the functions of Motorola Reliability and Quality Assurance Engineering is to evaluate new products for introduction, process changes (whether minor or major), and product line updates to verify the integrity and reliability of conformance, thereby ensuring satisfactory performance in the field. The reliability evaluations may be subjected to a series of extensive reliability testing, such as those outlined in the "Tests Performed" section, or special tests, depending on the nature of the qualification requirement.

High Reliability Power MOSFET Products

Motorola has the broadest line of MIL-qualified discrete and integrated circuits for the widest range of designs. Power MOSFETs are being processed at this time to join the qualified products portfolio available from Motorola.

Complete facilities are available to conduct all three product levels of testing on Power MOSFETs in TO-204AA and TO-205AF hermetic packages. Devices designated as "JTX" and "JTXV" devices or equivalents receive 100% screening.

Motorola offers Power MOSFETs of a custom nature which have been processed to the specific high reliability requirements of a critical scientific or industrial application.

Figure 13-5 illustrates the processing flow for JAN, JTX, and JTXV and their equivalent Power MOSFETs in accordance with MIL-S-19500.

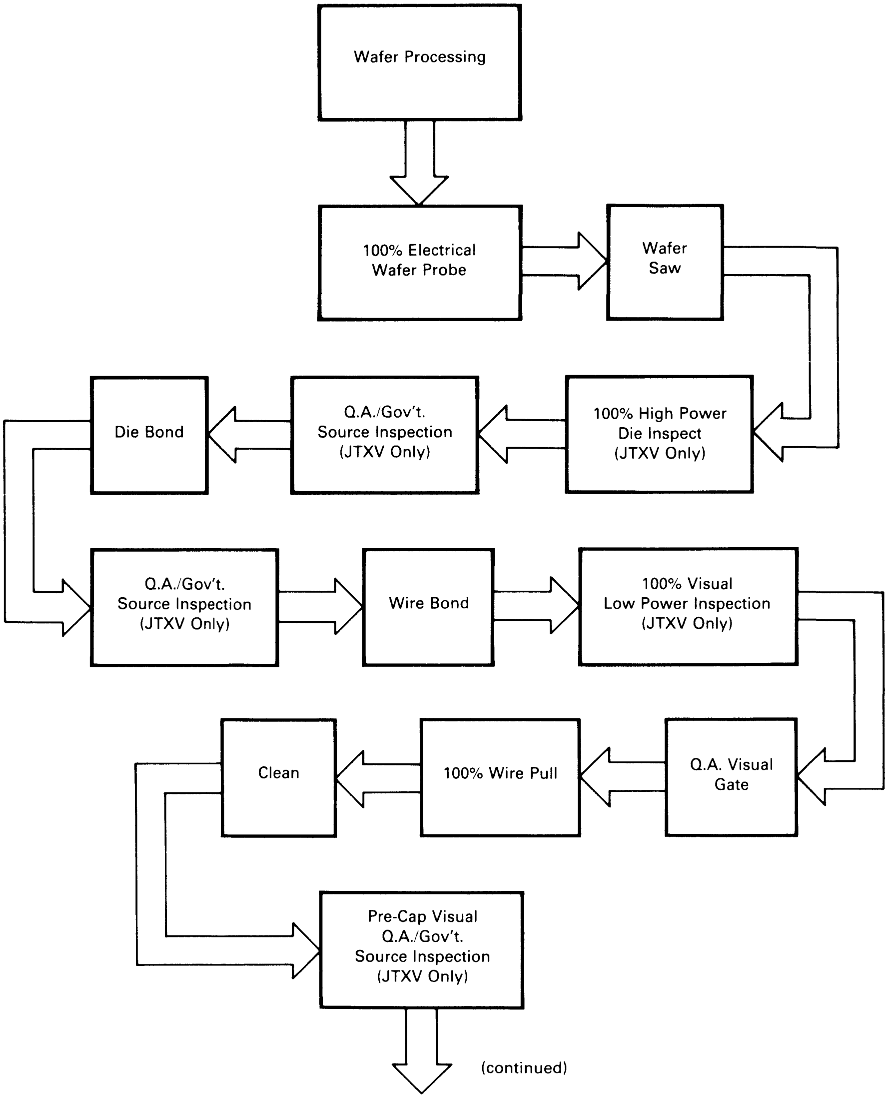


FIGURE 13-5 — JTX, JTXV AND/OR EQUIVALENT PROCESS FLOW:

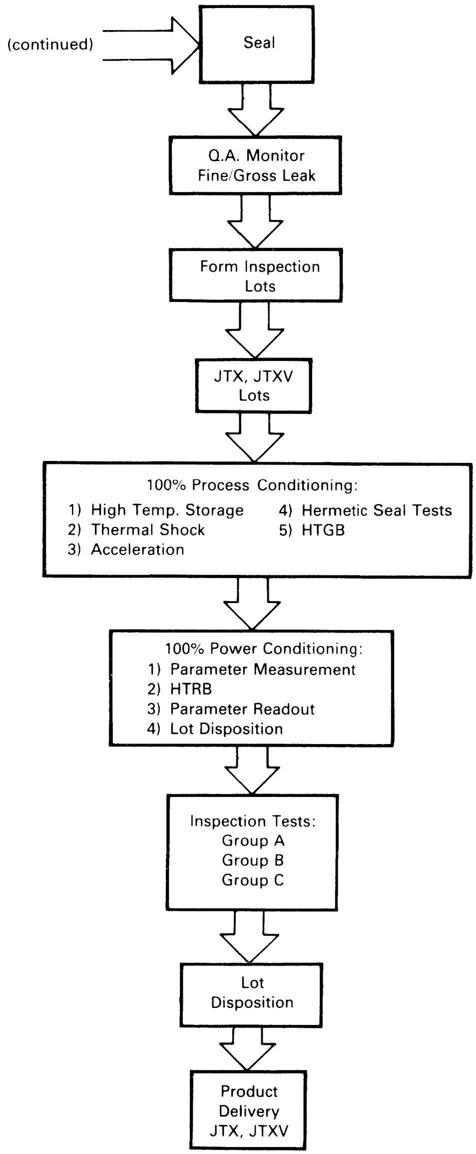


FIGURE 13-5 — JTX, JTXV AND/OR EQUIVALENT PROCESS FLOW (continued)

2

Motorola High Reliability Parts Pending QUAL as of JAN 1984

Device Type	MIL-S 19500/	Package	*QUAL Status	P_T (W)	I_D (A)	$V_{(BR)DSS}$ (V)	Ω $r_{DS(on)}$
2N6756 JTX	542B	TO-204AA TO-3	Q	75	14	100	0.18
2N6756 JTXV	542B	TO-204AA TO-3	Q	75	14	100	0.18
2N6758 JTX	542B	TO-204AA TO-3	Q	75	9.0	200	0.4
2N6758 JTXV	542B	TO-204AA TO-3	Q	75	9.0	200	0.4
2N6760 JTX	542B	TO-204AA TO-3	Q	75	5.5	400	1.0
2N6760 JTXV	542B	TO-204AA TO-3	Q	75	5.5	400	1.0
2N6762 JTX	542B	TO-204AA TO-3	Q	75	4.5	500	1.5
2N6762 JTXV	542B	TO-204AA TO-3	Q	75	4.5	500	1.5
2N6764 JTX	543B	TO-204AE TO-3	Q	150	38	100	0.055
2N6764 JTXV	543B	TO-204AE TO-3	Q	150	38	100	0.055
2N6766 JTX	543B	TO-204AE TO-3	Q	150	30	200	0.085
2N6766 JTXV	543B	TO-204AE TO-3	Q	150	30	200	0.085
2N6768 JTX	543B	TO-204AA TO-3	Q	150	14	400	0.3
2N6768 JTXV	543B	TO-204AA TO-3	Q	150	14	400	0.3
2N6770 JTX	543B	TO-204AA TO-3	Q	150	12	500	0.4
2N6770 JTXV	543B	TO-204AA TO-3	Q	150	12	500	0.4
2N6823 JTX	TBD	TO-204AA TO-3	P	100	3.0	600	2.8
2N6823 JTXV	TBD	TO-204AA TO-3	P	100	3.0	600	2.8
2N6826 JTX	TBD	TO-204AA TO-3	P	150	8.0	600	0.9

Motorola High Reliability Parts Pending QUAL as of JAN 1984 (Continued)

Device Type	MIL-S 19500/	Package	*QUAL Status	P_T (W)	I_D (A)	$V_{(BR)DSS}$ (V)	Ω $r_{DS(on)}$
2N6826 JTXV	TBD	TO-204AA TO-3	P	150	8.0	600	0.9
2N6782 JAN	556	TO-205AF TO-39	P	15	3.5	100	0.6
JTX	556	TO-205AF TO-39	P	15	3.5	100	0.6
JTXV	556	TO-205AF TO-39	P	15	3.5	100	0.6
2N6784 JAN	556	TO-205AF TO-39	P	15	2.25	200	1.5
JTX	556	TO-205AF TO-39	P	15	2.25	200	1.5
JTXV	556	TO-205AF TO-39	P	15	2.25	200	1.5
2N6786 JAN	556	TO-205AF TO-39	P	15	1.25	400	3.6
JTX	556	TO-205AF TO-39	P	15	1.25	400	3.6
JTXV	556	TO-205AF TO-39	P	15	1.25	400	3.6
2N6788 JAN	555	TO-205AF TO-39	P	20	6.0	100	0.3
JTX	555	TO-205AF TO-39	P	20	6.0	100	0.3
JTXV	555	TO-205AF TO-39	P	20	6.0	100	0.3
2N6790 JAN	555	TO-205AF TO-39	P	20	3.5	200	0.8
JTX	555	TO-205AF TO-39	P	20	3.5	200	0.8
JTXV	555	TO-205AF TO-39	P	20	3.5	200	0.8
2N6792 JAN	555	TO-205AF TO-39	P	20	2.0	400	1.8
JTX	555	TO-205AF TO-39	P	20	2.0	400	1.8
JTXV	555	TO-205AF TO-39	P	20	2.0	400	1.8
2N6794 JAN	555	TO-205AF TO-39	P	20	1.5	500	3.0
JTX	555	TO-205AF TO-39	P	20	1.5	500	3.0
JTXV	555	TO-205AF TO-39	P	20	1.5	500	3.0
2N6796 JAN	557	TO-205AF TO-39	P	25	8.0	100	0.18
JTX	557	TO-205AF TO-39	P	25	8.0	100	0.18
JTXV	557	TO-205AF TO-39	P	25	8.0	100	0.18
2N6798 JAN	557	TO-205AF TO-39	P	25	5.5	200	0.4
JTX	557	TO-205AF TO-39	P	25	5.5	200	0.4
JTXV	557	TO-205AF TO-39	P	25	5.5	200	0.4
2N6800 JAN	557	TO-205AF TO-39	P	25	3.0	400	1.0

Motorola High Reliability Parts Pending QUAL as of JAN 1984 (Continued)

Device Type	MIL-S 19500/	Package	*QUAL Status	P_T (W)	I_D (A)	$V_{(BR)DSS}$ (V)	Ω $r_{DS(on)}$
JTX	557	TO-205AF TO-39	P	25	3.0	400	1.0
JTXV	557	TO-205AF TO-39	P	25	3.0	400	1.0
2N6802 JAN	557	TO-205AF TO-39	P	25	2.5	500	1.5
JTX	557	TO-205AF TO-39	P	25	2.5	500	1.5
JTXV	557	TO-205AF TO-39	P	25	2.5	500	1.5

**P denotes proposed qualifications
***Q denotes qualified

Chapter 14: Mounting Considerations for Power Semiconductors

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INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead-mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one-half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic-packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

(1) MIL-HANDBOOK — 2178, SECTION 2.2.
(2) "Navy Power Supply Reliability — Design and Manufacturing Guidelines" NAVMAT P4855-1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.

Figure 14-1 shows an example of doing nearly everything wrong. A tab mount TO-220 package is shown being used as a replacement for a TO-213AA (TO-66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet-metal screw through a 1/4" hole containing a fiber-insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

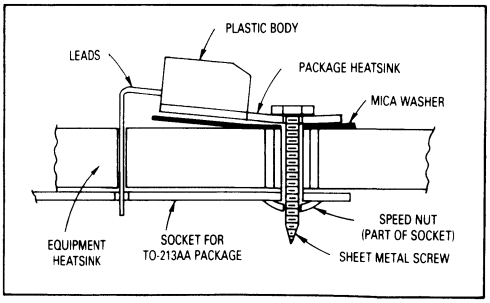


FIGURE 14-1 — EXTREME CASE OF IMPROPERLY MOUNTING A SEMICONDUCTOR (DISTORTION EXAGGERATED)

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc-over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high-power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 14-2. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e, Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO-204 (TO-3) package with a typical 32-microinch finish, showed that heatsink finishes between 16 and 64 μ-in caused less than $\pm 2.5\%$ difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high-power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

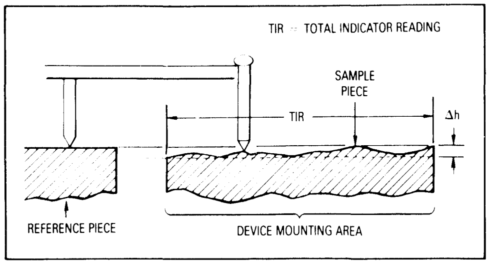


FIGURE 14-2 — SURFACE FLATNESS MEASUREMENT

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO-3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat-dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early-life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine-edge blanking or sheared-through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four-post die sets equipped with proper pressure pads and holding fixtures.

(3) Catalog #87-HS-9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381-0839.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black-anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate-acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock-marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease-like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic-encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 14-3. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called KON-DUX. It is made with a unique, grain oriented, flake-like structure (patent pending). Highly compressible, it becomes

Table 1
Approximate Values for Interface Thermal Resistance Data from Measurements Performed in Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
JEDEC Outlines	Description	Test Torque In-Lb	Metal-to-Metal Dry	Metal-to-Metal Lubed	With Insulator Dry	With Insulator Lubed	With Insulator Type	See Note
DO-203AA, TO-210AA TO-208AB	10-32 Stud 7/16″ Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO-203AB, TO-210AC TO-208	1/4-28 Stud 11/16″ Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO-208AA	Pressfit, 1/2″	—	0.15	0.1	—	—	—	
TO-204AA (TO-3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO-213AA (TO-66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO-126	Thermopad 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO-220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 14-3 and 14-4 for additional data on TO-3 and TO-220 packages.
2. Screw not insulated. See Figure 14-12.

formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non-isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal-to-metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO-204 (TO-3) and TO-220 packages, are shown in Figure 14-3, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 14-3, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut-through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By

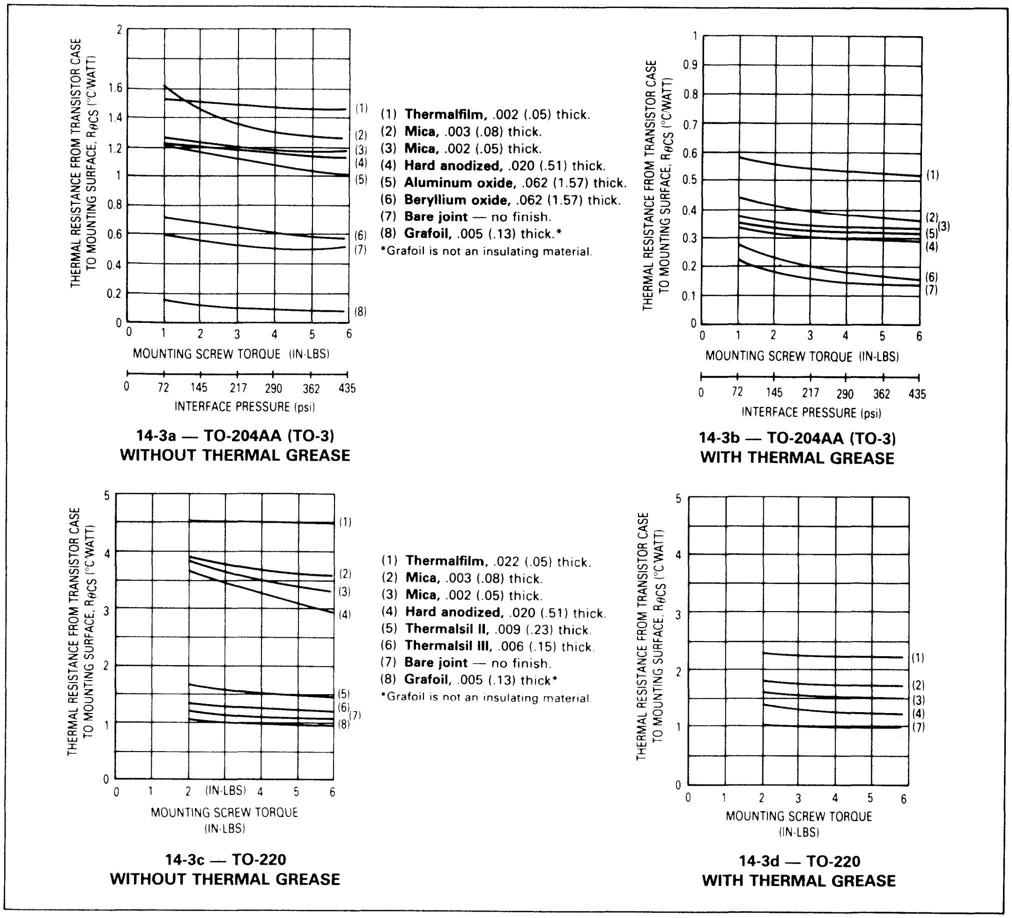


FIGURE 14-3 — INTERFACE THERMAL RESISTANCE FOR TO-204, TO-3 AND TO-220 PACKAGES USING DIFFERENT INSULATING MATERIALS AS A FUNCTION OF MOUNTING SCREW TORQUE (DATA COURTESY THERMALLOY)

comparing Figures 14-3c and 14-3d, it can be noted that Thermasil, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO-220 package.

A number of manufacturers offer silicone rubber insulators. Table 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out-of-flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K-10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called

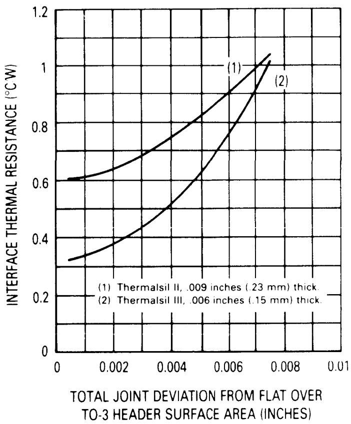
Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173-7	.790	1.175
Bergquist	Sil Pad K-4	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400-9	.735	1.205
Thermalloy	Thermalsil II	.680	1.045
Shin-Etsu	TC-30AG	.664	1.260
Bergquist	Sil Pad 400-7	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174-9	.574	.755
Bergquist	Sil Pad 1000	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermalsil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86-1010.

Rubber-Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO-204AA (TO-3) package insulated with Thermasil is shown on Figure 14-4. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

FIGURE 14-4 — EFFECT OF TOTAL SURFACE FLATNESS ON INTERFACE RESISTANCE USING SILICON RUBBER INSULATORS

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho-Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in-lb from an initial 6 in-lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi-pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost-effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 14-8, Case 806 (ICePAK) and Case 388A (TO-258AA) (see Figure 14-11) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak,

Table 3. Performance of Silicon Rubber Insulators Tested per MIL-I-49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	**Berquist Data(2)**
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho-Therm, 1617	0.233	—
Q Pad (non-insulated)	—	0.009
Sil-Pad, K-10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil-Pad 1000	0.400	0.300
Cho-therm 1674	0.433	—
Thermasil II	0.500	—
Sil-Pad 400	0.533	0.440
Sil-Pad K-4	0.583	0.440

(1) From Thermalloy EIR 87-1030
(2) From Berquist Data Sheet

Case 221C, illustrated in Figure 14-13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non-insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 14-5, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6-32 machine screw.(4)

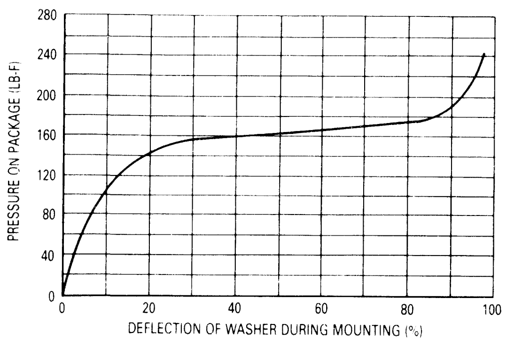


FIGURE 14-5 — CHARACTERISTICS OF THE CONICAL COMPRESSION WASHERS DESIGNED FOR USE WITH PLASTIC BODY MOUNTED SEMICONDUCTORS

(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board-mounted or free-standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO-220 and TO-126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO-220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync-nuts) can form a trouble-free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self-Tapping Screws

Under carefully controlled conditions, sheet-metal screws are acceptable. However, during the tapping-process with a standard screw, a volcano-like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed-nut. If a self tapping process is desired, the screw type must be used which roll-forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange-mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press-riveting is used. Crimping force must be applied slowly and evenly. Pop-riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt

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2-14

furnace, irons, vapor-phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non-field-servicable systems or low strength types for field-serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel- or gold-plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Stud Mount

Parts which fall into the stud-mount classification are shown in Figure 6. Mounting errors with non-insulated stud-mounted parts are generally confined to application

(5) Robert Batson, Elliot Fraunglass and James P. Moran, "Heat Dissipation Through Thermalloy Conductive Adhesives," EMTAS '83. Conference, February 1-3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

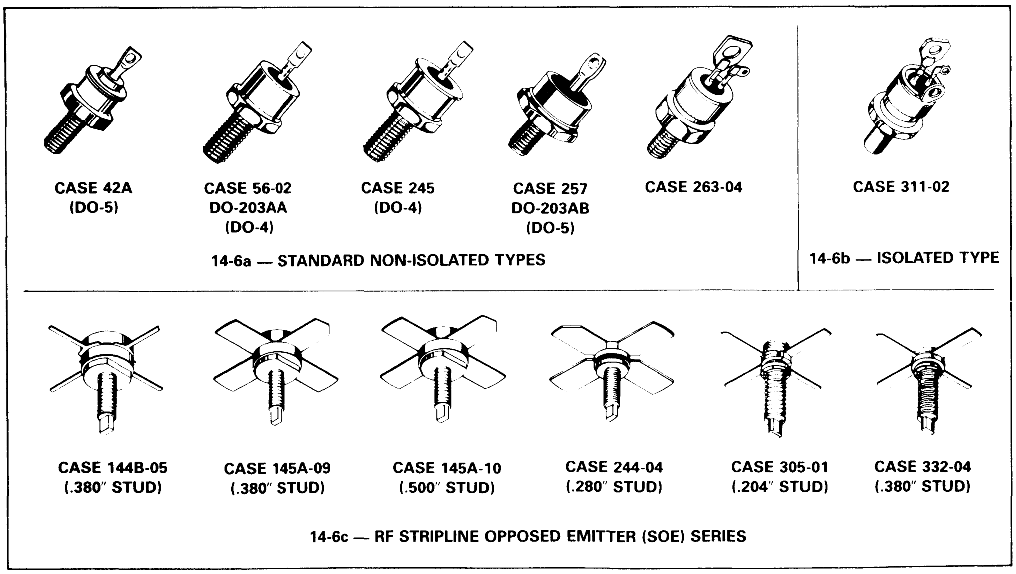


FIGURE 14-6 — A VARIETY OF STUD-MOUNT PARTS of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 14-7.

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non-insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a berrylium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

R.F. transistors in the stud-mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic — metal interface are discussed in the section entitled "Connecting and Handling Terminals."

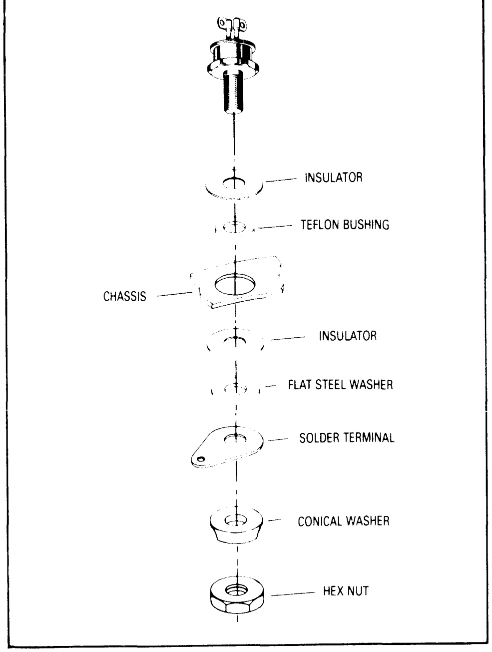
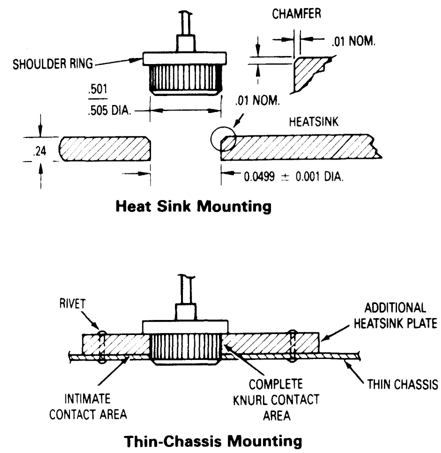


FIGURE 14-7 — ISOLATING HARDWARE USED FOR A NON-ISOLATED STUD-MOUNT PACKAGE

Press Fit

For most applications, the press-fit case should be mounted according to the instructions shown in Figure 14-8. A special fixture meeting the necessary requirements must be used.



The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press-in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper-less than 50 on the Rockwell F scale; aluminum-less than 65 on the Brinell scale. A heatsink as thin as 1/8" may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

FIGURE 14-8 — PRESS-FIT PACKAGE

Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 14-9. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO-204 (TO-3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger-tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 14-10. Machine screws (preferred) self-tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section. "Fastener and Hardware Characteristics."

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No

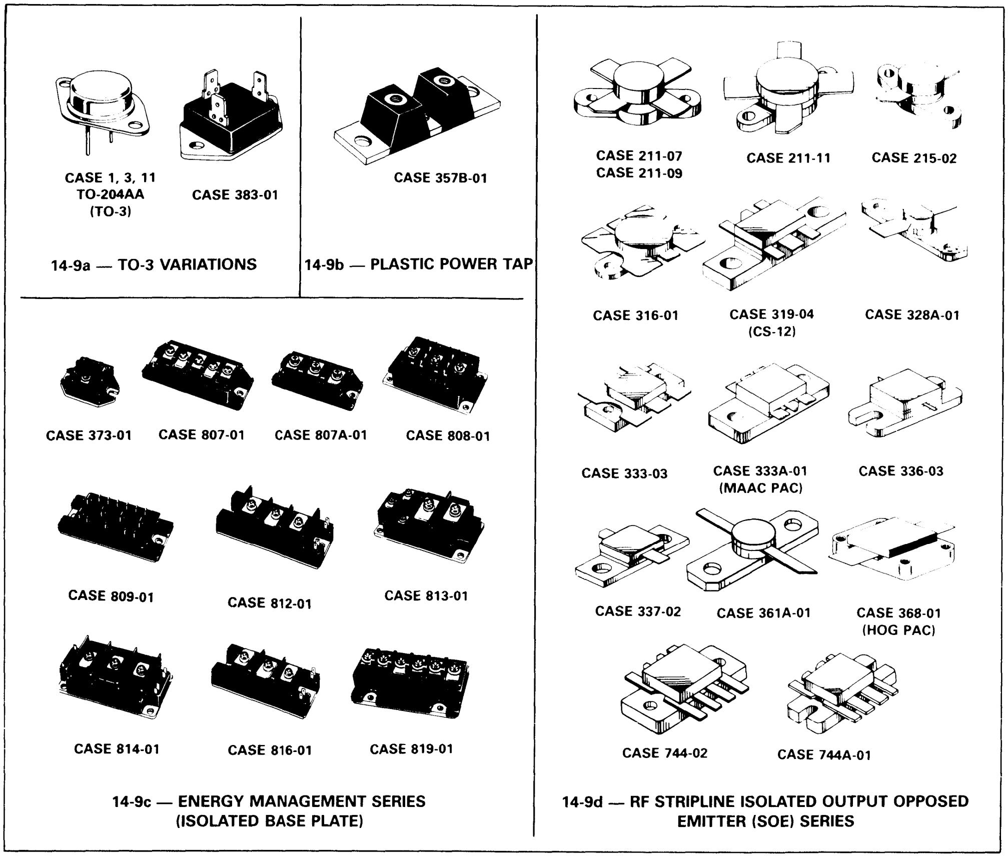


FIGURE 14-9 — A LARGE ARRAY OF PARTS FIT INTO THE FLANGE-MOUNT CLASSIFICATION

special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 14-9b, final torque should be applied first to the center position.

The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in EB107 "Mounting Considerations for Motorola RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368-1 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4–40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid-section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center

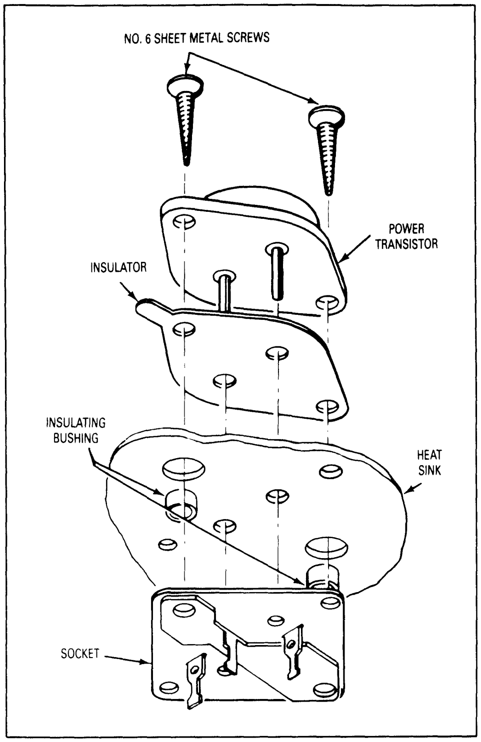


FIGURE 14-10 — HARDWARE USED FOR A TO-204AA (TO-3) FLANGE MOUNT PART

of the flange, deforming it. Deformations of 2–3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 14-11. Mounting considerations for all varieties are similar to that for the popular TO-220 package, whose suggested mounting arrangements and hardware are shown in Figure 14-12. The rectangular washer shown in Figure 14-12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO-220 packages have a chamfer on one end. TO-220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO-220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

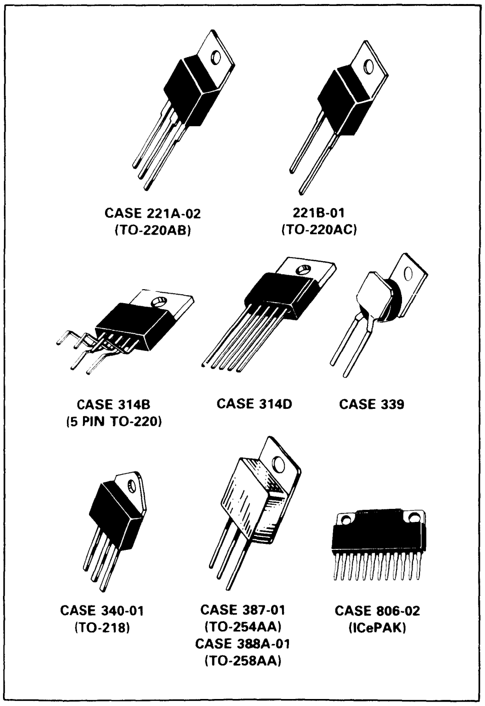


FIGURE 14-11 — SEVERAL TYPES OF TAB-MOUNT PARTS

2

2-14

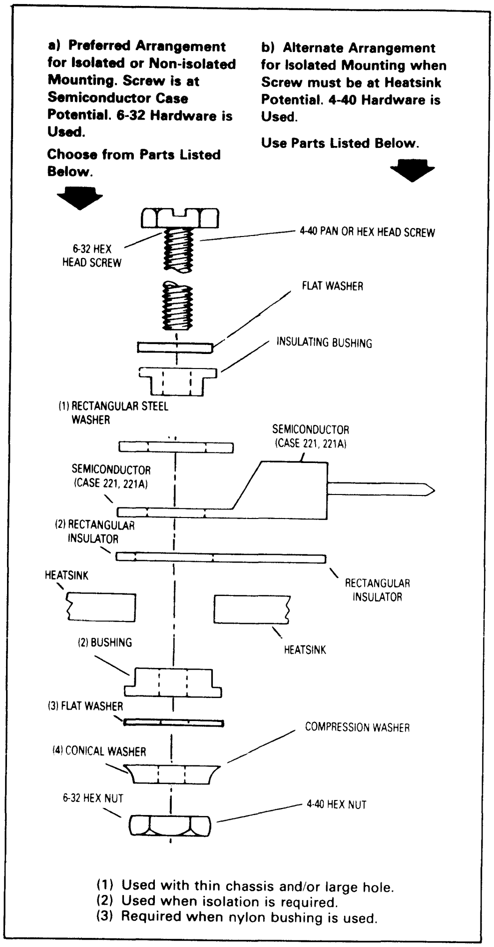


FIGURE 14-12 — MOUNTING ARRANGEMENTS FOR TAB MOUNT TO-220

the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 14-15c. To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806-02) is basically an elongated TO-220 package with isolated chips. The mounting precautions for the TO-220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.

Plastic Body Mount

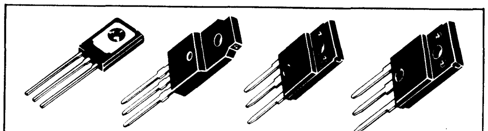
The Thermopad and Full Pak plastic power packages shown in Figure 14-13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die-bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The Full Pak (Case 221C-01) is similar to a TO-220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO-220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air-driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 14-5.

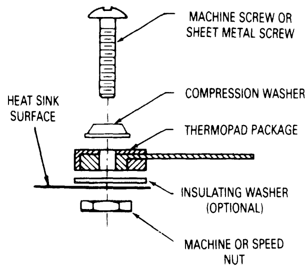
Figure 14-14 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The Full Pak, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO-220. As shown in Figure 14-15c, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 14-15b may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO-220 package which is shown in Figure 14-15a.

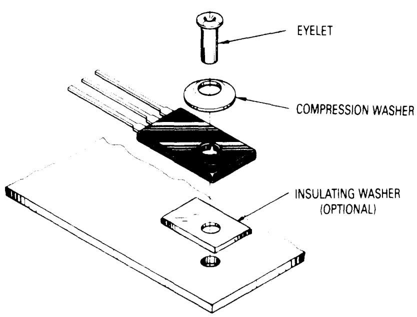


CASE 77 (TO-225AA/ TO-126) (THERMOPAD) | **CASE 221C-01 (Full Pak)** | **CASE 221D-01 (Full Pak)** | **CASE 340B-03 (Full Pak)**

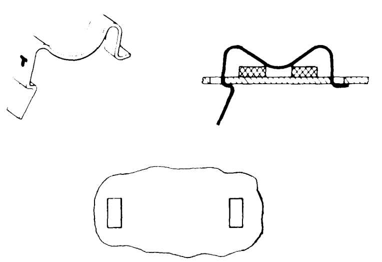
FIGURE 14-13 — PLASTIC BODY-MOUNT PACKAGES



14-14a — MACHINE SCREW MOUNTING

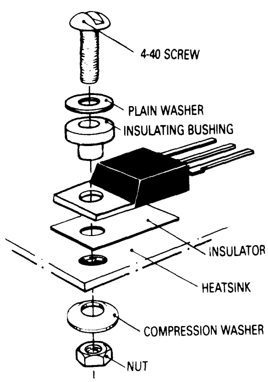


14-14b — EYELET MOUNTING

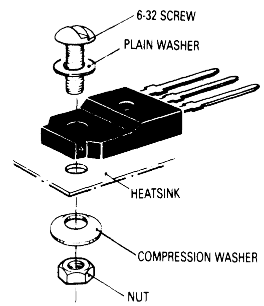


14-14c — CLIPS

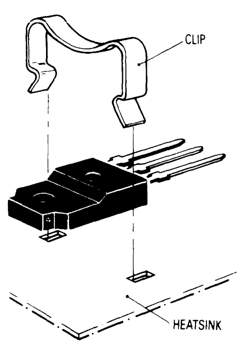
FIGURE 14-14 — RECOMMENDED MOUNTING ARRANGEMENTS FOR TO-225AA (TO-126) THERMOPAD PACKAGES



14-15a — SCREW-MOUNTED TO-220



14-15b — SCREW-MOUNTED FULL PAK



14-15c — CLIP-MOUNTED FULL PAK

FIGURE 14-15 — MOUNTING ARRANGEMENTS FOR THE FULL PAK AS COMPARED TO A CONVENTIONAL TO-220

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 14-16, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard Glass-Epoxy 2-ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 14-17 shows, thermal resistance asymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.[7] The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

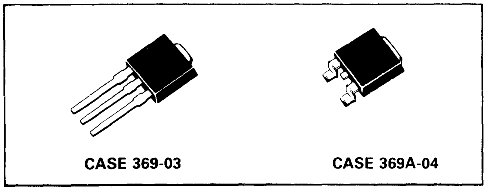


FIGURE 14-16 — SURFACE MOUNT DPAK PARTS

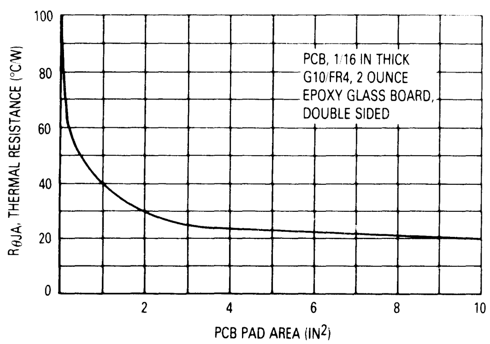


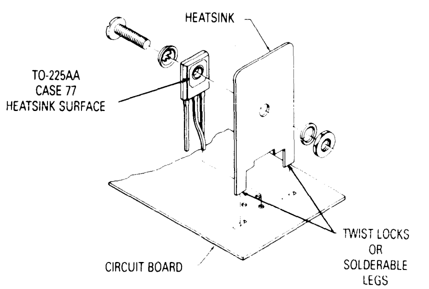
FIGURE 14-17 — EFFECT OF FOOTPRINT AREA ON THERMAL RESISTANCE OF DPAK MOUNTED ON A GLASS-EPOXY BOARD

FREE AIR AND SOCKET MOUNTING

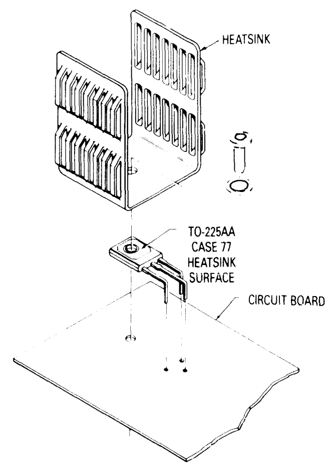
In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO-220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the CASE 77 (TO-225AA) (TO-127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 14-18. The arrangement of part (a) could be used with any plastic package, but the scheme of part (14-18b) is more practical

(7) Herb Fick, "Thermal Management of Surface Mount Power Devices," Powerconversion and Intelligent Motion, August 1987.



14-18a — SIMPLE PLATE, VERTICALLY MOUNTED



14-18b — COMMERCIAL SINK, HORIZONTALLY MOUNTED

FIGURE 14-18 — METHODS OF USING SMALL HEATSINKS WITH PLASTIC SEMICONDUCTOR PACKAGES

with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

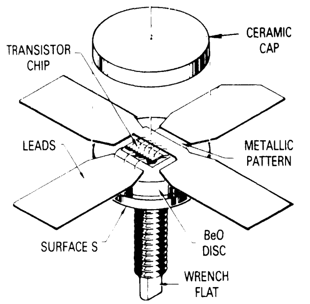
The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead-bending unnecessary. Numerous lead- and tab-forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead-bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

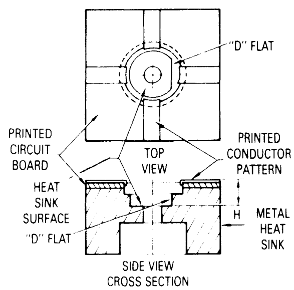
The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO-225AA (CASE 77) and 1/32 inch for TO-220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

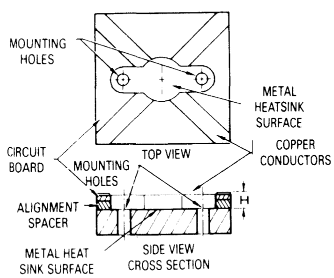
The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be



14-19a — COMPONENT PARTS OF A STUD MOUNT PACKAGE. FLANGE MOUNTED PACKAGES STRIPLINE ARE SIMILARLY CONSTRUCTED



14-19b — TYPICAL STUD TYPE SOE TRANSISTOR MOUNTING METHOD



14-19c — FLANGE TYPE SOE TRANSISTOR MOUNTING METHOD

FIGURE 14-19 — MOUNTING DETAILS FOR SOE TRANSISTORS

exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire-wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 14-19. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic-to-metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 14-19b shows a cross-section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D-flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud — BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead-soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

Figure 14-19c shows a typical mounting technique for flange-type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free-standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where
- T_J = junction temperature (°C)
- T_C = case temperature (°C)
- $R_{\theta JC}$ = thermal resistance junction-to-case as specified on the data sheet (°C/W)
- P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the "test" position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady-state conditions is generally written as:

$$q = hA\Delta T \qquad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \qquad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A1.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \qquad (3)$$

where T_J = junction temperature,
P_D = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heatsink),
$R_{\theta SA}$ = heatsink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal-resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short-pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

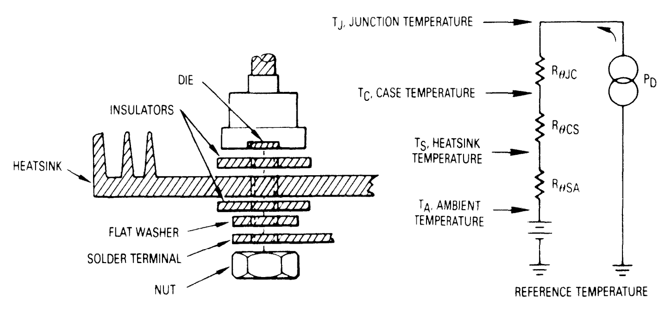


FIGURE A1 — BASIC THERMAL RESISTANCE MODEL SHOWING THERMAL TO ELECTRICAL ANALOGY FOR A SEMICONDUCTOR

2

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO-3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL-I-49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO-220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO-220 package shown in Figure B1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO-220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

a. The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

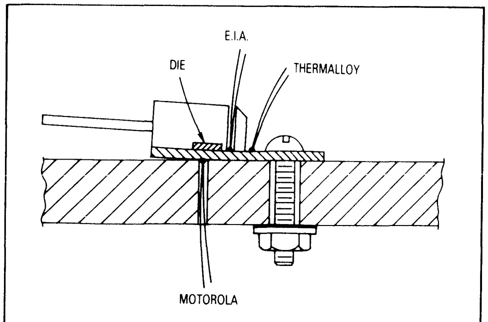


FIGURE B1 — JEDEC TO-220 PACKAGE MOUNTED TO HEATSINK SHOWING VARIOUS THERMOCOUPLE LOCATIONS AND LIFTING CAUSED BY PRESSURE AT ONE END

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction-to-sink thermal resistance must be constant for a given test setup, the calculated junction-to-case thermal resistance values decrease and case-to-sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO-220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction-to-case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ-inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application-oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction-to-case thermal resistance while testing for interface thermal resistance. If the junction-to-case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber	
Aavid Eng.	X	X	—	—	—	—	—	X	X
AHAM-TOR	—	—	—	—	—	—	—	—	X
Astrodynamis	X	—	—	—	—	—	—	—	X
Delbert Blinn	—	—	X	—	X	X	X	X	X
IERC	X	—	—	—	—	—	—	—	X
Staver	—	—	—	—	—	—	—	—	X
Thermalloy	X	X	X	X	X	X	X	X	X
Tran-tec	—	—	X	X	X	X	—	X	X
Wakefield Eng.	X	X	X	—	X	—	—	X	X

Other sources for silicone rubber pads: Chomerics, Berquist

Suppliers Addresses

Aavid Engineering, Inc., 30 Cook Court, Laconia, New Hampshire 03246 (603) 524-4443

AHAM-TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676-4151

Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935-4944

Berquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835-2322

Chomerics, Inc., 16 Flagstone Drive, Hudson, New Hampshire 03051 1-800-633-8800

Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 629-3900

International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849-2481

The Staver Company, Inc., 41-51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666-8000

Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243-4321

Tran-tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564-2748

Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245-5900

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non-related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re-registered to the new system as time permitted.

For example the venerable TO-3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO-204 family. The TO-204AA conforms to the original outline for the TO-3 having 40 mil pins while the TO-204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO-4, DO-5 and TO-3 still convey sufficient meaning for general verbal communication.

Motorola Case Number	JEDEC Outline: Original System	JEDEC Outline: Revised System	Notes	Mounting Class	See Page
001	TO-3	TO-204AA		Flange	14-9
003	TO-3		2	Flange	14-9
009	TO-61	TO-210AC		Stud	14-8
011	TO-3	TO-204AA	—	Flange	14-9
011A	TO-3	—	2	Flange	14-9
012	TO-3	—	2	Flange	14-9
036	TO-60	TO-210AB	—	Stud	14-8
042A	DO-5	DO-203AB	—	Stud	14-8
044	DO-4	DO-203AA	—	Stud	14-8
054	TO-3	—	2	Flange	14-9
056	DO-4	—	—	Stud	14-8
058	DO-5	—	2	Stud	14-8
61-03				Flange	14-9
63-02	TO-64	TO-208AB		Stud	14-8
63-03	TO-64	TO-2088AB		Stud	14-8
077	TO-126	TO-225AA	—	Plastic	14-12
080	TO-66	TO-213AA	—	Flange	14-9
086	—	TO-208	1	Stud	14-8
086L	—	TO-298	1	Stud	14-8
144B-05				Stud	14-8
145A-09				Stud	14-8
145A-10				Stud	14-8
145C	TO-232		1	Stud	14-8
157	—	DO-203	1	Stud	14-8
160-03	TO-59	TO-210AA	—	Stud	14-8
167	—	DO-203	1	Stud	14-8
174-04				Pressfit	14-9
175-03				Stud	14-8

Motorola Case Number	JEDEC Outline: Original System	JEDEC Outline: Revised System	Notes	Mounting Class	See Page
197	—	TO-204AE	—	Flange	14-9
211-07				Flange	14-9
211-09				Flange	14-9
211-11				Flange	14-9
215-02				Flange	14-9
221	—	TO-220AB	—	Tab	14-11
221C-02				Plastic	14-12
221D-01	—	—	Isolated TO-220	Plastic	14-12
235	—	TO-208	1	Stud	14-8
235-03				Stud	14-8
238	—	TO-208	1	Stud	14-8
239	—	TO-208	—	Stud	14-8
244-04				Stud	14-8
245	DO-4	—	—	Stud	14-8
257-01	DO-5	—	—	Stud	14-8
263	—	TO-208	—	Stud	14-8
263-04				Stud	14-8
283	DO-4	—	—	Stud	14-8
289	—	TO-209	1	Stud	14-8
305-01				Stud	14-8
310-02				Pressfit	14-9
311-01			Isolated	Stud	14-8
311-02				Pressfit	14-9
311-02				Stud	14-8
314B-01				Tab	14-11
314D-01				Tab	14-11
316-01				Flange	14-9

Motorola Case Number	JEDEC Outline Original System	JEDEC Outline Revised System	Notes	Mounting Class	See Page
319-04				Flange	14-9
328A-01				Flange	14-9
332-04				Stud	14-8
333-03				Flange	14-9
333A-01				Flange	14-9
336-03				Flange	14-9
337-02				Flange	14-9
340		TO-218AC		Tab	14-11
340A-02				Plastic	14-12
340B-03			Isolated TO-218	Plastic	14-12
342-01				Flange	14-9
357B-01				Flange	14-9
361-01				Flange	14-9
368-01				Flange	14-9
369-03		TO-251		Insertion	14-14
369A-04		TO-252		Surface	14-13
373-01			Isolated	Flange	14-9
383-01			Isolated	Flange	14-10

Motorola Case Number	JEDEC Outline Original System	JEDEC Outline Revised System	Notes	Mounting Class	See Page
387-01		TO-254AA	Isolated 2	Tab	14-11
388A-01		TO-258AA	Isolated 2	Tab	14-11
744-02				Flange	14-9
744A-01				Flange	14-9
806-02			Isolated	Flange	14-9
807-01			Isolated	Flange	14-9
807-02			Isolated	Flange	14-9
807A-01			Isolated	Flange	14-9
808-01			Isolated	Flange	14-9
809-01			Isolated	Flange	14-9
812-01			Isolated	Flange	14-9
813-01			Isolated	Flange	14-9
814-01			Isolated	Flange	14-9
814A-01			Isolated	Flange	14-9
084B-01			Isolated	Flange	14-9
816-01			Isolated	Flange	14-9
819-01			Isolated	Flange	14-9
043-02	DO-21	DO-208AA		Pressfit	14-9

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

2

2-14

Chapter 15: Electrostatic Discharge and Power MOSFETs

One of the major problems plaguing electronics components today is damage by electrostatic discharge (ESD). ESD can cause degradation or complete component failure. Shown in Table 1 are the susceptibility ranges of various technologies to ESD. As circuitry becomes more complex and dense, device geometries shrink, making ESD a major concern of the electronics Industry.

Generation of ESD

Electrostatic potential is a function of the relative position of non-conductors on the list of materials known as the Triboelectric Series, (See Table 2.) Additional factors in charge generation are the intimacy of contact, rate of separation and humidity, which makes the material surfaces partially conductive. Whenever two non-conductive materials are flowing or moving with respect to each other, an electrostatic potential is generated.

TABLE 1 — ESD Susceptibility of Various Technologies

Device Type	Range of ESD Susceptibility (Volts)
Power MOSFET	100–2,000
Power Darlingtons	20,000–40,000
JFET	140–10,000
Zener Diodes	40,000
Schottky Diodes	300–2,500
Bipolar Transistors	380–7,000
CMOS	250–2,000
ECL (ICs)	500
TTL	300–2,500

TABLE 2 — Triboelectric Series

Material	
Air	Increasingly Positive
Human Skin	
Glass	
Human Hair	
Wool	
Fur	
Paper	
Cotton	
Wood	Increasingly Negative
Hard Rubber	
Acetate Rayon	
Polyester	
Polyurethane	
PVC (Vinyl)	
Teflon	

*A more complete table appears in DOD-HDBK-263

From Table 2, it can be seen that cotton is relatively neutral. The materials that tend to reject moisture are the most significant contributors to ESD. Table 3, also excerpted from DOD-HDBK-263, gives examples of the potentials that can be generated under various conditions.

TABLE 3 — Typical Electrostatic Voltages

Means of Static Generation	Electrostatic Voltages: 10 to 20 Percent Relative Humidity	Electrostatic Voltages: 65 to 90 Percent Relative Humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes per work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

From these three Tables, it is apparent that sensitive electronic components can be damaged or destroyed if precautions are not taken, and that the necessary voltages can be *easily* generated.

ESD and Power MOSFETs

Being MOS devices, TMOS transistors can be damaged by ESD due to improper handling or installation. However, TMOS devices are not as susceptible as CMOS. Due to their large input capacitances, they are able to absorb more energy before being charged to the gate-breakdown voltage. Nevertheless, once breakdown begins, there is enough energy stored in the gate-source capacitance to cause complete perforation of the gate oxide. With a gate-to-source rating of $V_{GS} = \pm 20$ V maximum and electrostatic voltages typically being 100–25,000 volts, it becomes very clear that these devices require special handling procedures. Figure 15-1 shows curve tracer drawings of a good device, and the same device degraded by ESD.

Static Protection

The basic method for protecting electronic components combines the prevention of static build up with the removal of existing charges. The mechanism of charge removal from charged objects differs between insulators and conductors. Since charge cannot flow through an insulator, it cannot be removed by contact with a conductor. If the item to be discharged is an insulator (plastic box, person's clothing, etc.), ionized air is required. If the object to be discharged is a conductor (metal tray, conductive bag, person's body, etc.), complete discharge can be accomplished by grounding it.

A complete static-safe work station should include a grounded conductive table top, floor mats, grounded operators (wrist straps), conductive containers, and an ionized air blower to remove static from non-conductors. All soldering irons should be grounded. All non-conductive items such as styrofoam coffee cups, cellophane wrappers, paper, plastic handbags, etc. should be removed from the work area. A periodic survey of the work area with a static

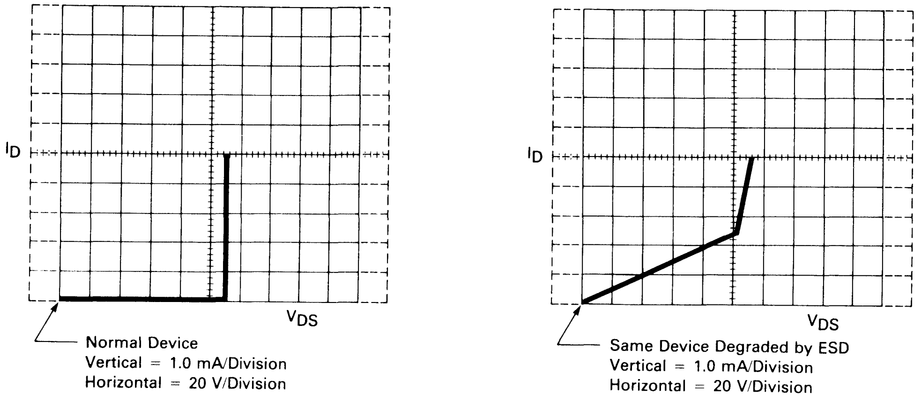


FIGURE 15-1 — CURVE TRACER DRAWINGS OF V_{DS} versus I_D OF A GOOD DEVICE (LEFT), AND A DEVICE IN WHICH THE GATE WAS DAMAGED WITH ESD (RIGHT). THE GATE IN THIS DEVICE IS LIKELY A RESISTIVE SHORT.

meter is good practice and any problems detected should be corrected immediately. Above all, education of all personnel in the proper handling of static-sensitive devices is key to preventing ESD failures. Figure 15-2 shows a typical ESD test work station.

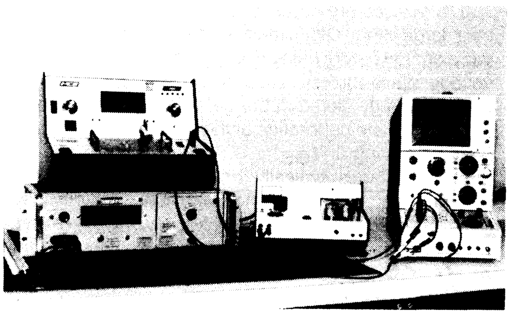


FIGURE 15-2 — TYPICAL ESD WORKSTATION WITH GROUNDED TABLE MAT. THE CIRCUIT DIAGRAM FOR THE ESD TESTER IN THE CENTER OF THE PHOTO APPEARS IN FIGURE 15-4. THE TESTER AT THE TOP LEFT IS A COMMERCIAL UNIT.

By following the above procedures, and using the proper equipment, ESD sensitive devices can be handled without being damaged. The key items to remember are:

1 — Handle all static sensitive components at a static safeguarded work area.

2 — Transport all static sensitive components in static shielding containers or packages.

3 — Education of all personnel in proper handling of static sensitive components.

Test Method:

Military specifications MIL-STD-883B Method 3015.1, MIL-STD-750C, Method 1020, DOD-HDBK263, and DOD-STD-1686 classify the sensitivity of semiconductor devices to electrostatic discharge as a function of exposure to the output of a charged network (Table 4). Through measurements and general agreement, the "human-body model" (HBM) was specified as a network that closely approximated the charge storage capability (100 pF) and the series resistance (1.5 k) of a typical individual (Figure 15-3). Discharge of this network directly into a device indicates that the model assumes a "hard" ground is in contact with the part. Although all pin combinations should be evaluated in both polarities (a total of six combinations for a TMOS Power MOSFET), preliminary tests usually show that gate-oxide breakdown is most likely, and that reverse-biased junctions are about an order of magnitude more sensitive than forward-biased ones. The amount of testing, and components required, can therefore be reduced to sensible levels, yet still yield statistically sound data. The damage mechanism, which can be identified through failure analysis of shorted or degraded samples, is usually oxide puncture or junction meltthrough.

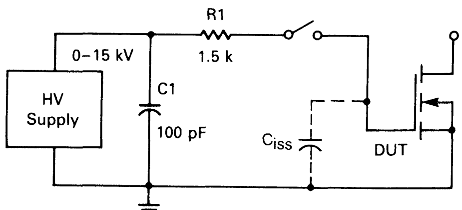


FIGURE 15-3 — THE HUMAN-BODY EQUIVALENT NETWORK WITH C_{iss} PARASITIC ELEMENT IN DASHED LINES.

Significance of Sensitivity Data

Assuming that corrective measures cannot be immediately applied in a manufacturing area, or that products manufactured using MOSFET components are likely to be exposed to ESD events in the field, the sensitivity of the device can be used as a general indicator of the likelihood of failure. Additionally, the extent and cost of protective measures increases as device susceptibility increases.

TABLE 4 — Sensitivity of Semiconductors to ESD from a Charged Network (HBM)

Device Sensitivity (C_1 Peak Voltage)	MIL-STD-883 Class	DOD-HDBK-263 Class	Typical Preventive Measures(2)
0–1000	A (Sensitive)	Class 1	Careful Case, Keyboard Design, Wrist Straps, Ionized Air,
1000–2000	A	Class 2	Conductive Flooring, Conductive Clothing, etc. Field-Strength Alarm.
2000–4000	B (Nonsensitive)	Class 3	Antistatic Carpet Spray, Wrist Straps, Conductive Packaging Materials.
4000–15,000(1)	B	Class 3	Humidity Adjustment

Notes: 1. Data collected in many applications have shown that under special conditions voltages considerably in excess of 15 kV can be generated with certain materials in the Triboelectric Series. (Table 3)

2. These examples are intended only as very general guidelines. The actual accuracy of a given method is highly variable, as a large number of interdependent factors influence electrostatic field generation. Operator awareness, complemented with a high quality hand-held electrostatic field-strength meter *referenced to ground,* can be very effective in controlling losses due to ESD.

Measuring Device Sensitivity

A Simple ESD Pulser

As shown in the circuit diagram, Figure 15-4, the tester consists of a high voltage supply utilizing a Darlington transistor oscillator driving a television flyback transformer. The high voltage is rectified by a commercially-available color television semiconductor tripler module. A single low-voltage power supply of about 20 volts is used for the entire tester. The high voltage power supply is adjusted by means of a ten-turn potentiometer and an I.C. series regulator. Use of a Bourns Knobpot®, having a clock-type turns-counting dial, gives coarse adjustment indication.

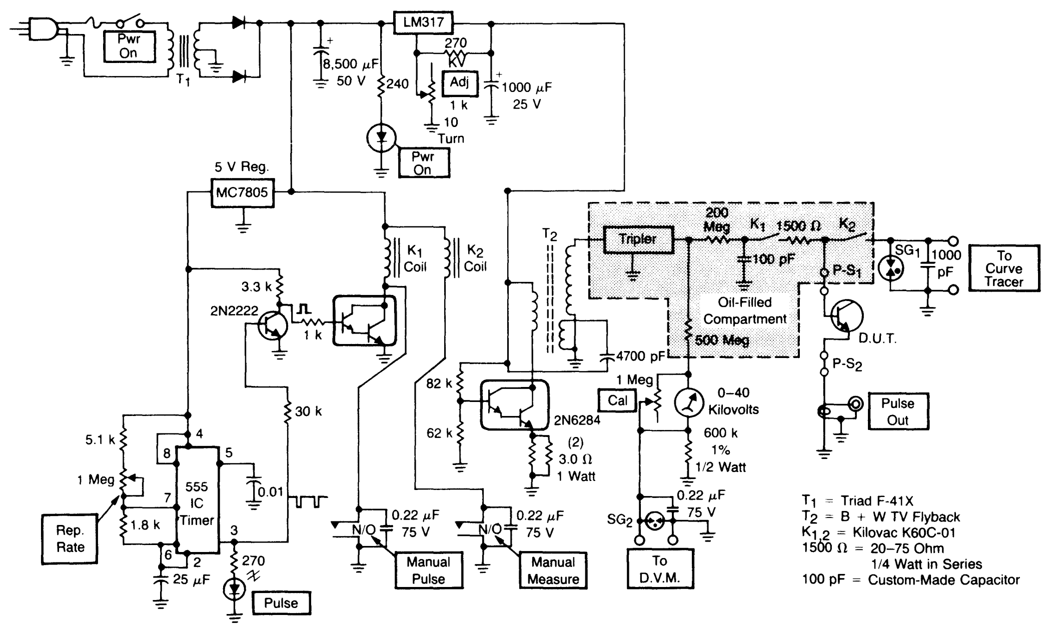


FIGURE 15-4 — ESD (ELECTRO STATIC DISCHARGE) TESTER WITH 40 KILOVOLT CAPABILITY

A small manually-operated ESD pulser is relatively easy to construct. A view of this pulser appears in the center of Figure 15-2.

Although this tester is capable of testing over the entire voltage range of DOD-HDBK-263 and is capable of much higher voltages than would be used for characterizing TMOS devices, its design is typical.

The high voltage is monitored by means of components removed from a color television hand-held high voltage probe. The probe is disassembled, and the meter, accurate to about 5%, was mounted on the front panel. An additional resistor is placed in series with the divider string, and front panel jacks are provided to connect it to an external digital voltmeter (DVM). A calibration potentiometer is provided, so that the instrument can be placed on a regular schedule of periodic calibration and maintenance. Bipolar transistors are used as drivers for the relays in the DUT circuit. Most ESD measurements were made by hand, alternately pushing the pulse button, then, after a safe delay, or "cooling period," the measurement button.

High-Voltage Components

The high-voltage circuit has been stippled for clarity. High-voltage vacuum reed relays are not used because they are limited in working voltage by the physical separation between the coil windings and the end of the glass envelope. Kilovac, of Santa Barbara, California, manufactures miniaturized vacuum relays to 100 kV. One type, the K-60-C, is ceramic-cased, and of small size suitable for the tester. The terminal spacing limits it to 15 kV operation, so the relay is purchased without the normal silicone rubber encapsulation and the tester high-voltage compartment is immersed in ordinary colorless mineral oil. The manufacturer further increases the voltage rating by filling the relay with sulfur hexafluoride gas (SF6) under pressure, which eliminates contact arcing.

High-voltage capacitors of reasonable size are obtained from the Maida Capacitor Company. The dielectric is carefully chosen to have a low voltage cofficient. Many ceramic dielectrics have a voltage coefficient as large as 40%, and the capacitance would not meet the +10% capacitance tolerance requirement in MIL-STDs 750 and 883A at extended voltages.

The 1.5 kOhm series resistor must be specially designed to be ESD-resistant. It is constructed by the series connection of 20–75 ohm, 1/4 watt carbon composition resistors. This is necessary because the breakdown of the resistors during pulsing would cause the test circuit to become the zero-ohm model, and improper ESD sensitivity values would be obtained.

The High-Voltage Compartment

The high-voltage section of the tester was built in a dielectric filled compartment. Mineral oil, castor oil, parafin oil, silicone oil, and transformer oil, all will work equally well. Beware that these liquids are flammable. Use of polychlorinated biphenyl (PCB), a fireproof dielectric liquid, should be avoided, as it is toxic. The inclusion of the 600 megohm divider resistor and the small custom-made high voltage ceramic capacitor in the oil-filled compartment eliminated the need for corona shields, large physical spacings, and silicone rubber terminal coverings. Operation to 43 kV is very reliable.

The design of flyback transformers has been perfected over the years for continuous operation in air, and it is not placed in the oil-filled compartment.

Test Method

The threshold, or step-stress, method is used to classify device sensitivity, as discussed in DOD-HDBK-263 in paragraph 6.6.2. This method is a time-saver compared to the categorization method, and is very useful with discrete devices. Additionally, the ESD sensitivity of a device can be determined exactly. The waveform is monitored with the use of a Tektronix 2467, 350 MHz real-time oscilloscope with a CT-1 current transformer and P6040 probe. The transformer was placed on the ground side of the device under test.

Failure Criteria

The tester is deliberately kept simple in design, so the relays are operated manually with pushbuttons. The voltage is manually adjusted in increasing increments until any change in the characteristics of the device under test is indicated on the curve tracer. No coincidence lockout circuit is provided. Simultaneous closure of K1 and K2 would shunt the DUT with the curve-tracer input capacitance. In some cases, the curve tracer could be damaged. Technically-oriented operators should be used.

It is easily understood that the resolution of the tester in this manual configuration is limited by the size of the voltage steps between relay closures. Automating this operation could be quite complex, depending on the test strategy and data reduction methods. Certainly, this tester lends itself to microprocessor or computer control, and interface circuits to accomplish this are already on the market. The voltage increment can then be set very small for good accuracy, and the system can be left unattended to find the threshold, stop testing, print out the data, and continue with the next part. Such testers, intended primarily for I.C.s, are commercially available.

Warning:

Caution is advised in the construction and operation of this circuit, as the potentials and stored energies in this circuit may be ***lethal.*** Every effort should be made to shield operators from the possibility of contact. Motorola cannot be responsible for claims resulting from the use, or misuse, of this circuit.

Test Results

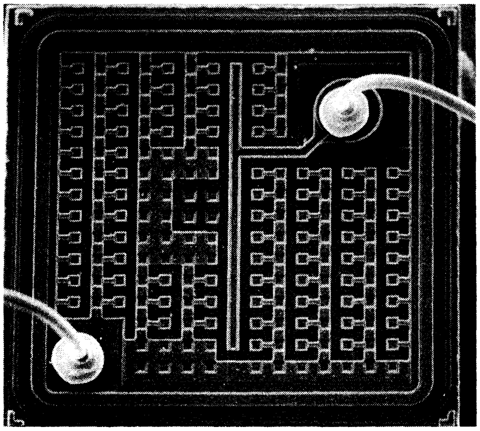
Measurement of ESD sensitivity thresholds using the 100 pF–1.5 k circuit has produced the results shown below. An important conclusion from this data is that the ESD sensitivity decreases as the die size (and power-handling capability) increase. Part of the explanation for this phenomenon is that C_{iss} increases as die size increases. Referring to Figure 15-3, we are discharging the HBM network into a larger and larger capacitive load. Also, these devices fall at or below the 2,000 volt limit, defined by Mil-Std-750C as that which classifies a device as static-sensitive. Power MOSFETs, then, should be handled with proper precautions.

TABLE 5 — Test Results

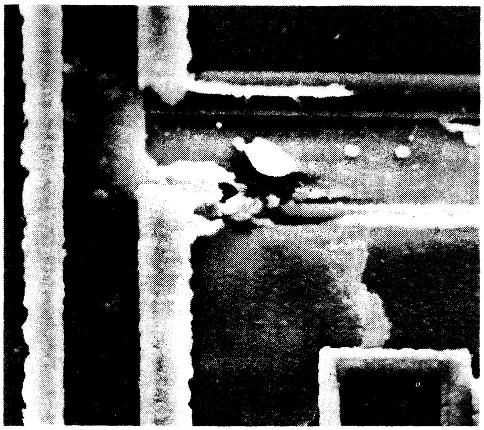
Device	Ratings	Die Size ($Mils^2$)	C_{iss} (pF)	Sensitivity (Volts)
2N7000 (Sm. Signal, TMOS)	0.5 A, 60 V, N-CH, Plastic (TO-92)	30^2	60	135
MTP5N05(1)	5.0 A, 50 V, N-CH, Plastic (TO-220)	76^2	150	520
MTP15N05	15 A, 50 V, N-CH, Plastic (TO-220)	150^2	700	880
MTM6N60	6.0 A, 600 V, N-CH, Metal (TO-3)	199^2	1400	1350
MTM8N60	8.0 A, 600 V, N-CH, Metal (TO-3)	250^2	2000	1500

(1) Tests were conducted with devices which were of the original TMOS technology. Newer devices have smaller input capacitances.

The scanning electron microscope (SEM) photos of Figure 15-5 illustrate the typical damage caused to power and small-signal MOSFETs by electrostatic discharge (ESD). The most prominent mechanism is puncturing of the thin gate oxide, followed by melting of the silicon.



Low Power (100X)



High Power (1300X)

FIGURE 5-5 — RESULT OF EXPOSURE OF THE GATE AND SOURCE OF A 2N7000 SMALL-SIGNAL TMOS DEVICE TO A SINGLE 1,000 VOLT ESD PULSE.

2

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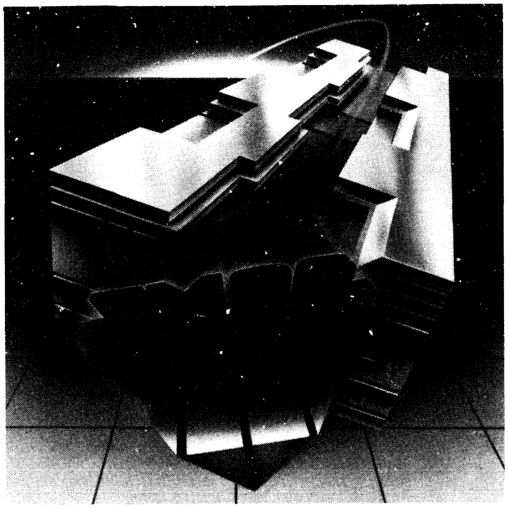
2

2-15



Data sheets are arranged in alphanumeric sequence except when information applies to more than one device, e.g., MTM5N35, MTM5N40, MTP5N35 and MTP5N40. Consult the table of contents for these part numbers.

Data Sheets

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

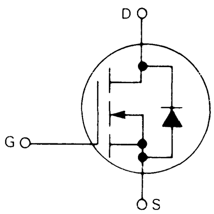
2N6660 MPF6660
2N6661 MPF6661

N-CHANNEL ENHANCEMENT-MODE
TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 5.0$ ns Max
- Low On-Resistance — 2.0 Ohm Typ — 2N6660/2N6661
  — MPF6660/MPF6661
- Low Drive Requirement, $V_{GS(th)} = 2.0$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

TMOS

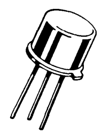


2.0 AMPERE

N-CHANNEL TMOS FET

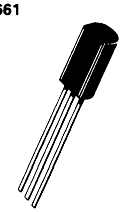
60, 90 VOLTS

2N6660
2N6661



CASE 79-04
TO-205AD

MPF6660
MPF6661



CASE 29-03
TO-226AE

MAXIMUM RATINGS

Rating	Symbol	2N6660 MPF6660	2N6661 MPF6661	Unit
Drain-Source Voltage	V_{DSS}	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	60	90	Vdc
Gate-Source Voltage	V_{GS}	± 30		Vdc
Drain Current — Continuous (1) Pulsed (2)	I_D I_{DM}	2.0 3.0		Adc

THERMAL CHARACTERISTICS

Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	6.25 50	2.5 20	Watts mW/°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	— —	1.0 8.0	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150		°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs Duty Cycle ≤ 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$				Vdc
2N6660, MPF6660		60	—	—	
2N6661, MPF6661		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)	I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 V, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	1.4	2.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 1.0 A)	$V_{DS(on)}$				Vdc
2N6660, MPF6660		—	—	3.0	
2N6661, MPF6661		—	—	4.0	
(V_{GS} = 5.0 V, I_D = 0.3 A)					
2N6660, MPF6660		—	0.9	1.5	
2N6661, MPF6661		—	0.9	1.6	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$r_{DS(on)}$				Ohms
2N6660, MPF6660		—	—	3.0	
2N6661, MPF6661		—	—	4.0	
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)	g_{FS}	170	—	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	30	50	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	20	40	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	3.6	10	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time (See Figure 1)	t_{on}	—	—	5.0	ns
Turn-Off Time (See Figure 1)	t_{off}	—	—	5.0	ns
Rise Time	t_r	—	—	5.0	ns
Fall Time	t_f	—	—	5.0	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

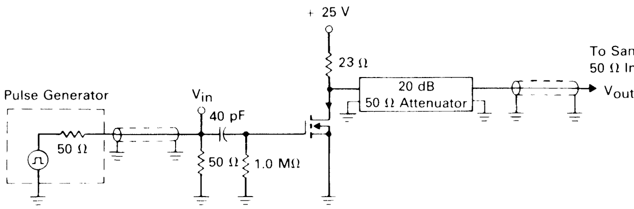


FIGURE 2 — SWITCHING WAVEFORMS

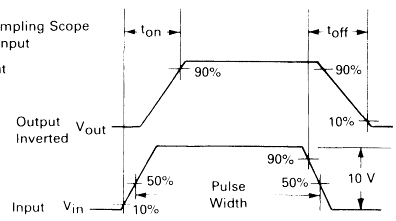


FIGURE 3 — $V_{GS(th)}$ NORMALIZED versus TEMPERATURE

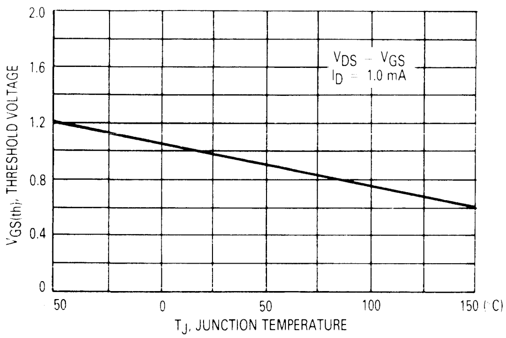


FIGURE 4 — ON-REGION CHARACTERISTICS

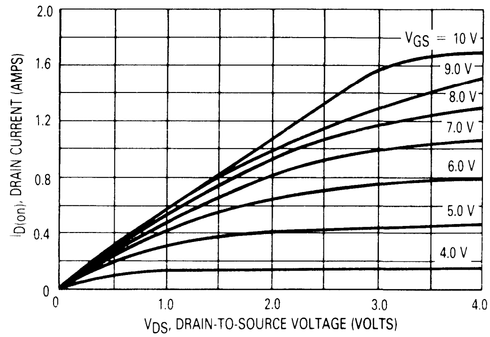


FIGURE 5 — OUTPUT CHARACTERISTICS

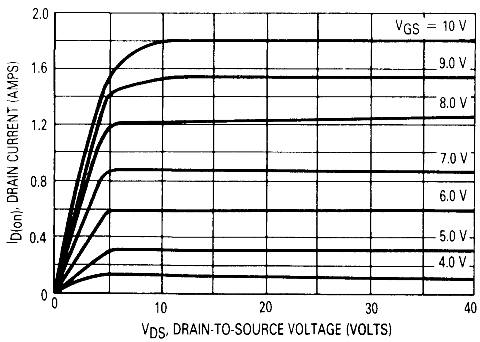


FIGURE 6 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE

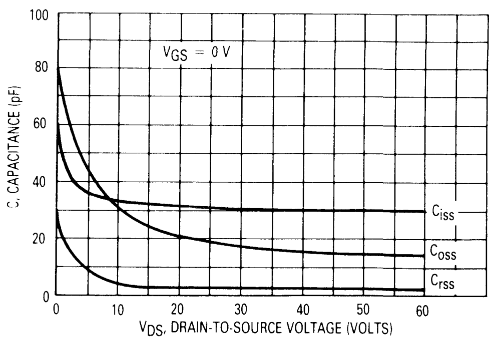
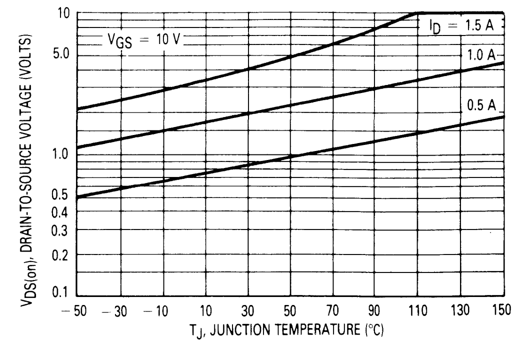
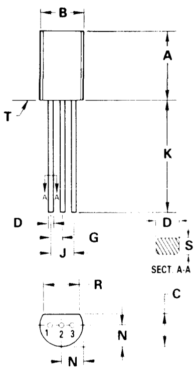


FIGURE 7 — ON-VOLTAGE versus TEMPERATURE



OUTLINE DIMENSIONS

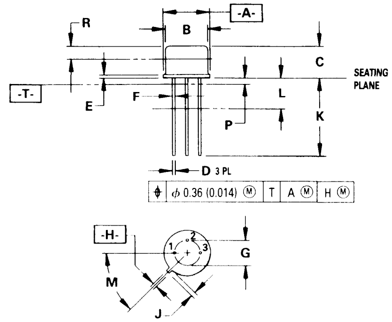


STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | ⌀ 0.10 (0.004) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
5. CONTROLLING DIM: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	—	0.500	—
N	2.03	2.92	0.080	0.115
R	3.43	—	0.135	—
S	0.46	0.61	0.018	0.024

CASE 29-03
TO-226AE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN
(CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

CASE 79-04
TO-205AD

2N6756

Designer's Data Sheet

14 AMPERE

N-CHANNEL TMOS POWER FET

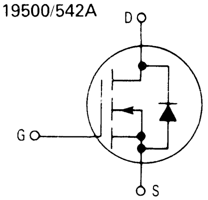
$r_{DS(on)}$ = 0.18 OHM
100 VOLTS

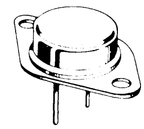
N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

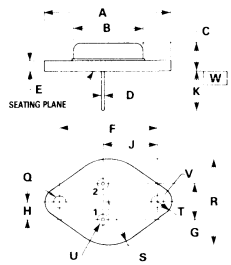
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6756 is Qualified to Mil-S 19500/542A

TMOS™







STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	100*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100*	Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 14* 9.0* 30*	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75* 0.6*	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16″ from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)		$V_{BR(DSS)}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS})		I_{DSS}	—	—	1.0*	mAdc
T_J = 125°C			—	—	4.0*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0*	—	4.0*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance (1) (V_{GS} = 10 Vdc, I_D = 9.0 Adc)		$r_{DS(on)}$	—	—	0.18*	Ohms
T_C = 125°C			—	—	0.33*	
Drain-Source On-Voltage (V_{GS} = 10 V) (1) (I_D = 14 Adc)		$V_{DS(on)}$	—	—	2.52*	Vdc
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 9.0 A)		g_{FS}	4.0*	—	12*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	150*	—	500*	
Reverse Transfer Capacitance		C_{rss}	50*	—	150*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 36 V, I_D = 9.0 Adc Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	75*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40*	
Fall Time		t_f	—	—	45*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0) I_S = 14 A		V_F	0.9*	—	1.8*	Vdc
Continuous Source Current, Body Diode		I_S	—	—	14*	Adc
Pulsed Source Current, Body Diode		I_{SM}	—	—	30	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time		t_{rr}	—	325	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	—	5.0	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	—	12.5	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

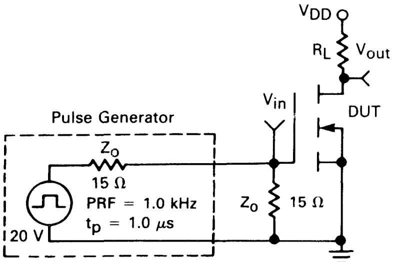
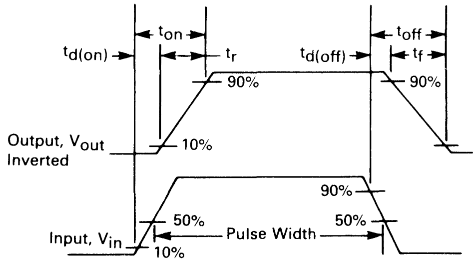


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

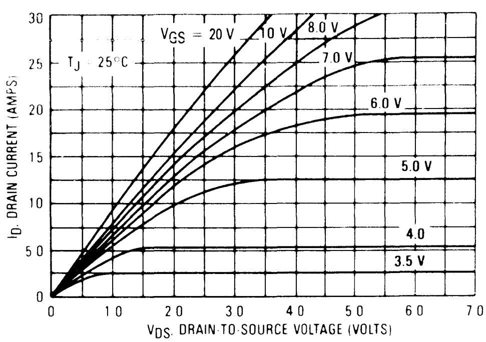


FIGURE 4 — ON-RESISTANCE VARIATION

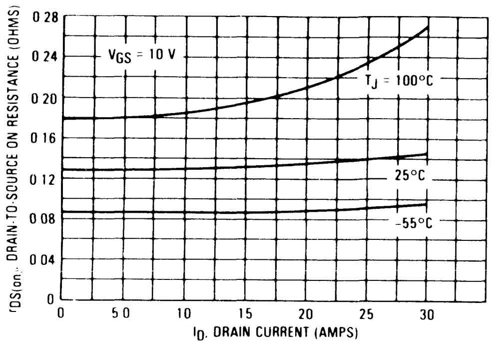


FIGURE 5 — TRANSFER CHARACTERISTICS

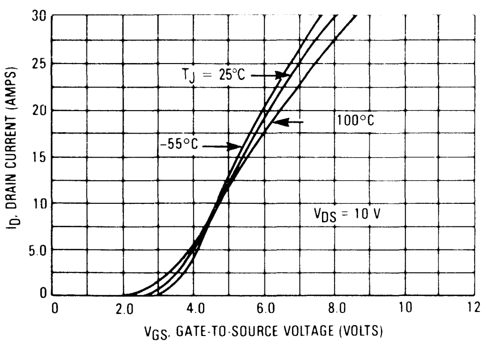


FIGURE 6 — GATE THRESHOLD VOLTAGE VARIATION

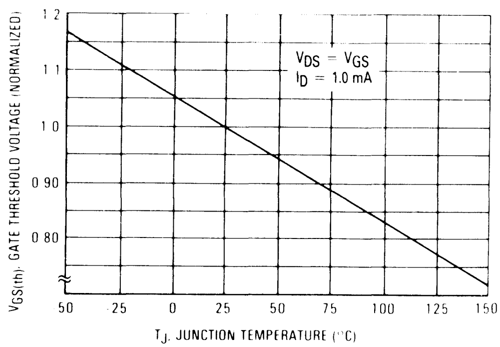
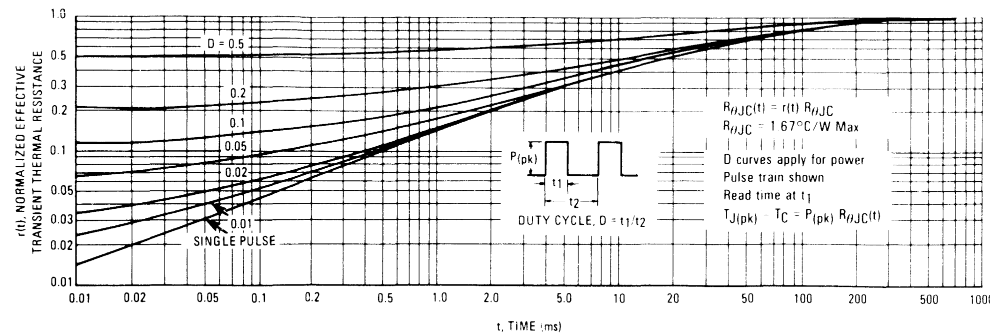


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

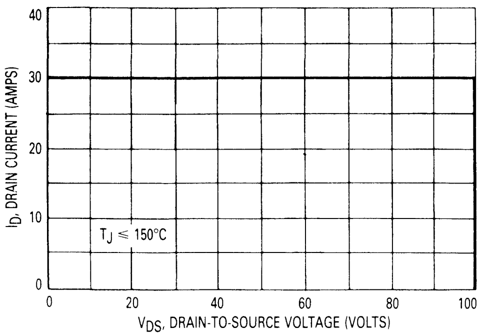


FIGURE 8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

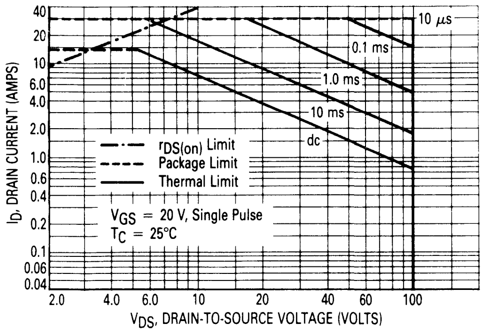


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6756

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 9
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7.

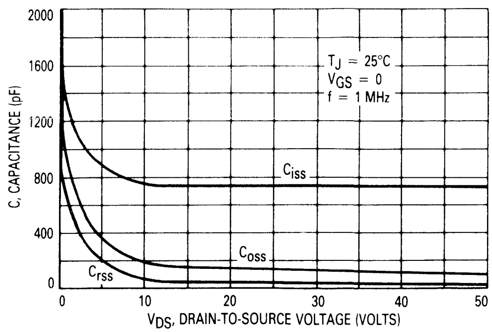
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the device for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 10 — CAPACITANCE VARIATION



2N6758

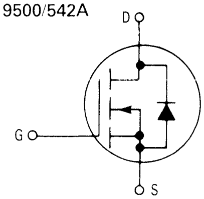
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6758 is Qualified to Mil-S 19500/542A

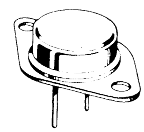
TMOS

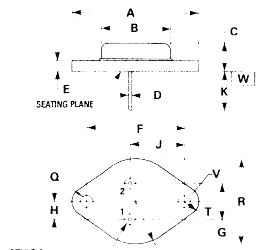


9.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.4 OHM
200 VOLTS





STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	200*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200*	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous T_C = 25°C	I_D	9.0*	Adc
T_C = 100°C		6.0*	
Pulsed	I_{DM}	15*	
Total Power Dissipation @ T_C = 25°C	P_D	75*	Watts
Derate above 25°C		0.6*	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67*	°C/W
Junction to Ambient	$R_{\theta JA}$	30*	
Maximum Lead Temp. for Soldering Purposes, 1/16″ from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)		$V_{BR(DSS)}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS})		I_{DSS}	—	—	1.0*	mAdc
T_J = 125°C			—	—	4.0*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2.0*	—	4.0*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance (1) (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	—	0.4*	Ohms
T_C = 125°C			—	—	0.75*	
Drain-Source On-Voltage (V_{GS} = 10 V) (1) (I_D = 9.0 Adc)		$V_{DS(on)}$	—	—	3.6*	Vdc
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 6.0 A)		g_{FS}	3.0*	—	9.0*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	100*	—	450*	
Reverse Transfer Capacitance		C_{rss}	40*	—	150*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{GS} = 90, I_D = 6.0 A Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	50*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	50*	
Fall Time		t_f	—	—	40*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0) I_S = 9.0 A		V_F	0.8*	—	1.6*	Vdc
Continuous Source Current, Body Diode		I_S	—	—	9.0*	Adc
Pulsed Source Current, Body Diode		I_{SM}	—	—	15	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	65	—	ns
Reverse Recovery Time		t_{rr}	—	325	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	—	5.0	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	—	12.5	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

2N6758, JTX, JTXV

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

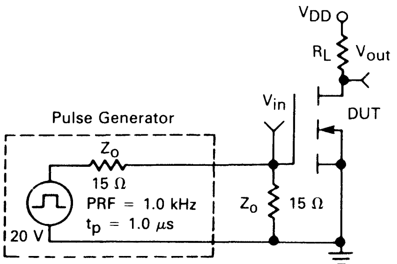
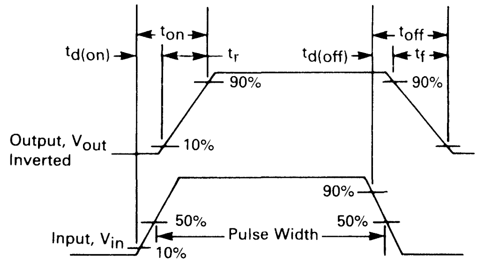


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

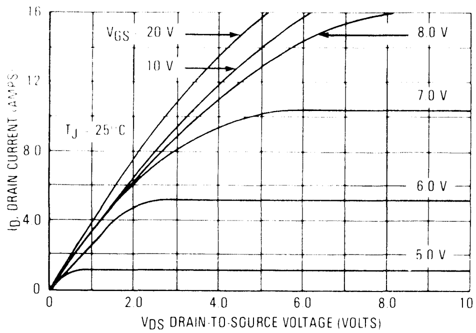


FIGURE 4 — ON-RESISTANCE VARIATION

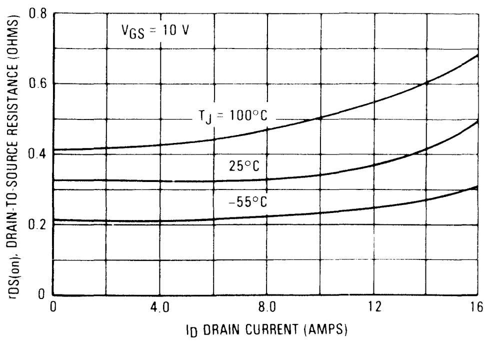


FIGURE 5 — TRANSFER CHARACTERISTICS

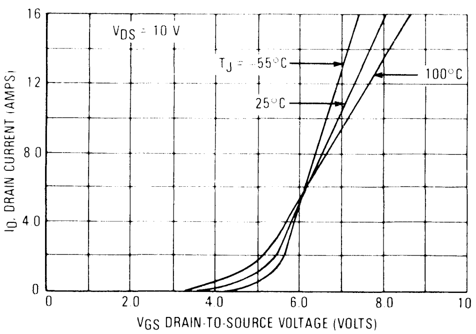


FIGURE 6 — GATE THRESHOLD VOLTAGE VARIATION

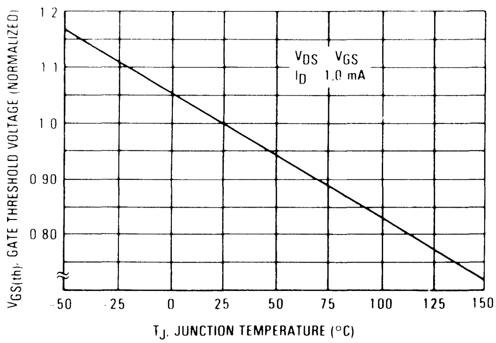
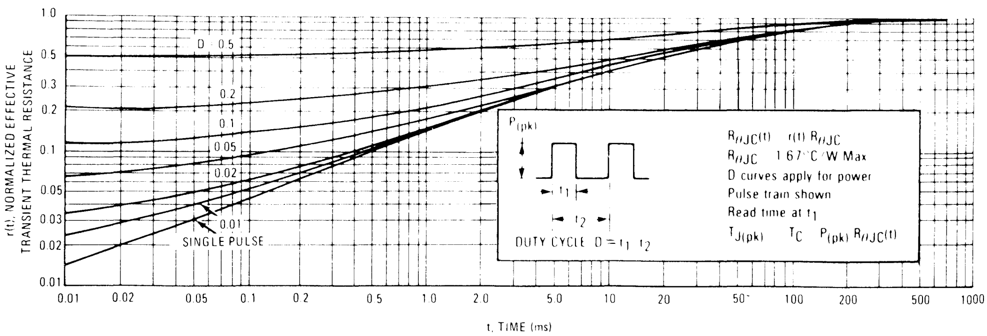


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

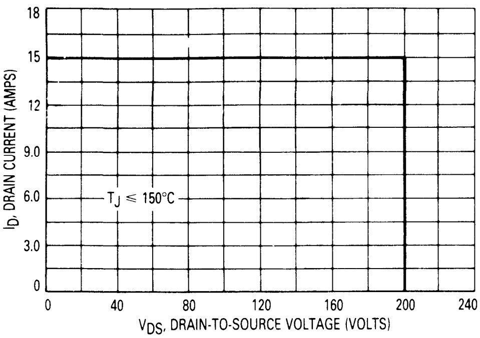
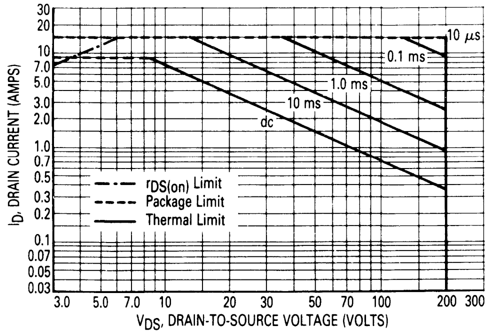


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6758



3

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C) \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_D(25°C)$ = dc drain current at T_C = 25°C from Figure 9
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7.

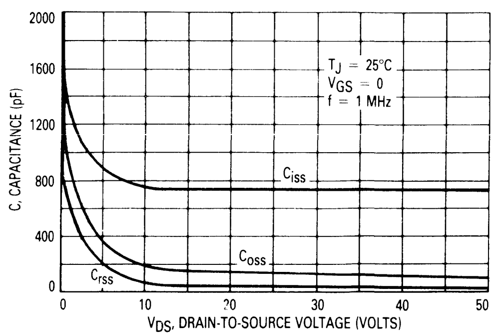
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 10 — CAPACITANCE VARIATION



2N6759
2N6760

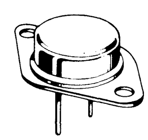
Designer's Data Sheet

4.5 and 5.5 AMPERE

N-CHANNEL TMOS POWER FETs

**$r_{DS(on)}$ = 1.5 OHM
350 VOLTS**

**$r_{DS(on)}$ = 1.0 OHM
400 VOLTS**

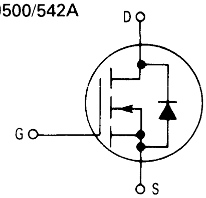


N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6760 is Qualified to Mil-S 19500/542A

TMOS



MAXIMUM RATINGS

Rating	Symbol	2N6759	2N6760†	Unit
Drain-Source Voltage	V_{DSS}	350*	400*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	350*	400*	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	I_D I_{DM}	4.5* 3.0* 7.0	5.5* 3.5* 8.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75* 0.6*		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*		°C

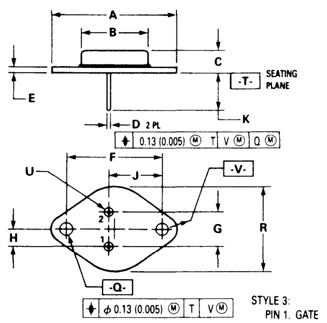
THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16″ from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

**CASE 1-06
TO-204AA**

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)	2N6759 2N6760	$V_{BR(DSS)}$	350 400	— —	— —	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, I_D = 1.0 mA) T_J = 125°C		I_{DSS}	— —	— —	1.0* 4.0*	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C		$V_{GS(th)}$	2.0* 1.5	— —	4.0* 3.5	Vdc
Static Drain-Source On-Resistance (1) (V_{GS} = 10 Vdc, I_D = 3.0 Adc) T_C = 125°C (V_{GS} = 10 Vdc, I_D = 3.5 Adc) T_C = 125°C	2N6759 2N6760	$r_{DS(on)}$	— — — —	— — — —	1.5* 3.3* 1.0* 2.2*	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (1) (I_D = 4.5 Adc) (I_D = 5.5 Adc)	2N6759 2N6760	$V_{DS(on)}$	— —	— —	7.0* 6.7*	Vdc
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 3.5 A)		g_{FS}	3.0*	—	9.0*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance		C_{oss}	50*	—	300*	
Reverse Transfer Capacitance		C_{rss}	20*	—	80*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 175 V, I_D = 3.5 Adc Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time		t_r	—	—	35*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	55*	
Fall Time		t_f	—	—	35*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0) I_S = 4.5 A I_S = 5.5 A	2N6759 2N6760	V_{SD}	0.70* 0.75*	— —	1.40* 1.50*	Vdc
Continuous Source Current, Body Diode	2N6759 2N6760	I_S	— —	— —	4.5* 5.5*	Adc
Pulsed Source Current, Body Diode	2N6759 2N6760	I_{SM}	— —	— —	7.0 8.0	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time		t_{rr}	—	420	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	—	5	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	—	12.5	—	

*JEDEC registered values. (1) Pulse Test = Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

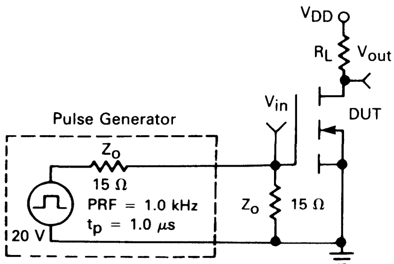
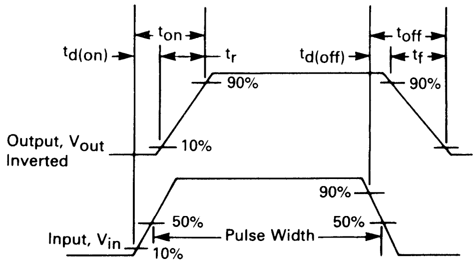


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

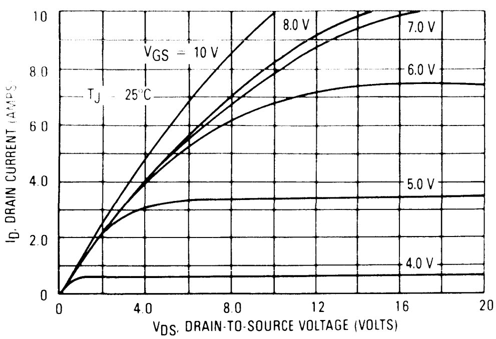


FIGURE 4 — ON-RESISTANCE VARIATION

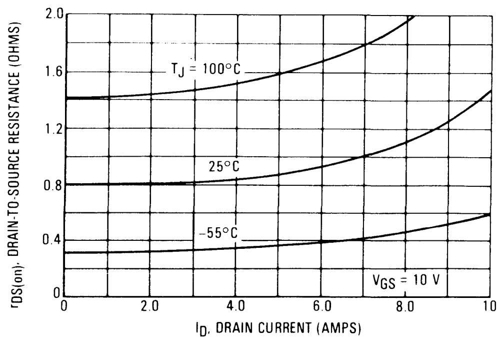


FIGURE 5 — TRANSFER CHARACTERISTICS

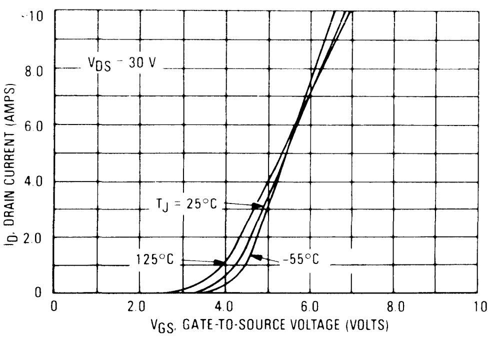


FIGURE 6 — GATE-THRESHOLD VOLTAGE VARIATION

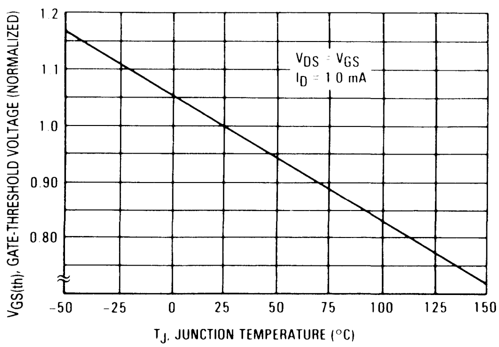
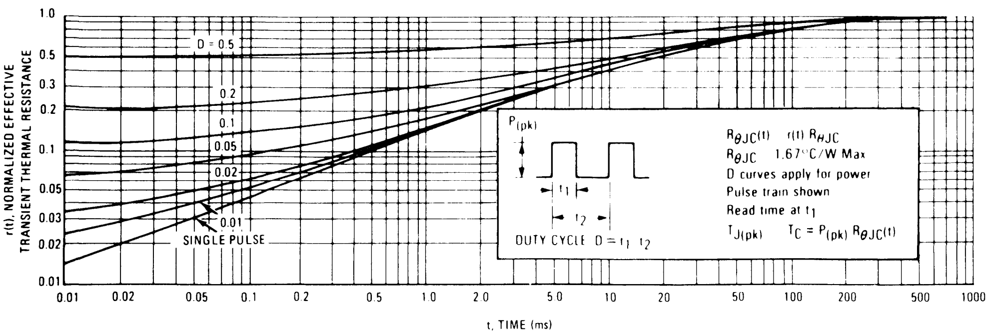


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6759

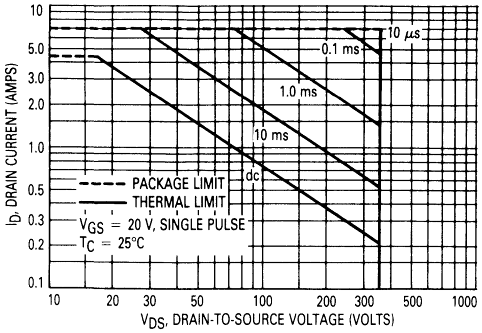


FIGURE 9 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

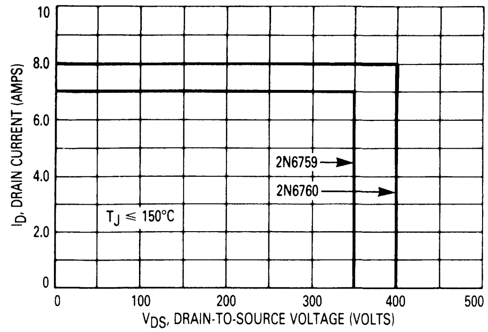


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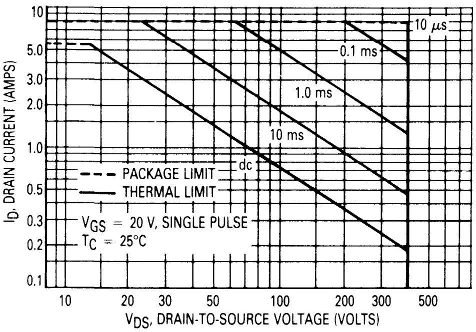
FIGURE 10 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6760



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 8 and 10 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C)\left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

- I_D (25°C) = dc drain current at T_C = 25°C from Figure 8 or 10
- T_{Jmax} = Rated maximum junction temperature
- T_C = Device case temperature
- P_D = Rated power dissipation at T_C = 25°C
- $R_{\theta JC}$ = Rated steady state thermal resistance
- $r(t)$ = Normalized thermal response from Figure 7.

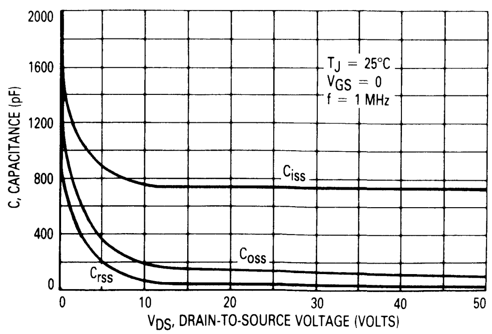
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 11 — CAPACITANCE VARIATION



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

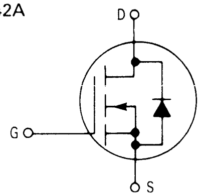
2N6762

Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

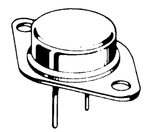
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6762 is Qualified to 19500/542A



4.5 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 1.5 OHMS
500 VOLTS



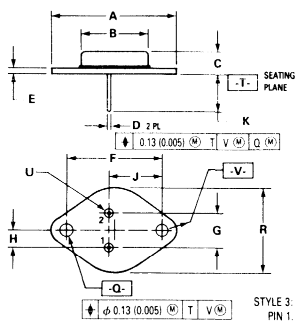
MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	500*	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500*	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous T_C = 25°C		4.5*	Adc
T_C = 100°C	I_D	3.0*	
Pulsed	I_{DM}	7.0*	
Total Power Dissipation @ T_C = 25°C	P_D	75*	Watts
Derate above 25°C		0.6*	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67*	
Junction to Ambient	$R_{\theta JA}$	30*	
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 4.0 mA)	$V_{BR(DSS)}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, I_D = 1.0 mA) T_J = 125°C	I_{DSS}	— —	— —	1.0* 4.0*	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc)	I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc)	I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS}) T_J = 100°C	$V_{GS(th)}$	2.0* 1.5	2.7 2.2	4.0* 3.5	Vdc
Static Drain-Source On-Resistance (1) (V_{GS} = 10 Vdc, I_D = 3.0 Adc) T_C = 125°C	$r_{DS(on)}$	— —	— —	1.5* 3.3*	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (1) (I_D = 4.5 Adc)	$V_{DS(on)}$	—	—	7.7*	Vdc
Forward Transconductance (1) (V_{DS} = 15 V, I_D = 3.0 A)	g_{FS}	2.5*	—	7.5*	mhos
CAPACITANCE					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	350*	—	800*	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	25*	—	200*	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	15*	—	60*	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay Time (V_{DS} = 225 V, I_D = 3.0 Adc, Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	30*	ns
Rise Time (V_{DS} = 225 V, I_D = 3.0 Adc, Z_o = 15 Ω) See Figs. 1 and 2	t_r	—	—	30*	ns
Turn-Off Delay Time (V_{DS} = 225 V, I_D = 3.0 Adc, Z_o = 15 Ω) See Figs. 1 and 2	$t_{d(off)}$	—	—	55*	ns
Fall Time (V_{DS} = 225 V, I_D = 3.0 Adc, Z_o = 15 Ω) See Figs. 1 and 2	t_f	—	—	30*	ns
SOURCE-DRAIN DIODE CHARACTERISTICS					
Diode Forward Voltage (V_{GS} = 0) I_S = 4.5 A	V_{SD}	0.7*	1.15*	1.4*	Vdc
Continuous Source Current, Body Diode	I_S	—	—	4.5*	Adc
Pulsed Source Current, Body Diode	I_{SM}	—	—	7.0	A
Forward Turn-On Time (I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	250	—	ns
Reverse Recovery Time (I_S = Rated I_S, V_{GS} = 0)	t_{rr}	—	420	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	—	5.0	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)	L_s	—	12.5	—	nH

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

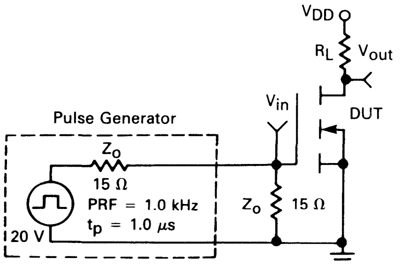
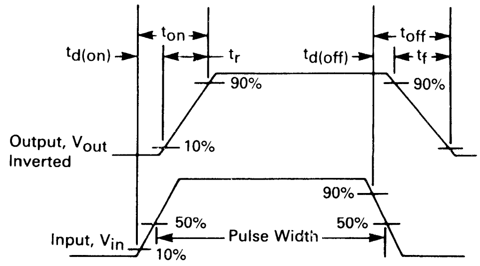


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — ON-REGION CHARACTERISTICS

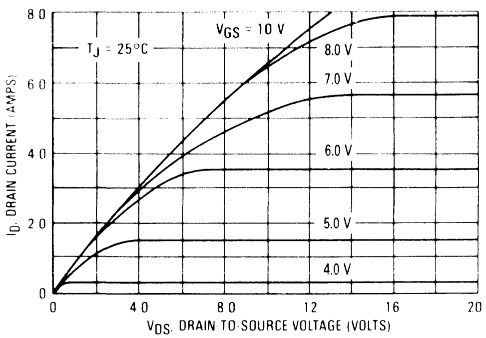


FIGURE 4 — ON-RESISTANCE VARIATION

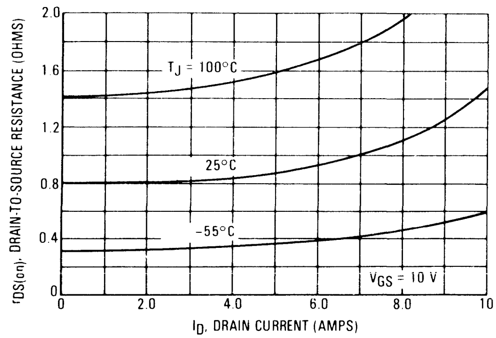


FIGURE 5 — TRANSFER CHARACTERISTICS

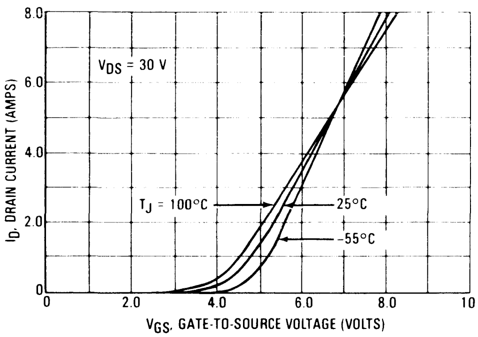


FIGURE 6 — GATE THRESHOLD VOLTAGE VARIATION

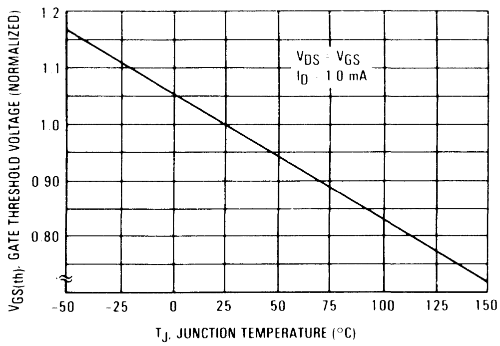
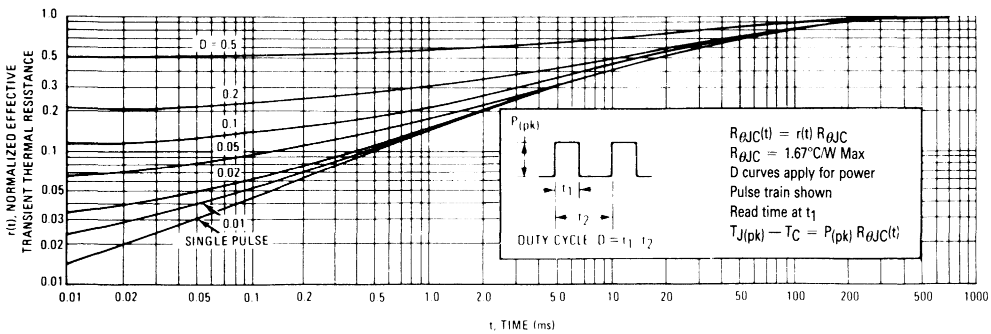


FIGURE 7 — THERMAL RESPONSE



OPERATING AREA INFORMATION

FIGURE 8 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

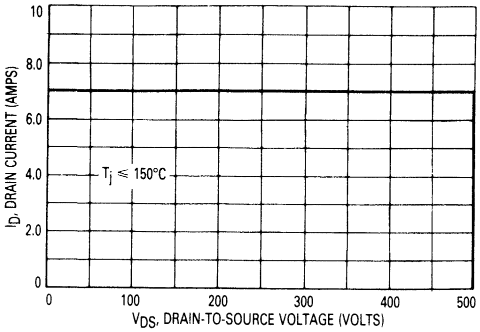
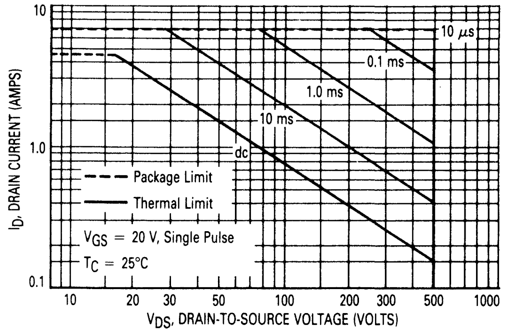


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA, 2N6762



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FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{Jmax} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 9
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7.

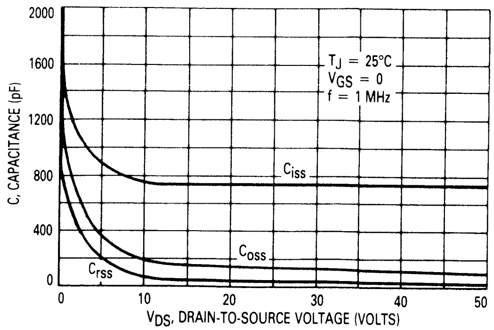
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

FIGURE 10 — CAPACITANCE VARIATION



3

2N6764

Designer's Data Sheet

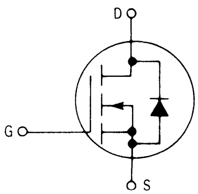
Power Field Effect Transistor

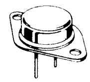
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
38 AMPERES
$r_{DS(on)}$ = 0.055 OHM
100 VOLTS

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6764 is Qualified to Mil-S 19500/543A





CASE 197A-02
TO-204AE

MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	100*	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100*	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 38* 24* 70*	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	 150* 60* 1.2*	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)		$V_{BR(DSS)}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS})		I_{DSS}	—	—	1*	mAdc
T_J = 125°C			—	—	4*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2*	—	4*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 24 Adc)		$r_{DS(on)}$	—	—	0.055*	Ohms
T_C = 125°C			—	—	0.094*	
Drain-Source On-Voltage (V_{GS} = 10 V)(1) (I_D = 38 Adc)		$V_{DS(on)}$	—	—	2.09*	Vdc
Forward Transconductance(1) (V_{DS} = 15 V, I_D = 24 A)		g_{FS}	9*	—	27*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	1000*	—	3000*	pF
Output Capacitance		C_{oss}	500*	—	1500*	
Reverse Transfer Capacitance		C_{rss}	150*	—	500*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} ≈ 24 V, I_D = 24 Adc Z_o = 4.7 Ω) See Figs. 9 and 10	$t_{d(on)}$	—	—	35*	ns
Rise Time		t_r	—	—	100*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	125*	
Fall Time		t_f	—	—	100*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0) I_S = 38 A		V_F	0.95*	—	1.9*	Vdc
Continuous Source Current, Body Diode		I_S	—	—	38*	Adc
Pulsed Source Current, Body Diode		I_{SM}	—	—	70	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	85	—	ns
Reverse Recovery Time		t_{rr}	—	200	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	—	5	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	—	12.5	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

TYPICAL CHARACTERISTICS

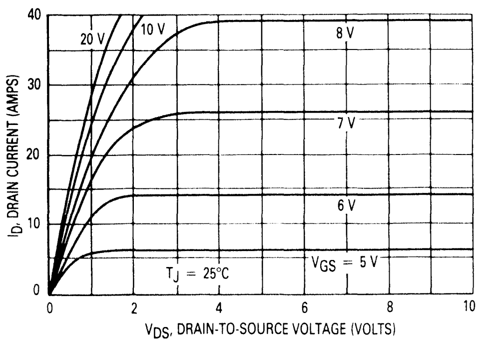


Figure 1. On-Region Characteristics

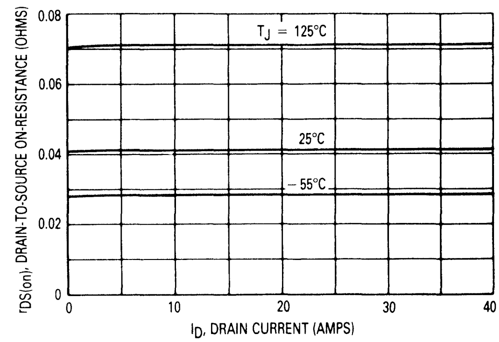


Figure 2. On-Resistance Variation

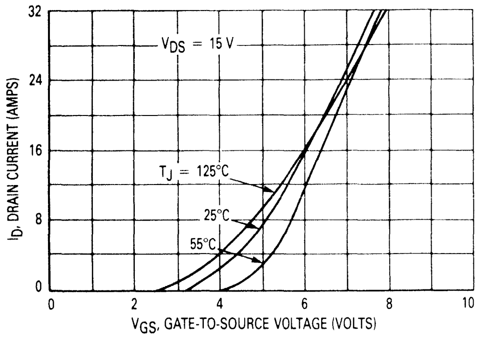


Figure 3. Transfer Characteristics

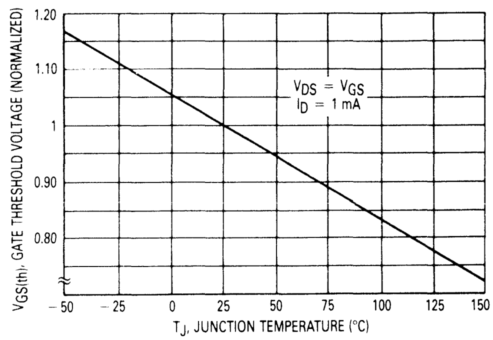


Figure 4. Gate Threshold Voltage Variation

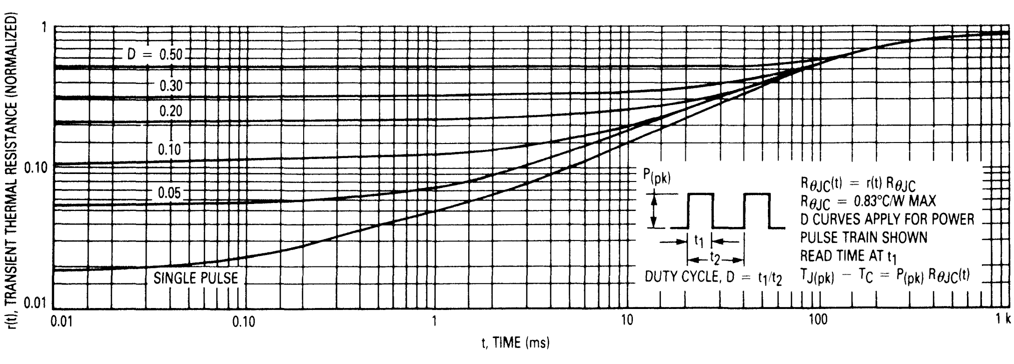


Figure 5. Thermal Response

SAFE OPERATING AREA INFORMATION

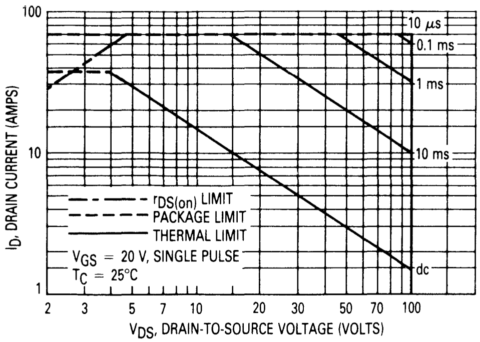


Figure 6. Maximum Rated Forward Biased Safe Operating Area

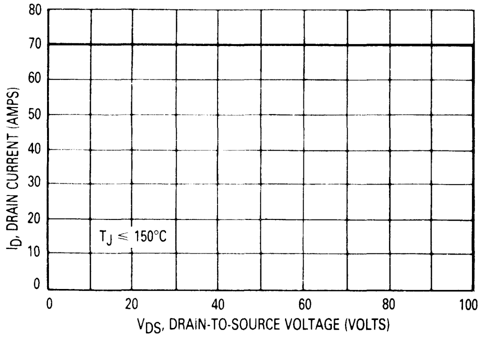


Figure 7. Maximum Rated Switching Safe Operating Area

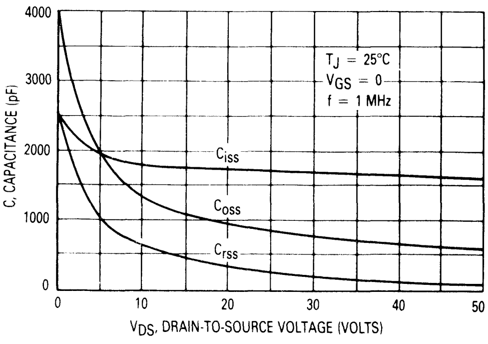


Figure 8. Capacitance Variation

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 6 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 6.

T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

P_D = Rated power dissipation at T_C = 25°C

$R_{\theta JC}$ = Rated steady state thermal resistance

r(t) = Normalized thermal response from Figure 5

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 7, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

3

RESISTIVE SWITCHING

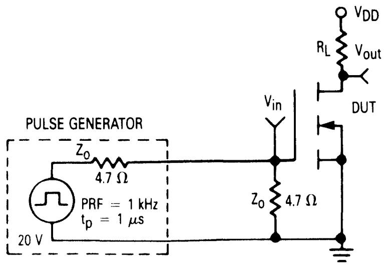


Figure 9. Switching Test Circuit

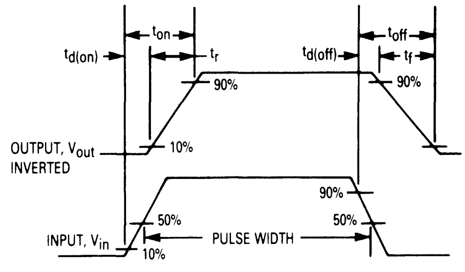
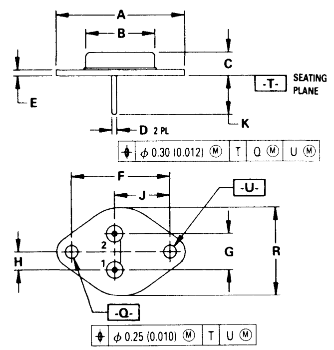


Figure 10. Switching Waveforms



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. SOURCE
2. GATE
CASE. DRAIN

CASE 197A-02
TO-204AE

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6766

Designer's Data Sheet

Power Field Effect Transistor

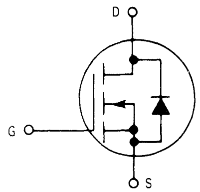
N-Channel Enhancement-Mode Silicon Gate TMOS

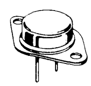
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6766 is Qualified to Mil-S 19500/543A

TMOS™

TMOS POWER FET
30 AMPERES
$r_{DS(on)}$ = 0.085 OHM
200 VOLTS





CASE 197A-02
TO-204AE

MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	200*	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200*	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 30* 19* 60*	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	150* 60* 1.2*	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{BR(DSS)}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS})	I_{DSS}	—	—	1*	mAdc
T_J = 125°C		—	—	4*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)	I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)	I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 1 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	2*	—	4*	Vdc
T_J = 100°C		1.5	—	3.5	
Static Drain-Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 19 Adc)	$r_{DS(on)}$	—	—	0.085*	Ohms
T_C = 125°C		—	—	0.153*	
Drain-Source On-Voltage (V_{GS} = 10 V)(1) (I_D = 30 Adc)	$V_{DS(on)}$	—	—	2.7*	Vdc
Forward Transconductance(1) (V_{DS} = 15 V, I_D = 19 A)	g_{FS}	9*	—	27*	mhos
CAPACITANCE					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	1000*	—	3000*	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	450*	—	1200*	
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	150*	—	500*	
SWITCHING CHARACTERISTICS					
Turn-On Delay Time (V_{DS} ≈ 95 V, I_D = 19 Adc, Z_o = 4.7 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	35*	ns
Rise Time	t_r	—	—	100*	
Turn-Off Delay Time	$t_{d(off)}$	—	—	125*	
Fall Time	t_f	—	—	100*	
SOURCE-DRAIN DIODE CHARACTERISTICS					
Diode Forward Voltage (V_{GS} = 0) I_S = 30 A	V_F	0.9*	—	1.8*	Vdc
Continuous Source Current, Body Diode	I_S	—	—	30*	Adc
Pulsed Source Current, Body Diode	I_{SM}	—	—	60	A
Forward Turn-On Time (I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	80	—	ns
Reverse Recovery Time (I_S = Rated I_S, V_{GS} = 0)	t_{rr}	—	200	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	—	5	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)	L_s	—	12.5	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

RESISTIVE SWITCHING

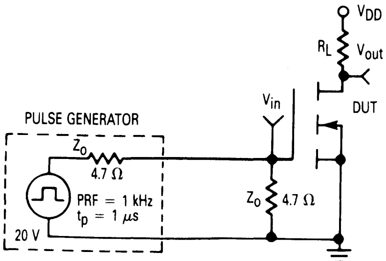


Figure 1. Switching Test Circuit

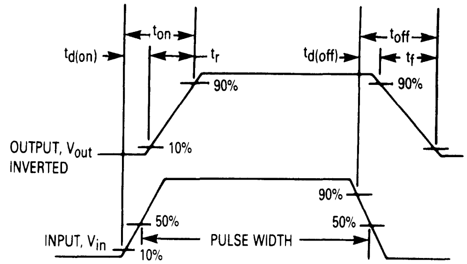


Figure 2. Switching Waveforms

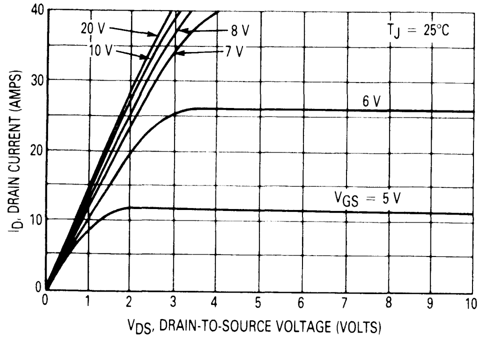


Figure 3. On-Region Characteristics

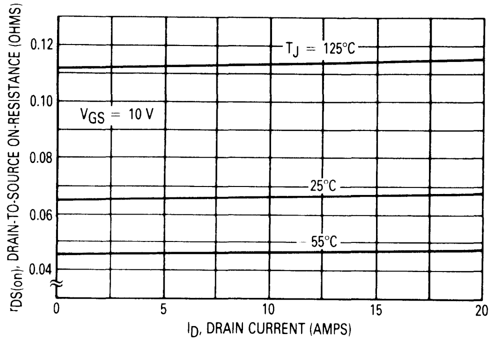


Figure 4. On-Resistance Variation

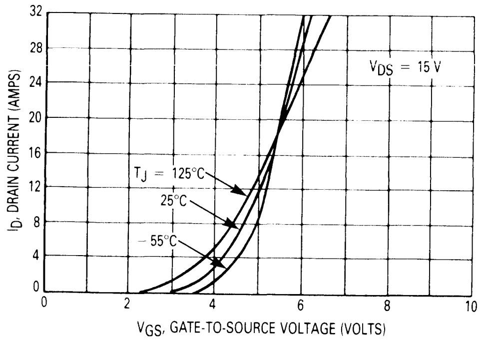


Figure 5. Transfer Characteristics

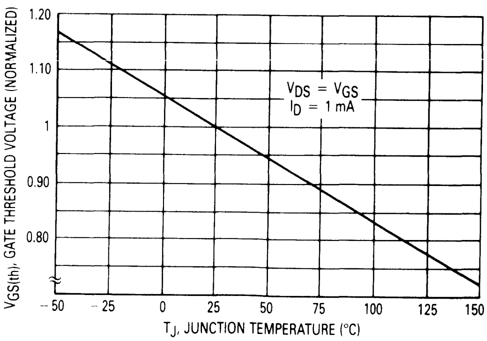


Figure 6. Gate-Threshold Voltage Variation

TYPICAL CHARACTERISTICS

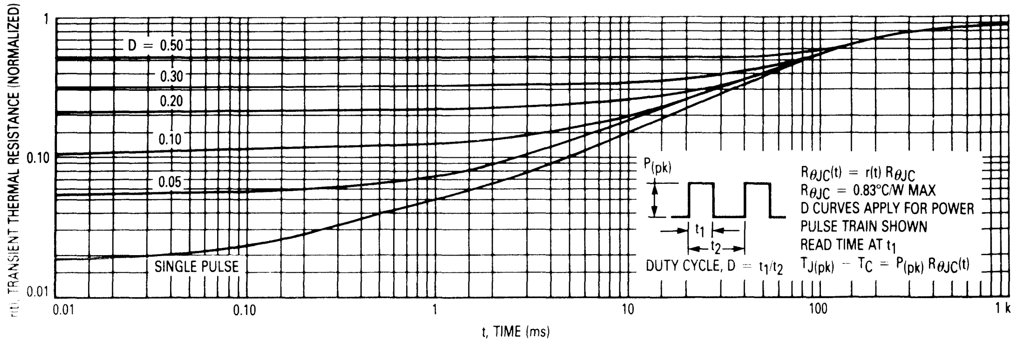


Figure 7. Thermal Response

OPERATING AREA INFORMATION

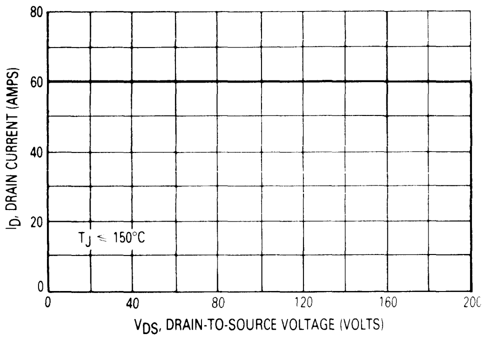


Figure 8. Maximum Rated Switching Safe Operating Area

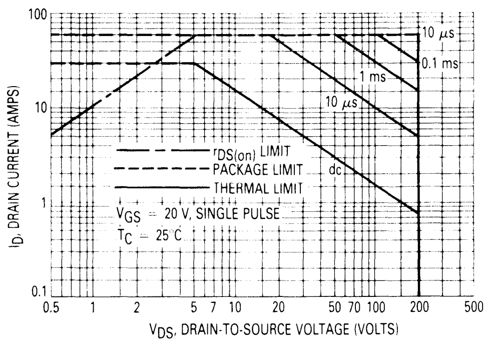


Figure 9. Maximum Rated Forward Biased Safe Operating Area

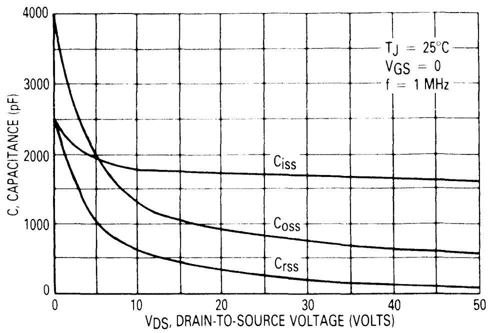


Figure 10. Capacitance Variation

TYPICAL CHARACTERISTICS (continued)

OPERATING AREA INFORMATION (continued)

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{J(max)} - T_C}{P_D \bullet R_{\theta JC} \bullet r(t)} \right]$$

Where

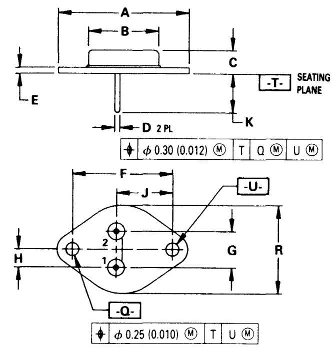
$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 9.
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
r(t) = Normalized thermal response from Figure 7

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. SOURCE
2. GATE
CASE. DRAIN

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 197A-02
TO-204AE

3

Designer's Data Sheet

Power Field Effect Transistor

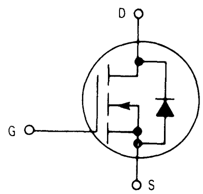
N-Channel Enhancement-Mode
Silicon Gate TMOS

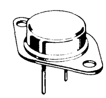
2N6768

TMOS POWER FET
14 AMPERES
$r_{DS(on)}$ = 0.3 OHM
400 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6768 is Qualified to Mil-S 19500/543A





CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	400*	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	400*	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 14* 9* 25*	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	150* 60* 1.2*	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)		$V_{BR(DSS)}$	400	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	—	1*	mAdc
T_J = 125°C			—	—	4*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)		I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 1 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	2*	—	4*	Vdc
T_J = 100°C			1.5	—	3.5	
Static Drain-Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 9 Adc)		$r_{DS(on)}$	—	—	0.3*	Ohms
T_C = 125°C			—	—	0.66*	
Drain-Source On-Voltage (V_{GS} = 10 V)(1) (I_D = 14 Adc)		$V_{DS(on)}$	—	—	5.6*	Vdc
Forward Transconductance(1) (V_{DS} = 15 V, I_D = 9 A)		g_{FS}	8*	—	24*	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	1000*	—	3000*	pF
Output Capacitance		C_{oss}	200*	—	600*	
Reverse Transfer Capacitance		C_{rss}	50*	—	200*	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} ≈ 180 V, I_D = 9 Adc Z_o = 4.7 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	35*	ns
Rise Time		t_r	—	—	65*	
Turn-Off Delay Time		$t_{d(off)}$	—	—	150*	
Fall Time		t_f	—	—	75*	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0) (I_S = 14) A		V_{SD}	0.85*	—	1.7*	Vdc
Continuous Source Current, Body Diode		I_S	—	—	14*	Adc
Pulsed Source Current, Body Diode		I_{SM}	—	—	25	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	175	—	ns
Reverse Recovery Time		t_{rr}	—	600	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	—	5	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	—	12.5	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

3

RESISTIVE SWITCHING

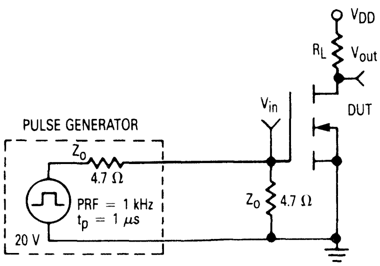


Figure 1. Switching Test Circuit

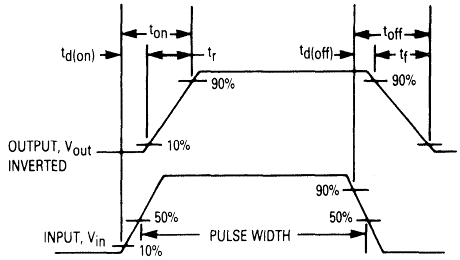


Figure 2. Switching Waveforms

TYPICAL CHARACTERISTICS

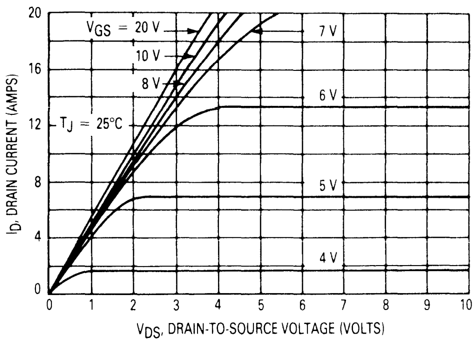


Figure 3. On-Region Characteristics

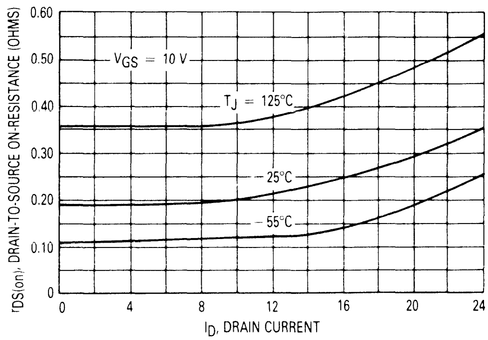


Figure 4. On-Resistance Variation

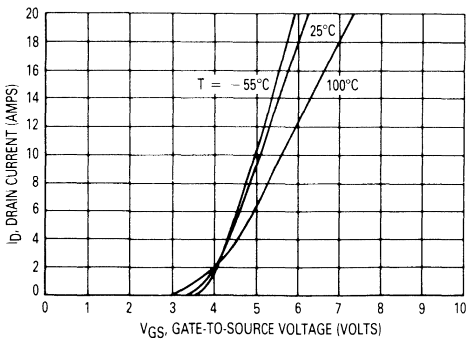


Figure 5. Transfer Characteristics

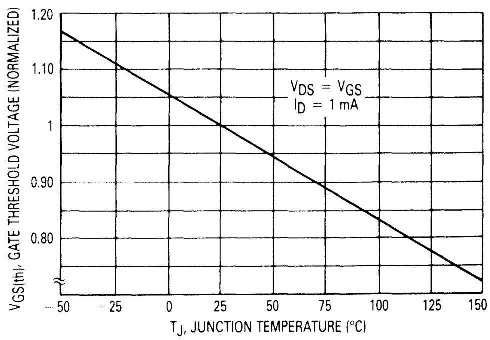


Figure 6. Gate-Threshold Voltage Variation

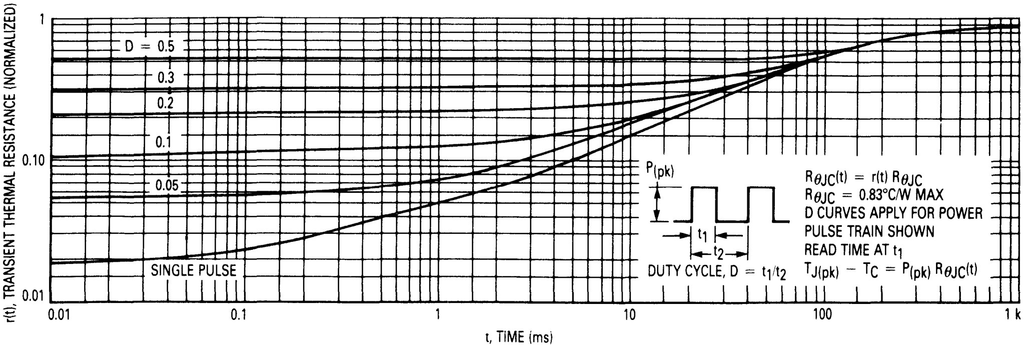


Figure 7. Thermal Response

OPERATING AREA INFORMATION

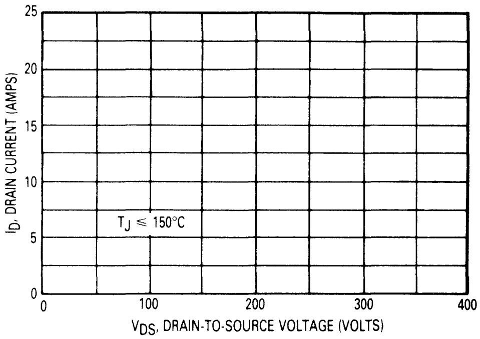


Figure 8. Maximum Rated Switching Safe Operating Area

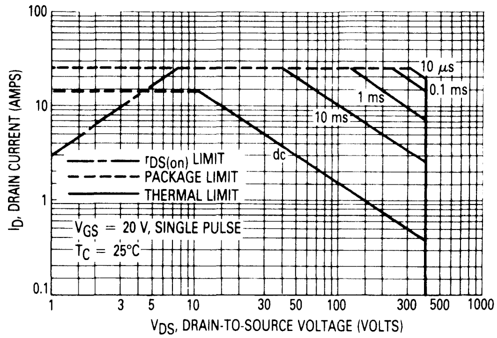


Figure 9. Maximum Rated Forward Biased Safe Operating Area

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{Jmax} - T_C}{R_{\theta JC}}$$

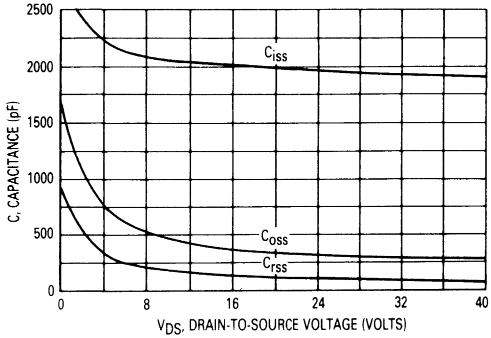


Figure 10. Capacitance Variation

FORWARD BIASED SAFE OPERATING AREA

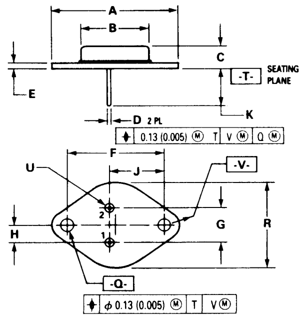
The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 9.
T_{Jmax} = Rated maximum junction temperature
T_C = Device case temperature
P_D = Rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = Rated steady state thermal resistance
$r(t)$ = Normalized thermal response from Figure 7

CASE 1-06
TO-204AA



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

2N6770

Designer's Data Sheet

Power Field Effect Transistor

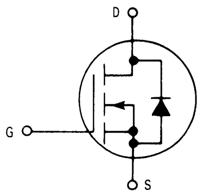
N-Channel Enhancement-Mode Silicon Gate TMOS

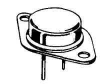
TMOS

TMOS POWER FET
12 AMPERES
$r_{DS(on)}$ = 0.4 OHM
500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- 2N6770 is Qualified to Mil-S 19500/543A





CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Value†	Unit
Drain-Source Voltage	V_{DSS}	500*	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	500*	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 12* 7.75* 25*	Adc
Total Power Dissipation @ T_C = 25°C T_C = 100°C Derate above 25°C	P_D	 150* 60* 1.2*	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55* to 150*	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83* 30*	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/16" from case for 5 seconds	T_L	300*	°C

*JEDEC registered values.
†JTX, JTXV available.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 4 mA)	$V_{BR(DSS)}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	—	1*	mAdc
T_J = 125°C		—	—	4*	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)	I_{GSSF}	—	—	100*	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)	I_{GSSR}	—	—	100*	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 1 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	2*	2.7	4*	Vdc
T_J = 100°C		1.5	2.2	3.5	
Static Drain-Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 7.75 Adc)	$r_{DS(on)}$	—	—	0.4*	Ohms
T_C = 125°C		—	—	0.88*	
Drain-Source On-Voltage (V_{GS} = 10 V)(1) (I_D = 12 Adc)	$V_{DS(on)}$	—	—	6*	Vdc
Forward Transconductance(1) (V_{DS} = 15 V, I_D = 7.75 A)	g_{FS}	8*	—	24*	mhos
CAPACITANCE					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	1000*	—	3000*	pF
Output Capacitance	C_{oss}	200*	—	600*	
Reverse Transfer Capacitance	C_{rss}	50*	—	200*	
SWITCHING CHARACTERISTICS					
Turn-On Delay Time (V_{DS} ≈ 210 V, I_D = 7.75 Adc, Z_o = 4.7 Ω) See Figs. 1 and 2	$t_{d(on)}$	—	—	35*	ns
Rise Time	t_r	—	—	50*	
Turn-Off Delay Time	$t_{d(off)}$	—	—	150*	
Fall Time	t_f	—	—	70*	
SOURCE-DRAIN DIODE CHARACTERISTICS					
Diode Forward Voltage (V_{GS} = 0) (I_S = 12) A	V_{SD}	0.8*	—	1.6*	Vdc
Continuous Source Current, Body Diode	I_S	—	—	12*	Adc
Pulsed Source Current, Body Diode	I_{SM}	—	—	25	A
Forward Turn-On Time (I_S = Rated I_S, V_{GS} = 0)	t_{on}	—	200	—	ns
Reverse Recovery Time	t_{rr}	—	700	—	
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	—	5	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)	L_s	—	12.5	—	

*JEDEC registered values.
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

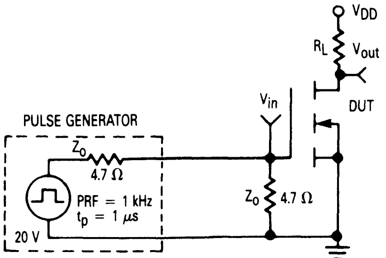


Figure 1. Switching Test Circuit

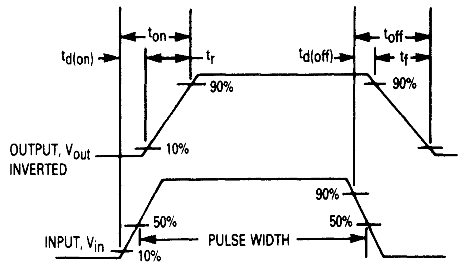


Figure 2. Switching Waveforms

TYPICAL CHARACTERISTICS

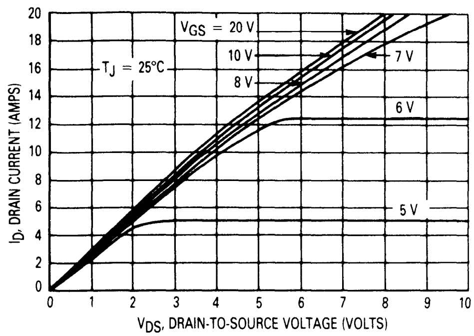


Figure 3. On-Region Characteristics

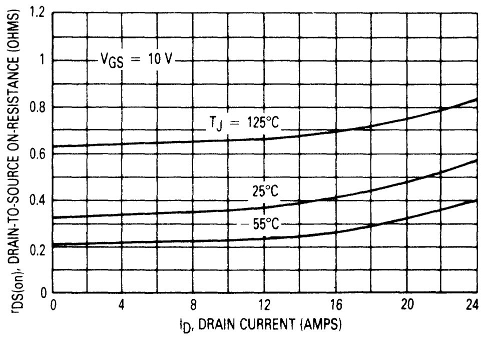


Figure 4. On-Resistance Variation

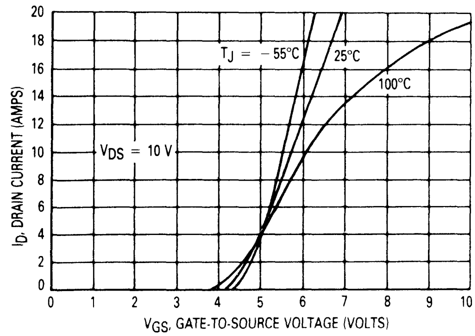


Figure 5. Transfer Characteristics

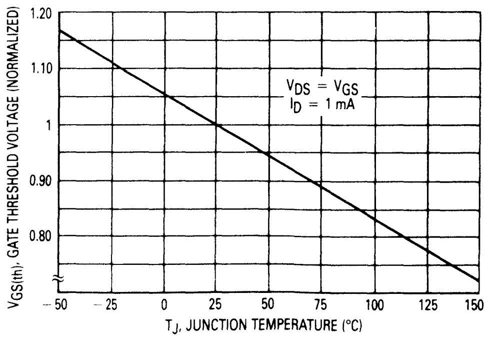


Figure 6. Gate Threshold Voltage Variation

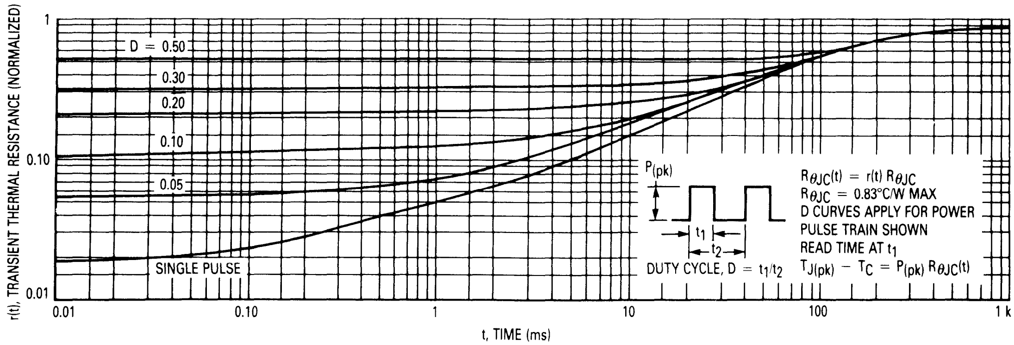


Figure 7. Thermal Response

OPERATING AREA INFORMATION

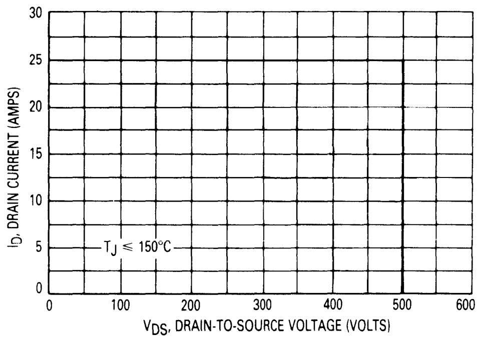


Figure 8. Maximum Rated Switching Safe Operating Area

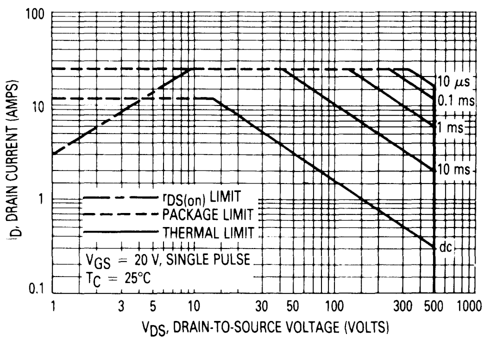


Figure 9. Maximum Rated Forward Biased Safe Operating Area

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

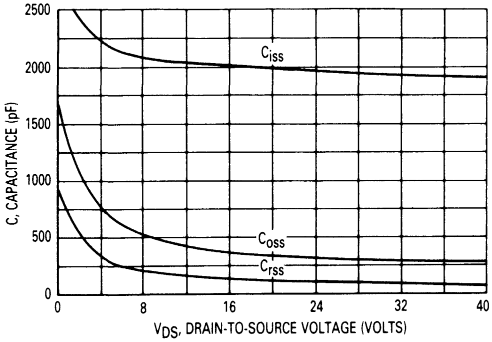


Figure 10. Capacitance Variation

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°C. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)} \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)} \right]$$

Where

$I_{D(25°C)}$ = dc drain current at T_C = 25°C from Figure 9.

T_{Jmax} = Rated maximum junction temperature

T_C = Device case temperature

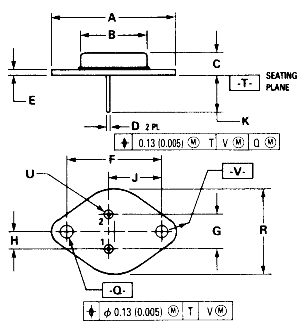
P_D = Rated power dissipation at T_C = 25°C

$R_{\theta JC}$ = Rated steady state thermal resistance

r(t) = Normalized thermal response from Figure 7

3

CASE 1-06
TO-204AA



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

Advance Information

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

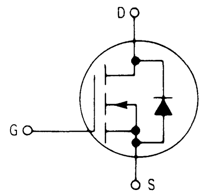
2N6782

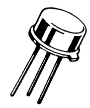
TMOS

N-CHANNEL
TMOS POWER FETs
$r_{DS(on)}$ = 0.6 OHM
100 VOLTS

... designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoids, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability





CASE 79-05

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 mΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.5 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	8.33 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 100 V, V_{GS} = 0 V) (V_{DS} = 80 V, V_{GS} = 0 V, T_J = 125°C)	I_{DSS}	 — —	 250 1000	μAdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

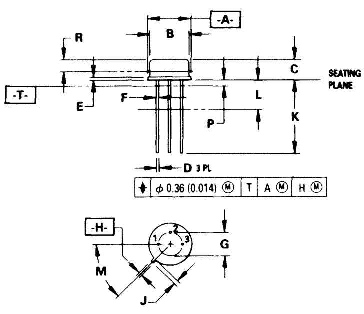
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Body Leakage Current, Forward (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GS} = −20 Vdc, V_{DS} = 0)		I_{GSSR}	—	−100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.5 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.25 Adc) T_A = 25°C		$r_{DS(on)}$	—	0.6	Ohm
T_A = 125°C			—	1.08	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3.5 Adc)		$V_{DS(on)}$	—	2.1	Vdc
Forward Transconductance (V_{DS} = 5 V, I_D = 2.25 Adc)		g_{FS}	1	3	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	60	200	pF
Output Capacitance		C_{oss}	40	100	
Reverse Transfer Capacitance		C_{rss}	10	25	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 34 V, I_D = 2.25 Rated I_D R_{gen} = 50 ohms)	$t_{d(on)}$	—	15	ns
Rise Time		t_r	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	25	
Fall Time		t_f	—	20	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Diode Forward Voltage	(I_S = Rated $I_{D(on)}$ V_{GS} = 0)	V_{SD}	0.75	1.5	Vdc
Forward Turn-On Time		t_{on}	—	Negligible	ns
Reverse Recovery Time		t_{rr}	—	200	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS

CASE 79-05



STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN
(CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6784

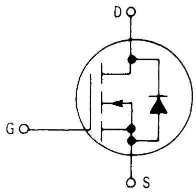
Advance Information

Power Field Effect Transistor

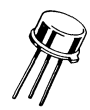
N-Channel Enhancement-Mode Silicon Gate TMOS

... designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoids, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability



N-CHANNEL
TMOS POWER FET
$r_{DS(on)}$ = 1.5 OHMS
200 VOLTS



CASE 79-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 mΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 2.25 9	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	8.33 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 250 1000	μAdc

(continued)

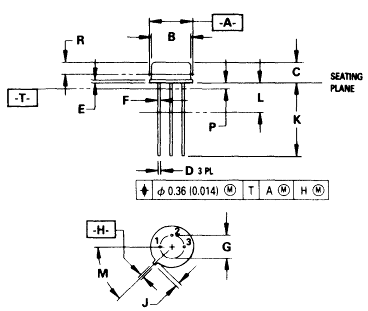
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Body Leakage Current, Forward (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GS} = −20 Vdc, V_{DS} = 0)		I_{GSSR}	—	−100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.5 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	T_A = 25°C	$r_{DS(on)}$	—	1.5	Ohms
	T_A = 125°C		—	2.81	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2.25 Adc)		$V_{DS(on)}$	—	3.37	Vdc
Forward Transconductance (V_{DS} = 5 V, I_D = 1.5 Adc)		g_{FS}	0.9	2.7	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	60	200	pF
Output Capacitance		C_{oss}	20	80	
Reverse Transfer Capacitance		C_{rss}	5	25	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 75 V, I_D = 1.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	15	ns
Rise Time		t_r	—	20	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	20	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Diode Forward Voltage	(I_S = Rated $I_{D(on)}$ V_{GS} = 0)	V_{SD}	0.7	1.5	Vdc
Forward Turn-On Time		t_{on}	—	Negligible	ns
Reverse Recovery Time		t_{rr}	290 (Typ)	—	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 79-05

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
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DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

3

Advance Information

Power Field Effect Transistor

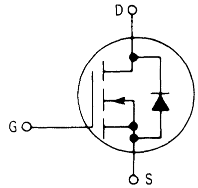
N-Channel Enhancement-Mode Silicon Gate TMOS

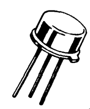
2N6788

N-CHANNEL
TMOS POWER FET
$r_{DS(on)}$ = 0.3 OHM
100 VOLTS

... designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoids, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability





CASE 79-05

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 mΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 6 24	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	6.25 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 80 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 250 1000	μAdc

(continued)

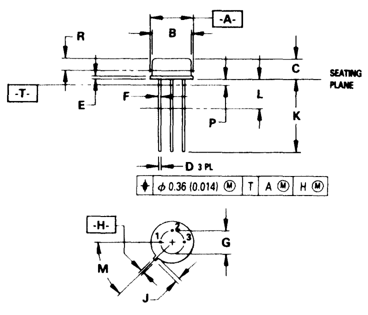
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Body Leakage Current, Forward (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GS} = −20 Vdc, V_{DS} = 0)	I_{GSSR}	—	−100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc) T_A = 25°C	$r_{DS(on)}$	—	0.3	Ohm
T_A = 125°C		—	0.54	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc)	$V_{DS(on)}$	—	1.8	Vdc
Forward Transconductance (V_{DS} = 5 V, I_D = 3.5 Adc)	g_{FS}	1.5	4.5	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	200	600	pF
Output Capacitance	C_{oss}	100	400	
Reverse Transfer Capacitance	C_{rss}	20	100	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} = 35 V, I_D = 3.5 A R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time	t_r	—	70	
Turn-Off Delay Time	$t_{d(off)}$	—	40	
Fall Time	t_f	—	70	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Diode Forward Voltage (I_S = Rated $I_{D(on)}$ V_{GS} = 0)	V_{SD}	0.8	1.8	Vdc
Forward Turn-On Time	t_{on}	—	Negligible	ns
Reverse Recovery Time	t_{rr}	—	230	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 79-05
TO-205AF TYPE

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

3

2N6823

Designer's Data Sheet

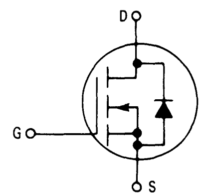
Power Field Effect Transistor

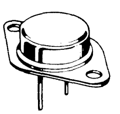
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
3 AMPERES
$r_{DS(on)}$ = 2.8 OHMS
600 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	2N6823	Unit
Drain-Source Voltage	V_{DSS}	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	600	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous @ T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 3 2.5 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating Junction Temperature Range	T_J	−65 to 150	°C
Storage Temperature Range	T_{stg}	−65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.25 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	600	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	2.8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc) (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 8.4 15	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)		g_{FS}	1.5	7.5	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	400	1000	pF
Output Capacitance		C_{oss}	40	200	
Reverse Transfer Capacitance		C_{rss}	10	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 2 A R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	180	
Fall Time		t_f	—	80	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	16 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 3 A, V_{GS} = 0)	V_{SD}	0.7	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	—	500	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

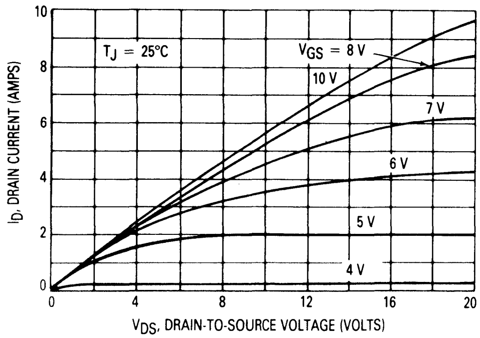


Figure 1. On-Region Characteristics

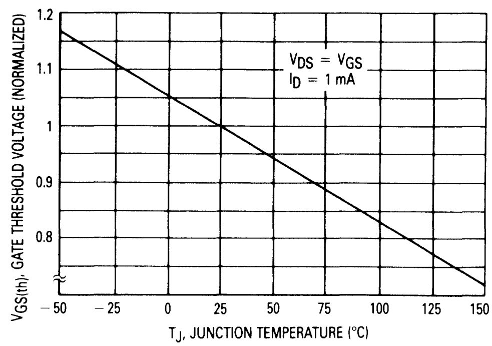


Figure 2. Gate-Threshold Voltage Variation With Temperature

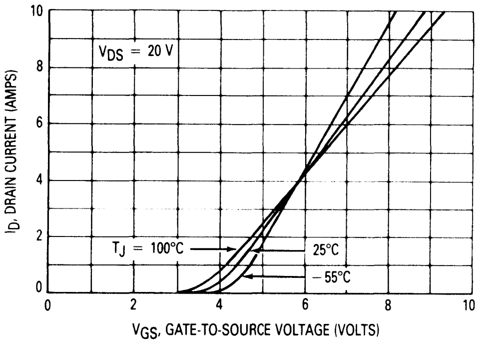


Figure 3. Transfer Characteristics

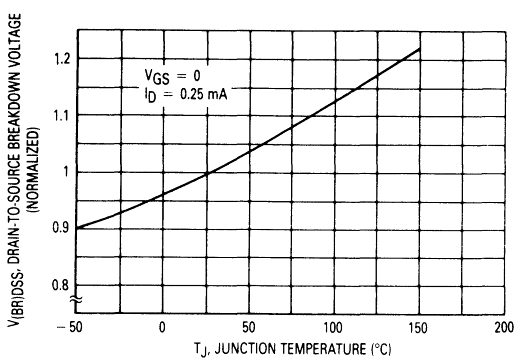


Figure 4. Breakdown Voltage Variation With Temperature

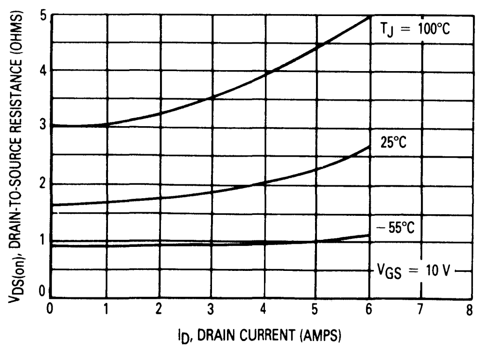


Figure 5. On-Resistance versus Drain Current

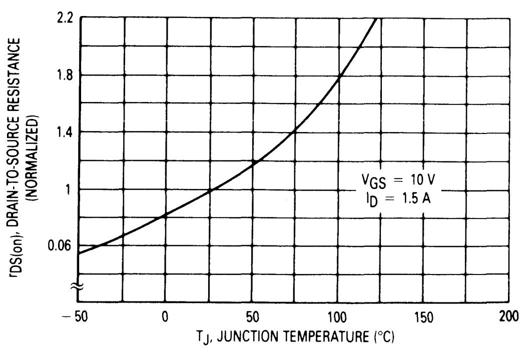


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

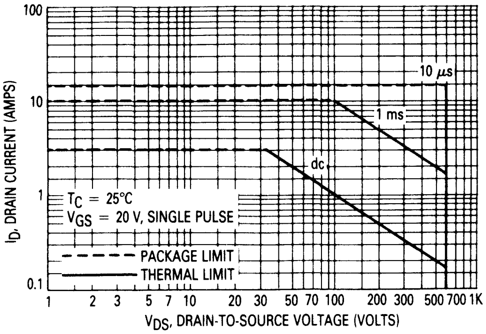


Figure 7. Maximum Rated Forward Biased Safe Operating Area

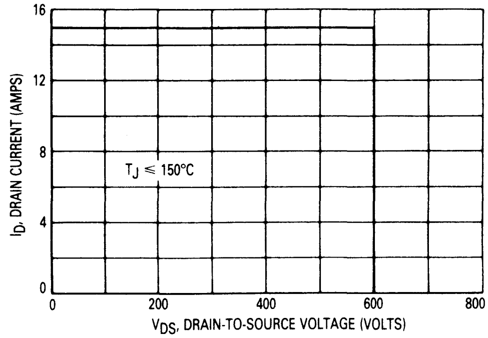


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

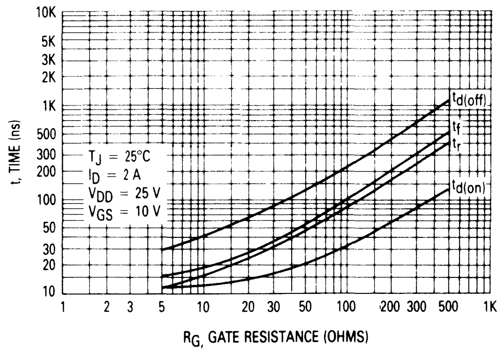


Figure 9. Resistive Switching Time Variation versus Gate Resistance

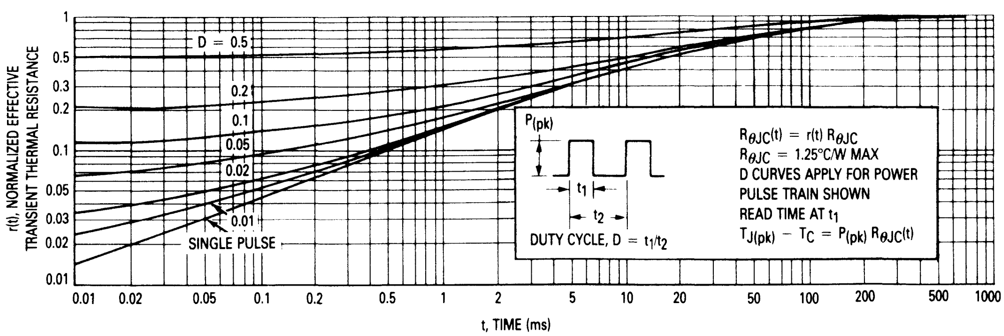


Figure 10. Thermal Response

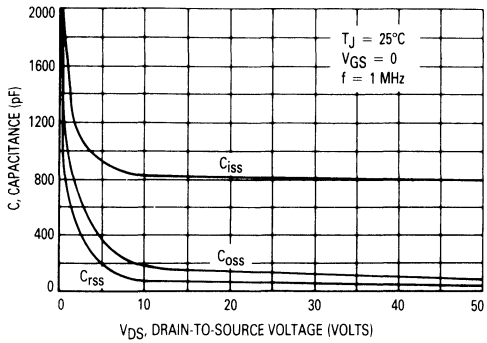


Figure 11. Capacitance Variation

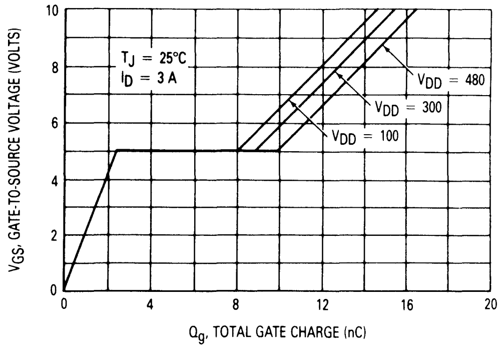


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

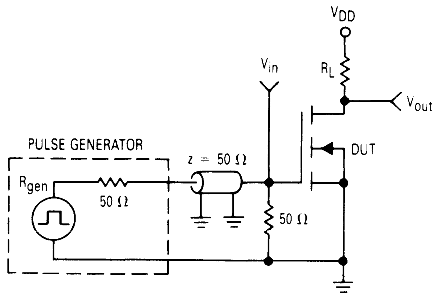


Figure 13. Switching Test Circuit

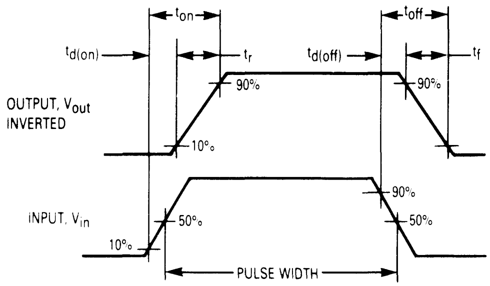
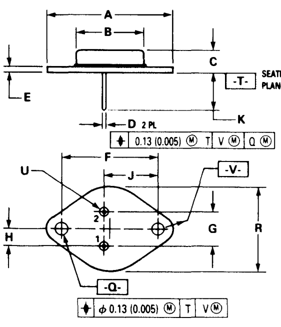


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

2N6826

Designer's Data Sheet

Power Field Effect Transistor

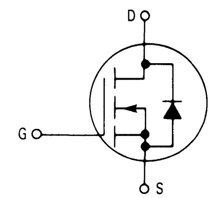
N-Channel Enhancement-Mode Silicon Gate TMOS

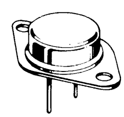
TMOS POWER FETs
6 AMPERES
$r_{DS(on)}$ = 1.6 OHM
600 VOLTS

3

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	2N6826	Unit
Drain-Source Voltage	V_{DSS}	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	600	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous @ T_C = 25°C T_C = 100°C Pulsed	 I_D I_{DM}	 6 4 30	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150	Watts W/°C
Operating Junction Temperature Range	T_J	−65 to 150	°C
Storage Temperature Range	T_{stg}	−65 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	600	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.25 2.5	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	1.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	9.6 13.6	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	2	10	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	750	1500	pF
Output Capacitance		C_{oss}	75	400	
Reverse Transfer Capacitance		C_{rss}	25	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 3 A R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	80	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	55 (Typ)	65	nC
Gate-Source Charge		Q_{gs}	25 (Typ)	—	
Gate-Drain Charge		Q_{gd}	30 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 6 A, V_{GS} = 0)	V_{SD}	0.7	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	—	1000	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

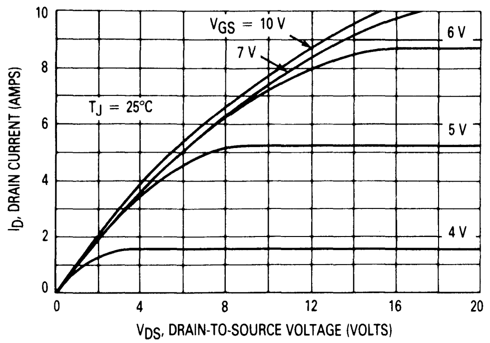


Figure 1. On-Region Characteristics

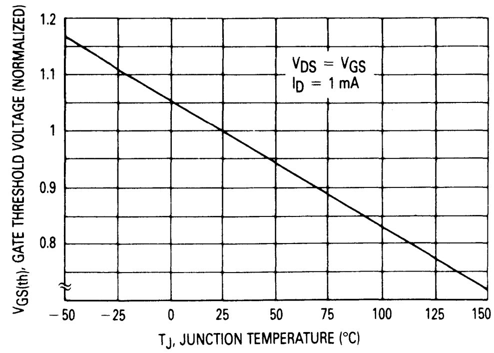


Figure 2. Gate-Threshold Voltage Variation With Temperature

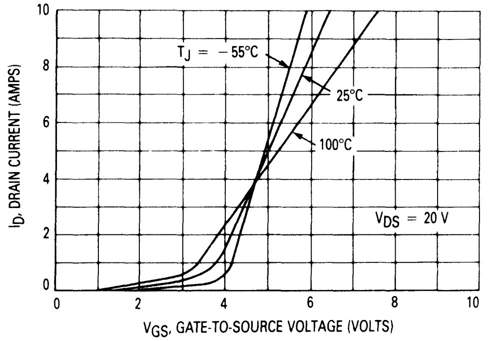


Figure 3. Transfer Characteristics

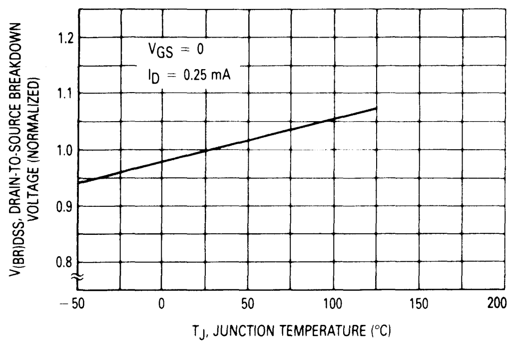


Figure 4. Breakdown Voltage Variation With Temperature

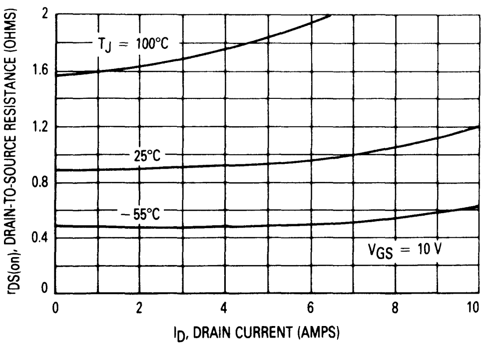


Figure 5. On-Resistance versus Drain Current

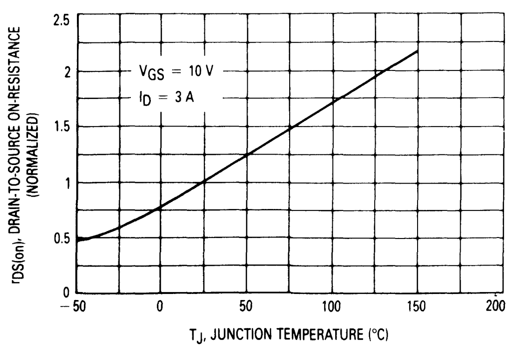


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

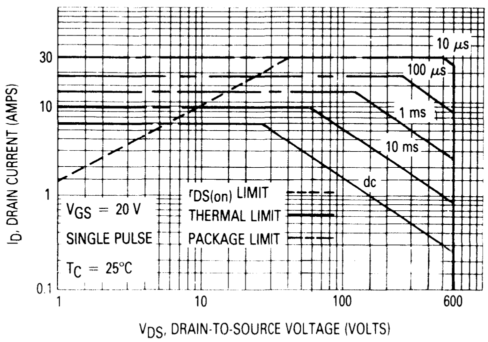


Figure 7. Maximum Rated Forward Biased Safe Operating Area

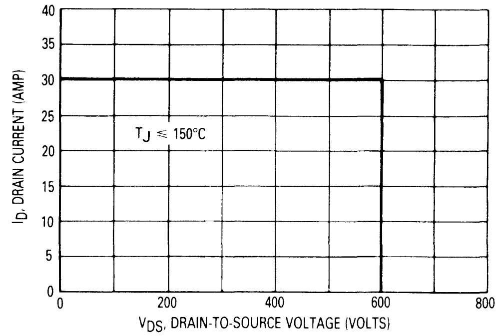


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

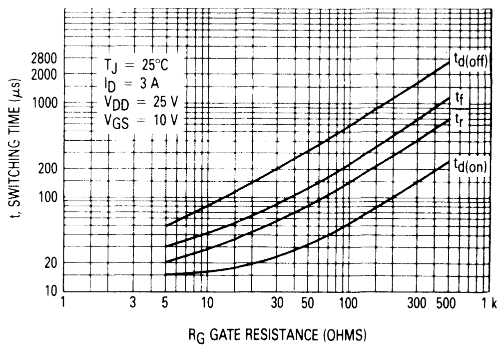


Figure 9. Resistive Switching Time Variation versus Gate Resistance

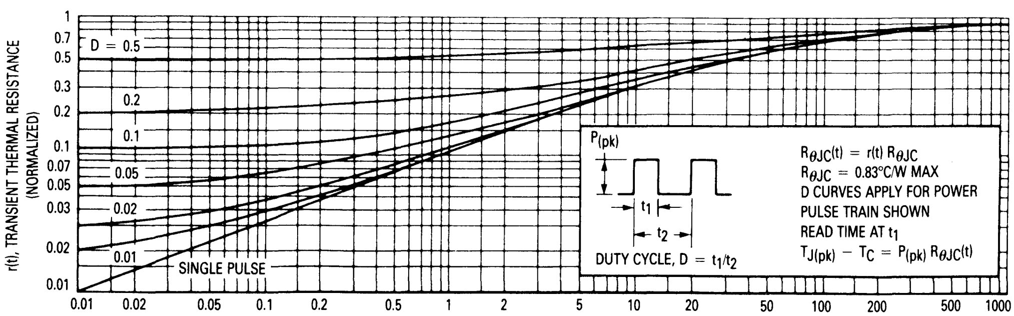


Figure 10. Thermal Response

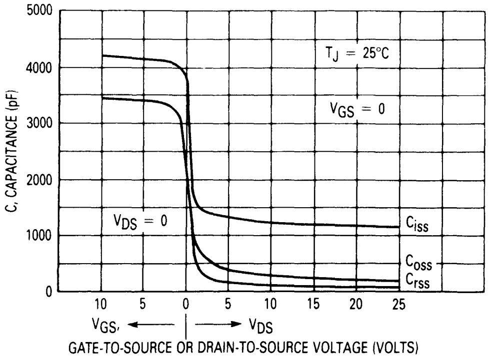


Figure 11. Capacitance Variation

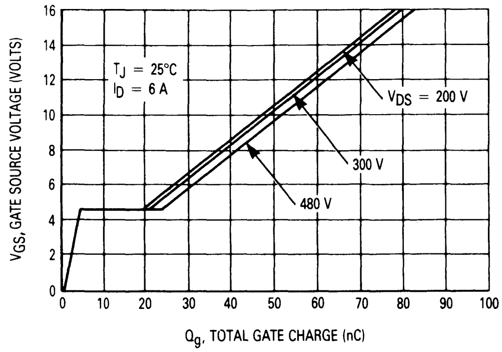


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

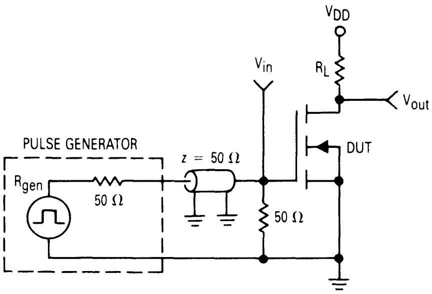


Figure 13. Switching Test Circuit

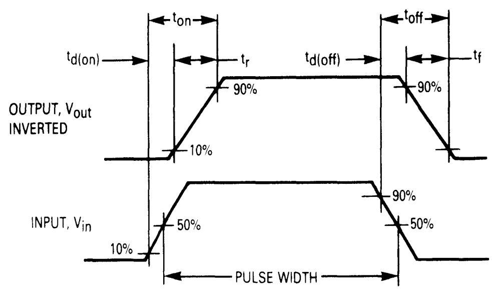
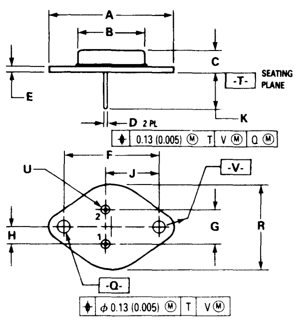


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

3

Advance Information

Small-Signal Field Effect Transistor

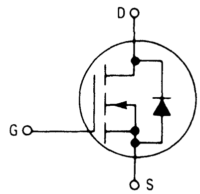
N-Channel Enhancement-Mode Silicon Gate TMOS

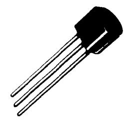
2N7000

**N-CHANNEL
SMALL-SIGNAL TMOS FET
$r_{DS(on)}$ = 5 OHMS
60 VOLTS**

. . . are designed for high voltage, high speed applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Logic Level Switch
- CMOS Logic Interface
- Bipolar Darlington Replacement
- Lamp Relay Driver or Buffer
- Analog Signal Switching





**CASE 29-04
(TO-226AA)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 200 500	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 48 V, V_{GS} = 0) (V_{DS} = 48 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 1	 μAdc mA
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	−10	nAdc

(continued)

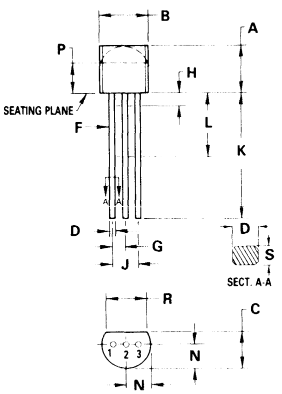
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*				
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)	$V_{GS(th)}$	0.8	3	Vdc
Static Drain-Source On-Resistance	$r_{DS(on)}$			Ohm
(V_{GS} = 10 Vdc, I_D = 0.5 Adc)		—	5	
(V_{GS} = 10 Vdc, I_D = 0.5 V, T_C = 125°C)		—	9	
Drain-Source On-Voltage	$V_{DS(on)}$			Vdc
(V_{GS} = 10 V, I_D = 0.5 Adc)		—	2.5	
(V_{GS} = 4.5 V, I_D = 75 mA)		—	0.4	
On-State Drain Current (V_{GS} = 4.5 V, V_{DS} = 10 V)	$I_{D(on)}$	75	—	mA
Forward Transconductance (V_{DS} = 10 V, I_D = 200 mA)	g_{fs}	100	—	μmhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	60	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	25	
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} = 15 V, I_D = 500 mA, R_{gen} = 25 ohms, R_L = 25 ohms)	t_{on}	—	10	ns
Turn-Off Delay Time (V_{DD} = 15 V, I_D = 500 mA, R_{gen} = 25 ohms, R_L = 25 ohms)	t_{off}	—	10	

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

All JEDEC dimensions and notes apply

CASE 29-04
(TO-226AA)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N7002

Advance Information

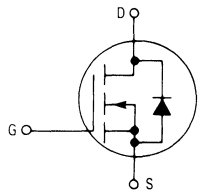
Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

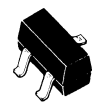
This TMOS FET is designed for high-speed switching applications such as line drivers, relay drivers, CMOS logic, or microprocessor interface applications.

- General Purpose Switch
- Hybrid Assemblies
- Surface Mount Package
- Available in 8 mm Tape and Reel

TMOS™



**N-CHANNEL
SMALL-SIGNAL
TMOS FET
$r_{DS(on)}$ = 7.5 OHM
60 VOLTS**



**CASE 318-02
SOT-23
(TO-236AA)**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Drain Current — Continuous T_C = 25°C (1) T_C = 100°C (1) — Pulsed (2)	I_D I_D I_{DM}	±115 ±75 ±800	mA
Gate-Source Voltage	V_{GS}	±40	Vdc
Total Power Dissipation T_C = 25°C T_C = 100°C Derate above 25°C ambient	P_D	200 80 0.16	mW mW/°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	625	°C/W
Operating and Storage Temperature Range	T_J	−55 to +150	°C
Lead Temperature	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0, V_{DS} = 60 V) T_J = 25°C T_J = 125°C	I_{DSS}	 — —	 — —	 1 500	μAdc
Gate-Body Leakage Current Forward (V_{GS} = 20 Vdc)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current Reverse (V_{GS} = −20 Vdc)	I_{GSSR}	—	—	−100	nAdc

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

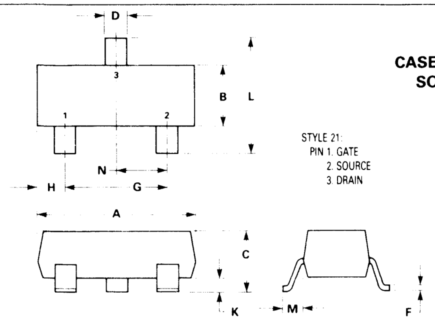
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 250 μA)	$V_{GS(th)}$	1	—	2.5	Vdc
On-State Drain Current ($V_{DS} \geq 2\ V_{DS(on)}$, V_{GS} = 10 V)	$I_{D(on)}$	500	—	—	mA
Static Drain-Source On-State Voltage (V_{GS} = 10 V, I_D = 500 mA) (V_{GS} = 5 V, I_D = 50 mA)	$V_{DS(on)}$	 — —	 — —	 3.75 1.5	Vdc
Static Drain-Source On-State Resistance (V_{GS} = 10 V, I_D = 500 mA) T_C = 25°C T_C = 100°C (V_{GS} = 5 V, I_D = 50 mA) T_C = 25°C T_C = 100°C	$r_{DS(on)}$	 — — — —	 — — — —	 7.5 13.5 7.5 13.5	Ohms
Forward Transconductance ($V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA)	g_{FS}	80	—	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	50	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	—	25	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	—	5	pF
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time (V_{DD} = 30 V, $I_D \cong$ 200 mA, R_G = 25 Ω, R_L = 150 Ω)	$t_{d(on)}$	—	—	20	ns
Turn-Off Delay Time	$t_{d(off)}$	—	—	20	ns
BODY-DRAIN DIODE RATINGS					
Diode Forward On-Voltage (I_S = 11.5 mA , V_{GS} = 0 V)	V_{SD}	—	—	−1.5	V
Source Current Continuous (Body Diode)	I_S	—	—	−115	mA
Source Current Pulsed	I_{SM}	—	—	−800	mA

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 318-02
SOT-23

NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.50	0.0150	0.020
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.45	0.60	0.0177	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

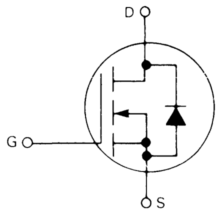
BS170

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high voltage display drivers.

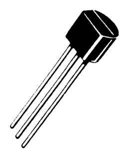
- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance — 5.0 Ohms Max
- Low Drive Requirement, $V_{GS(th)} = 3.0$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

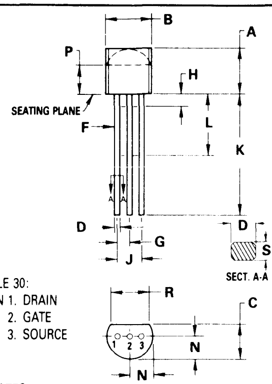
TMOS



60 VOLTS

N-CHANNEL TMOS FET





STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

CASE 29-04
TO-226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (1)	I_D	0.5	Adc
Total Power Dissipation @ $T_C = 25°C$	P_D	0.83	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	90	—	Vdc
Gate-Body Leakage Current (V_{GS} = 15 V, V_{DS} = 0)	I_{GSS}	—	0.01	10	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.8	2.0	3.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 0 V)	$I_{D(off)}$	—	—	0.5	μA
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 200 mA)	$r_{DS(on)}$	—	1.8	5.0	Ohms
Forward Transconductance (V_{DS} = 10 V, I_D = 250 mA)	g_{FS}	—	200	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	60	—	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time (I_D = 0.2 A) See Figure 1	t_{on}	—	4.0	10	ns
Turn-Off Time (I_D = 0.2 A) See Figure 1	t_{off}	—	4.0	10	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

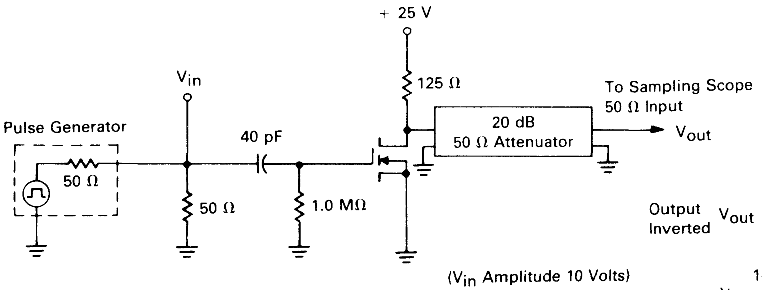


FIGURE 2 — SWITCHING WAVEFORMS

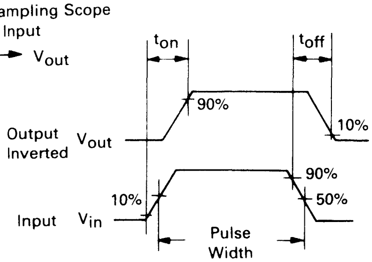


FIGURE 3 — $V_{GS(th)}$ NORMALIZED versus TEMPERATURE

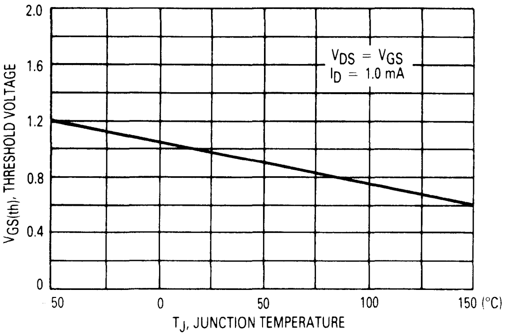


FIGURE 4 — ON-REGION CHARACTERISTICS

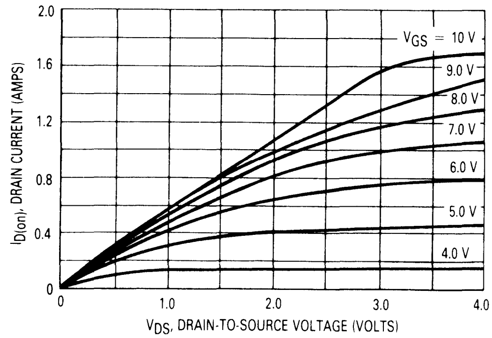


FIGURE 5 — OUTPUT CHARACTERISTICS

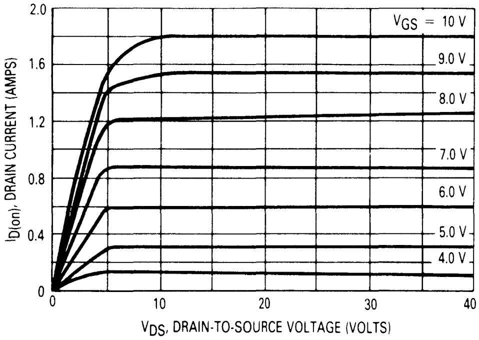
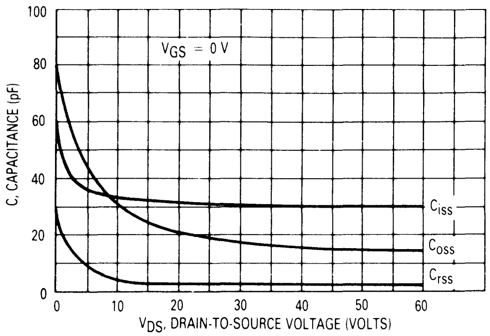


FIGURE 6 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE



BSS123

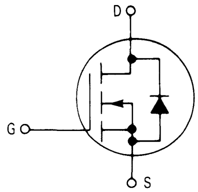
Advance Information

Small-Signal Field Effect Transistor

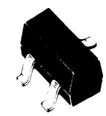
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL-to-high voltage interface and high-voltage display drivers.

- Low On-Resistance — 6 Ohms Typ
- Surface Mount Package



**N-CHANNEL
SMALL-SIGNAL
TMOS FET
$r_{DS(on)}$ = 6 OHMS
100 VOLTS**



**CASE 318-02
SOT-23
(TO-236AA)**

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}	 0.17 0.68	Adc
Total Power Dissipation FR5 Board 1″ x 0.75″ x 0.062″ Derate above 25°C Ambient	P_D	 550 4.4	 mW mW/°C
Operating Temperature	T_J	−55 to +125	°C
Storage Temperature	T_{stg}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0, V_{DS} = 100 V) T_J = 25°C T_J = 125°C	I_{DSS}	 — —	 — —	 15 60	nAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	50	nAdc

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

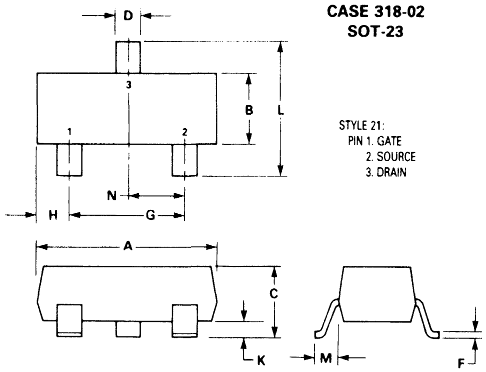
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	0.8	—	2.8	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 100 mA)		$r_{DS(on)}$	—	5	6	Ohms
Forward Transconductance (V_{DS} = 25 V, I_D = 100 mA)		g_{FS}	80	—	—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	20	—	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	9	—	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	4	—	pF
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{CC} = 30 V, I_C = 0.28 A, V_{GS} = 10 V, R_{GS} = 50 Ω)	$t_{d(on)}$	—	20	—	ns
Turn-Off Delay Time		$t_{d(off)}$	—	40	—	ns
REVERSE DIODE						
Diode Forward On-Voltage (I_D = 0.34 A, V_{GS} = 0 V)		V_{SD}	—	—	1.3	V

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 318-02
SOT-23

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.46	0.0150	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

BUZ11
BUZ11A

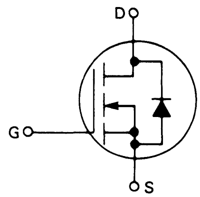
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

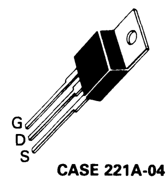
These TMOS III Power FETs are designed for low voltage, high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.04 Ω max and 0.06 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- High Peak Current Capabilities — 75 and 90 A
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max

TMOS

TMOS POWER FETs
25 and 30 AMPERES
$r_{DS(on)}$ = 0.04 and 0.06 OHMS
50 VOLTS





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	BUZ11	BUZ11A	Unit
Drain-Source Voltage	V_{DSS}	50		Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	50		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 120	25 100	A
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

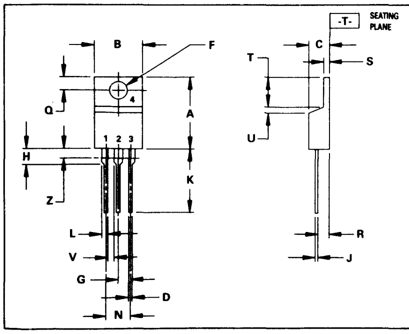
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{(BR)DSS}$	50	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 Volts, V_{GS} = 0) (V_{DS} = 50 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 10 mA)		$V_{GS(th)}$	2.1	3	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)	BUZ11 BUZ11A	$r_{DS(on)}$	— —	— —	0.04 0.06	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc) (I_D = 15 Adc)	BUZ11 BUZ11A	$V_{DS(on)}$	— —	0.54 0.83	— —	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 15 A)		g_{FS}	4	8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	900	2000	pF
Output Capacitance		C_{oss}	—	800	1100	
Reverse Transfer Capacitance		C_{rss}	—	300	400	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 3 A, R_{gen} = 50 ohms) See Figures 4 and 5	$t_{d(on)}$	—	—	45	ns
Rise Time		t_r	—	—	110	
Turn-Off Delay Time		$t_{d(off)}$	—	—	230	
Fall Time		t_f	—	—	170	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Diode Forward Voltage (V_{GS} = 0, I_S = 2 Rated I_S)	BUZ11 BUZ11A	V_{SD}	— —	— —	2.6 2.4	Vdc
Continuous Source Current, Body Diode	BUZ11 BUZ11A	I_S	— —	— —	30 25	Adc
Pulsed Source Current, Body Diode	BUZ11 BUZ11A	I_{SM}	— —	— —	120 100	A
Forward Turn-On Time	(I_S = Rated Value) V_{GS} = 0)	t_{on}	—	260	—	ns
Reverse Recovery Time		t_{rr}	—	200	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



CASE 221A-04
TO-220AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

BUZ11

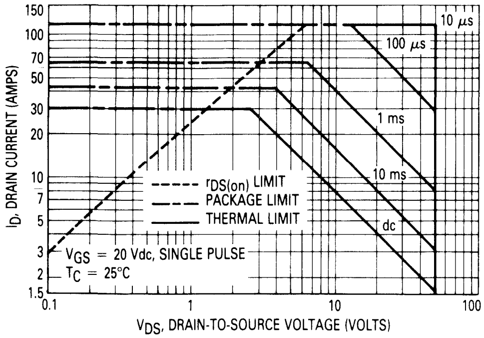


Figure 1. Maximum Rated Forward Biased Safe Operating Area

BUZ11A

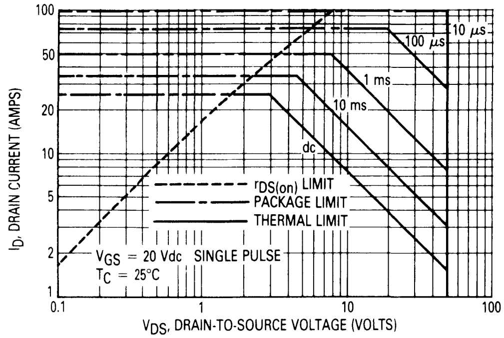


Figure 2. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 1 and 2 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_D(25°C)\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

Where

- $I_D(25°C)$ = the dc drain current at T_C = 25°C from Figure 1 or 2
- $T_{J(max)}$ = rated maximum junction temperature
- T_C = device case temperature
- P_D = rated power dissipation at T_C = 25°C
- $R_{\theta JC}$ = rated steady state thermal resistance
- $r(t)$ = normalized thermal response from Figure 3

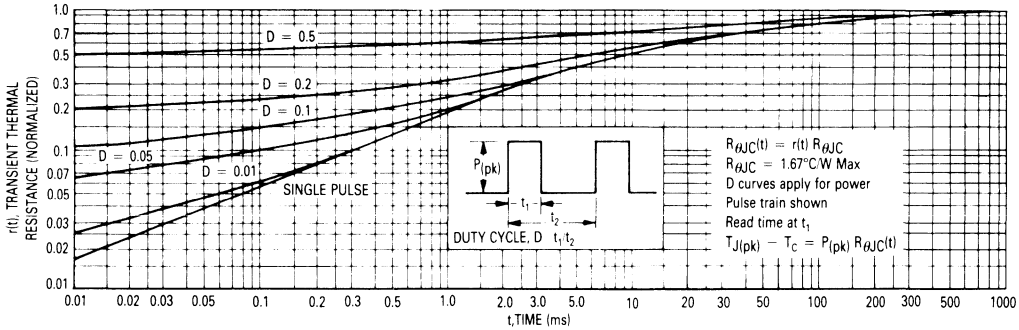


Figure 3. Thermal Response

RESISTIVE SWITCHING

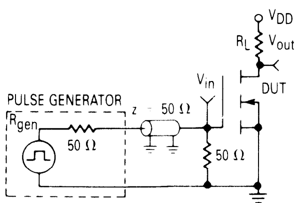


Figure 4. Switching Test Circuit

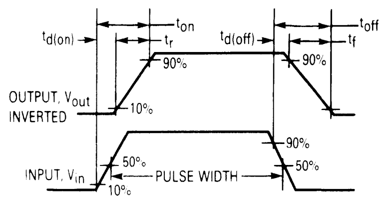


Figure 5. Switching Waveforms

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

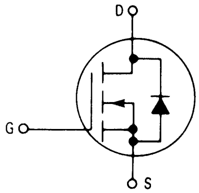
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

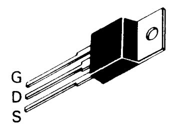
BUZ71
BUZ71A

These TMOS III Power FETs are designed for low voltage, high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.10 Ω max and 0.12 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max



TMOS POWER FETs
12 AMPERES
$r_{DS(on)}$ = 0.10 and 0.12 OHMS
50 VOLTS



CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	BUZ71	BUZ71A	Unit
Drain-Source Voltage	V_{DSS}	50		Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	50		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 48		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction toAmbient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

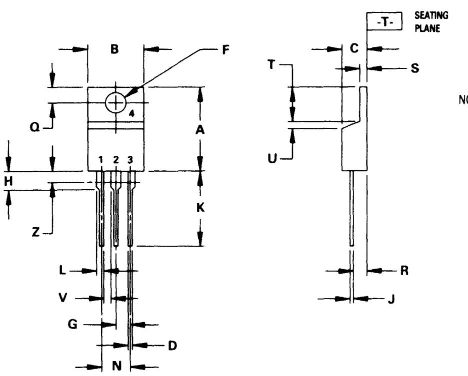
Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{(BR)DSS}$	50	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 Volts, V_{GS} = 0) (V_{DS} = 50 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 10 mA)		$V_{GS(th)}$	2.1	3.1	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)	BUZ71 BUZ71A	$r_{DS(on)}$	— —	0.08 0.10	0.10 0.12	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc) (I_D = 6 Adc)	BUZ71 BUZ71A	$V_{DS(on)}$	— —	0.48 0.60	— —	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 6 A)		g_{FS}	3	5.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	650	pF
Output Capacitance		C_{oss}	—	—	450	
Reverse Transfer Capacitance		C_{rss}	—	—	280	
Total Gate Charge	(V_{DS} = 40 V, V_{GS} = 10 Vdc, I_D = 12 A) See Figures 6 and 12	Q_g	—	14	—	nC
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 3 A, R_{gen} = 50 ohms) See Figures 11 and 12	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	85	
Turn-Off Delay Time		$t_{d(off)}$	—	—	90	
Fall Time		t_f	—	—	110	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 24 A, V_{GS} = 0)	V_{SD}	—	—	2.2	Vdc
Forward Turn-On Time		t_{on}	—	120	—	ns
Reverse Recovery Time		t_{rr}	—	110	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.



CASE 221A-04
TO-220AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

3

3

TYPICAL CHARACTERISTICS

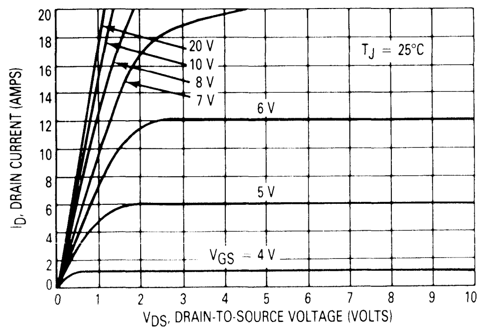


Figure 1. On-Region Characteristics

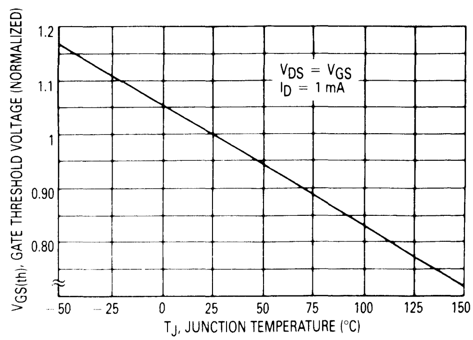


Figure 2. Gate-Threshold Voltage Variation With Temperature

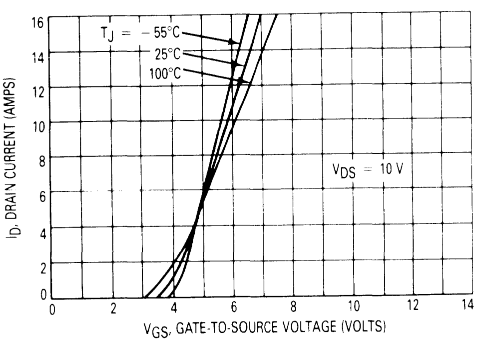


Figure 3. Transfer Characteristics

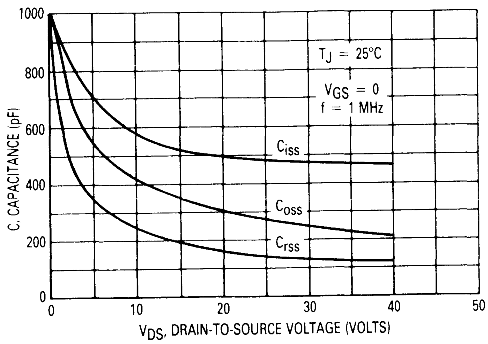


Figure 4. Capacitance Variation

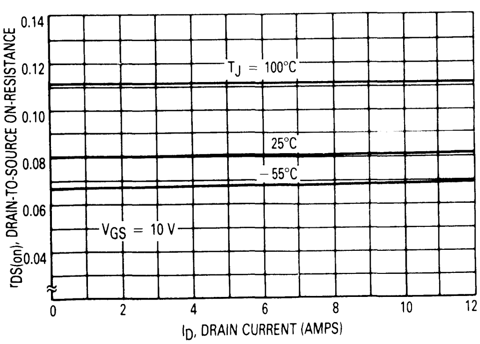


Figure 5. On-Resistance versus Drain Current

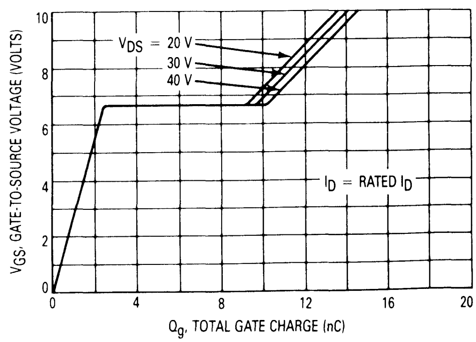


Figure 6. Gate Charge versus Gate-To-Source Voltage

RATED SAFE OPERATING AREA INFORMATION

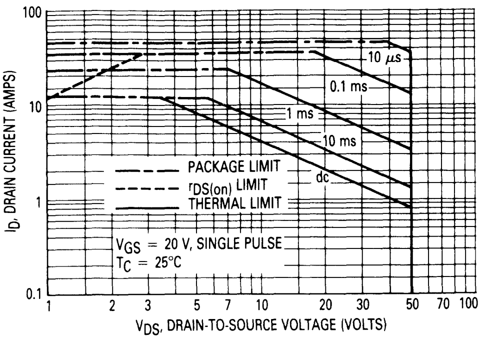


Figure 7. Maximum Rated Forward Biased Safe Operating Area

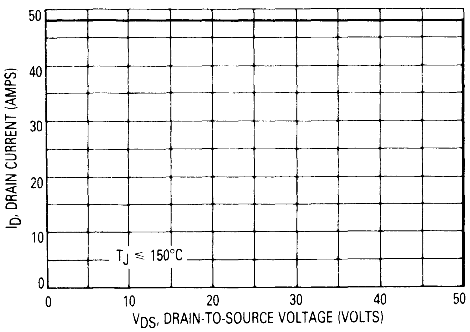


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 7
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 9

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

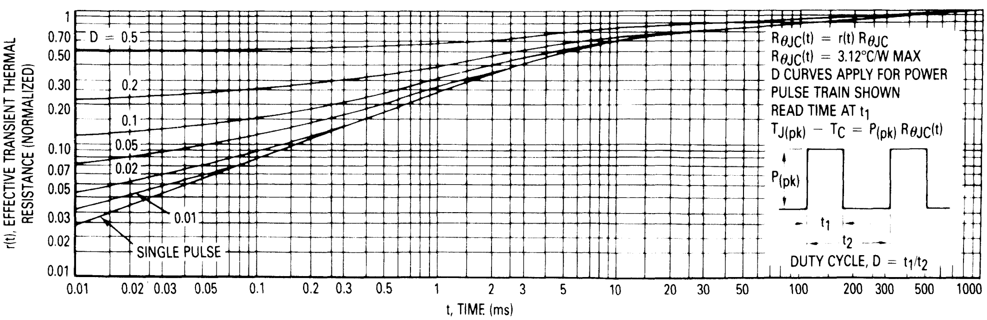


Figure 9. Thermal Response

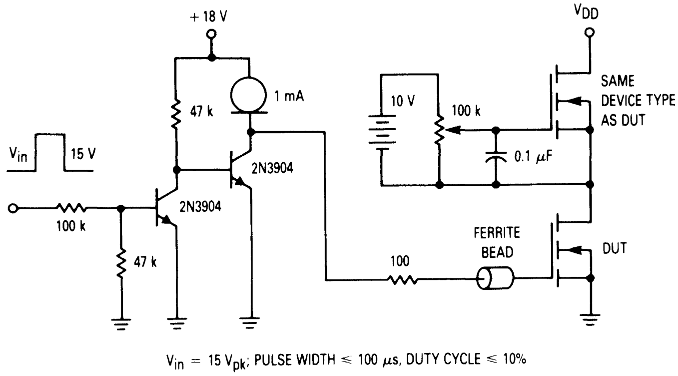


Figure 10. Gate Charge Test Circuit

3

RESISTIVE SWITCHING

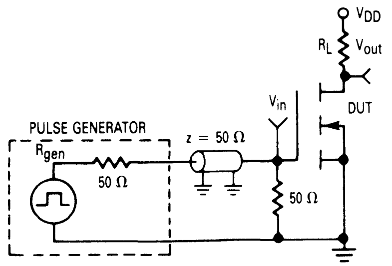


Figure 11. Switching Test Circuit

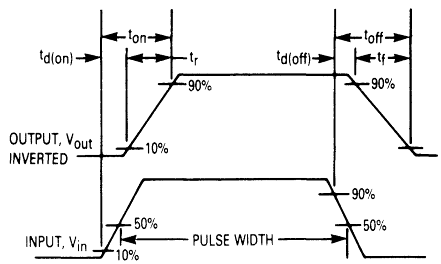


Figure 12. Switching Waveforms

Power Field Effect Transistor

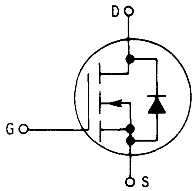
N-Channel Enhancement-Mode Silicon Gate

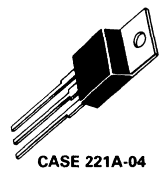
BUZ73

This TMOS Power FET s designed for high speed, low loss power switching applcations such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.4 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max

TMOS POWER FET
7 AMPERES
$r_{DS(on)}$ = 0.4 OHMS
200 VOLTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	7 28	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{(BR)DSS}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 200 Volts, V_{GS} = 0) (V_{DS} = 200 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

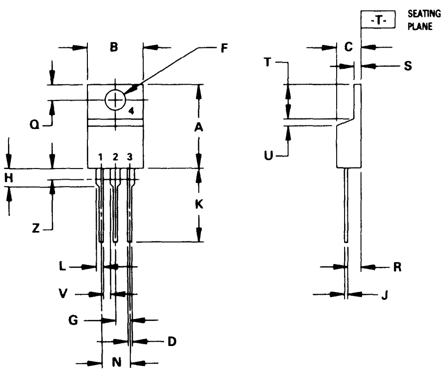
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 10 mA)		$V_{GS(th)}$	2.1	3	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$r_{DS(on)}$	—	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7 Adc)		$V_{DS(on)}$	—	3.2	—	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 3.5 A)		g_{FS}	2.2	3.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	600	pF
Output Capacitance		C_{oss}	—	—	160	
Reverse Transfer Capacitance		C_{rss}	—	—	80	
Total Gate Charge	(V_{DS} = 160 V, V_{GS} = 10 Vdc, I_D = 7 A)	Q_g	—	15	—	nC
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 3 A, V_{GS} = 10 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	—	20	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	90	
Fall Time		t_f	—	—	55	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 14 A, V_{GS} = 0)	V_{SD}	—	—	1.7	Vdc
Forward Turn-On Time		t_{on}	—	120	—	ns
Reverse Recovery Time		t_{rr}	—	325	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

CASE 221A-04
TO-220AB



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONNG AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.8	5.33	0.190	0.210
Q	2.5	3.04	0.100	0.120
R	2.0	2.79	0.080	0.110
S	1.1	1.39	0.045	0.055
T	5.9	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

TYPICAL ELECTRICAL CHARACTERISTICS

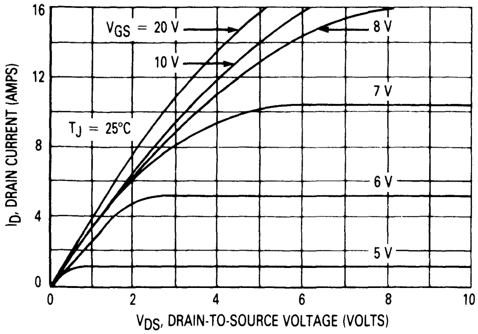


Figure 1. On-Region Characteristics

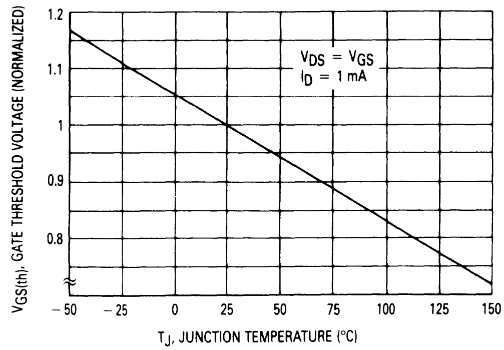


Figure 2. Gate-Threshold Voltage Variation With Temperature

3

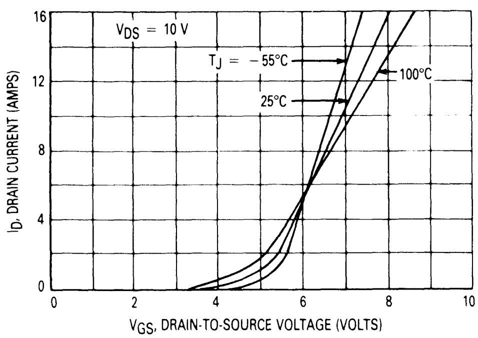


Figure 3. Transfer Characteristics

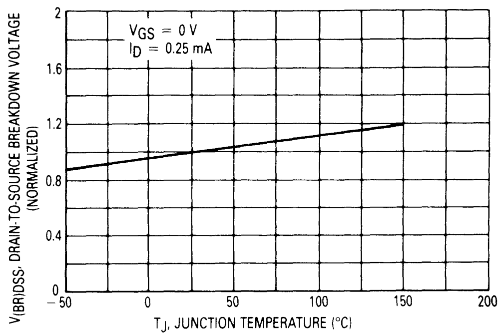


Figure 4. Breakdown Voltage Variation With Temperature

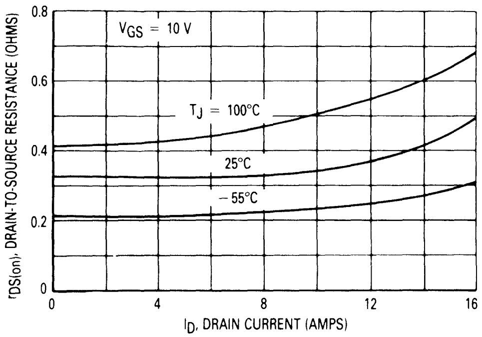


Figure 5. On-Resistance versus Drain Current

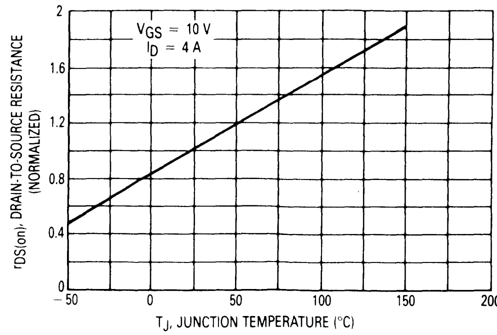


Figure 6. On-Resistance Variation With Temperature

RATED SAFE OPERATING AREA INFORMATION

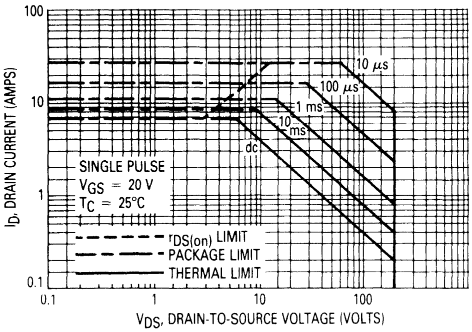


Figure 7. Maximum Rated Forward Biased Safe Operating Area

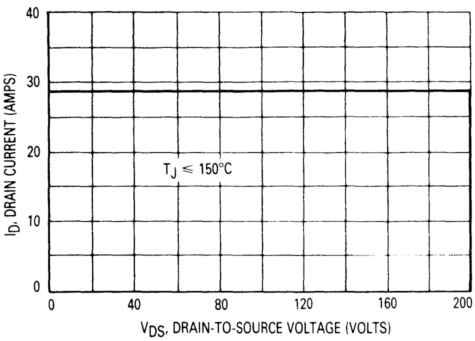


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$	=	the dc drain current at T_C = 25°C from Figure 7
$T_{J(max)}$	=	rated maximum junction temperature
T_C	=	device case temperature
P_D	=	rated power dissipation at T_C = 25°C
$R_{\theta JC}$	=	rated steady state thermal resistance
$r(t)$	=	normalized thermal response from Figure 9

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

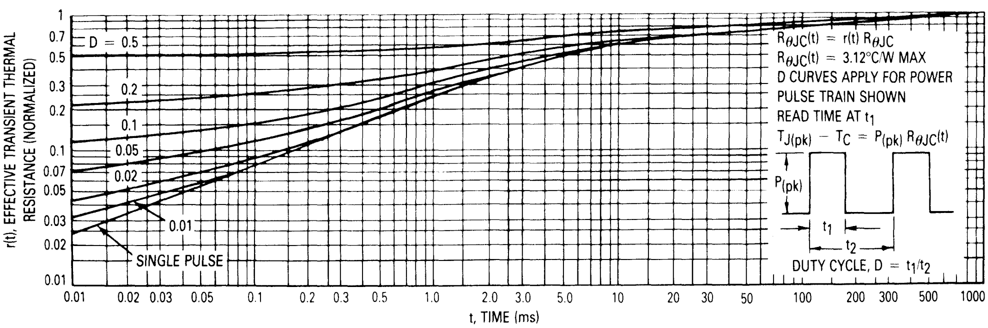


Figure 9. Thermal Response

BUZ80A

Power Field Effect Transistor

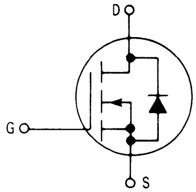
N-Channel Enhancement-Mode
Silicon Gate

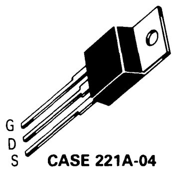
TMOS POWER FET
3 AMPERES
$r_{DS(on)}$ = 3 OHMS
800 VOLTS

This TMOS Power FET is designed for high voltage, high speed, low loss power switching applications, such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 3 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max

TMOS





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	800	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	800	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	3 12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	800	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 800 Volts, V_{GS} = 0) (V_{DS} = 800 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

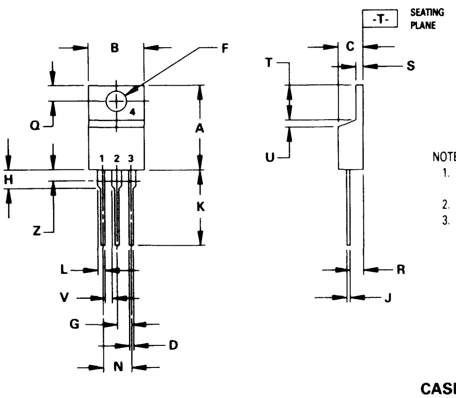
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2.1	3	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.7 Adc)		$r_{DS(on)}$	—	2.1	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1.7 Adc)		$V_{DS(on)}$	—	3.6	—	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 1.7 A)		g_{FS}	1	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	2100	pF
Output Capacitance		C_{oss}	—	—	150	
Reverse Transfer Capacitance		C_{rss}	—	—	55	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 2.3 A, V_{GS} = 10 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	—	45	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	140	
Fall Time		t_f	—	—	80	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 6 A, V_{GS} = 0)	V_{SD}	—	—	1.3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	—	600	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

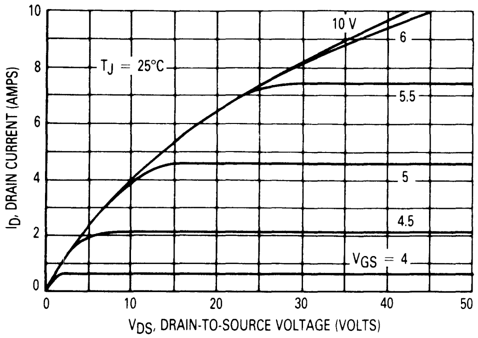


Figure 2. Gate-To-Source Threshold Voltage Variation With Temperature

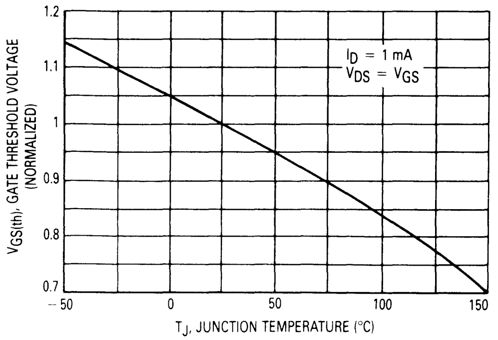


Figure 3. Transfer Characteristics

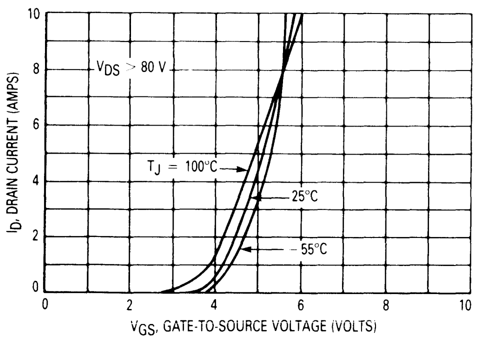


Figure 4. Breakdown Voltage Variation With Temperature

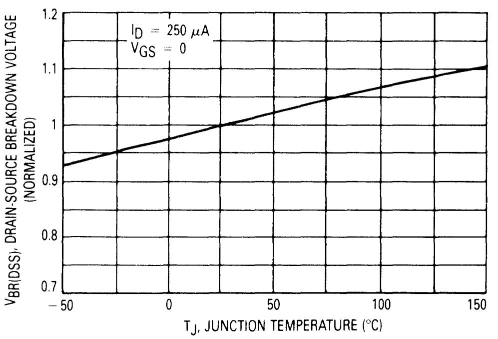


Figure 5. On-Resistance Variation With Drain Current

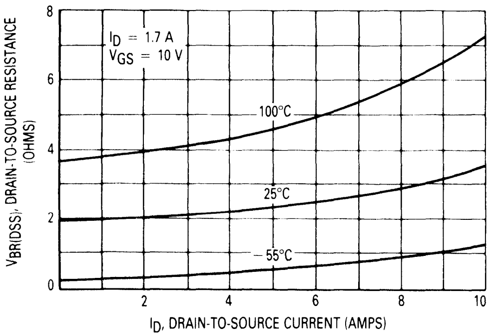
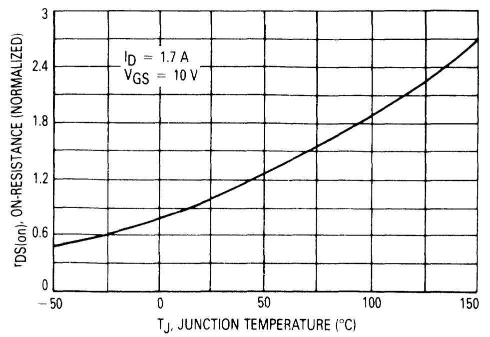
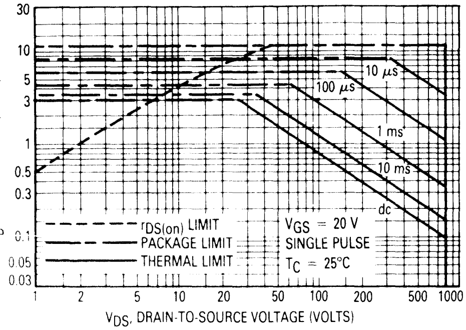


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Bias Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 8. Thermal Response

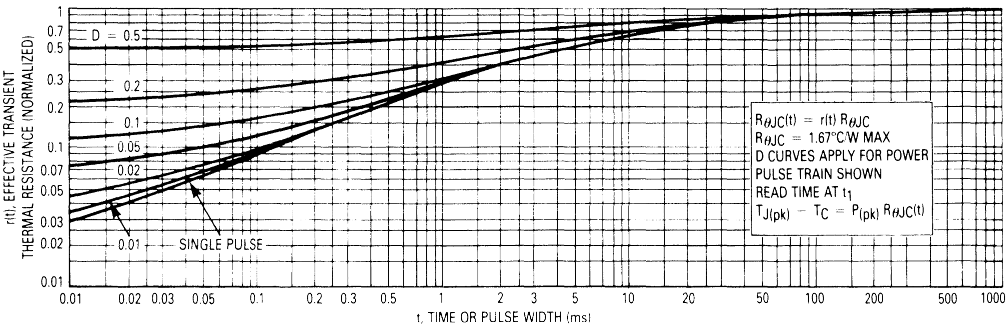


Figure 9. Capacitance Variation With Voltage

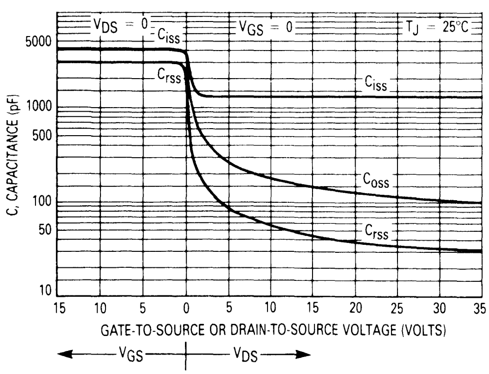
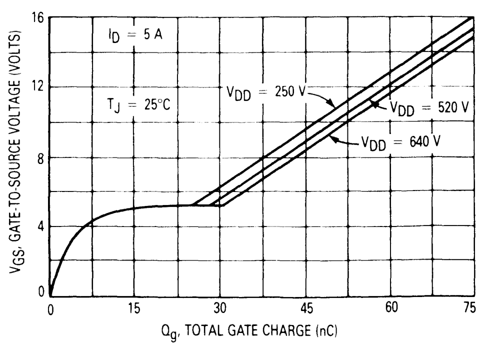


Figure 10. Gate Charge versus Gate-To-Source Voltage



BUZ84
BUZ84A

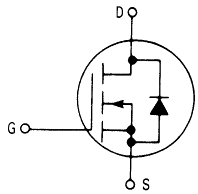
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

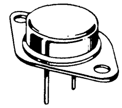
TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max



TMOS POWER MOSFETs
5.3 and 6 AMPERES
$r_{DS(on)}$ = 1.5 and 2 OHMS
800 VOLTS



3

MAXIMUM RATINGS

Rating	Symbol	BUZ84	BUZ84A	Unit
Drain-Source Voltage	V_{DSS}	800		Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	800		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous T_C = 25°C T_C = 100°C Pulsed	I_D I_{DM}	5.3 3.3 21	6 3.8 24	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	300	°C

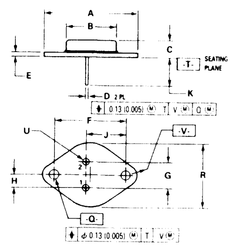
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA)	$V_{BR(DSS)}$	800	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = 800 V, V_{GS} = 0) T_J = 125°C	I_{DSS}	 — —	 — —	 0.25 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 V)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (I_D = 10 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	2.1	—	4	Vdc

See the MTM5N90 Designer's Data Sheet for a complete set of design curves for this device.
Design curves of the MTM6N85 are applicable for this device.

(continued)

OUTLINE DIMENSIONS



STYLE 3
PIN 1 GATE
2 SOURCE
CASE DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH
3 ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS — continued						
Static Drain Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 3 Adc)	BUZ84 BUZ84A	$r_{DS(on)}$	— —	— —	2 1.5	Ohms
Forward Transconductance(1) (V_{DS} = 25 Vdc, I_D = 3 A)		g_{FS}	1.8	—	—	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	2000	5000	pF
Output Capacitance		C_{oss}	—	200	350	
Reverse Transfer Capacitance		C_{rss}	—	80	140	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 30 V, I_D = 2.5 Adc BUZ84 I_D = 2.6 Adc BUZ84A Z_o = 50 Ω, V_{GS} = 10 V) See Figs. 1 and 2	$t_{d(on)}$	—	50	90	ns
Rise Time		t_r	—	100	140	
Turn-Off Delay Time		$t_{d(off)}$	—	320	430	
Fall Time		t_f	—	100	140	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0) (I_S = 10.6 A BUZ84) (I_S = 12 A BUZ84A)		V_{SD}	— —	— —	1.45 1.5	Vdc
Continuous Source Current, Body Diode	BUZ84 BUZ84A	I_S	— —	— —	5.3 6	Adc
Pulsed Source Current, Body Diode	BUZ84 BUZ84A	I_{SM}	— —	— —	21 24	A
Forward Turn-On Time	(I_S = 5.3 A, V_{GS} = 0)	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	—	1200	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die.)		L_d	—	5	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad.)		L_s	—	12.5	—	

(1) Pulse Test = Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

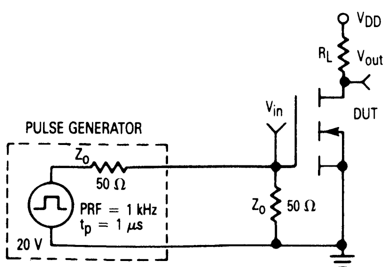


Figure 1. Switching Test Circuit

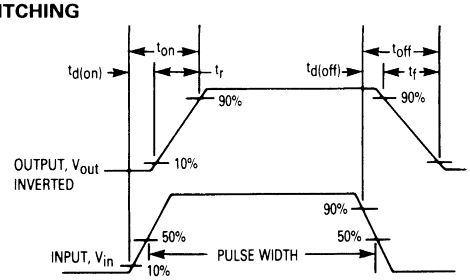


Figure 2. Switching Waveforms

Power Field Effect Transistor

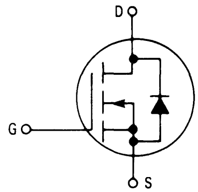
N-Channel Enhancement-Mode
Silicon Gate

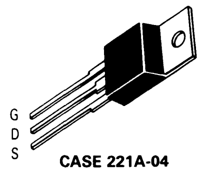
BUZ90

This TMOS IV Power FET is designed for high voltage, high speed, low loss power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 2 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max

TMOS POWER FET
4 AMPERES
$r_{DS(on)}$ = 2 OHMS
600 VOLTS





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	600	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	600	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	4 16	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	600	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 600 Volts, V_{GS} = 0) (V_{DS} = 600 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 20 100	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

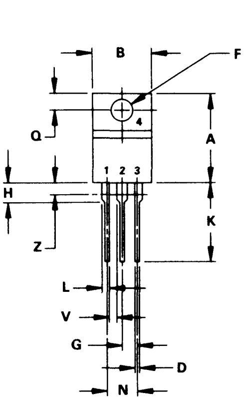
(continued)

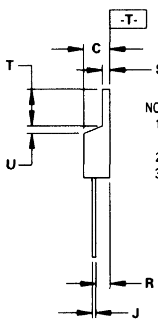
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	2.1	3	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	1.8	2	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2.5 Adc)		$V_{DS(on)}$	—	4.5	—	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 2.5 A)		g_{FS}	1.5	2.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	2000	pF
Output Capacitance		C_{oss}	—	—	170	
Reverse Transfer Capacitance		C_{rss}	—	—	70	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 2.5 A, V_{GS} = 10 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	—	45	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	140	
Fall Time		t_f	—	—	60	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 8 A, V_{GS} = 0)	V_{SD}	—	0.95	1.2	Vdc
Forward Turn-On Time	(I_S = 4 A, dI_S/dt = 100 A/μs V_R = 100 V, V_{GS} = 0)	t_{on}	Limited by stray inductance.			
Reverse Recovery Time		t_{rr}	—	1200	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

Power Field Effect Transistor

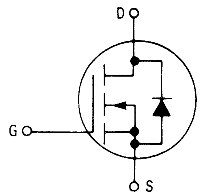
N-Channel Enhancement-Mode Silicon Gate

BUZ330

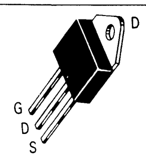
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.6 Ω Max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



TMOS POWER FET
9.5 AMPERES
$r_{DS(on)}$ = 0.6 OHMS
500 VOLTS



CASE 340-02
TO-218

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	500	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	500	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	9.5 38	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 Volts, V_{GS} = 0) (V_{DS} = 500 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1.0 10	 80 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

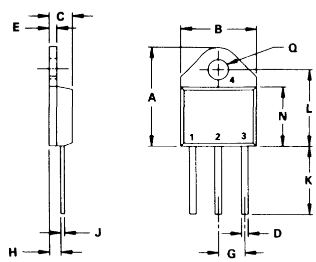
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 10 mA)		$V_{GS(th)}$	2.1	3.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.47	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 9.5 Adc)		$V_{DS(on)}$	—	4.75	—	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 6.0 A)		g_{FS}	5.0	8.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	1800	pF
Output Capacitance		C_{oss}	—	—	270	
Reverse Transfer Capacitance		C_{rss}	—	—	120	
Total Gate Charge	(V_{DS} = 400 V, V_{GS} = 10 Vdc, I_D = 12.8 A)	Q_g	—	70	—	nC
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	—	40	ns
Rise Time		t_r	—	—	70	
Turn-Off Delay Time		$t_{d(off)}$	—	—	310	
Fall Time		t_f	—	—	90	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 19 A, V_{GS} = 0)	V_{SD}	—	1.0	1.4	Vdc
Forward Turn-On Time	(I_S = 9.5 A, dI_S/dt = 100 A/μs, V_R = 100 V)	t_{on}	Negligible			ns
Reverse Recovery Time		t_{rr}	—	400	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

CASE 340-02
TO-218



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. Output Characteristics

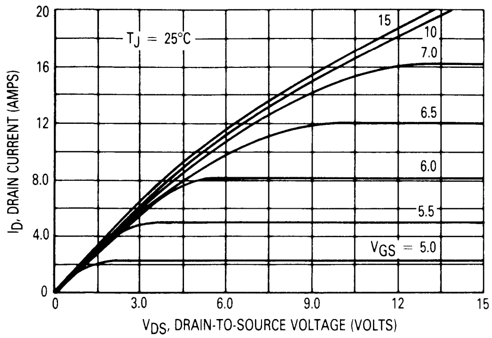


Figure 2. Gate-To-Source Threshold Voltage Variation With Temperature

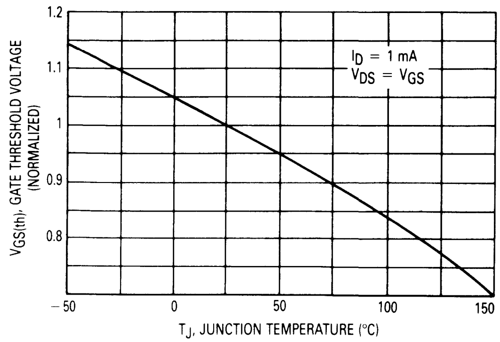


Figure 3. Transfer Characteristics

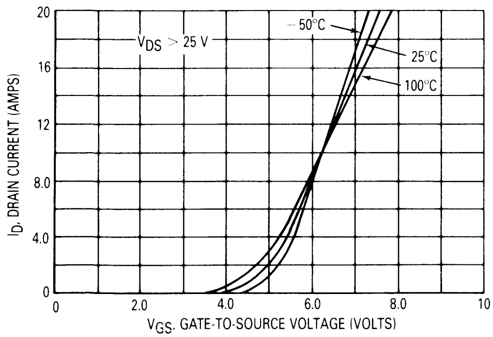


Figure 4. Breakdown Voltage Variation With Temperature

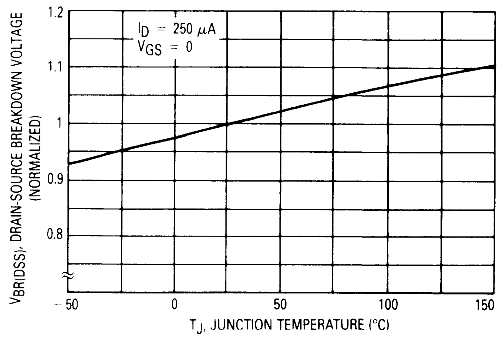


Figure 5. On-Resistance versus Drain Current

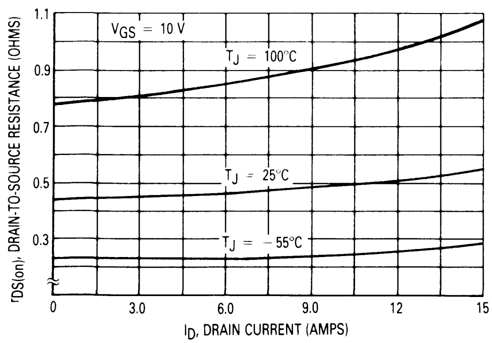
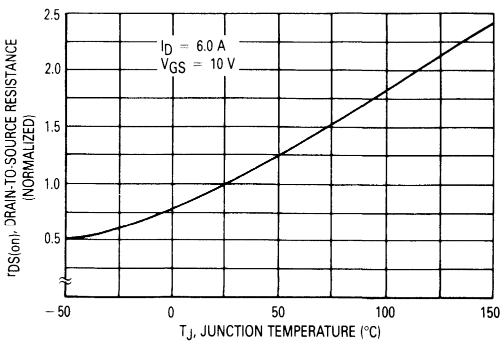


Figure 6. On-Resistance Variation With Temperature



3

SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

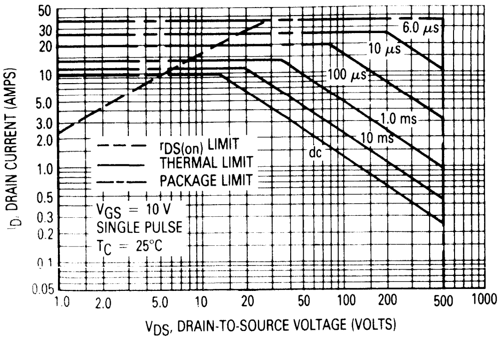
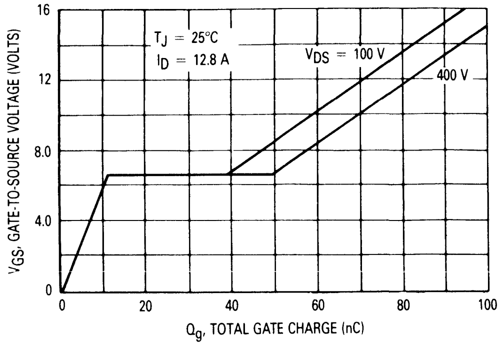


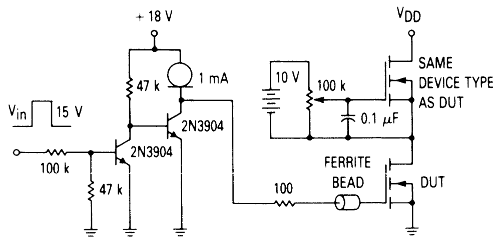
Figure 8. Gate Charge versus Gate-To-Source Voltage



FORWARD BIASED SAFE OPERATING AREA

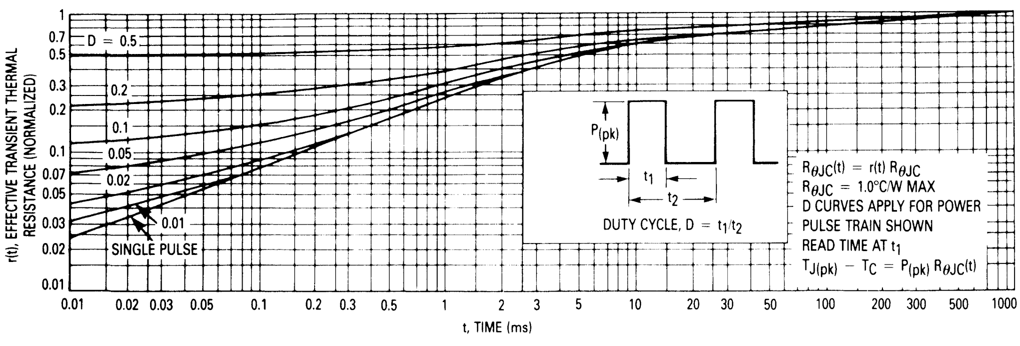
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 9. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Thermal Response



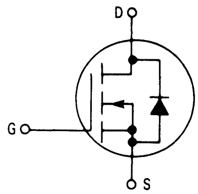
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate

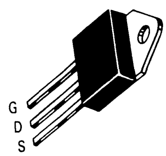
BUZ355

This TMOS IV Power FET is designed for low voltage, high speed, low loss power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.10 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max

TMOS POWER FET
6 AMPERES
$r_{DS(on)}$ = 1.5 OHMS
800 VOLTS





CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	800	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	800	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	6 24	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	$V_{(BR)DSS}$	800	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 800 Volts, V_{GS} = 0) (V_{DS} = 800 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 20 100	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

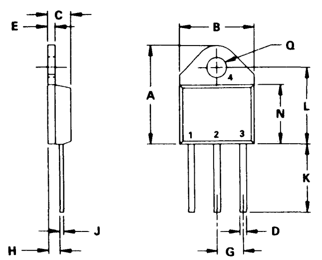
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	2.1	3	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.8 Adc)		$r_{DS(on)}$	—	1.3	1.5	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3.8 Adc)		$V_{DS(on)}$	—	5	—	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 3.8 A)		g_{FS}	1.8	3.3	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	5000	pF
Output Capacitance		C_{oss}	—	—	350	
Reverse Transfer Capacitance		C_{rss}	—	—	140	
Total Gate Charge	(V_{DS} = 40 V, V_{GS} = 10 Vdc, I_D = 12 A)	Q_g	—	14	—	nC
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 2.6 A, V_{GS} = 10 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	—	90	ns
Rise Time		t_r	—	—	140	
Turn-Off Delay Time		$t_{d(off)}$	—	—	430	
Fall Time		t_f	—	—	140	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	—	1.1	1.3	Vdc
Forward Turn-On Time	(I_S = 6 A, dI_S/dt = 100 A/μs V_R = 100 V, V_{GS} = 0)	t_{on}	Limited by stray inductance.			
Reverse Recovery Time		t_{rr}	—	1800	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

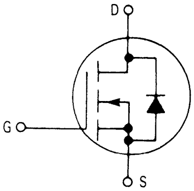
IRF130

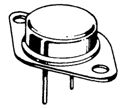
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FET
14 AMPERES
$r_{DS(on)}$ = 0.18 OHM
100 VOLTS





CASE 1-04
TO-204AA

MAXIMUM RATINGS

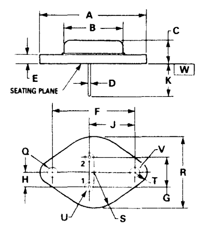
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 14 9 56	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 Seconds	T_L	300	°C

See the MTM12N08 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM12N10 are applicable for this series of product.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 8 Adc)	$r_{DS(on)}$	—	0.18	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 2.5 Vdc)	$I_{D(on)}$	14	—	Adc
Forward Transconductance (V_{DS} ≥ 2.5 V, I_D = 8 A)	g_{FS}	4	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	150	

SWITCHING CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} ≈ 36 V, I_D = 8 Apk, R_{gen} = 15 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	75	
Turn-Off Delay Time		$t_{d(off)}$	—	40	
Fall Time		t_f	—	45	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	17 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	9 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	2.3(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

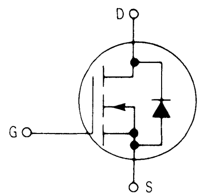
IRF140
IRF141
IRF142

Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

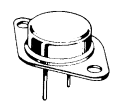
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



TMOS POWER FETs
24 and 27 AMPERES
$r_{DS(on)}$ = 0.085 OHM
60 and 100 VOLTS
$r_{DS(on)}$ = 0.11 OHMS
100 VOLTS



CASE 197A-02
TO-204AE

3

MAXIMUM RATINGS

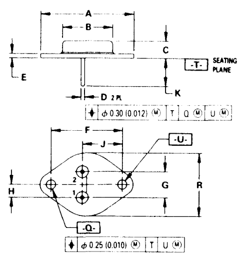
Rating	Symbol	IRF 140	IRF 141	IRF 142	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	100	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 27 17 108		 24 15 96	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM25N10 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF140, IRF142 IRF141	$V_{(BR)DSS}$	100 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)	IRF140, IRF141 IRF142	$r_{DS(on)}$	— —	0.085 0.11	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 2.3 Vdc) (V_{DS} ≥ 2.6 Vdc)	IRF140, IRF141 IRF142	$I_{D(on)}$	27 24	— —	Adc
Forward Transconductance (V_{DS} ≥ 2.3 V, I_D = 15 A) (V_{DS} ≥ 2.6 V, I_D = 15 A)	IRF140, IRF141 IRF142	g_{FS}	6.0 6.0	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	800	
Reverse Transfer Capacitance		C_{rss}	—	300	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 30 V, I_D = 15 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	17 (Typ)	—	
Gate-Drain Charge		Q_{gd}	23 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.2 V for IRF140 and IRF141.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

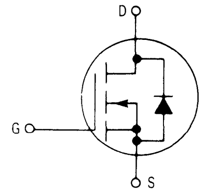
IRF150
IRF151
IRF152

Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

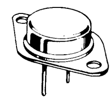
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

3



TMOS POWER FETs
33 and 40 AMPERES
$r_{DS(on)}$ = 0.055 OHM
60 and 100 VOLTS
$r_{DS(on)}$ = 0.08 OHMS
100 VOLTS



CASE 197A-02
TO-204AE

MAXIMUM RATINGS

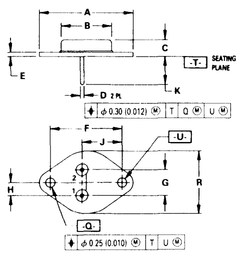
Rating	Symbol	IRF 150	IRF 151	IRF 152	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	100	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 40 25 160		 33 20 132	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM55N08 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM55N10 are applicable for this series of product.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF150, IRF152 IRF151	$V_{(BR)DSS}$	100 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc)	IRF150, IRF151 IRF152	$r_{DS(on)}$	— —	0.055 0.080	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 2.2 Vdc) (V_{DS} ≥ 2.6 Vdc)	IRF150, IRF151 IRF152	$I_{D(on)}$	40 33	— —	Adc
Forward Transconductance (V_{DS} ≥ 2.2 V, I_D = 20 A) (V_{DS} ≥ 2.6 V, I_D = 20 A)	IRF150, IRF151 IRF152	g_{FS}	9 9	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 24 V, I_D = 20 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	125	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	60 (Typ)	120	nC
Gate-Source Charge		Q_{gs}	25 (Typ)	—	
Gate-Drain Charge		Q_{gd}	35 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.2 V for IRF150 and IRF151.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF230

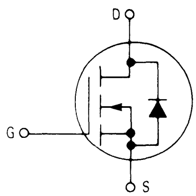
Power Field Effect Transistor

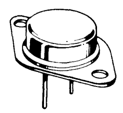
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
9 AMPERES
$r_{DS(on)}$ = 0.4 OHM
200 VOLTS

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 1-06
TO-204AA

3

MAXIMUM RATINGS

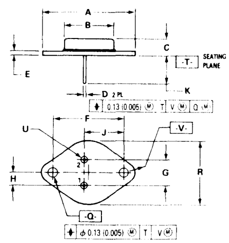
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous, T_C = 25°C T_C = 200°C Peak, T_C = 25°C	I_D	 9 6 36	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM8N20 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)			—	0.2	
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.4	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 3.6 Vdc)		$I_{D(on)}$	9	—	Adc
Forward Transconductance (V_{DS} ≥ 3.6 V, I_D = 5 A)		g_{FS}	3	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	450	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 90 V, I_D = 5 Apk, R_{gen} = 15 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	40	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	15 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.7 (Typ)	2.0	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

IRF240
IRF241
IRF243

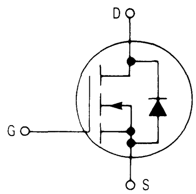
Power Field Effect Transistor

N-Channel Enhancement-Mode
Silicon Gate TMOS

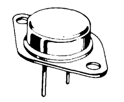
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



TMOS POWER FETs
16 and 18 AMPERES
$r_{DS(on)}$ = 0.18 OHM
150 and 200 VOLTS
$r_{DS(on)}$ = 0.22 OHMS
150 VOLTS



CASE 197A-02
TO-204AE

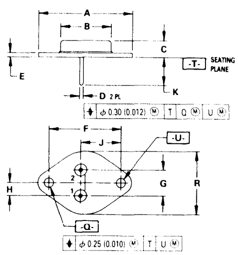
MAXIMUM RATINGS

Rating	Symbol	IRF 240	IRF 241	IRF 243	Unit
Drain-Source Voltage	V_{DSS}	200	150	150	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	150	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 200°C Peak, T_C = 25°C	I_D	 18 11 72		 16 10 64	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) IRF240	$V_{(BR)DSS}$	200	—	Vdc
IRF241, IRF243		150	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc) IRF240, IRF241	$r_{DS(on)}$	—	0.18	Ohm
IRF243		—	0.22	
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 3.2 Vdc) IRF240, IRF241	$I_{D(on)}$	18	—	Adc
(V_{DS} ≥ 3.5 Vdc) IRF243		16	—	
Forward Transconductance (V_{DS} ≥ 3.2 V, I_D = 10 A) IRF240, IRF241	g_{FS}	6	—	mhos
(V_{DS} ≥ 3.5 V, I_D = 10 A) IRF243		6	—	
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1600	pF
Output Capacitance	C_{oss}	—	750	
Reverse Transfer Capacitance	C_{rss}	—	300	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} ≈ 75 V, I_D = 10 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time	t_r	—	60	
Turn-Off Delay Time	$t_{d(off)}$	—	80	
Fall Time	t_f	—	60	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	38 (Typ)	60	nC
Gate-Source Charge	Q_{gs}	16 (Typ)	—	
Gate-Drain Charge	Q_{gd}	22 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8 (Typ)	1.9(1)	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.1 V for IRF240 and IRF241.

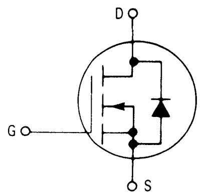
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF250
IRF251
IRF252
IRF253

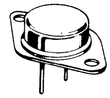
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETs
25 and 30 AMPERES
$r_{DS(on)}$ = 0.085 OHM
150 and 200 VOLTS
$r_{DS(on)}$ = 0.12 OHMS
150 and 200 VOLTS



CASE 197A-02
TO-204AE

MAXIMUM RATINGS

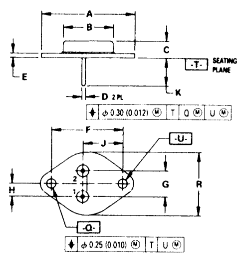
Rating	Symbol	IRF 250	IRF 251	IRF 252	IRF 253	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 30 19 120		 25 16 100		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM40N20 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) IRF250, IRF252 IRF251, IRF253		$V_{(BR)DSS}$	200 150	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc) IRF250, IRF251 IRF252, IRF253		$r_{DS(on)}$	— —	0.085 0.120	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 2.5 Vdc) IRF250, IRF251 (V_{DS} ≥ 3.0 Vdc) IRF252, IRF253		$I_{D(on)}$	30 25	— —	Adc
Forward Transconductance (V_{DS} ≥ 2.5 V, I_D = 16 A) IRF250, IRF251 (V_{DS} ≥ 3.0 V, I_D = 16 A) IRF252, IRF253		g_{FS}	8 8	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1200	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 95 V, I_D = 16 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	125	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	85 (Typ)	120	nC
Gate-Source Charge		Q_{gs}	45 (Typ)	—	
Gate-Drain Charge		Q_{gd}	44 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	1.8(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.2 V for IRF250 and IRF251.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF330
IRF331
IRF333

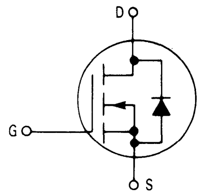
Power Field Effect Transistor

N-Channel Enhancement-Mode
Silicon Gate TMOS

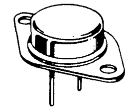
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



TMOS POWER FETs
4.5 and 5.5 AMPERES
$r_{DS(on)}$ = 1 OHM
350 and 400 VOLTS
$r_{DS(on)}$ = 1.5 OHMS
350 VOLTS



CASE 1-06
TO-204AA

MAXIMUM RATINGS

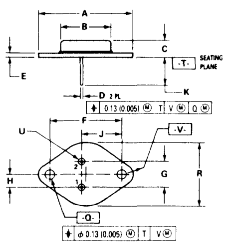
Rating	Symbol	IRF 330	IRF 331	IRF 333	Unit
Drain-Source Voltage	V_{DSS}	400	350	350	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	400	350	350	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 5.5 3.5 22		 4.5 3 18	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM5N35 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

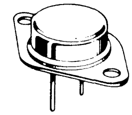
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	 IRF331, IRF333 IRF330	$V_{(BR)DSS}$	 350 400	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)	 IRF330, IRF331 IRF333	$r_{DS(on)}$	 — —	 1 1.5	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 5.5 Vdc) (V_{DS} ≥ 6.75 Vdc)	 IRF330, IRF331 IRF333	$I_{D(on)}$	 5.5 4.5	 — —	Adc
Forward Transconductance (V_{DS} ≥ 5.5 V, I_D = 3 A) (V_{DS} ≥ 6.75 V, I_D = 3 A)	 IRF330, IRF331 IRF333	g_{FS}	 3 3	 — —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	900	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 200 V, I_D = 3 Apk, R_{gen} = 15 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	35	
Turn-Off Delay Time		$t_{d(off)}$	—	55	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	18 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	1.5(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	420 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.1 V for IRF330 and IRF331.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF340

Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF340	400 V	0.55 Ω	10 A

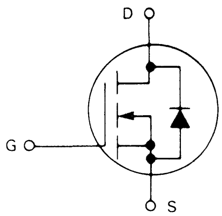


N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



MAXIMUM RATINGS

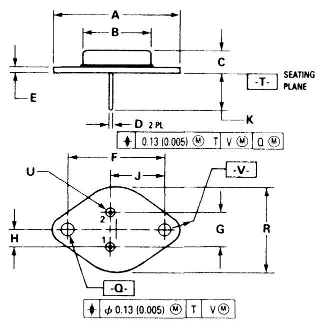
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 40	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0	 Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.0 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP10N35 are applicable for this series of products.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

3

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	400	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.25 1.00	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)		$r_{DS(on)}$	—	0.55	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 6.4 Vdc)		$I_{D(on)}$	10	—	Adc
Forward Transconductance (V_{DS} ≥ 5.5 V, I_D = 5.0 A)		g_{FS}	4.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	450	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 5.0 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	2.0	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF350
IRF351
IRF352

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

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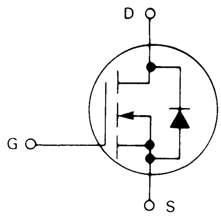
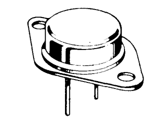
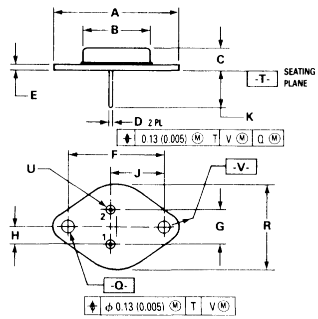
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF350	400 V	0.3 Ω	15 A
IRF351	350 V	0.3 Ω	15 A
IRF352	400 V	0.4 Ω	13 A





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	IRF 350	IRF 351	IRF 352	Unit
Drain-Source Voltage	V_{DSS}	400	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	350	400	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 15 60		 13 52	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 150 1.2			 Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTH15N35 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTH15N35 are applicable for this series of products.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF351 IRF350, IRF352	$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.25 1.00	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)	IRF350, IRF351 IRF352	$r_{DS(on)}$	— —	0.3 0.4	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 4.5 Vdc) (V_{DS} ≥ 5.2 Vdc)	IRF350, IRF351 IRF352	$I_{D(on)}$	15 13	— —	Adc
Forward Transconductance (V_{DS} ≥ 4.5 V, I_D = 8.0 A) (V_{DS} ≥ 5.2 V, I_D = 8.0 A)	IRF350, IRF351 IRF352	g_{FS}	8.0 8.0	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 8.0 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	65	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	75	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	110 (Typ)	120	nC
Gate-Source Charge		Q_{gs}	60 (Typ)	—	
Gate-Drain Charge		Q_{gd}	50 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	—	1.5(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(1) Add 0.1 V for IRF350 and IRF351.

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

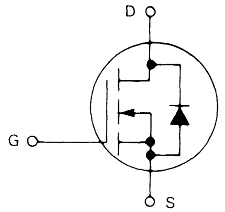
IRF440
IRF441

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

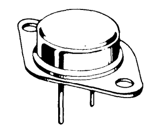
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

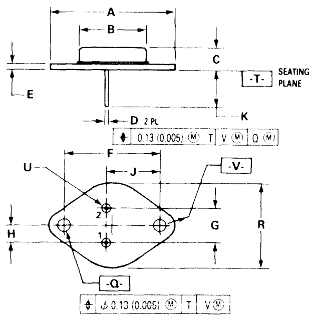
- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF440	500 V	0.85 Ω	8.0 A
IRF441	450 V	0.85 Ω	8.0 A





STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	IRF 440	IRF 441	Unit
Drain-Source Voltage	V_{DSS}	500	450	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 8.0 3.2		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0		 Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.0 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

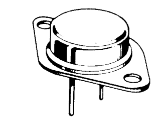
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	450	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)			—	0.25	
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1.0	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$r_{DS(on)}$	—	0.85	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 6.8 Vdc)		$I_{D(on)}$	8.0	—	Adc
Forward Transconductance (V_{DS} ≥ 6.8 V, I_D = 4.0 A)		g_{FS}	4.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 200 V, I_D = 4.0 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{GS} = 10 V, V_{DS} = 0.8 × Rated V_{DSS}, I_D = Rated I_D)	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	—	2.0	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF450
IRF451
IRF452

Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF450	500 V	0.4 Ω	13 A
IRF451	450 V	0.4 Ω	13 A
IRF452	500 V	0.5 Ω	12 A



N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
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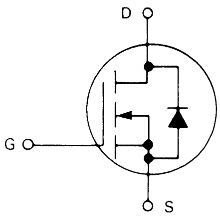
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



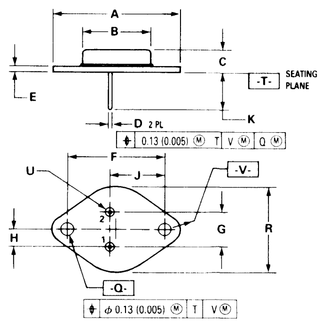
MAXIMUM RATINGS

Rating	Symbol	IRF 450	IRF 451	IRF 452	Unit
Drain-Source Voltage	V_{DSS}	500	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	450	500	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 13 52		 12 48	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 150 1.2			 Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83 30	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTH13N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristcs — are given to facilitate "worst case" design.



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE COLLECTOR

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$			Vdc
	IRF451		450	—	
	IRF450, IRF452		500	—	
Zero Gate Voltage Drain Current		I_{DSS}			mAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)			—	0.25	
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1.00	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.0 Adc)		$r_{DS(on)}$			Ohm
	IRF450, IRF451		—	0.4	
	IRF452		—	0.5	
On-State Drain Current (V_{GS} = 10 V)		$I_{D(on)}$			Adc
(V_{DS} ≥ 5.2 Vdc)	IRF450, IRF451		13	—	
(V_{DS} ≥ 6.0 Vdc)	IRF452		12	—	
Forward Transconductance		g_{FS}			mhos
(V_{DS} ≥ 5.2 V, I_D = 7.0 A)	IRF450, IRF451		6.0	—	
(V_{DS} ≥ 6.0 V, I_D = 7.0 A)	IRF452		6.0	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 200 V, I_D = 7.0 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	70	
Total Gate Charge	(V_{GS} = 10 V, V_{DS} = 0.8 × Rated V_{DSS}, I_D = Rated I_D)	Q_g	110 (Typ)	120	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	—	1.3(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(1) Add 0.1 V for IRF450 and IRF451.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF510
IRF511
IRF512
IRF513

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
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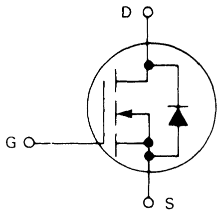
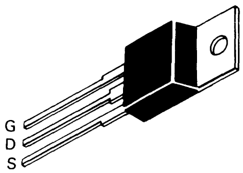
TM
TMOS



Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF510	100 V	0.6 Ω	4.0 A
IRF511	60 V	0.6 Ω	4.0 A
IRF512	100 V	0.8 Ω	3.5 A
IRF513	60 V	0.8 Ω	3.5 A

IRF510
IRF511
IRF512
IRF513



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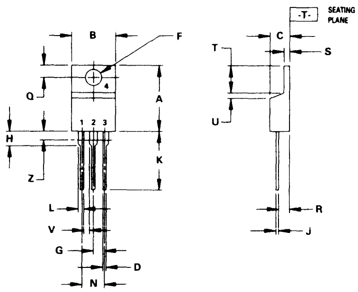
MAXIMUM RATINGS

Rating	Symbol	IRF 510	IRF 511	IRF 512	IRF 513	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	4.0	4.0	3.5	3.5	Adc
Continuous Drain Current T_C = 100°C	I_D	2.5	2.5	2.0	2.0	Adc
Drain Current Pulsed	I_{DM}	16	16	14	14	Adc
Total Power Dissipation @ T_C = 25°C	P_D	20				Watts
Derate above 25°C		0.16				W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	6.4	
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	300	°C

See the MTP6N10 Designer's Data Sheet for a complete set of design curves for this product.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) IRF510,512	$V_{(BR)DSS}$	100	—	—	Vdc
IRF511,513		60	—	—	
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS})	I_{DSS}	—	—	0.25	mAdc
(V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)		—	—	1.0	
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)	I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V) IRF510,511	$I_{D(on)}$	4.0	—	—	Adc
IRF512,513		3.5	—	—	
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 2.0 A) IRF510,511	$r_{DS(on)}$	—	—	0.6	Ohms
IRF512,513		—	—	0.8	
Forward Transconductance (V_{DS} = 15 V, I_D = 2.0 A)	g_{FS}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	150	pF
Output Capacitance	C_{oss}	—	—	100	
Reverse Transfer Capacitance	C_{rss}	—	—	25	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time (V_{DD} = 0.5 V_{DSS}, I_D = 2.0 A, Z_o = 50 Ω)	$t_{d(on)}$	—	—	20	ns
Rise Time	t_r	—	—	25	
Turn-Off Delay Time	$t_{d(off)}$	—	—	25	
Fall Time	t_f	—	—	20	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Condition	Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance	
Reverse Recovery Time		t_{rr}	230	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

	Symbol	Min	Typ	Max	Unit
Internal Drain Inductance	L_d				nH
(Measured from the contact screw on tab to center of die)		—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)		—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

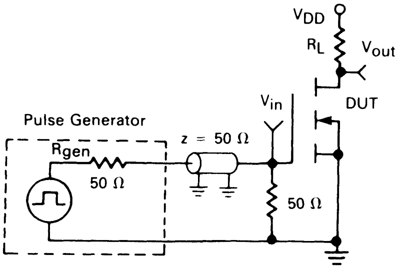
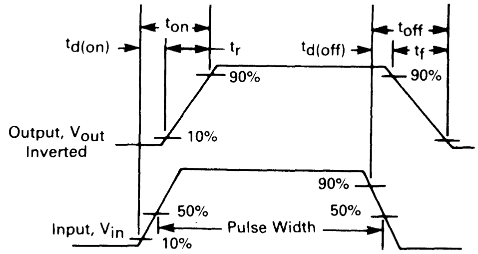


FIGURE 2 — SWITCHING WAVEFORMS



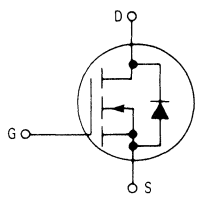
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF520
IRF521
IRF522
IRF523

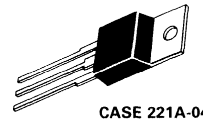
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETs
7 and 8 AMPERES
$r_{DS(on)}$ = 0.3 OHM
60 and 100 VOLTS
$r_{DS(on)}$ = 0.4 OHMS
60 and 100 VOLTS



CASE 221A-04
(TO-220AB)

MAXIMUM RATINGS

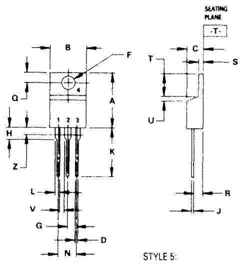
Rating	Symbol	IRF 520	IRF 521	IRF 522	IRF 523	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 8 5 32		 7 4 28		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP10N10E Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) IRF521, IRF523	$V_{(BR)DSS}$	60	—	Vdc
IRF520, IRF522		100	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc) IRF520, IRF521	$r_{DS(on)}$	—	0.3	Ohm
IRF522, IRF523		—	0.4	
On-State Drain Current (V_{GS} = 10 V) ($V_{DS} \geq$ 2.4 Vdc) IRF520, IRF521	$I_{D(on)}$	8	—	Adc
($V_{DS} \geq$ 2.8 Vdc) IRF522, IRF523		7	—	
Forward Transconductance ($V_{DS} \geq$ 2.4 V, I_D = 4 A) IRF520, IRF521	g_{FS}	1.5	—	mhos
($V_{DS} \geq$ 2.8 V, I_D = 4 A) IRF522, IRF523		1.5	—	
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	600	pF
Output Capacitance	C_{oss}	—	400	
Reverse Transfer Capacitance	C_{rss}		100	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time ($V_{DD} \approx$ 0.5 V_{DSS}, I_D = 4 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	40	ns
Rise Time	t_r	—	70	
Turn-Off Delay Time	$t_{d(off)}$	—	100	
Fall Time	t_f	—	70	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	13 (Typ)	15	nC
Gate-Source Charge	Q_{gs}	7 (Typ)	—	
Gate-Drain Charge	Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.4 (Typ)	2.3(1)	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	280 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE				
Internal Drain Inductance (Measured from the contact screw on tab to center of die)	L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.
(1) Add 0.1 V for IRF520 and IRF521.

IRF530
IRF531
IRF532
IRF533

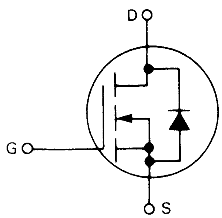
Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF530	100 V	0.18 Ω	14 A
IRF531	60 V	0.18 Ω	14 A
IRF532	100 V	0.25 Ω	12 A
IRF533	60 V	0.25 Ω	12 A

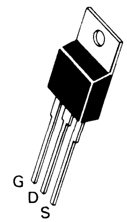
N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™





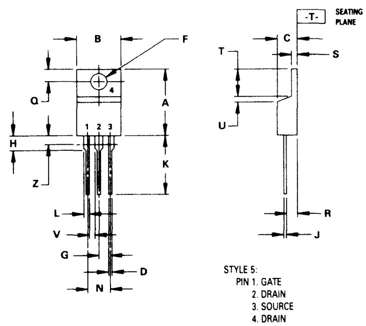
MAXIMUM RATINGS

Rating	Symbol	IRF 530	IRF 531	IRF 532	IRF 533	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C = 25°C	I_D	14	14	12	12	Adc
Continuous Drain Current T_C = 100°C	I_D	9.0	9.0	8.0	8.0	Adc
Drain Current — Pulsed	I_{DM}	56	56	48	48	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	300	°C

See the MTM12N10 Designer's Data Sheet for a complete set of design curves for this product.



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
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Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRF530,532 IRF531,533	$V_{(BR)DSS}$	100 60	— —	— —	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS}) (V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mAdc
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)		I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)		$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	IRF530,531 IRF532,533	$I_{D(on)}$	14 12	— —	— —	Adc
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 8.0 A)	IRF530,531 IRF532,533	$r_{DS(on)}$	— —	— —	0.18 0.25	Ohm
Forward Transconductance (V_{DS} = 15 V, I_D = 8.0 A)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	800	pF
Output Capacitance		C_{oss}	—	—	500	
Reverse Transfer Capacitance		C_{rss}	—	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time	V_{DD} = 36 V, I_D = 8.0 A Z_o = 15 Ω	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	75	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		t_f	—	—	45	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance	
Reverse Recovery Time		t_{rr}	360	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

	Symbol	Min	Typ	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

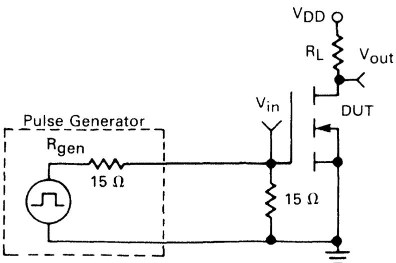
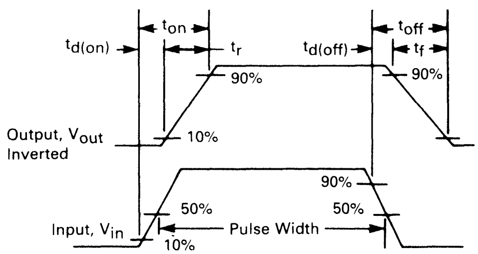


FIGURE 2 — SWITCHING WAVEFORMS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF540
IRF541
IRF542

Power Field Effect Transistor

N-Channel Enhancement-Mode
Silicon Gate TMOS

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- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
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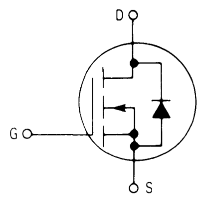
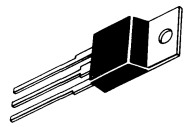


TMOS POWER FETs
24 and 27 AMPERES
$r_{DS(on)}$ = 0.085 OHM
60 and 100 VOLTS
$r_{DS(on)}$ = 0.11 OHMS
100 VOLTS



CASE 221A-04
(TO-220AB)

MAXIMUM RATINGS

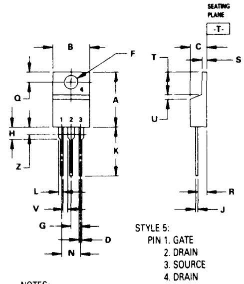
Rating	Symbol	IRF 540	IRF 541	IRF 542	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	100	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 27 17 108		 24 15 96	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP25N10 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		IRF540, IRF542 IRF541	$V_{(BR)DSS}$	100 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)			I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)			I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)			$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		IRF540, IRF541 IRF542	$r_{DS(on)}$	— —	0.085 0.11	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 2.3 Vdc) (V_{DS} ≥ 2.6 Vdc)		IRF540, IRF541 IRF542	$I_{D(on)}$	27 24	— —	Adc
Forward Transconductance (V_{DS} ≥ 2.3 V, I_D = 15 A) (V_{DS} ≥ 2.6 V, I_D = 15 A)		IRF540, IRF541 IRF542	g_{FS}	6.0 6.0	— —	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	1600	pF
Output Capacitance			C_{oss}	—	800	
Reverse Transfer Capacitance			C_{rss}	—	300	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} ≈ 30 V, I_D = 15 Apk, R_{gen} = 4.7 Ohms)		$t_{d(on)}$	—	30	ns
Rise Time			t_r	—	60	
Turn-Off Delay Time			$t_{d(off)}$	—	80	
Fall Time			t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)		Q_g	40 (Typ)	60	nC
Gate-Source Charge			Q_{gs}	17 (Typ)	—	
Gate-Drain Charge			Q_{gd}	23 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)		V_{SD}	1.5 (Typ)	2.3(1)	Vdc
Forward Turn-On Time			t_{on}	Limited by stray inductance		
Reverse Recovery Time			t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)			L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)			L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(1) Add 0.1 V for IRF540 and IRF541.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF610
IRF612

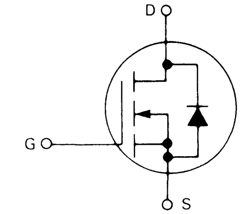
Part Number	V_{DS}	$r_{DS(on)}$	I_D
IRF610	200 V	1.5 Ω	2.5 A
IRF612	200 V	2.4 Ω	2.0 A

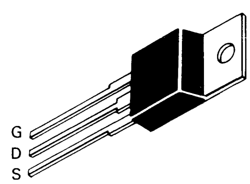
N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TM
TMOS





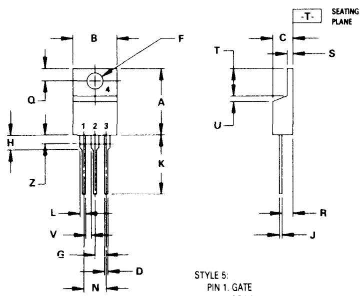
MAXIMUM RATINGS

Rating	Symbol	IRF 610	IRF 612	Unit
Drain-Source Voltage	V_{DSS}	200	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	200	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Continuous Drain Current T_C = 25°C	I_D	2.5	2.0	Adc
Continuous Drain Current T_C = 100°C	I_D	1.5	1.25	Adc
Drain Current — Pulsed	I_{DM}	10	8.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 6.4 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	300	°C

See the MTP2N20 Designer's Data Sheet for a complete set of design curves for this product.



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	$V_{(BR)DSS}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0 V, V_{DS} = Rated V_{DSS}) (V_{GS} = 0 V, V_{DS} = 0.8 Rated V_{DSS}, T_C = 125°C)	I_{DSS}	— —	— —	0.25 1.0	mAdc
Forward Gate-Body Leakage Current (V_{GS} = 20 V, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Reverse Gate-Body Leakage Current (V_{GS} = −20 V, V_{DS} = 0)	I_{GSSR}	—	—	−100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	2.0	—	4.0	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V) IRF610 IRF612	$I_{D(on)}$	2.5 2.0	— —	— —	Adc
Static Drain-Source On-Resistance (V_{GS} = 10 V, I_D = 1.25 A) IRF610 IRF612	$r_{DS(on)}$	— —	— —	1.5 2.4	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.25 A)	g_{FS}	0.8	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	150	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	—	80	
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	—	25	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time (V_{DD} ≈ 0.5 V_{DSS}, I_D = 1.25 A, Z_o = 50 Ω)	$t_{d(on)}$	—	—	15	ns
Rise Time (V_{DD} ≈ 0.5 V_{DSS}, I_D = 1.25 A, Z_o = 50 Ω)	t_r	—	—	25	
Turn-Off Delay Time (V_{DD} ≈ 0.5 V_{DSS}, I_D = 1.25 A, Z_o = 50 Ω)	$t_{d(off)}$	—	—	15	
Fall Time (V_{DD} ≈ 0.5 V_{DSS}, I_D = 1.25 A, Z_o = 50 Ω)	t_f	—	—	15	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Typ	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8	Vdc
Forward Turn-On Time	(I_S = Rated I_D, V_{GS} = 0)	t_{on}	Limited by stray inductance	
Reverse Recovery Time	(I_S = Rated I_D, V_{GS} = 0)	t_{rr}	290	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

	Symbol	Min	Typ	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	—	7.5	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0 %.

FIGURE 1 — SWITCHING TEST CIRCUIT

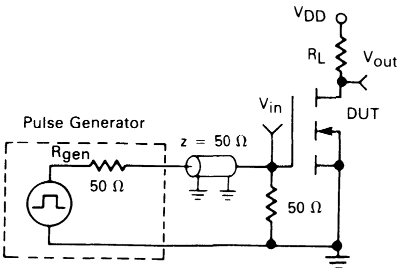
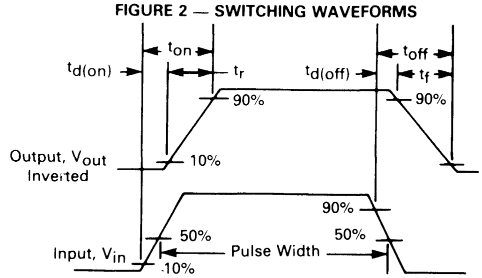


FIGURE 2 — SWITCHING WAVEFORMS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

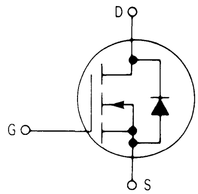
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

IRF620
IRF621

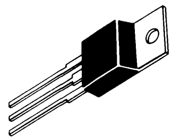
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETs
4 and 5 AMPERES
$r_{DS(on)}$ = 0.8 OHM
150 and 200 VOLTS

3



CASE 221A-04
(TO-220AB)

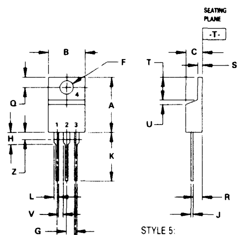
MAXIMUM RATINGS

Rating	Symbol	IRF 620	IRF 621	Unit
Drain-Source Voltage	V_{DSS}	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 5 3 20		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) IRF620 IRF621		$V_{(BR)DSS}$	200 150	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	0.8	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 4 Vdc)		$I_{D(on)}$	5	—	Adc
Forward Transconductance (V_{DS} ≥ 4 V, I_D = 2.5 A)		g_{FS}	1.3	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 0.5 Rated V_{DSS}, I_D = 2.5 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	11 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.7 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF630 IRF631 IRF632

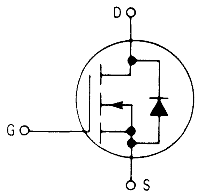
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

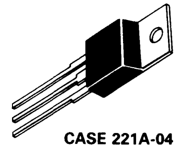
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



TMOS POWER FETs
8 and 9 AMPERES
$r_{DS(on)}$ = 0.4 OHM
150 and 200 VOLTS
$r_{DS(on)}$ = 0.6 OHMS
200 VOLTS



CASE 221A-04
(TO-220AB)

3

MAXIMUM RATINGS

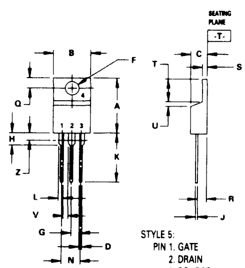
Rating	Symbol	IRF 630	IRF 631	IRF 632	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	200	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 9 6 36		 8 5 32	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6			Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM8N20 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTM8N20 are applicable for this series of product.

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF630, IRF632 IRF631	$V_{(BR)DSS}$	200 150	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)	IRF630, IRF631 IRF632	$r_{DS(on)}$	— —	0.4 0.6	Ohm
On-State Drain Current (V_{GS} = 10 V) ($V_{DS} \geq$ 3.6 Vdc) ($V_{DS} \geq$ 4.8 Vdc)	IRF630, IRF631 IRF632	$I_{D(on)}$	9 8	— —	Adc
Forward Transconductance ($V_{DS} \geq$ 3.6 V, I_D = 5 A) ($V_{DS} \geq$ 4.8 V, I_D = 5 A)	IRF630, IRF631 IRF632	g_{FS}	3 3	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	450	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	($V_{DD} \approx$ 90 V, I_D = 5 Apk, R_{gen} = 15 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	40	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	15 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.7 (Typ)	1.8(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2.0%.
(1) Add 0.1 V for IRF630.

3

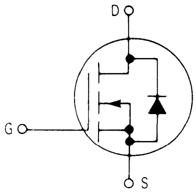
IRF640 IRF641 IRF642 IRF643

Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate TMOS

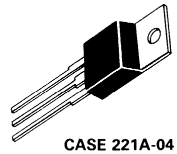
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



TMOS POWER FETs
16 and 18 AMPERES
$r_{DS(on)}$ = 0.18 OHM
150 and 200 VOLTS
$r_{DS(on)}$ = 0.22 OHMS
150 and 200 VOLTS



CASE 221A-04
(TO-220AB)

3

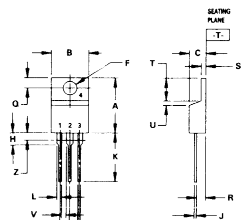
MAXIMUM RATINGS

Rating	Symbol	IRF 640	IRF 641	IRF 642	IRF 643	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 18 11 72		 16 10 64		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

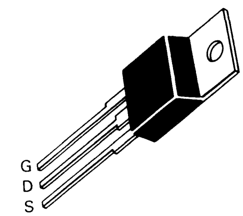
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF640, IRF642 IRF641, IRF643	$V_{(BR)DSS}$	200 150	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)	IRF640, IRF641 IRF642, IRF643	$r_{DS(on)}$	— —	0.18 0.22	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 3.2 Vdc) (V_{DS} ≥ 3.5 Vdc)	IRF640, IRF641 IRF642, IRF643	$I_{D(on)}$	18 16	— —	Adc
Forward Transconductance (V_{DS} ≥ 3.2 V, I_D = 10 A) (V_{DS} ≥ 3.5 V, I_D = 10 A)	IRF640, IRF641 IRF642, IRF643	g_{FS}	6 6	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	750	
Reverse Transfer Capacitance		C_{rss}	—	300	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 75 V, I_D = 10 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	38 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	16 (Typ)	—	
Gate-Drain Charge		Q_{gd}	22 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8 (Typ)	1.9(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(1) Add 0.1 V for IRF640 and IRF641.

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

IRF710

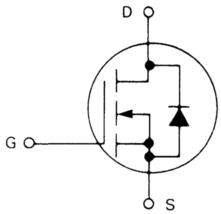
Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF710	400 V	3.6 Ω	1.5 A



N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

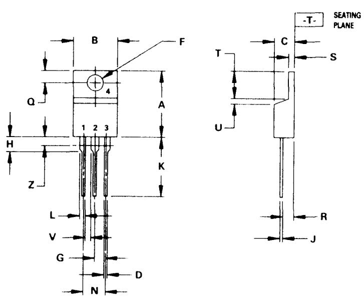


MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate-Source Voltage	V_{GS}	± 20	Vdc
Drain Current			Adc
Continuous	I_D	1.5	
Pulsed	I_{DM}	6.0	
Total Power Dissipation	P_D		
@ T_C = 25°C		20	Watts
Derate above 25°C		0.16	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	− 55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	6.4	
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	300	°C



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

Design curves of the MTP2N35 are applicable for this series of products.
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	400	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}			mAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	0.25	
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	1.00	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.8 Adc)	$r_{DS(on)}$	—	3.6	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 5.4 Vdc)	$I_{D(on)}$	1.5	—	Adc
Forward Transconductance (V_{DS} ≥ 5.4 V, I_D = 0.8 A)	g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	150	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	50	
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	15	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} = 0.5 V_{DSS}, I_D = 0.8 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	10	ns
Rise Time (V_{DD} = 0.5 V_{DSS}, I_D = 0.8 Apk, R_{gen} = 50 Ohms)	t_r	—	20	
Turn-Off Delay Time (V_{DD} = 0.5 V_{DSS}, I_D = 0.8 Apk, R_{gen} = 50 Ohms)	$t_{d(off)}$	—	10	
Fall Time (V_{DD} = 0.5 V_{DSS}, I_D = 0.8 Apk, R_{gen} = 50 Ohms)	t_f	—	15	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = 2.0 A)	Q_g	6.0 (Typ)	7.5	nC
Gate-Source Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = 2.0 A)	Q_{gs}	3.0 (Typ)	—	
Gate-Drain Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = 2.0 A)	Q_{gd}	3.0 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = 2.0 A, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.6	Vdc
Forward Turn-On Time (I_S = 2.0 A, V_{GS} = 0)	t_{on}	Limited by stray inductance		
Reverse Recovery Time (I_S = 2.0 A, V_{GS} = 0)	t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE				
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on the tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead, 0.25″ from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

IRF720 IRF722

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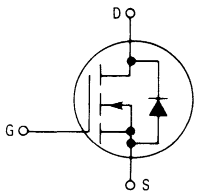
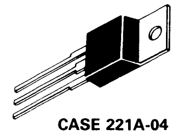
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



TMOS POWER FETs
2.5 and 3 AMPERES
$r_{DS(on)}$ = 1.8 OHM
400 VOLTS
$r_{DS(on)}$ = 2.5 OHM
400 VOLTS



CASE 221A-04
(TO-220AB)

3

MAXIMUM RATINGS

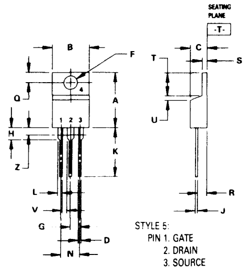
Rating	Symbol	IRF 720	IRF 722	Unit
Drain-Source Voltage	V_{DSS}	400	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	400	400	Vdc
Drain Current				Adc
Continuous	I_D	3	2.5	
Pulsed	I_{DM}	12	10	
Total Power Dissipation @ T_C = 25°C	P_D	40		Watts
Derate above 25°C		0.32		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	3.12	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP3N40 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
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J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	400	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.25 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	IRF720 IRF722	$r_{DS(on)}$	— —	1.8 2.5	Ohm
On-State Drain Current (V_{GS} = 10 V) ($V_{DS} \geq$ 5.4 Vdc) ($V_{DS} \geq$ 6.25 Vdc)	IRF720 IRF722	$I_{D(on)}$	3 2.5	— —	Adc
Forward Transconductance ($V_{DS} \geq$ 5.4 V, I_D = 1.5 A) ($V_{DS} \geq$ 6.25 V, I_D = 1.5 A)	IRF720 IRF722	g_{FS}	1 1	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	200	
Reverse Transfer Capacitance		C_{rss}	—	40	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	($V_{DD} \approx$ 200 V, I_D = 1.5 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	12 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq$ 300 μs, Duty Cycle $\leq$ 2%.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF730
IRF731
IRF732
IRF733

Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

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- Silicon Gate for Fast Switching Speeds
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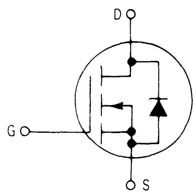
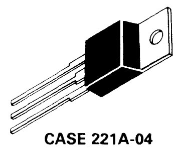


TMOS POWER FETs
4.5 and 5.5 AMPERES
$r_{DS(on)}$ = 1 OHM
350 and 400 VOLTS
$r_{DS(on)}$ = 1.5 OHM
350 and 400 VOLTS



CASE 221A-04
(TO-220AB)

3

MAXIMUM RATINGS

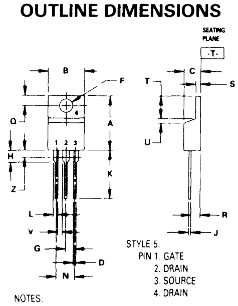
Rating	Symbol	IRF 730	IRF 731	IRF 732	IRF 733	Unit
Drain-Source Voltage	V_{DSS}	400	350	400	350	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	400	350	400	350	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 5.5 3.5 22		 4.5 3 18		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM5N35 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	 IRF731, IRF733 IRF730, IRF732	$V_{(BR)DSS}$	 350 400	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)	 IRF730, IRF731 IRF732, IRF733	$r_{DS(on)}$	 — —	 1 1.5	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 5.5 Vdc) (V_{DS} ≥ 6.75 Vdc)	 IRF730, IRF731 IRF732, IRF733	$I_{D(on)}$	 5.5 4.5	 — —	Adc
Forward Transconductance (V_{DS} ≥ 5.5 V, I_D = 3 A) (V_{DS} ≥ 6.75 V, I_D = 3 A)	 IRF730, IRF731 IRF732, IRF733	g_{FS}	 3 3	 — —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}		80	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 200 V, I_D = 3 Apk, R_{gen} = 15 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	35	
Turn-Off Delay Time		$t_{d(off)}$	—	55	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	18 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	1.5(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	420 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1)Add 0.1 V for IRF730 and IRF731.

IRF740
IRF741

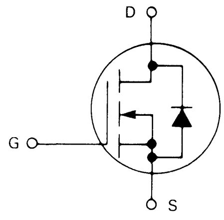
Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF740	400 V	0.55 Ω	10 A
IRF741	350 V	0.55 Ω	10 A

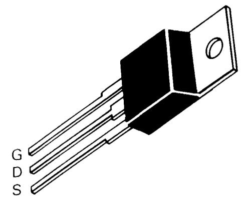
N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS





MAXIMUM RATINGS

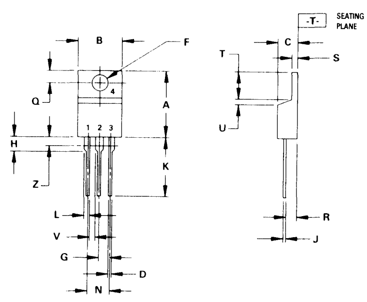
Rating	Symbol	IRF 740	IRF 741	Unit
Drain-Source Voltage	V_{DSS}	400	350	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	350	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 40		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0		 Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.0 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	275	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP10N35 are applicable for this series of products.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF741 IRF740	$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.25 1.0	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$r_{DS(on)}$	—	0.55	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 5.5 Vdc)		$I_{D(on)}$	10	—	Adc
Forward Transconductance (V_{DS} ≥ 5.5 V, I_D = 5.0 A)		g_{FS}	4.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	450	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 5.0 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	2.0	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead, 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

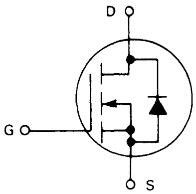
IRF820
IRF821
IRF823

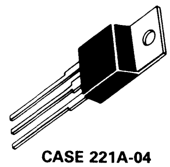
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

TMOS POWER FETs
2 and 2.5 AMPERES
$r_{DS(on)}$ = 3 OHM
450 and 500 VOLTS
$r_{DS(on)}$ = 4 OHM
450 VOLTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

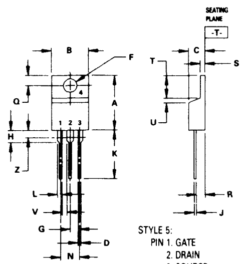
Rating	Symbol	IRF 820	IRF 821	IRF 823	Unit
Drain-Source Voltage	V_{DSS}	500	450	450	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	500	450	450	Vdc
Gate-Source Voltage	V_{GS}	±20			Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	2.5 10		2 8	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32			Adc
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150			°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 3.12 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP3N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Condition / Type	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF821, IRF823	$V_{(BR)DSS}$	450	—	Vdc
	IRF820		500	—	
Zero Gate Voltage Drain Current	(V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	0.25	mAdc
	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)	IRF820, IRF821	$r_{DS(on)}$	—	3	Ohm
	IRF823		—	4	
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 7.5 Vdc)	IRF820, IRF821	$I_{D(on)}$	2.5	—	Adc
(V_{DS} ≥ 8 Vdc)	IRF823		2	—	
Forward Transconductance (V_{DS} ≥ 7.5 V, I_D = 1 A)	IRF820, IRF821	g_{FS}	1	—	mhos
(V_{DS} ≥ 8 V, I_D = 1 A)	IRF823		1	—	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f= 1 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	40	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	V_{DD} ≈ 200 V, I_D = 1 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	60	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{GS} = 10 V, V_{DS} = 0.8 x Rated V_{DSS}, I_D = Rated I_D)	Q_g	12 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	—	1.5(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance	(Measured from the contact screw on tab to center of die)	L_d	3.5 (Typ)	—	nH
	(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance	(Measured from the source lead 0.25″ from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.1 V for IRF820 and IRF821.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

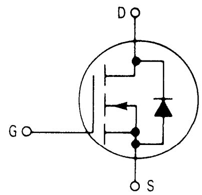
IRF830
IRF831
IRF832
IRF833

Power Field Effect Transistor
N-Channel Enhancement Mode
Silicon Gate TMOS

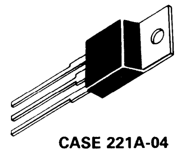
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



TMOS POWER FETs
4 and 4.5 AMPERES
$r_{DS(on)}$ = 1.5 OHMS
450 and 500 VOLTS
$r_{DS(on)}$ = 2 OHMS
450 and 500 VOLTS



CASE 221A-04
(TO-220AB)

MAXIMUM RATINGS

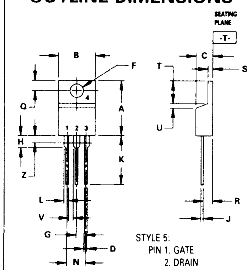
Rating	Symbol	IRF 830	IRF 831	IRF 832	IRF 833	Unit
Drain-Source Voltage	V_{DSS}	500	450	500	450	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Drain Current Continuous, T_C = 25°C T_C = 100°C Peak, T_C = 25°C	I_D	 4.5 3 18		 4 2.5 16		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTM4N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet. Design curves of the MTP4N45 are applicable for this series of product.

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

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F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF831, IRF833 IRF830, IRF832	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	IRF830, IRF831 IRF832, IRF833	$r_{DS(on)}$	— —	1.5 2	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 6.75 Vdc) (V_{DS} ≥ 8 Vdc)	IRF830, IRF831 IRF832, IRF833	$I_{D(on)}$	4.5 4	— —	Adc
Forward Transconductance (V_{DS} ≥ 6.75 V, I_D = 2.5 A) (V_{DS} ≥ 8 V, I_D = 2.5 A)	IRF830, IRF831 IRF832, IRF833	g_{FS}	2.5 2.5	— —	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	200	
Reverse Transfer Capacitance		C_{rss}	—	60	

SWITCHING CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} ≈ 200 V, I_D = 2.5 Apk, R_{gen} = 15 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	30	
Turn-Off Delay Time		$t_{d(off)}$	—	55	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	22 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	12 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

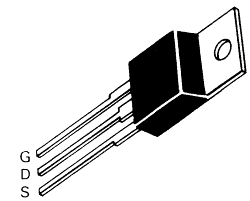
Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.1 V for IRF830 and IRF831.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRF840
IRF841
IRF842
IRF843

Part Number	V_{DSS}	$r_{DS(on)}$	I_D
IRF840	500 V	0.85 Ω	8.0 A
IRF841	450 V	0.85 Ω	8.0 A
IRF842	500 V	1.10 Ω	7.0 A
IRF843	450 V	1.10 Ω	7.0 A

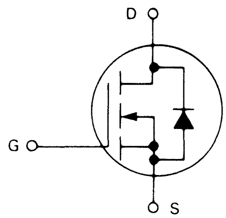


N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™



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MAXIMUM RATINGS

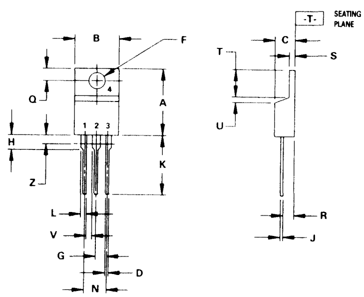
Rating	Symbol	IRF 840	IRF 841	IRF 842	IRF 843	Unit
Drain-Source Voltage	V_{DSS}	500	450	500	450	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	450	500	450	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 8.0 32		 7.0 28		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 125 1.0				 Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.0 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	275	°C

See the MTP8N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	IRF841, IRF843	$V_{(BR)DSS}$	450	—	Vdc
	IRF840, IRF842		500	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.25	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1.00	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	IRF840, IRF841	$r_{DS(on)}$	—	0.85	Ohm
	IRF842, IRF843		—	1.0	
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 6.8 Vdc)	IRF840, IRF841	$I_{D(on)}$	8.0	—	Adc
(V_{DS} ≥ 7.0 Vdc)	IRF842, IRF843		7.0	—	
Forward Transconductance (V_{DS} ≥ 6.8 V, I_D = 4.0 A)	IRF840, IRF841	g_{FS}	4.0	—	mhos
(V_{DS} ≥ 7.0 V, I_D = 4.0 A)	IRF842, IRF843		4.0	—	

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	

SWITCHING CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} ≈ 200 V, I_D = 4.0 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	35	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{GS} = 10 V, V_{DS} = 0.8 × Rated V_{DSS}, I_D = Rated I_D)	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	—	1.9 (1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die)	L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(1) Add 0.1 V for IRF840 and IRF841.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Power Field Effect Transistors

P-Channel Enhancement-Mode Silicon Gate TMOS

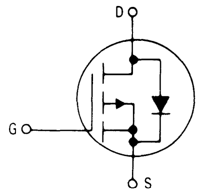
IRF9630

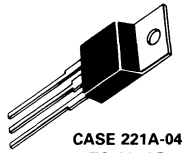
This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TM
TMOS

TMOS POWER FET
6.5 AMPERES
$r_{DS(on)}$ = 0.8 OHM
200 VOLTS





G
D
S

CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Pulsed @ T_C = 25°C	I_D I_{DM}	6.5 4 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP7P20 Data Sheet for a complete set of design curves.

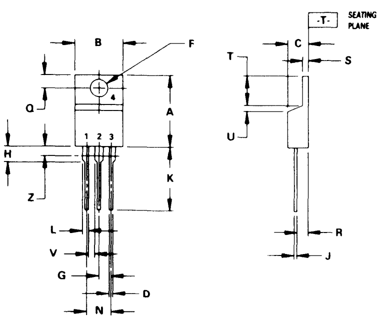
TMOS is a trademark of Motorola Inc.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	250	μAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1000	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$r_{DS(on)}$	—	0.8	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 5.2 Vdc)		$I_{D(on)}$	6.5	—	Adc
Forward Transconductance (V_{DS} ≥ 5.2 V, I_D = 3.5 A)		g_{FS}	2.2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	650	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	90	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 100 V, I_D = 3.5 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	80	
Total Gate Charge	(V_{DS} = 160 V, V_{GS} = 15 Vdc, I_D = 8 A)	Q_g	31 (Typ)	45	nC
Gate-Source Charge		Q_{gs}	18 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 6.5 A, V_{GS} = 0)	V_{SD}	3.5 (Typ)	6.5 V	Vdc
Forward Turn-On Time	(I_S = 6.5 A, dI_S/dt = 100 A/μs, V_R = 50 V, V_{GS} = 0)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	400 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Power Field Effect Transistors

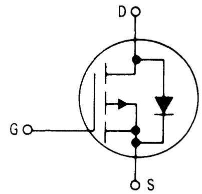
P-Channel Enhancement-Mode Silicon Gate TMOS

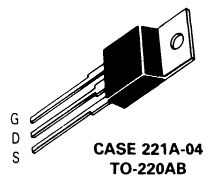
IRF9640

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FET
11 AMPERES
$r_{DS(on)}$ = 0.5 OHM
200 VOLTS
$r_{DS(on)}$ = 0.035 OHM





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Pulsed @ T_C = 25°C	I_D I_{DM}	11 7 44	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP12P20 Data Sheet for a complete set of design curves.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.5	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 25 Vdc)	$I_{D(on)}$	11	—	Adc
Forward Transconductance (V_{DS} ≥ 5.5 V, I_D = 6 A)	g_{FS}	4	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1300	pF
Output Capacitance		C_{oss}	—	450	
Reverse Transfer Capacitance		C_{rss}	—	250	

SWITCHING CHARACTERISTICS*

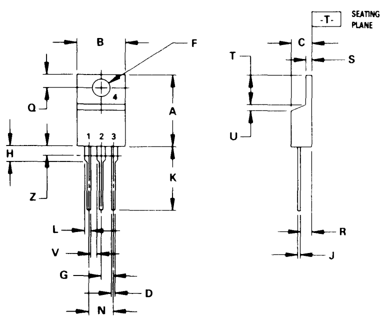
Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} ≈ 100 V, I_D = 6 Apk, R_{gen} = 4.7 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	18	
Fall Time		t_f	—	12	
Total Gate Charge	(V_{DS} = 160 V, V_{GS} = 15 Vdc, I_D = 22 A)	Q_g	70 (Typ)	90	nC
Gate-Source Charge		Q_{gs}	55 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = 11 A, V_{GS} = 0)	V_{SD}	2.7 (Typ)	4.6	Vdc
Forward Turn-On Time	(I_S = 11 A, V_{GS} = 0 dI_S/dt = 100 A/μs, V_R = 50 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	270 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



NOTES:
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2. CONTROLLING DIMENSION: INCH.
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STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFD1Z0
IRFD1Z3

Advance Information

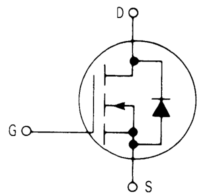
Small-Signal TMOS Field Effect Transistor

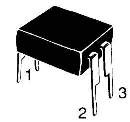
N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

1 WATT
TMOS FETs
$r_{DS(on)}$ = 0.8 OHM
60 VOLTS
$r_{DS(on)}$ = 0.6 OHM
100 VOLTS

These TMOS FETs are designed for low voltage, high speed switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertation
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged — SOA is Power Dissipation Limited





CASE 370-01

MAXIMUM RATINGS

Rating	Symbol	IRFD1Z0	IRFD1Z3	Unit
Drain-Source Voltage	V_{DSS}	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous T_C = 25°C Pulsed	 I_D I_{DM}	 0.5 4	 0.4 3.2	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1 8		 Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient (Free Air Operation)	$R_{\theta JA}$	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRFD1Z0 IRFD1Z3	$V_{(BR)DSS}$	100 60	— —	— —	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0 V)		I_{DSS}	—	—	250	μAdc
Gate-Body Leakage Current, Foward (V_{GSF} = 20 V)		I_{GSSF}	—	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 V)		I_{GSSR}	—	—	500	nAdc

(continued)

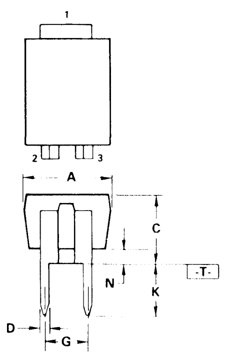
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

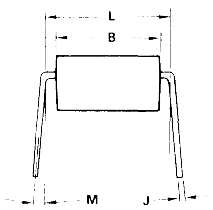
Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 250 μA, V_{DS} = V_{GS})		$V_{GS(th)}$	2	—	4	Vdc
Static Drain-Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 0.25 A)	IRFD1Z0 IRFD1Z3	$r_{DS(on)}$	— —	— —	2.4 3.2	Ohms
On-State Drain Current(1) (V_{GS} = 10 V, V_{DS} = 5 V)	IRFD1Z0 IRFD1Z3	$I_{D(on)}$	0.5 0.4	— —	— —	Adc
Forward Transconductance(1) (I_D = 0.25 A, V_{DS} = 5 V)		g_{fs}	0.25	—	—	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	—	70	pF
Output Capacitance		C_{oss}	—	—	30	
Reverse Transfer Capacitance		C_{rss}	—	—	10	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 0.5 $V_{(BR)DSS}$ I_D = 0.25 A, Z_o = 50 Ω)	$t_{d(on)}$	—	—	20	ns
Rise Time		t_r	—	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	—	25	
Fall Time		t_f	—	—	20	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)(1)	I_S = 0.5 A, IRFD1Z0 I_S = 0.4 A, IRFD1Z3	V_F	— —	— —	1.4 1.3	Vdc
Continuous Source Current, Body Diode	IRFD1Z0 IRFD1Z3	I_S	— —	— —	0.5 0.4	Adc
Pulsed Source Current, Body Diode	IRFD1Z0 IRFD1Z3	I_{SM}	— —	— —	4 3.2	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	negligible			ns
Reverse Recovery Time		t_{rr}	—	100	—	

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE



NOTES:
1. SURFACE "T" IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS: D DIM 4 PL
⌖ 0.27 (.010) Ⓜ -T- A Ⓜ
LEADS; J DIM 4 PL
⌖ 0.27 (0.010) Ⓜ -T- B Ⓜ
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.
5. DIMENSION "J" PRIOR TO SOLDER DIP PLATING.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.70	5.02	0.185	0.198
B	6.10	7.11	0.240	0.280
C	4.06	5.08	0.160	0.200
D	0.38	0.63	0.015	0.025
G	2.54 BSC		0.100 BSC	
J	0.30	0.43	0.012	0.017
K	2.79	3.81	0.110	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.77	0.020	0.070

CASE 370-01

IRFD110
IRFD113

Advance Information

Small-Signal TMOS Field Effect Transistor

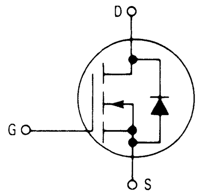
N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

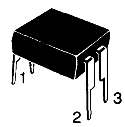
TMOS

1 WATT
TMOS FETs
$r_{DS(on)}$ = 0.8 OHM
60 VOLTS
$r_{DS(on)}$ = 0.6 OHM
100 VOLTS

These TMOS FETs are designed for low voltage, high speed power switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertation
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged — SOA is Power Dissipation Limited





CASE 370-01

3

MAXIMUM RATINGS

Rating	Symbol	IRFD110	IRFD113	Unit
Drain-Source Voltage	V_{DSS}	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous T_C = 25°C Pulsed	 I_D I_{DM}	 1 8	 0.8 6.4	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1 8		Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRFD110 IRFD113	$V_{(BR)DSS}$	100 60	— —	— —	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0 V)		I_{DSS}	—	—	250	μAdc
Gate-Body Leakage Current, Foward (V_{GSF} = 20 V)		I_{GSSF}	—	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = −20 V)		I_{GSSR}	—	—	−500	nAdc

(continued)

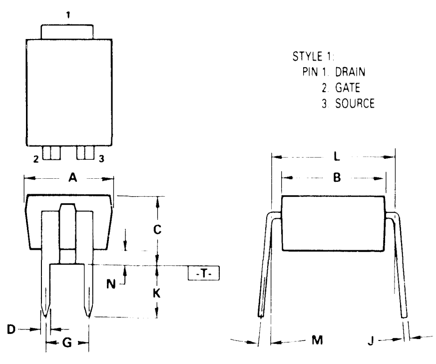
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — Continued ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage ($I_D = 250\ \mu A$, $V_{DS} = V_{GS}$)		$V_{GS(th)}$	2	—	4	Vdc
Static Drain-Source On-Resistance[1] ($V_{GS} = 10$ Vdc, $I_D = 0.8$ A)	IRFD110 IRFD113	$r_{DS(on)}$	— —	— —	0.6 0.8	Ohms
On-State Drain Current[1] ($V_{GS} = 10$ V, $V_{DS} = 5$ V)	IRFD110 IRFD113	$I_{D(on)}$	1 0.8	— —	— —	Adc
Forward Transconductance[1] ($I_D = 0.8$ A, $V_{DS} = 5$ V)		g_{fs}	0.8	—	—	mhos
CAPACITANCE						
Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, f = 1 MHz)	C_{iss}	—	—	200	pF
Output Capacitance		C_{oss}	—	—	100	
Reverse Transfer Capacitance		C_{rss}	—	—	25	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	($V_{DS} = 0.5\ V_{(BR)DSS}$, $I_D = 0.8$ A, $Z_o = 50\ \Omega$)	$t_{d(on)}$	—	—	20	ns
Rise Time		t_r	—	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	—	25	
Fall Time		t_f	—	—	20	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage ($V_{GS} = 0$)	$I_S = 1$ A, IRFD110 $I_S = 0.8$ A, IRFD113	V_F	— —	— —	2.5 2	Vdc
Continuous Source Current, Body Diode	IRFD110 IRFD113	I_S	— —	— —	1 0.8	Adc
Pulsed Source Current, Body Diode	IRFD110 IRFD113	I_{SM}	— —	— —	8 6.4	A
Forward Turn-On Time	(I_S = Rated I_S, $V_{GS} = 0$)	t_{on}	negligible			ns
Reverse Recovery Time		t_{rr}	—	100	—	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.70	5.02	0.185	0.198
B	6.10	7.11	0.240	0.280
C	4.06	5.08	0.160	0.200
D	0.38	0.63	0.015	0.025
G	2.54 BSC		0.100 BSC	
J	0.30	0.43	0.012	0.017
K	2.79	3.81	0.110	0.150
L	7.62 BSC		0.300 BSC	
M	0	15	0	15
N	0.51	1.77	0.020	0.070

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS; D DIM 4 PL
   | ⌖ | 0.27 (.010) Ⓜ | -T- | A Ⓜ |
   LEADS; J DIM 4 PL
   | ⌖ | 0.27 (0.010) Ⓜ | -T- | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH
5. DIMENSION "J" PRIOR TO SOLDER DIP PLATING

CASE 370-01

IRFD120
IRFD121
IRFD122
IRFD123

Advance Information

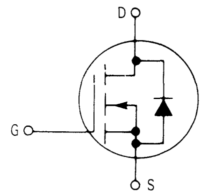
Small-Signal TMOS Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

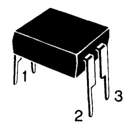
These TMOS FETs are designed for low voltage, high speed power switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertion
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged — SOA is Power Dissipation Limited

TMOS



1 WATT
TMOS FETs
$r_{DS(on)}$ = 0.3 OHM
100 VOLTS
$r_{DS(on)}$ = 0.4 OHM
60 VOLTS



CASE 370-01

3

MAXIMUM RATINGS

Rating	Symbol	IRFD120	IRFD121	IRFD122	IRFD123	Unit
Drain-Source Voltage	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous T_C = 25°C Pulsed	 I_D I_{DM}	 1.3 5.2		 1.1 4.4		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1 8				 Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Ambient	$R_{\theta JA}$	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) IRFD120, IRFD122 IRFD121, IRFD123	$V_{(BR)DSS}$	 100 60	 — —	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0 V)	I_{DSS}	—	—	250	μAdc
Gate-Body Leakage Current, Foward (V_{GSF} = 20 V)	I_{GSSF}	—	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = −20 V)	I_{GSSR}	—	—	−500	nAdc

(continued)

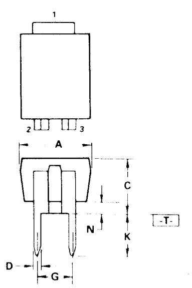
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

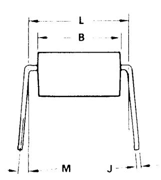
Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 250 μA, V_{DS} = V_{GS})		$V_{GS(th)}$	2	—	4	Vdc
Static Drain-Source On-Resistance[1] (V_{GS} = 10 Vdc, I_D = 0.6 A)	IRFD120, IRFD121 IRFD122, IRFD123	$r_{DS(on)}$	— —	— —	0.3 0.4	Ohms
On-State Drain Current[1] (V_{GS} = 10 V, V_{DS} = 5 V)	IRFD120, IRFD121 IRFD122, IRFD123	$I_{D(on)}$	1.3 1.1	— —	— —	Adc
Forward Transconductance[1] (I_D = 0.6 A, V_{DS} = 5 V)		g_{fs}	0.9	—	—	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	—	600	pF
Output Capacitance		C_{oss}	—	—	400	
Reverse Transfer Capacitance		C_{rss}	—	—	100	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 0.5 $V_{(BR)DSS}$, I_D = 0.6 A, Z_o = 50 Ω)	$t_{d(on)}$	—	—	40	ns
Rise Time		t_r	—	—	70	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	70	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)	I_S = 1.3 A, IRFD120, IRFD121 I_S = 1.1 A, IRFD122, IRFD123	V_{SD}	— —	— —	2.5 2.3	Vdc
Continuous Source Current, Body Diode	IRFD120, IRFD121 IRFD122, IRFD123	I_S	— —	— —	1.3 1.1	Adc
Pulsed Source Current, Body Diode	IRFD120, IRFD121 IRFD122, IRFD123	I_{SM}	— —	— —	5.2 4.4	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	negligible			ns
Reverse Recovery Time		t_{rr}	—	280	—	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



STYLE 1
PIN 1 DRAIN
2 GATE
3 SOURCE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.70	5.02	0.185	0.198
B	6.10	7.11	0.240	0.280
C	4.06	5.08	0.160	0.200
D	0.38	0.63	0.015	0.025
G	2.54 BSC		0.100 BSC	
J	0.30	0.43	0.012	0.017
K	2.79	3.81	0.110	0.150
L	7.62 BSC		0.300 BSC	
M	0	15	0	15
N	0.51	1.77	0.020	0.070

CASE 370-01

NOTES
1. SURFACE "T" IS BOTH A DATUM AND SEATING PLANE
2. POSITIONAL TOLERANCE FOR LEADS; D DIM 4 PL
   | ⌖ | 0.27 (.010) Ⓜ | -T- | A Ⓜ |
   LEADS; J DIM 4 PL
   | ⌖ | 0.27 (0.010) Ⓜ | -T- | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH
5. DIMENSION "J" PRIOR TO SOLDER DIP PLATING

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFD210
IRFD211
IRFD212
IRFD213

Advance Information

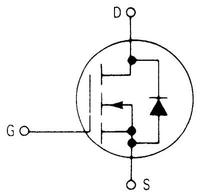
Small-Signal TMOS Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

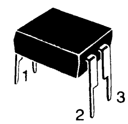
These TMOS FETs are designed for low voltage, high speed power switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertion
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged — SOA is Power Dissipation Limited

TMOS™



1 WATT
TMOS FETs
$r_{DS(on)}$ = 1.5 OHM
200 VOLTS
$r_{DS(on)}$ = 2.4 OHM
150 VOLTS



CASE 370-01

3

MAXIMUM RATINGS

Rating	Symbol	IRFD210	IRFD211	IRFD212	IRFD213	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	± 20				Vdc
Drain Current Continuous T_C = 25°C Pulsed	 I_D I_{DM}	 0.6 2.5		 0.45 1.8		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1 0.008				 Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	 IRFD120, IRFD122 IRFD121, IRFD123	$V_{(BR)DSS}$	 200 150	 — —	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0 V)		I_{DSS}	—	—	250	μAdc
Gate-Body Leakage Current, Foward (V_{GSF} = 20 V)		I_{GSSF}	—	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = −20 V)		I_{GSSR}	—	—	−500	nAdc

(continued)

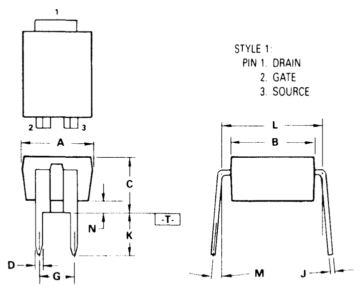
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 250 μA, V_{DS} = V_{GS})		$V_{GS(th)}$	2	—	4	Vdc
Static Drain-Source On-Resistance(1) (V_{GS} = 10 Vdc, I_D = 0.3 A)	IRFD210, IRFD211	$r_{DS(on)}$	—	—	1.5	Ohms
	IRFD212, IRFD213		—	—	2.4	
On-State Drain Current(1) (V_{GS} = 10 V, V_{DS} = 5 V)	IRFD210, IRFD211	$I_{D(on)}$	1.5	—	—	Adc
	IRFD212, IRFD213		2.4	—	—	
Forward Transconductance(1) (I_D = 0.3 A, V_{DS} = 5 V)		g_{fs}	0.5	—	—	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	—	150	pF
Output Capacitance		C_{oss}	—	—	80	
Reverse Transfer Capacitance		C_{rss}	—	—	25	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} = 0.5 $V_{(BR)DSS}$, I_D = 0.3 A, Z_o = 50 Ω)	$t_{d(on)}$	—	—	15	ns
Rise Time		t_r	—	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	—	15	
Fall Time		t_f	—	—	15	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)	I_S = 0.6 A, IRFD210, IRFD211	V_{SD}	—	—	2	Vdc
	I_S = 0.45 A, IRFD212, IRFD213		—	—	1.8	
Continuous Source Current, Body Diode	IRFD210, IRFD211	I_S	—	—	0.6	Adc
	IRFD212, IRFD213		—	—	0.45	
Pulsed Source Current, Body Diode	IRFD210, IRFD211	I_{SM}	—	—	2.5	A
	IRFD212, IRFD213		—	—	1.8	
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	negligible			ns
Reverse Recovery Time		t_{rr}	—	290	—	

(1)Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.70	5.02	0.185	0.198
B	6.10	7.11	0.240	0.280
C	4.06	5.08	0.160	0.200
D	0.38	0.63	0.015	0.025
G	2.54 BSC		0.100 BSC	
J	0.30	0.43	0.012	0.017
K	2.79	3.81	0.110	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.77	0.020	0.070

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS; D DIM 4 PL
   | ⌖ | 0.27 (.010) Ⓜ | -T- | A Ⓜ |
   LEADS; J DIM 4 PL
   | ⌖ | 0.27 (0.010) Ⓜ | -T- | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH
5. DIMENSION "J" PRIOR TO SOLDER DIP PLATING

CASE 370-01

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFD220
IRFD221
IRFD222
IRFD223

Advance Information

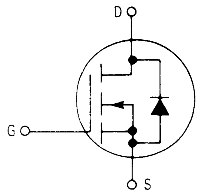
Small-Signal TMOS Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS 4-Pin DIP

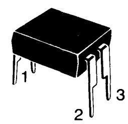
These TMOS FETs are designed for low voltage, high speed power switching applications which require very low on-state resistance, high transconductance, and high device ruggedness.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current
- Package Designed for Auto Insertion
- Ease of Paralleling
- No Second Breakdown
- Stable Over Wide Temperature Range
- Rugged — SOA is Power Dissipation Limited

TMOS



1 WATT
TMOS FETs
$r_{DS(on)}$ = 0.8 OHM
200 VOLTS
$r_{DS(on)}$ = 1.2 OHM
150 VOLTS



CASE 370-01

3

MAXIMUM RATINGS

Rating	Symbol	IRFD220	IRFD221	IRFD222	IRFD223	Unit
Drain-Source Voltage	V_{DSS}	200	150	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	200	150	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Drain Current Continuous T_C = 25°C Pulsed	 I_D I_{DM}	 0.8 6.4		 0.7 5.6		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1 0.008				 Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150				°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	120	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) IRFD220, IRFD222 IRFD221, IRFD223	$V_{(BR)DSS}$	 200 150	 — —	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = Rated V_{DSS}, V_{GS} = 0 V)	I_{DSS}	—	—	250	μAdc
Gate-Body Leakage Current, Foward (V_{GSF} = 20 V)	I_{GSSF}	—	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = −20 V)	I_{GSSR}	—	—	500	nAdc

(continued)

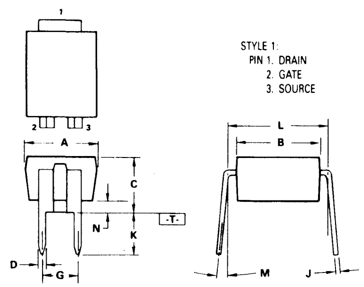
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — Continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS						
Gate Threshold Voltage (I_D = 250 μA, V_{DS} = V_{GS})		$V_{GS(th)}$	2	—	4	Vdc
Static Drain-Source On-Resistance[1] (V_{GS} = 10 Vdc, I_D = 0.4 A)	IRFD220, IRFD221 IRFD222, IRFD223	$r_{DS(on)}$	— —	— —	0.8 1.2	Ohms
On-State Drain Current[1] (V_{GS} = 10 V, V_{DS} = 5 V)	IRFD220, IRFD221 IRFD222, IRFD223	$I_{D(on)}$	0.8 0.7	— —	— —	Adc
Forward Transconductance[1] (I_D = 0.4 A, V_{DS} = 5 V)		g_{fs}	0.5	—	—	mhos
CAPACITANCE						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	—	600	pF
Output Capacitance		C_{oss}	—	—	300	
Reverse Transfer Capacitance		C_{rss}	—	—	80	
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	(V_{DS} ≈ 0.5 $V_{(BR)DSS}$, I_D = 0.4 A, Z_o = 50 Ω)	$t_{d(on)}$	—	—	40	ns
Rise Time		t_r	—	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	60	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Diode Forward Voltage (V_{GS} = 0)	I_S = 0.8 A IRFD220, IRFD221 I_S = 0.7 A IRFD222, IRFD223	V_{SD}	— —	— —	2 1.8	Vdc
Continuous Source Current, Body Diode	IRFD220, IRFD221 IRFD222, IRFD223	I_S	— —	— —	0.8 0.7	Adc
Pulsed Source Current, Body Diode	IRFD220, IRFD221 IRFD222, IRFD223	I_{SM}	— —	— —	6.4 5.6	A
Forward Turn-On Time	(I_S = Rated I_S, V_{GS} = 0)	t_{on}	negligible			ns
Reverse Recovery Time		t_{rr}	—	150	—	

[1]Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.70	5.02	0.185	0.198
B	6.10	7.11	0.240	0.280
C	4.06	5.08	0.160	0.200
D	0.38	0.63	0.015	0.025
G	2.54 BSC		0.100 BSC	
J	0.30	0.43	0.012	0.017
K	2.79	3.81	0.110	0.150
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.77	0.020	0.070

CASE 370-01

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS; D DIM 4 PL
   | ⌖ | 0.27 (.010) Ⓜ | -T- | A Ⓜ |
   LEADS; J DIM 4 PL
   | ⌖ | 0.27 (0.010) Ⓜ | -T- | B Ⓜ |
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH
5. DIMENSION "J" PRIOR TO SOLDER DIP PLATING

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

IRFF110
IRFF113

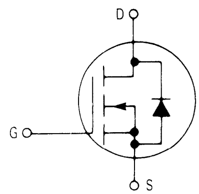
N-CHANNEL
TMOS POWER FETs
$r_{DS(on)}$ = 0.6 OHM
100 VOLTS
$r_{DS(on)}$ = 0.8 OHM
60 VOLTS

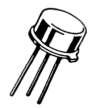
3

... designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability

TMOS





CASE 79-05

MAXIMUM RATINGS

Rating	Symbol	IRFF110	IRFF113	Unit
Drain-Source Voltage	V_{DSS}	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 mΩ)	V_{DGR}	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.5 14	 3 12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	15 0.12		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	8.33 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 s	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) IRFF110 IRFF113	$V_{(BR)DSS}$	 100 60	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	250	μAdc

(continued)

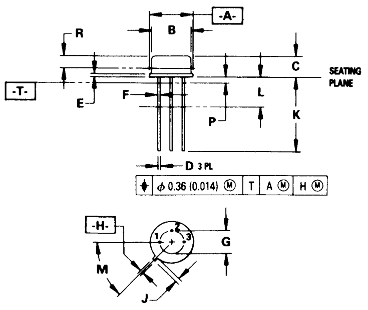
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Body Leakage Current, Forward (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	μAdc
Gate-Body Leakage Current, Reverse (V_{GS} = −20 Vdc, V_{DS} = 0)	I_{GSSR}	—	−100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc) IRFF110	$r_{DS(on)}$	—	0.6	Ohm
IRFF113		—	0.8	
On-State Drain Current (V_{GS} = 10 Vdc, V_{DS} = 5 V) IRFF110	$I_{D(on)}$	3.5	—	A
IRFF113		3	—	
Forward Transconductance (I_D = 1.5 A) IRFF110, IRFF111 V_{DS} = 5 V; IRFF112, IRFF113 V_{DS} = 5 V	g_{fs}	1	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	200	pF
Output Capacitance	C_{oss}	—	100	
Reverse Transfer Capacitance	C_{rss}	—	25	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} = 0.5 Rated V_{DSS}, I_D = 1.5 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time	t_r	—	25	
Turn-Off Delay Time	$t_{d(off)}$	—	25	
Fall Time	t_f	—	20	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage IRFF110	V_{SD}	—	2.5	Vdc
IRFF113	V_{SD}	—	2	Vdc
Forward Turn-On Time (I_S = Rated $I_{D(on)}$, V_{GS} = 0)	t_{on}	—	Negligible	ns
Reverse Recovery Time	t_{rr}	—	200 (Typ)	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 79-05

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFF120
IRFF123

Advance Information

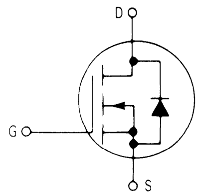
Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

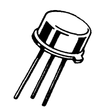
. . . designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid, relay drivers, inverters, choppers, audio amplifiers, and high energy pulse circuits.

- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability

TMOS



N-CHANNEL TMOS POWER FETs
$r_{DS(on)}$ = 0.3 OHM
100 VOLTS
$r_{DS(on)}$ = 0.4 OHM
60 VOLTS



CASE 79-05

3

MAXIMUM RATINGS

Rating	Symbol	IRFF120	IRFF123	Unit
Drain-Source Voltage	V_{DSS}	100	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	I_D I_{DM}	6 24	5 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	6.25 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 s	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	IRFF120 IRFF123	$V_{(BR)DSS}$	100 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	250	μAdc

(continued)

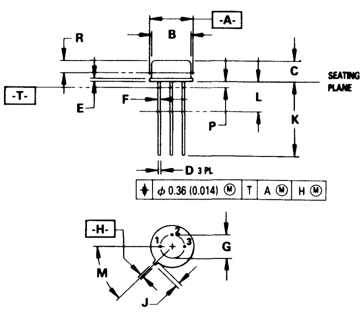
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Body Leakage Current, Forward (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	−100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc) IRFF120	$r_{DS(on)}$	—	0.3	Ohm
IRFF123		—	0.4	
On-State Drain Current (V_{GS} = 10 V, V_{DS} = 5 V) IRFF120	$I_{D(on)}$	6	—	A
IRFF123		5	—	
Forward Transconductance (I_D = 3 A) IRFF120, IRFF121 V_{DS} = 5 V; IRFF122, IRFF123 V_{DS} = 5 V	g_{fs}	1.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	600	pF
Output Capacitance	C_{oss}	—	400	
Reverse Transfer Capacitance	C_{rss}	—	100	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} = 0.5 Rated V_{DSS}, I_D = 3 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time	t_r	—	70	
Turn-Off Delay Time	$t_{d(off)}$	—	100	
Fall Time	t_f	—	70	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated $I_{D(on)}$, V_{GS} = 0) IRFF120	V_{SD}	—	2.5	Vdc
IRFF123	V_{SD}	—	2.3	Vdc
Forward Turn-On Time	t_{on}	—	Negligible	ns
Reverse Recovery Time	t_{rr}	—	200 (Typ)	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 79-05

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFF220
IRFF223

Advance Information

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

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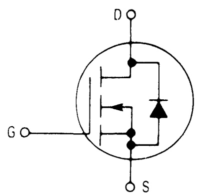
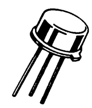
- Silicon Gate for Fast Switching Speeds
- Low Drive Current Required
- Easy Paralleling
- No Second Breakdown
- Excellent Temperature Stability

N-CHANNEL
TMOS POWER FETs
$r_{DS(on)}$ = 0.8 OHM
200 VOLTS
$r_{DS(on)}$ = 1.2 OHMS
150 VOLTS





CASE 79-05

MAXIMUM RATINGS

Rating	Symbol	IRFF220	IRFF223	Unit
Drain-Source Voltage	V_{DSS}	200	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 mΩ)	V_{DGR}	200	150	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 3.5 14	 3 12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	6.25 175	°C/W
Maximum Lead Temperature 1.6 mm from Case for 10 s	T_L	300	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) IRFF220 IRFF223	$V_{(BR)DSS}$	 200 150	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	250	μAdc

(continued)

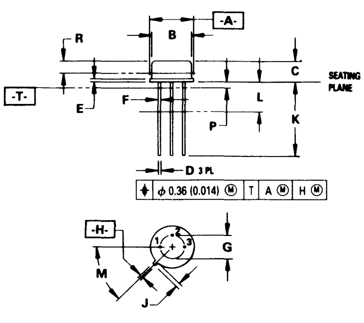
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate-Body Leakage Current, Forward (V_{GS} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GS} = −20 Vdc, V_{DS} = 0)	I_{GSSR}	—	−100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc) IRFF220 IRFF223	$r_{DS(on)}$	— —	0.8 1.2	Ohm
On-State Drain Current (V_{GS} = 10 Vdc, V_{DS} = 5 Vdc) IRFF220 IRFF223	$I_{D(on)}$	3.5 3	— —	A
Forward Transconductance (I_D = 2 A) IRFF220, IRFF221 V_{DS} = 5 V IRFF222, IRFF223 V_{DS} = 5 V	g_{fs}	1.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	600	pF
Output Capacitance	C_{oss}	—	300	
Reverse Transfer Capacitance	C_{rss}	—	80	
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} ≈ 0.5 Rated $V_{(BR)DSS}$, I_D = 2 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time	t_r	—	60	
Turn-Off Delay Time	$t_{d(off)}$	—	100	
Fall Time	t_f	—	60	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage IRFF220	V_{SD}	—	2	Vdc
IRFF223	V_{SD}	—	1.8	Vdc
Forward Turn-On Time (I_S = Rated $I_{D(on)}$, V_{GS} = 0)	t_{on}	—	Negligible	ns
Reverse Recovery Time	t_{rr}	—	350 (Typ)	ns

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



CASE 79-05

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN
(CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.02	9.29	0.355	0.366
B	8.01	8.50	0.315	0.335
C	4.20	4.57	0.165	0.180
D	0.44	0.53	0.017	0.021
E	0.44	0.88	0.017	0.035
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.01	0.029	0.040
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFZ20
IRFZ22

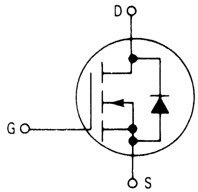
Power Field Effect Transistors
N-Channel Enhancement-Mode
Silicon Gate TMOS

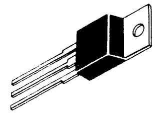
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS

TMOS POWER FETs
14 and 15 AMPERES
$r_{DS(on)}$ = 0.1 OHM
50 VOLTS
$r_{DS(on)}$ = 0.12 OHM





CASE 221A-04
(TO-220AB)

3

MAXIMUM RATINGS

Rating	Symbol	Device IRFZ20	Device IRFZ22	Unit
Drain-Source Voltage	V_{DSS}	50		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Pulsed @ T_C = 25°C	I_D I_{DM}	15 10 60	14 9 56	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

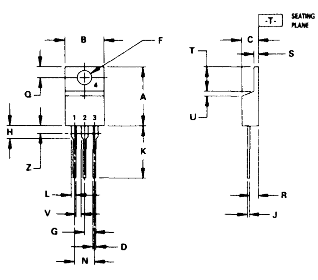
Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP15N05E Designer's Data Sheet for a complete set of design curves for the IRFZ20. See the MTP12N05E Designer's Data Sheet for a complete set of design curves for the IRFZ22.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 9 Adc)	IRFZ20 IRFZ22	$r_{DS(on)}$	— —	0.1 0.12	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 1.5 Vdc) (V_{DS} ≥ 1.7 Vdc)	 IRFZ20 IRFZ22	$I_{D(on)}$	 15 14	 — —	Adc
Forward Transconductance (V_{DS} ≥ 1.5 V, I_D = 9 A) (V_{DS} ≥ 1.7 V, I_D = 9 A)	 IRFZ20 IRFZ22	g_{FS}	 5 5	 — —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	850	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 25 V, I_D = 9 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	90	
Turn-Off Delay Time		$t_{d(off)}$	—	40	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	12 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	9 (Typ)	—	
Gate-Drain Charge		Q_{gd}	3 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	0.8 (Typ)	$1.1^{(1)}$	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	100 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.15 V for IRFZ20.



CASE 221A-04
TO-220AB

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH
3 DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

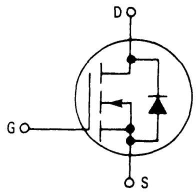
IRFZ30
IRFZ32

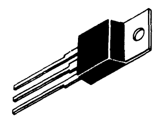
Power Field Effect Transistors
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
25 and 30 AMPERES
$r_{DS(on)}$ = 0.05 OHM
50 VOLTS
$r_{DS(on)}$ = 0.07 OHM





CASE 221A-04
(TO-220AB)

MAXIMUM RATINGS

Rating	Symbol	Device		Unit
		IRFZ30	IRFZ32	
Drain-Source Voltage	V_{DSS}	50		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Pulsed @ T_C = 25°C	I_D I_{DM}	30 19 80	25 16 60	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	300	°C

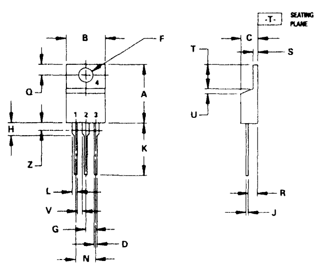
See the MTP30N05E Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc) IRFZ30 IRFZ32	$r_{DS(on)}$	 — —	 0.05 0.07	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 1.5 Vdc) IRFZ30 (V_{DS} ≥ 1.75 Vdc) IRFZ32	$I_{D(on)}$	 30 25	 — —	Adc
Forward Transconductance (V_{DS} ≥ 1.5 V, I_D = 16 A) IRFZ30 (V_{DS} ≥ 1.75 V, I_D = 16 A) IRFZ32	g_{FS}	 9 9	 — —	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1600	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	800	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	200	pF
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} ≈ 25 V, I_D = 16 Apk, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	25	ns
Rise Time (V_{DD} ≈ 25 V, I_D = 16 Apk, R_{gen} = 50 Ohms)	t_r	—	35	ns
Turn-Off Delay Time (V_{DD} ≈ 25 V, I_D = 16 Apk, R_{gen} = 50 Ohms)	$t_{d(off)}$	—	45	ns
Fall Time (V_{DD} ≈ 25 V, I_D = 16 Apk, R_{gen} = 50 Ohms)	t_f	—	35	ns
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	26 (Typ)	30	nC
Gate-Source Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_{gs}	14 (Typ)	—	nC
Gate-Drain Charge (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_{gd}	12 (Typ)	—	nC
SOURCE-DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	1.5(1)	Vdc
Forward Turn-On Time (I_S = Rated I_D, V_{GS} = 0)	t_{on}	Limited by stray inductance		
Reverse Recovery Time (I_S = Rated I_D, V_{GS} = 0)	t_{rr}	150 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.1 V for IRFZ30.



CASE 221A-04
(TO-220AB)

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

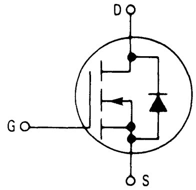
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

IRFZ40
IRFZ42

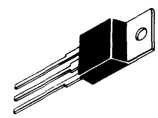
Power Field Effect Transistors
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FETs
46 and 51 AMPERES
$r_{DS(on)}$ = 0.028 OHM
50 VOLTS
$r_{DS(on)}$ = 0.035 OHM



CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Device IRFZ40	Device IRFZ42	Unit
Drain-Source Voltage	V_{DSS}	50		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50		Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Pulsed @ T_C = 25°C	I_D I_{DM}	51 32 160	46 29 145	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

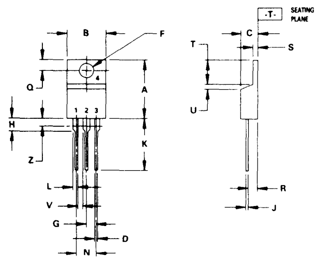
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 Seconds	T_L	300	°C

See the MTP50N05E Designer's Data Sheet for a complete set of design curves for these devices.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 29 Adc)	IRFZ40 IRFZ42	$r_{DS(on)}$	— —	0.028 0.035	Ohm
On-State Drain Current (V_{GS} = 10 V) (V_{DS} ≥ 1.4 Vdc) (V_{DS} ≥ 1.6 Vdc)	 IRFZ40 IRFZ42	$I_{D(on)}$	 51 45	 — —	Adc
Forward Transconductance (V_{DS} ≥ 1.4 V, I_D = 29 A) (V_{DS} ≥ 1.6 V, I_D = 29 A)	 IRFZ40 IRFZ42	g_{FS}	 17 17	 — —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1200	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} ≈ 25 V, I_D = 29 Apk, R_{gen} = Ohms)	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	70	
Fall Time		t_f	—	25	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 10 Vdc, I_D = Rated I_D)	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	22 (Typ)	—	
Gate-Drain Charge		Q_{gd}	18 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.3 (Typ)	2.2(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	350 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(1) Add 0.3 V for IRFZ40.



CASE 221A-04
TO-220AB

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION INCH
3 DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

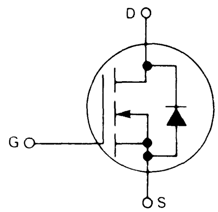
MFE910
MPF910

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high-voltage, high-speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor of TTL-to-high voltage interface and high voltage display drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns Typ
- Low On-Resistance — 2.0 Ohms Typ
- Low Drive Requirement, $V_{GS(th)} = 2.5$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

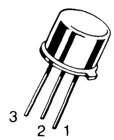
TMOS™



60 VOLTS

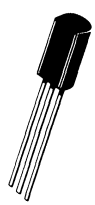
N-CHANNEL TMOS FET

MFE910



CASE 79-04
TO-205AD

MPF910



CASE 29-03
TO-226AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Gate-Source Voltage	V_{GS}	±15	Vdc
Drain Current — Continuous (1) Pulsed (2)	I_D I_{DM}	0.5 1.0	Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C MFE910	P_D	6.25 50	Watts mW/°C
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C MPF910	P_D	1.0 8.0	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	90	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 40 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate-Body Leakage Current (V_{GS} = 10 V, V_{DS} = 0)	I_{GSS}	—	0.01	10	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	0.3	1.5	2.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V, I_D = 500 mA)	$V_{DS(on)}$	—	—	2.5	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	$I_{D(on)}$	500	—	—	mA
Forward Transconductance (V_{DS} = 15 V, I_D = 500 mA)	g_{FS}	100	—	—	mmhos

3

FIGURE 1 — $V_{GS(th)}$ NORMALIZED versus TEMPERATURE

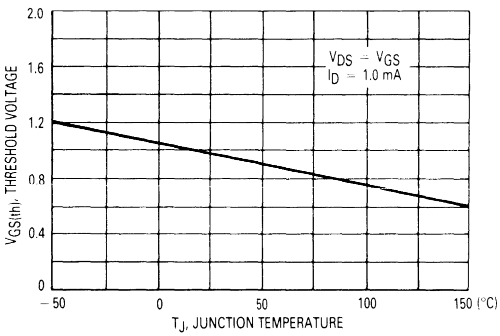


FIGURE 2 — ON-REGION CHARACTERISTICS

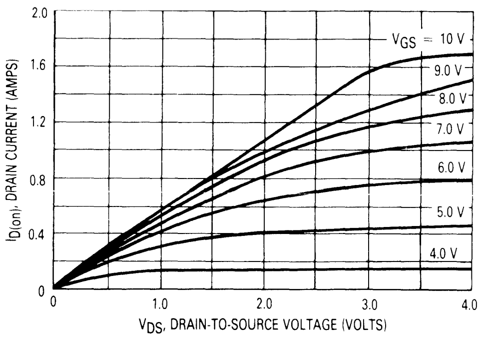


FIGURE 3 — OUTPUT CHARACTERISTICS

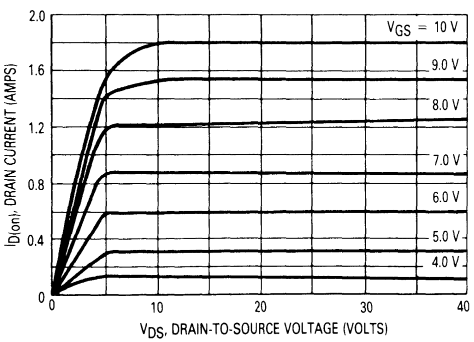
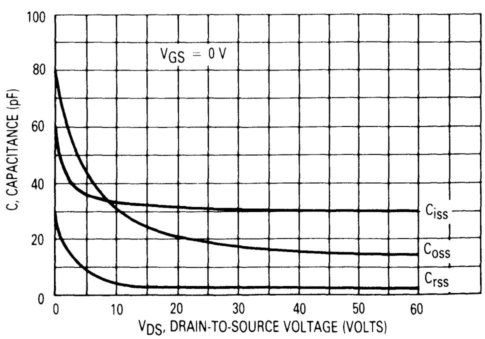
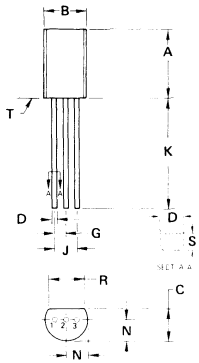


FIGURE 4 — CAPACITANCE versus DRAIN-TO-SOURCE VOLTAGE



OUTLINE DIMENSIONS

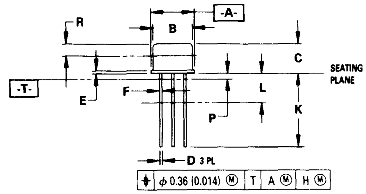


STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | Ø 0.10 (0.004) Ⓜ | T | A Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

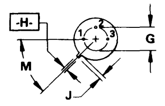
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
N	2.03	2.92	0.080	0.115
R	3.43	–	0.135	–
S	0.46	0.61	0.018	0.024

CASE 29-03
TO-226AE



⌖ | ϕ 0.36 (0.014) Ⓜ | T | A Ⓜ | H Ⓜ

STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN
(CASE)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

CASE 79-04
TO-205AD

3

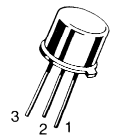
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MFE930
MFE960
MFE990

2.0 AMPERE

N-CHANNEL TMOS FET

30, 60, 90 VOLTS

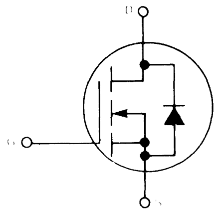


N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL-to-high current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 7.0$ ns Typ
- Low On-Resistance — 0.9 Ohm Typ MFE930
  1.2 Ohm Typ MFE960 and MFE990
- Low Drive Requirement, $V_{GS(th)} = 3.5$ V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

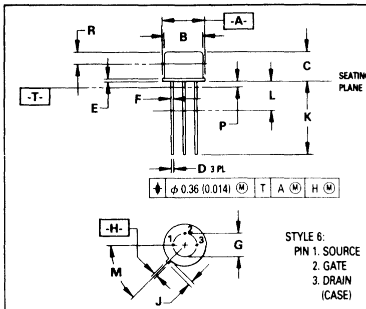
TMOS



MAXIMUM RATINGS

Rating	Symbol	MFE930	MFE960	MFE990	Unit
Drain-Source Voltage	V_{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	35	60	90	Vdc
Gate Source Voltage	V_{GS}		±30		Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}		 2.0 3.0		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D		 6.25 50		 Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}		−55 to 150		°C

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.



STYLE 6:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

CASE 79-04
TO-205AD

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	MFE930	$V_{(BR)DSS}$	35	—	—	Vdc
	MFE960		60	—	—	
	MFE990		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	50	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	1.0	—	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 0.5A)	MFE930	$V_{DS(on)}$	—	0.4	0.7	Vdc
	MFE960		—	0.6	0.8	
	MFE990		—	0.6	1.0	
(I_D = 1.0 A)	MFE930		—	0.9	1.4	
	MFE960		—	1.2	1.7	
	MFE990		—	1.2	2.0	
(I_D = 2.0 A)	MFE930		—	2.2	3.0	
	MFE960		—	2.8	3.5	
	MFE990		—	2.8	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MFE930	$r_{DS(on)}$	—	0.9	1.4	Ohms
	MFE960		—	1.2	1.7	
	MFE990		—	1.2	2.0	
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)		$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)		g_{FS}	200	380	—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	60	70	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{oss}	—	49	60	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)		C_{rss}	—	13	18	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time See Figure 1		t_{on}	—	7.0	15	ns
Turn-Off Time See Figure 1		t_{off}	—	7.0	15	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

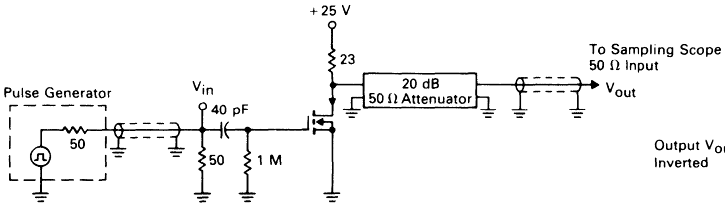


FIGURE 2 — SWITCHING WAVEFORMS

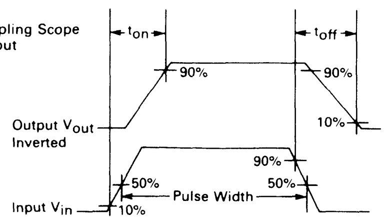


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

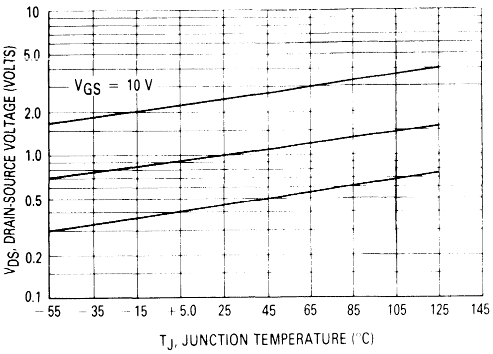


FIGURE 4 — CAPACITANCE VARIATION

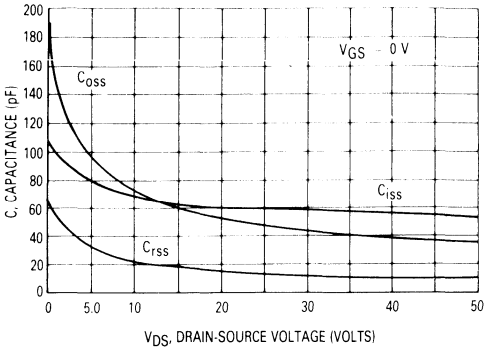


FIGURE 5 — TRANSFER CHARACTERISTIC

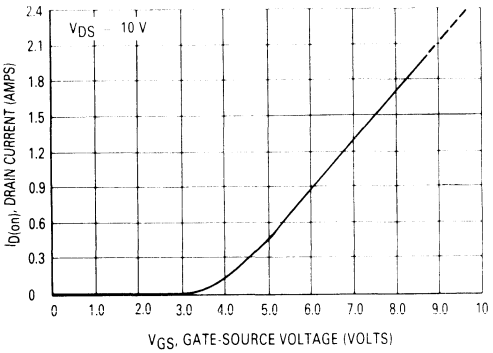


FIGURE 6 — OUTPUT CHARACTERISTIC

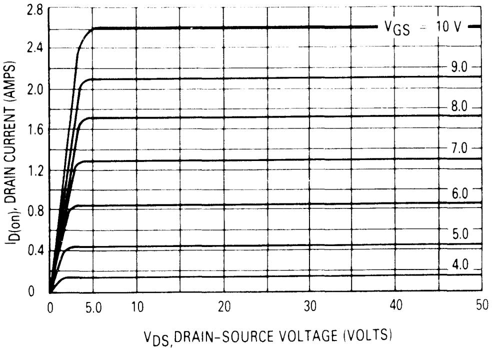
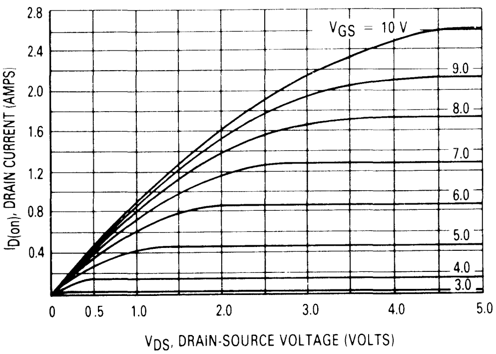


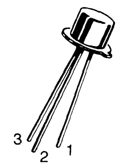
FIGURE 7 — SATURATION CHARACTERISTIC



MFE9200

200 VOLTS

N-CHANNEL TMOS FET



N-CHANNEL ENHANCEMENT-MODE TMOS FIELD EFFECT TRANSISTOR

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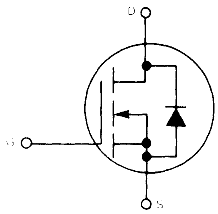
- Fast Switching Speed — t_{on} = t_{off} = 6.0 ns Typ
- Low On-Resistance — 4.5 Ohms Typ
- Low Drive Requirement, $V_{GS(th)}$ = 4.0 V Max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

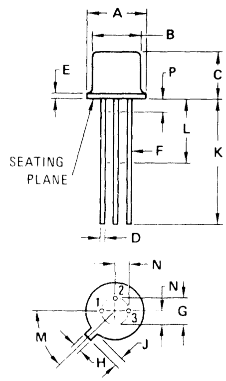
TMOS™



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}	 400 800	 mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 1.8 14.4	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

(1) The Power Dissipation of the package may result in a lower continuous drain current
(2) Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.



STYLE 12:
PIN 1. SOURCE
2. GATE
3. DRAIN (CASE)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.31	5.84	0.209	0.230
B	4.52	4.95	0.178	0.195
C	4.32	5.33	0.170	0.210
D	0.406	0.533	0.016	0.021
E	–	0.762	–	0.030
F	0.406	0.483	0.016	0.019
G	2.54 BSC		0.100 BSC	
H	0.914	1.17	0.036	0.046
J	0.711	1.22	0.028	0.048
K	12.70	–	0.500	–
L	6.35	–	0.250	–
M	45° BSC		45° BSC	
N	1.27 BSC		0.050 BSC	
P	–	1.27	–	0.050

All JEDEC notes and dimensions apply.

**CASE 22-03
TO-18**

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 200 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	0.01	50	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)	$V_{GS(th)}$	1.0	—	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 100 mA) (I_D = 250 mA) (I_D = 500 mA)	$V_{DS(on)}$	 — — —	 0.45 1.20 3.0	 0.6 1.60 —	Vdc
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V)	$I_{D(on)}$	400	700	—	mA
State Drain-Source On-Resistance (V_{GS} = 10 Vdc) (I_D = 100 mA) (I_D = 250 mA) (I_D = 500 mA)	$r_{DS(on)}$	 — — —	 4.5 4.8 6.0	 6.0 6.4 —	Ohms
Forward Transconductance (V_{DS} = 25 V, I_D = 250 mA)	g_{fs}	200	400	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	72	90	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	15	20	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.8	3.5	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time See Figure 1	t_{on}	—	6.0	15	ns
Turn-Off Time See Figure 1	t_{off}	—	6.0	15	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

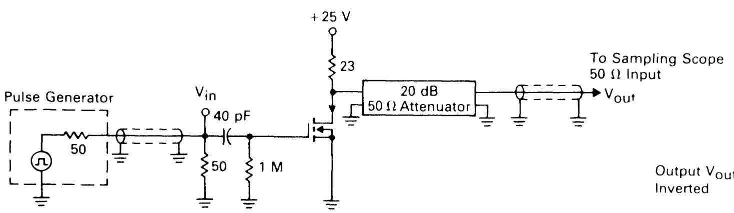


FIGURE 2 — SWITCHING WAVEFORMS

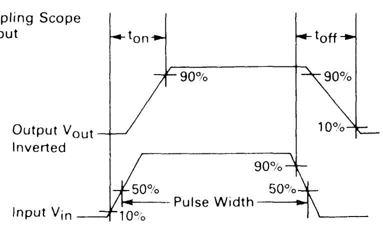


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

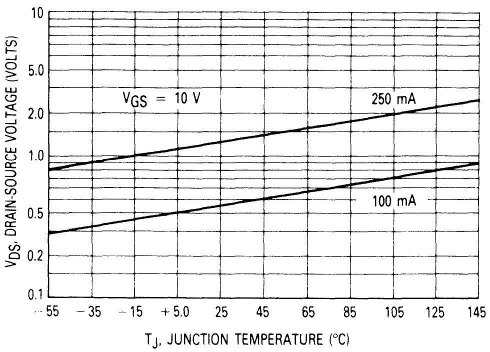


FIGURE 4 — CAPACITANCE VARIATION

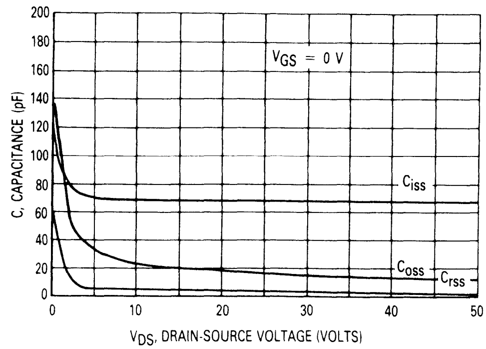


FIGURE 5 — TRANSFER CHARACTERISTIC

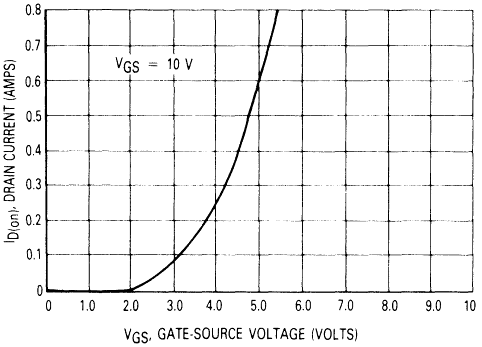


FIGURE 6 — OUTPUT CHARACTERISTIC

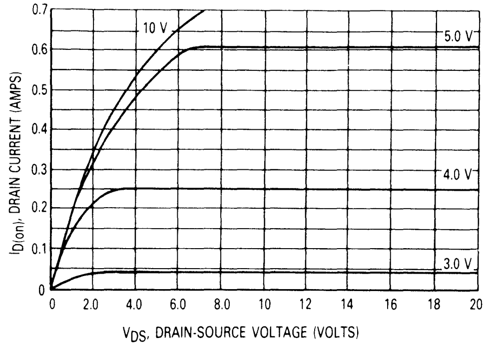
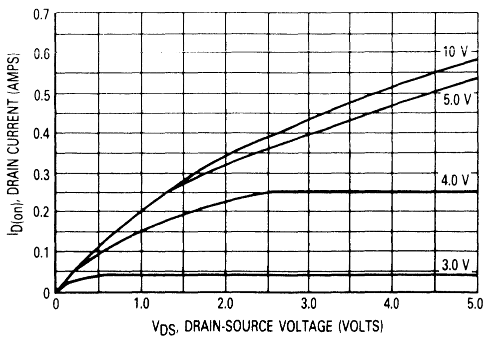


FIGURE 7 — SATURATION CHARACTERISTIC



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MGM5N45 MGM5N50 MGP5N45 MGP5N50

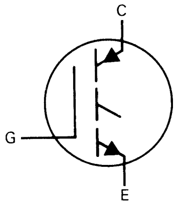
Designer's Data Sheet

N-CHANNEL ENHANCEMENT-MODE SILICON GATE, INSULATED GATE BIPOLAR TRANSISTOR

These GEMFETS are designed for high voltage, high current power controls such as line operated motor controls and converters.

- High Input Impedance
- Low On-Voltage, 4.0 V max @ 2.5 A @ T_J = 100°C
- Fast Turn-On Time
- Voltage Driven Device
- No Parasitic Source to Drain Diode

TMOS

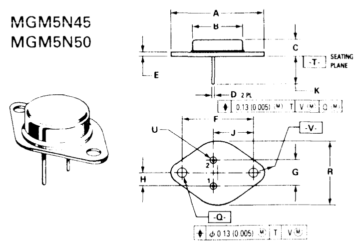


5.0 AMPERE

N-CHANNEL TMOS GEMFET

$r_{CE(on)}$ = 1.6 Ohm
450 and 500 Volts

MGM5N45
MGM5N50

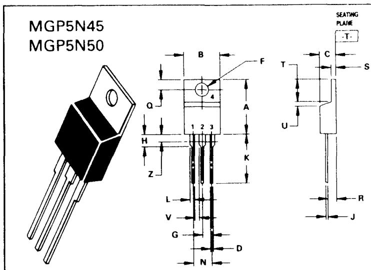


STYLE 6:
PIN 1. GATE
2. EMITTER
CASE COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

CASE 1-06
TO-204AA

MGP5N45
MGP5N50



STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MAXIMUM RATINGSS

Rating	Symbol	MGM5N45 MGP5N45	MGM5N50 MGP5N50	Unit
Collector-Emitter Voltage	V_{CES}	450	500	Vdc
Collector-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{CGR}	450	500	Vdc
Gate-Emitter Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GE} V_{GEM}	±20 ±40		Vdc Vpk
Collector Current — Continuous — Pulsed	I_C I_{CM}	5.0 8.0		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 30(1)	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

(1) Add 32.5°C/W for MGP5N45 and MGP5N50.

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage (V_{GE} = 0, I_C = 5.0 mA)	MGM5N45, MGP5N45	$V_{(BR)CES}$	450	—	Vdc
	MGM5N50, MGP5N50		500	—	
Zero Gate Voltage Collector Current (V_{CE} = 0.85 Rated V_{CE}, V_{GE} = 0)		I_{CES}	—	0.1	mAdc
T_J = 100°C			—	1.0	
Gate-Body Leakage Current (V_{GE} = 20 Vdc, V_{CE} = 0)		I_{GES}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_C = 1.0 mA, V_{CE} = V_{GE})		$V_{GE(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Collector-Emitter On-Voltage (I_C = 2.5 Adc, V_{GE} = 10 V)		$V_{CE(on)}$	—	4.0	Vdc
(I_C = 5.0 Adc, V_{GE} = 15 V)			—	5.0	
(I_C = 2.5 Adc, V_{GE} = 10 V, T_J = 100°C)			—	4.0	
Static Collector-Emitter On-Resistance (V_{GE} = 10 Vdc, I_C = 2.5 Adc)		$r_{CE(on)}$	—	1.6	Ohms
Forward Transconductance (V_{CE} = 10 V, I_C = 5.0 A)		g_{FS}	1.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{CE} = 25 V, V_{GE} = 0, f = 1.0 MHz)	C_{iss}	—	300	pF
Output Capacitance		C_{oss}	—	50	
Reverse Transfer Capacitance		C_{rss}	—	10	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

RESISTIVE SWITCHING

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{CE} = 250 V, I_C = 5.0 A, R_G = 250 Ω, V_{in} = 15 V)	$t_{d(on)}$	—	0.04	μs
Rise Time		t_r	—	0.5	
Turn-Off Delay Time		$t_{d(off)}$	—	0.25	
Fall Time		t_f	—	5.0	

INDUCTIVE SWITCHING

Characteristic	Conditions		Symbol	Min	Max	Unit
Turn-Off Delay Time	(V_{clamp} = 250 V, I_{CM} = 5.0 A, L = 180 μH, V_{in} = 15 V)	R_G = 0.25 kΩ	$t_{d(off)}$	—	0.25	μs
Crossover Time			t_c	—	5.0	
Turn-Off Delay Time		R_G = 1.0 kΩ	$t_{d(off)}$	—	1.0	
Crossover Time			t_c	—	5.0	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

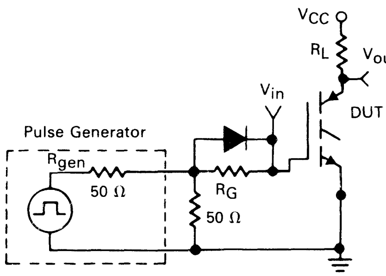
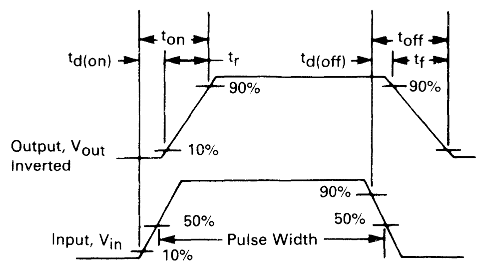


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

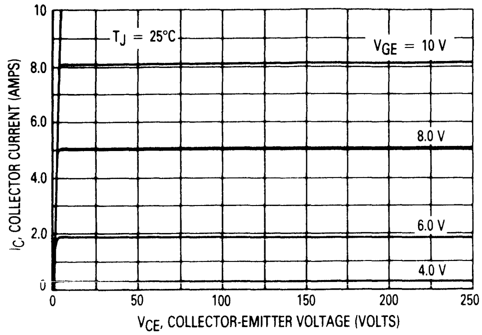


FIGURE 4 — ON-REGION CHARACTERISTICS

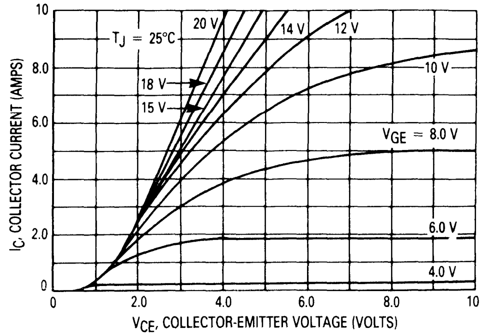


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

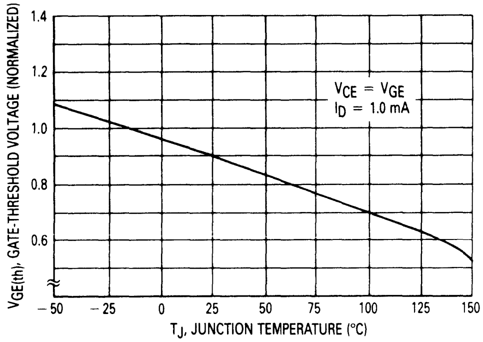


FIGURE 6 — TRANSFER CHARACTERISTICS

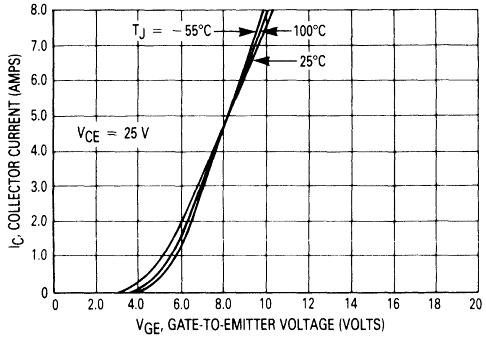


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

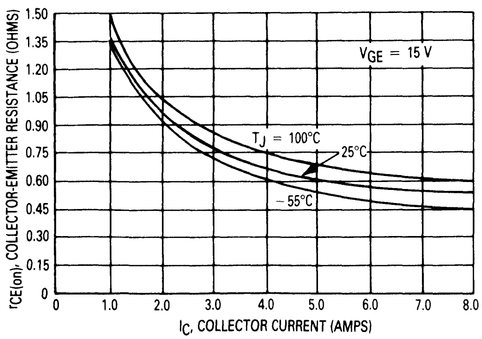


FIGURE 8 — CAPACITANCE VARIATION

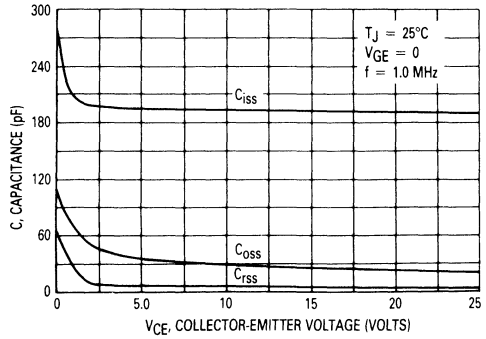


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

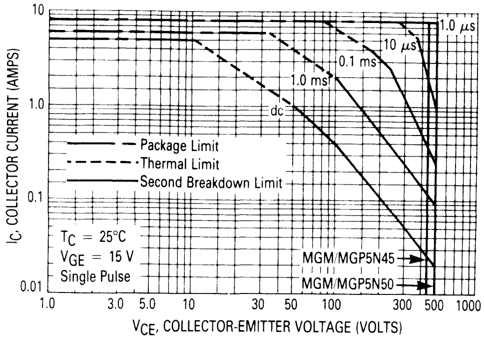
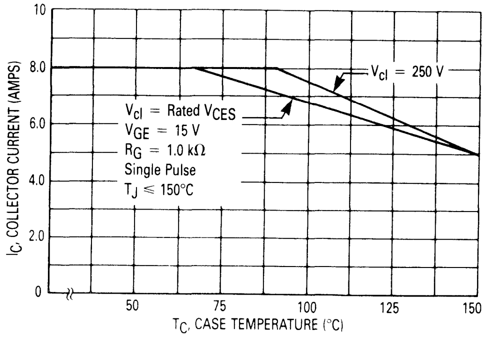


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



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FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable collector current (I_{CM}) may be calculated with the aid of the following equation:

$$I_{CM} = I_{C(25°C)} \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{C(25°C)}$ = the dc collector current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SSOA) of a GEMFET device is a composite function of gate turn-off time, inductive clamp voltage (Vcl) and device junction temperature (T_J). Figure 10 illustrates that I_C is 8.0 A for Vcl ≤ 250 V and T_J ≤ 90°C, and for Vcl ≤ 500 V and T_J ≤ 65°C. Additionally, it is seen that for a peak collector current of 6.0 A, T_J must be maintained less than 130°C for V_{cl} = 250 V, and less than 120°C for V_{cl} = 500 V.

T_J may be calculated from the equation:

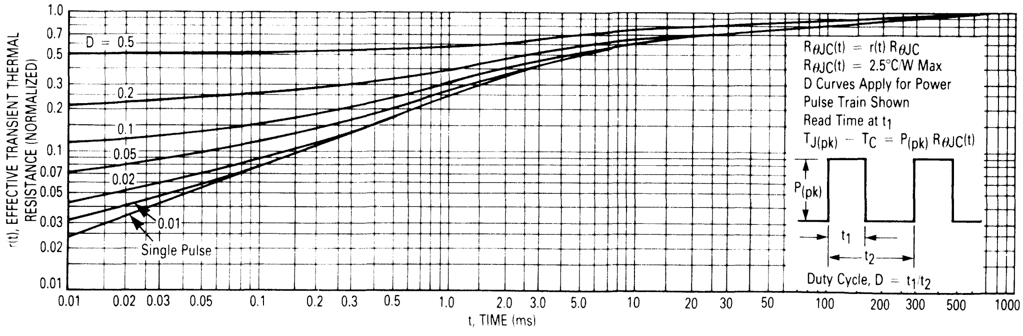
$$T_J = T_C + P_D \cdot R_{\theta JC} \cdot r(t)$$

where

P_D is the power averaged over a complete switching cycle.

Generally, SSOA current declines with decreasing gate turn-off time. Gate turn-off time is controlled by R_G; lowering R_G decreases gate turn-off time. A suggested rule-of-thumb is to derate the I_C of Figure 10 by 1.0 A for every 250 ohms of R_G below 1.0 kΩ for case temperatures greater than 65°C.

FIGURE 11 — THERMAL RESPONSE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MGM20N45
MGM20N50
MGP20N45
MGP20N50

Designer's Data Sheet

20 AMPERE

N-CHANNEL TMOS GEMFET

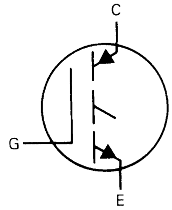
$r_{CE(on)}$ = 0.27 Ohm
450 and 500 Volts

N-CHANNEL ENHANCEMENT-MODE SILICON GATE, INSULATED GATE BIPOLAR TRANSISTOR

These GEMFETS are designed for high voltage, high current power controls such as line operated motor controls and converters.

- High Input Impedance
- Low On-Voltage, 2.7 V max @ 10 A
- High Peak Current Capability — 30 A
- Voltage Driven Device

TMOS™



MAXIMUM RATINGSS

Rating	Symbol	MGM20N45 MGP20N45	MGM20N50 MGP20N50	Unit
Collector-Emitter Voltage	V_{CES}	450	500	Vdc
Collector-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{CER}	450	500	Vdc
Gate-Emitter Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GE} V_{GEM}	 ±20 ±40		 Vdc Vpk
Collector Current Continuous Pulsed	 I_C I_{CM}	 20 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 100 0.8		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

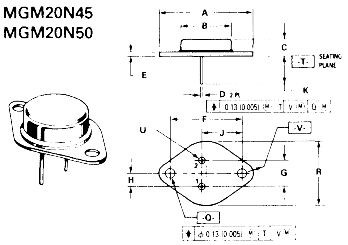
THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.25 30(1)	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

(1) Add 32.5°C/W for MGP20N45 and MGP20N50.

Designer's Data for "Worst Case" Conditions
The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MGM20N45
MGM20N50

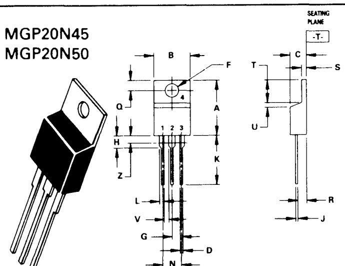


STYLE 6:
PIN 1. GATE
2. EMITTER
CASE COLLECTOR

CASE 1-06
TO-204AA

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

MGP20N45
MGP20N50



STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A-04
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (V_{GE} = 0, I_C = 5.0 mA) MGM20N45, MGP20N45	$V_{(BR)CES}$	450	—	Vdc
MGM20N50, MGP20N50		500	—	
Zero Gate Voltage Collector Current (V_{CE} = 0.85 Rated V_{CE}, V_{GE} = 0)	I_{CES}	—	0.25	mAdc
T_J = 100°C		—	2.5	
Gate-Body Leakage Current (V_{GE} = 20 Vdc, V_{CE} = 0)	I_{GES}	—	500	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (I_C = 1.0 mA, V_{CE} = V_{GE})	$V_{GE(th)}$	2.0	4.5	Vdc
T_J = 100°C		1.5	4.0	
Collector-Emitter On-Voltage (I_C = 10 Adc, V_{GE} = 10 V)	$V_{CE(on)}$	—	2.7	Vdc
(I_C = 20 Adc, V_{GE} = 15 V)		—	5.0	
(I_C = 10 Adc, V_{GE} = 10 V, T_J = 100°C)		—	3.0	
Static Collector-Emitter On-Resistance (V_{GE} = 10 Vdc, I_C = 10 Adc)	$r_{CE(on)}$	—	0.27	Ohms
Forward Transconductance (V_{CE} = 10 V, I_C = 10 A)	g_{FS}	3.0	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{CE} = 25 V, V_{GE} = 0, f = 1.0 MHz)	C_{iss}	—	950	pF
Output Capacitance	C_{oss}	—	150	
Reverse Transfer Capacitance	C_{rss}	—	60	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
RESISTIVE SWITCHING				
Turn-On Delay Time (V_{CE} = 250 V, I_C = 20 A, R_G = 1.0 Ω, V_{in} = 15 V)	$t_{d(on)}$	—	0.075	μs
Rise Time	t_r	—	0.15	
Turn-Off Delay Time	$t_{d(off)}$	—	4.0	
Fall Time	t_f	—	8.0	
INDUCTIVE SWITCHING				
Turn-Off Delay Time (V_{clamp} = 250 V, I_{CM} = 20 A, L = 180 μH, V_{in} = 15 V) R_G = 1.0 kΩ	$t_{d(off)}$	—	4.0	μs
Crossover Time	t_c	—	6.0	
Turn-Off Delay Time R_G = 4.0 kΩ	$t_{d(off)}$	—	9.5	
Crossover Time	t_c	—	9.5	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

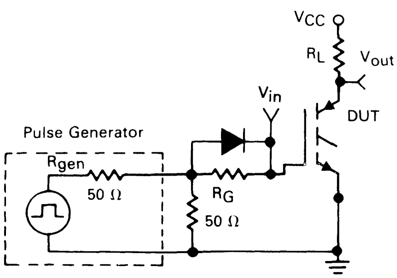
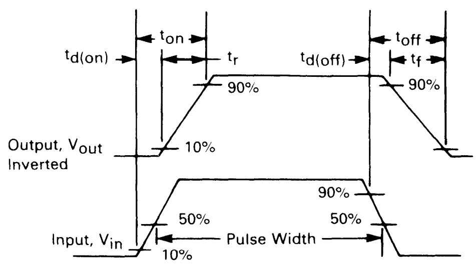


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

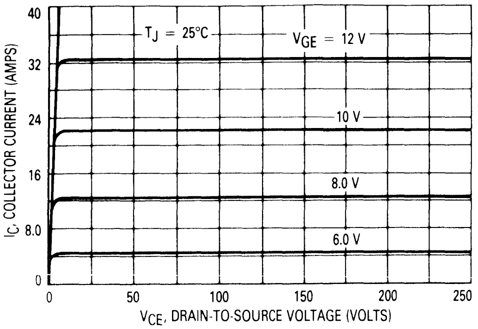


FIGURE 4 — ON-REGION CHARACTERISTICS

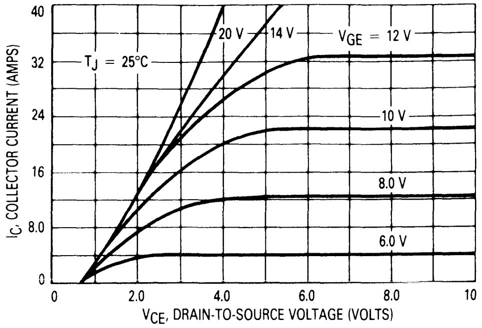


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

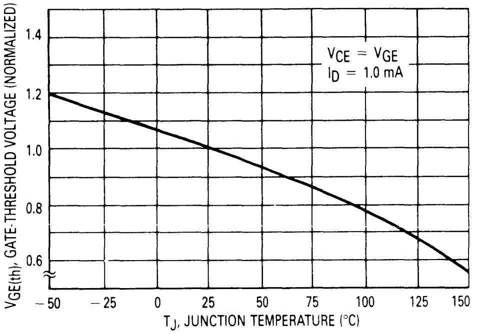


FIGURE 6 — TRANSFER CHARACTERISTICS

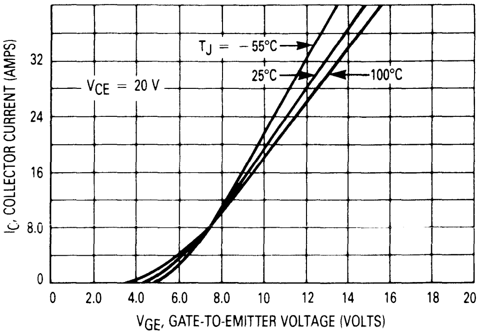


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

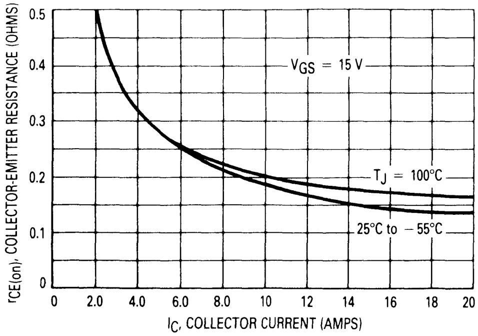


FIGURE 8 — CAPACITANCE VARIATION

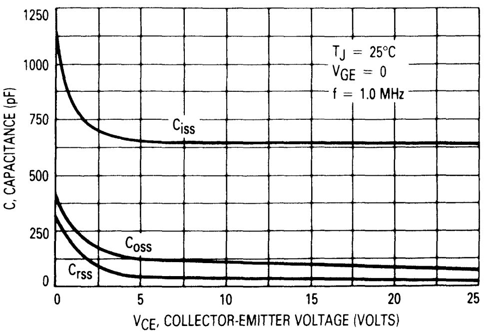


FIGURE 9 — MAXIMUM RATED FORWARD BIAS SAFE OPERATING AREA

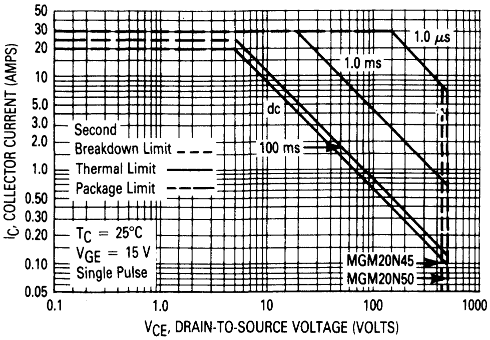
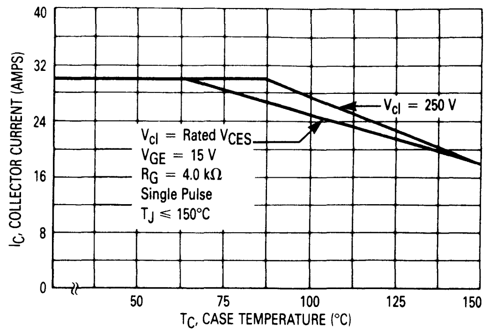


FIGURE 10 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA



3

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 9 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable collector current (I_{CM}) may be calculated with the aid of the following equation:

$$I_{CM} = I_C(25°C) \left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_C(25°C)$ = the dc collector current at T_C = 25°C from Figure 9.
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
r(t) = normalized thermal response from Figure 11

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SSOA) of a GEMFET device is a composite function of gate turn-off time, inductive clamp voltage (Vcl) and device junction temperature (T_J). Figure 10 illustrates that I_C is 30 A for Vcl ≤ 250 V and T_J ≤ 87.5°C, and for Vcl ≤ 500 V and T_J ≤ 62.5°C. Additionally, it is seen that for a peak collector current of 24 A, T_J must be maintained less than 118°C for V_{cl} = 250 V, and less than 106°C for V_{cl} = 500 V.

T_J may be calculated from the equation:

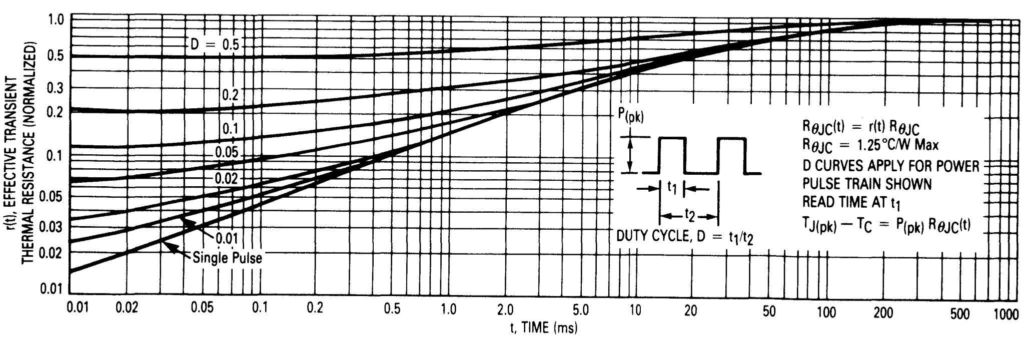
$$T_J = T_C + P_D \cdot R_{\theta JC} \cdot r(t)$$

where

P_D is the power averaged over a complete switching cycle.

Generally, SSOA current declines with decreasing gate turn-off time. Gate turn-off time is controlled by R_G; lowering R_G decreases gate turn-off time. A suggested rule-of-thumb is to derate the I_C of Figure 10 by 25 A for every 1100 ohms of R_G below 4.0 kΩ for case temperatures greater than 55°C.

FIGURE 11 — THERMAL RESPONSE



MMBF170

Advance Information

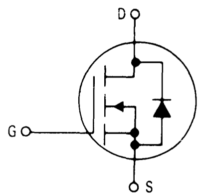
Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds

N-CHANNEL SMALL-SIGNAL TMOS FET $r_{DS(on)}$ = 5 OHMS 60 VOLTS



CASE 318-02 SOT-23 (TO-236AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	0.5 0.8	Adc
Total Power Dissipation FR5 Board 1″ x 0.75″ x 0.62″ Derate above 25°C	P_D	550 4.4	mW mW/°C
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	60	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	—	Vdc
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	10	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	0.8	3	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 200 mA)	$r_{DS(on)}$	—	5	Ohm
On-State Drain Current (V_{DS} = 25 V, V_{GS} = 0)	$I_{D(off)}$	—	0.5	μA

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz)		C_{iss}	—	60	pF
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 500 mA, R_{gen} = 50 Ohms) Figure 1	$t_{d(on)}$	—	10	ns
Turn-Off Delay Time		$t_{d(off)}$	—	10	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

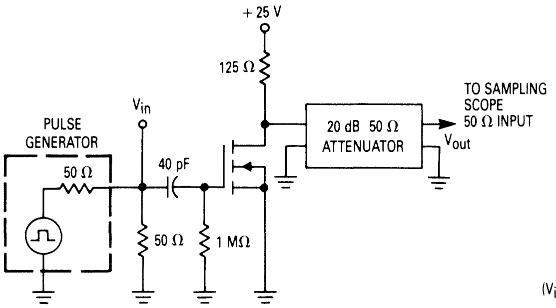
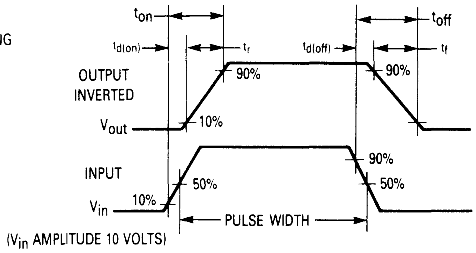
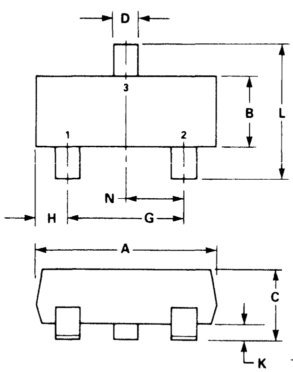


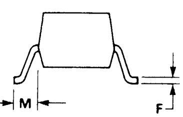
Figure 1. Switching Test Circuit

SWITCHING WAVEFORM



OUTLINE DIMENSIONS





NOTES:
1. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.80	3.04	0.1102	0.1197
B	1.20	1.40	0.0472	0.0551
C	0.85	1.20	0.033	0.0472
D	0.37	0.46	0.0150	0.0177
F	0.085	0.130	0.0034	0.0051
G	1.78	2.04	0.0701	0.0807
H	0.51	0.60	0.0200	0.0236
K	0.10	0.25	0.0040	0.0098
L	2.10	2.50	0.0830	0.0984
M	0.45	0.60	0.0180	0.0236
N	0.89	1.02	0.0350	0.0401

CASE 318-02
SOT-23

MPF930
MPF960
MPF990

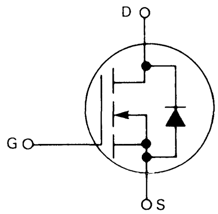
3

N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

These TMOS FETs are designed for high-speed switching applications such as switching power supplies, CMOS logic, microprocessor or TTL to current interface and line drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 7.0$ ns typ
- Low On-Resistance — 0.9 Ohm typ MPF930
  1.2 Ohm typ MPF960 and MPF990
- Low Drive Requirement, $V_{GS(th)} = 3.5$ V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

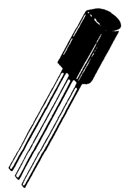
TMOS

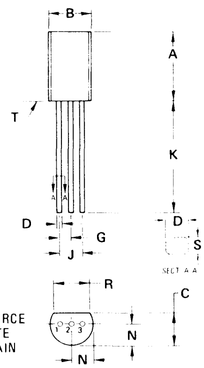


2.0 AMPERE

N-CHANNEL TMOS FETs

35, 60, 90 VOLTS





STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

NOTES:
1. DIMENSIONS -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ Ø 0.10 (0.004) Ⓜ T A Ⓜ B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.37	7.87	0.290	0.310
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.46	0.61	0.018	0.024
G	1.27 BSC		0.050 BSC	
J	2.54 BSC		0.100 BSC	
K	12.70	–	0.500	–
N	2.03	2.92	0.080	0.115
R	3.43	–	0.135	–
S	0.46	0.61	0.018	0.024

CASE 29-03
TO-226AE

MAXIMUM RATINGS

Rating	Symbol	MPF930	MPF960	MPF990	Unit
Drain-Source Voltage	V_{DSS}	35	60	90	Vdc
Drain-Gate Voltage	V_{DGO}	35	60	90	Vdc
Gate Source Voltage	V_{GS}		±30		Vdc
Drain Current Continuous (1) Pulsed (2)	 I_D I_{DM}		 2.0 3.0		Adc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D		1.0 8.0		Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}		-55 to 150		°C
Thermal Resistance	θ_{JA}		125		°C/W

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	MPF930	$V_{(BR)DSS}$	35	—	—	Vdc
	MPF960		60	—	—	
	MPF990		90	—	—	
Zero Gate Voltage Drain Current (V_{DS} = Maximum Rating, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	50	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})		$V_{GS(th)}$	1.0	—	3.5	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 0.5 A)	MPF930	$V_{DS(on)}$	—	0.4	0.7	Vdc
	MPF960		—	0.6	0.8	
	MPF990		—	0.6	1.0	
(I_D = 1.0 A)	MPF930		—	0.9	1.4	
	MPF960		—	1.2	1.7	
	MPF990		—	1.2	2.0	
(I_D = 2.0 A)	MPF930		—	2.2	3.0	
	MPF960		—	2.8	3.5	
	MPF990		—	2.8	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	MPF930	$r_{DS(on)}$	—	0.9	1.4	Ohms
	MPF960		—	1.2	1.7	
	MPF990		—	1.2	2.0	
On State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V		$I_{D(on)}$	1.0	2.0	—	Amps
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)		g_{FS}	200	380	—	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{iss}	—	60	70	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{oss}	—	49	60	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)		C_{rss}	—	13	18	pF
SWITCHING CHARACTERISTICS*						
Turn-On Time See Figure 1		t_{on}	—	7.0	15	ns
Turn-Off Time See Figure 1		t_{off}	—	7.0	15	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

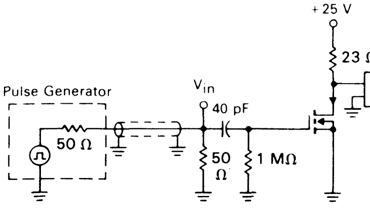


FIGURE 2 — SWITCHING WAVEFORMS

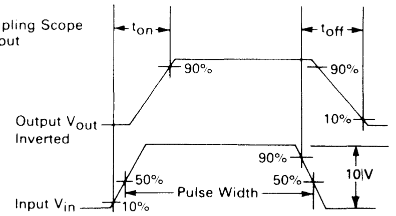


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

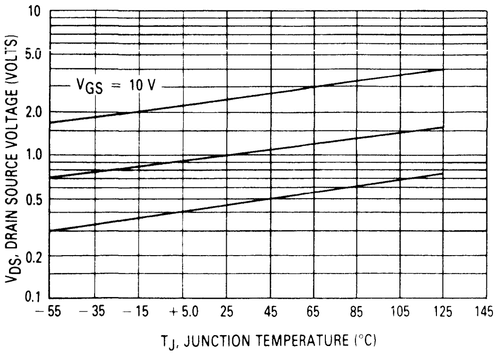


FIGURE 4 — CAPACITANCE VARIATION

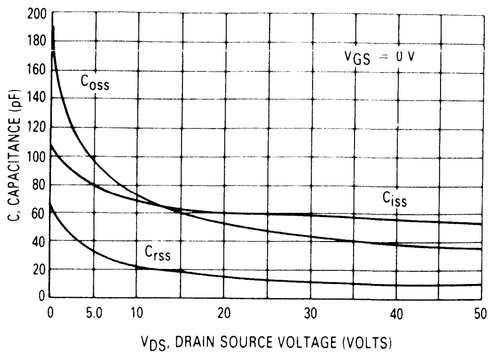


FIGURE 5 — TRANSFER CHARACTERISTIC

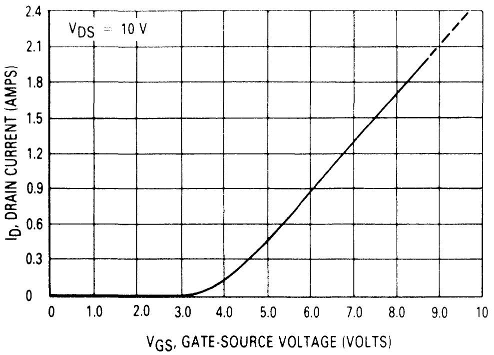


FIGURE 6 — OUTPUT CHARACTERISTIC

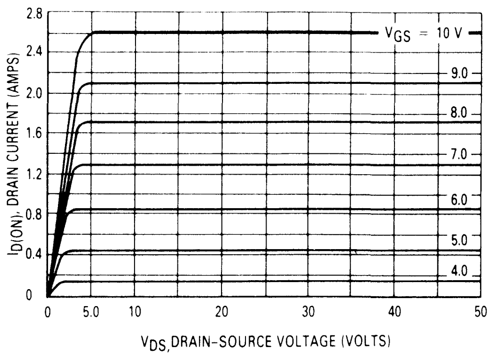
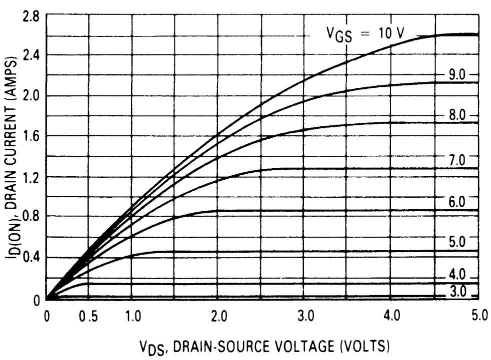


FIGURE 7 — SATURATION CHARACTERISTIC

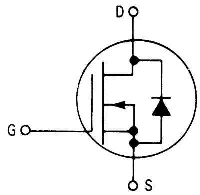


MPF4150

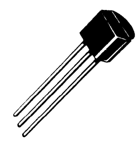
Advance Information

Small-Signal Field Effect Transistor
Silicon Gate TMOS

- Normally Closed Relay
- Telephone Line Switching
- Fail Safe Systems
- Current Regulator Circuits



625 mW
TMOS FET
$r_{DS(on)}$ = 12 OHMS
150 VOLTS
N-CHANNEL
DEPLETION MODE



CASE 29-04
TO-226AA
PLASTIC PACKAGE

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	150	Vdc
Drain-Gate Voltage	V_{DG}	150	Vdc
Drain Current — Continuous — Pulsed (1)	I_D I_{DM}	250 500	mA
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

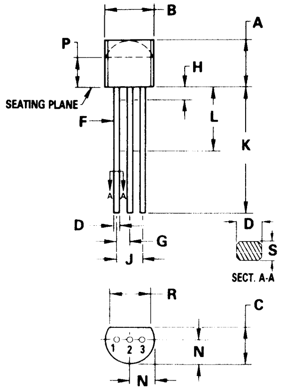
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Breakdown Voltage Drain to Source ($V_{GS} = -10$ V, $I_D = 10$ μA)	$V_{(BR)DSX}$	−150	—	Vdc
Gate-Source Cutoff Voltage ($V_{DS} = 3.5$ V, $I_D = 1$ μA)	$V_{GS(off)}$	−1	−6	Vdc
Gate Reverse Leakage ($V_{GS} = -20$ V, $V_{DS} = 0$)	I_{GSS}	—	1	nAdc
ON CHARACTERISTICS				
Zero-Gate Voltage Drain Current (2) ($V_{DS} = 10$ V, $V_{GS} = 0$)	I_{DSS}	−100	−800	mAdc
Static Drain-Source On-Resistance ($V_{GS} = 0$ V, $I_D = 100$ mA)	$r_{DS(on)}$	—	12	Ohms
SMALL-SIGNAL CHARACTERISTICS				
Forward Transadmittance (2) ($V_{DS} = 10$ V, $I_D = 50$ mA, f = 1 kHz)	Y_{fs}	100	—	mmhos
Input Capacitance ($V_{DS} = 10$ Vdc, $V_{GS} = -10$ V, f = 1 MHz)	C_{iss}	—	125	pF
Reverse Transfer Capacitance ($V_{DS} = 10$ V, $V_{GS} = -10$ V, f = 1 MHz)	C_{rss}	—	15	pF

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

OUTLINE DIMENSIONS



NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

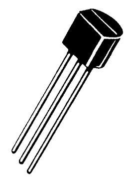
CASE 29-04
PLASTIC PACKAGE
TO-226AA

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

MPF9200

200 VOLTS

N-CHANNEL TMOS FET

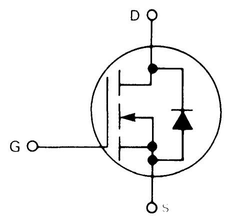


N-CHANNEL ENHANCEMENT-MODE TMOS FIELD-EFFECT TRANSISTOR

This TMOS FET is designed for high voltage, high speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL to high voltage interface and high voltage display drivers.

- Fast Switching Speed — $t_{on} = t_{off} = 6.0$ ns typ
- Low On-Resistance — 4.5 Ohms typ
- Low Drive Requirement, $V_{GS(th)} = 4.0$ V max
- Inherent Current Sharing Capability Permits Easy Paralleling of Many Devices

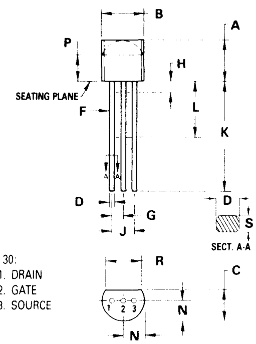
TMOS™



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (1) Pulsed (2)	I_D I_{DM}	400 800	mAdc
Total Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	0.6 4.8	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Thermal Resistance Junction to Ambient	θ_{JA}	208	°C/W

(1) The Power Dissipation of the package may result in a lower continuous drain current.
(2) Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.



STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

CASE 29-04
(TO-92)
(TO-226AA)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	200	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 200 V, V_{GS} = 0)	I_{DSS}	—	0.1	10	μAdc
Gate-Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	0.01	50	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	$V_{GS(th)}$	1.0	—	4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$				Vdc
(I_D = 100 mA)		—	0.45	0.6	
(I_D = 250 mA)		—	1.20	1.60	
(I_D = 500 mA)		—	3.0	—	
On State Drain Current (V_{DS} = 25 V, V_{GS} = 10 V	$I_{D(on)}$	400	700	—	mA
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc)	$r_{DS(on)}$				Ohms
(I_D = 100 mA)		—	4.5	6.0	
(I_D = 250 mA)		—	4.8	6.4	
(I_D = 500 mA)		—	6.0	—	
Forward Transconductance (V_{DS} = 25 V, I_D = 250 mA)	g_{FS}	200	400	—	mmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance OV_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	72	90	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	15	20	pF
Reverse Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	—	2.8	3.5	pF
SWITCHING CHARACTERISTICS*					
Turn-On Time See Figure 1	t_{on}	—	6.0	15	ns
Turn-Off Time See Figure 1	t_{off}	—	12	15	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

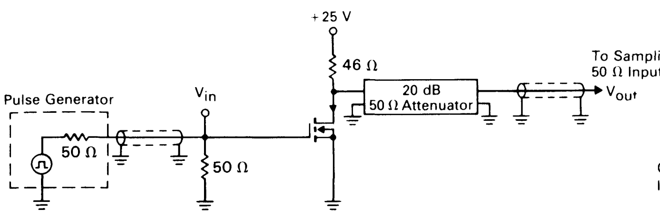


FIGURE 2 — SWITCHING WAVEFORMS

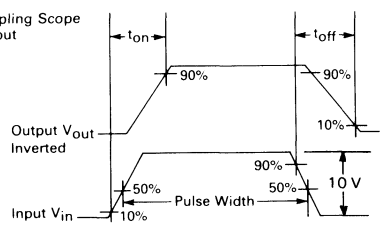


FIGURE 3 — ON VOLTAGE versus TEMPERATURE

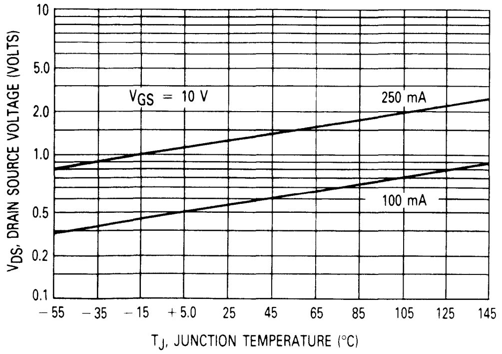


FIGURE 4 — CAPACITANCE VARIATION

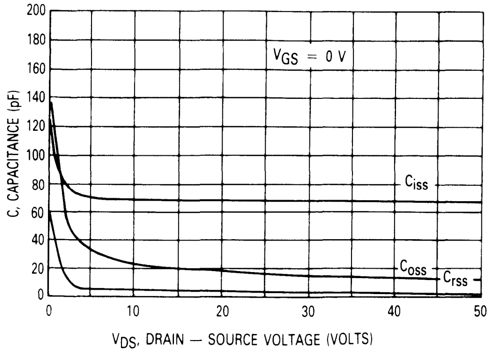


FIGURE 5 — TRANSFER CHARACTERISTIC

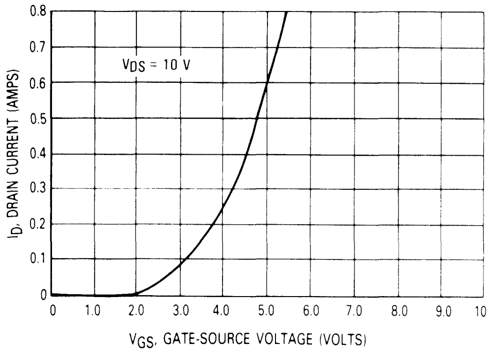


FIGURE 6 — OUTPUT CHARACTERISTIC

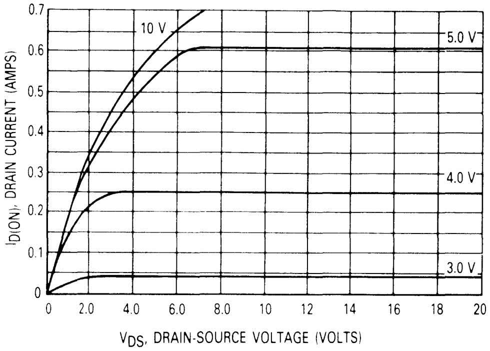
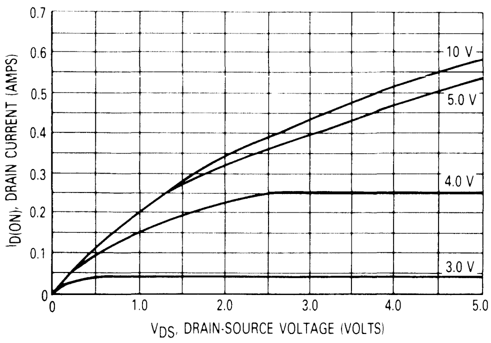


FIGURE 7 — SATURATION CHARACTERISTIC



3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MPM3002

Advance Information

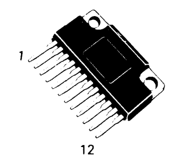
TMOS ICePAK Power Module

P-Channel Power MOSFET and N-Channel SENSEFET™ in a Full H-Bridge Configuration

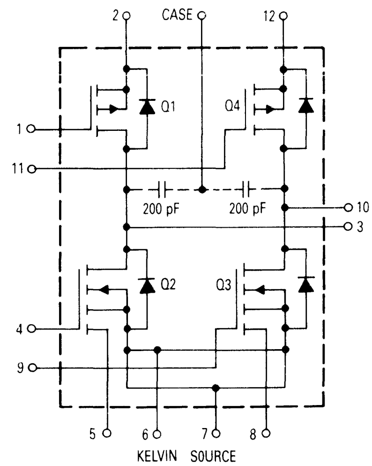
TMOS POWER MOSFET
H-BRIDGE
100 VOLTS
8 AMPERES

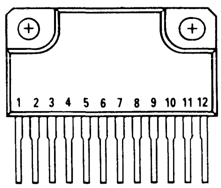
The MPM3002 is a H-Bridge power circuit with lossless current sensing capability. The upper legs of the bridge consists of P-Channel power MOSFETs and the lower legs of the bridge consist of two SENSEFETs. This power circuit packaged in the ICePAK is ideal for applications such as servo motor drives, stepper motor controls and switching power supplies. Features of this product include:

- P and N-Channel Power MOSFET Configuration for Ease of Drive
- Lossless Current Sensing in Each Lower Leg of the H-Bridge
- Isolated Package with 2 kV Isolation Voltage Rating
- High Power Handling Capability — 62.5 Watts
- High Peak Current Handling Capability — 25 Amperes



MPM3002 Schematic





STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. GATE
5. MIRROR
6. KELVIN
7. SOURCE
8. MIRROR
9. GATE
10. DRAIN
11. GATE
12. SOURCE

CASE 806-02

This document contains information on a new product. Specifications and information herein are subject to change without notice.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage	(All Types)	V_{DSS}	100	Volts
Drain-to-Gate Voltage (R_{GS} = 1MΩ)	(All Types)	V_{DGR}	100	
Gate-to-Source Voltage	(All Types)	V_{GS}	±20	
Drain-to-Mirror Voltage	(Q2 and Q3)	V_{DM}	100	
Gate-to-Mirror Voltage	(Q2 and Q3)	V_{GM}	±20	
Drain Current — Continuous — Pulsed	(Q2 and Q3)	I_D I_{DM}	12 30	Amps
— Continuous — Pulsed	(Q1 and Q4)	I_D I_{DM}	8 25	
— Continuous — Pulsed	(N/P-Channel Combination)	I_D I_{DM}	8 25	
Sense Current — Continuous — Pulsed	(Q2 and Q3)	I_M I_{MM}	13 33	mA
RMS Isolation Voltage	(Any Pin to Case)	V_{ISO}	2000	Volts
Operating and Storage Temperature Range		T_J, T_{stg}	−40 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Power Dissipation — T_C = 25°C (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	P_D	 62.5 62.5 31.25	Watts
Power Derating — Derate above T_C = 25°C (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	$1/R_{\theta JC}$	 0.5 0.5 0.25	W/°C
Thermal Resistance — Junction to Case — Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2 35	°C/W
Thermal Coupling Coefficient (Q1 to Q2 or Q4 to Q3) See Table 1 (Q1 to Q3, Q1 to Q4, Q2 to Q3 or Q2 to Q4)	α β	0.5 0.01	—
Maximum Lead Temperature for Soldering Purposes 1/8″ from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{MS} = 0 unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	(All Devices)	$V_{(BR)DSS}$	100	—	—	Vdc
Drain-to-Mirror Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	(Q2 and Q3)	$V_{(BR)DMS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 80 V, V_{GS} = 0) (V_{DS} = 80 V, V_{GS} = 0, T_J = 125°C)	(Any Single Device)	I_{DSS}	 — —	 — —	 0.2 1	mAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	(Any Single Device)	I_{GSSF}	—	—	100	nAdc
Gate Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	(Any Single Device)	I_{GSSR}	—	—	100	—
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mAdc) (T_J = 125°C)	(Any Single Device)	$V_{GS(th)}$	 2 1	 3 —	 4.5 3.5	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	(Q2 and Q3)	$r_{DS(on)}$	—	—	0.15	Ohms

(continued)

3

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C, V_{MS} = 0 unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	(Q1 and Q4)	$r_{DS(on)}$	—	—	0.4	Ohms
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	(Q2 and Q3)	g_{FS}	3	—	—	Mhos
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 4 Adc)	(Q1 and Q4)	g_{FS}	2	—	—	Mhos
CURRENT SENSING CHARACTERISTICS (N-Channel, Q2 and Q3)						
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 8 A, V_{GS} = 10 V)		n	750	—	850	—
Mirror Compliance Ratio (V_{GS} = 10 Vdc, I_D = 4 Adc)		K_{mc}	—	0.78	—	—
Source Active Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc, R_S = 10 megohm)		$r_{a(on)}$	—	140	—	mΩ
Mirror Active Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{m(on)}$	—	112	—	Ohms
DYNAMIC CHARACTERISTICS (All Types)						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	—	—	900	pF
Output Capacitance		C_{oss}	—	—	450	
Transfer Capacitance		C_{rss}	—	—	200	
SWITCHING CHARACTERISTICS* (N-Channel, Q2 and Q3)						
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 4 A R_{gen} = 50 Ohms)	$t_{d(on)}$	—	—	30	ns
Rise Time		t_r	—	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	—	120	
Fall Time		t_f	—	—	125	
Total Gate Charge	(V_{DS} = 80 V, I_D = 8 A V_{GS} = 10 V)	Q_g	—	38	45	nC
Gate-Source Charge		Q_{gs}	—	15	—	
Gate-Drain Charge		Q_{gd}	—	23	—	
SWITCHING CHARACTERISTICS* (P-Channel, Q1 and Q4)						
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 4 A R_{gen} = 50 Ohms)	$t_{d(on)}$	—	—	25	ns
Rise Time		t_r	—	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		t_f	—	—	60	
Total Gate Charge	(V_{DS} = 80 V, I_D = 8 A V_{GS} = 10 V)	Q_g	—	23	30	nC
Gate-Source Charge		Q_{gs}	—	10	—	
Gate-Drain Charge		Q_{gd}	—	13	—	
SOURCE-DRAIN DIODE CHARACTERISTICS (N-Channel, Q2 and Q3)						
Forward On-Voltage	(I_S = 8 A)	V_{SD}	—	1.2	—	Vdc
Forward Turn-On Time		t_{on}	—	25	—	ns
Reverse Recovery Time		t_{rr}	—	155	—	
SOURCE-DRAIN DIODE CHARACTERISTICS (P-Channel, Q1 and Q4)						
Forward On-Voltage	(I_S = 8 A)	V_{SD}	—	4	—	Vdc
Forward Turn-On Time		t_{on}	—	25	—	ns
Reverse Recovery Time		t_{rr}	—	150	—	

*Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle = 2%.
Note 1: Handling precautions to protect against electrostatic discharge is mandatory.
Note 2: Do not use the mirror FET independent of the power FET.
Note 3: It is recommended that the mirror terminal (M) be shorted to the source terminal (S) when current sensing is not required.

TYPICAL CHARACTERISTICS

N-CHANNEL

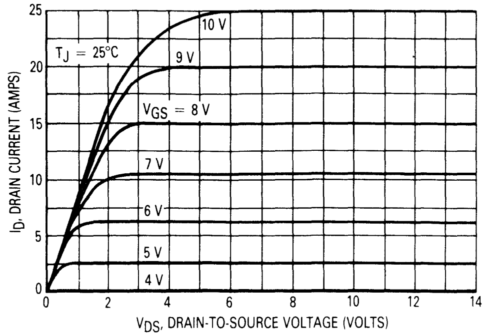


Figure 1. On-Region Characteristics

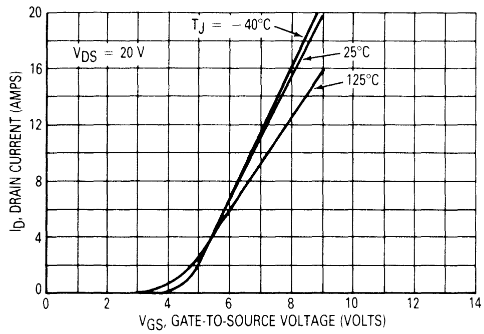


Figure 3. Transfer Characteristics

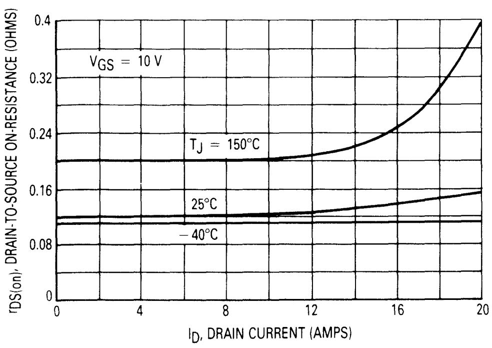


Figure 5. On-Resistance versus Drain Current

P-CHANNEL

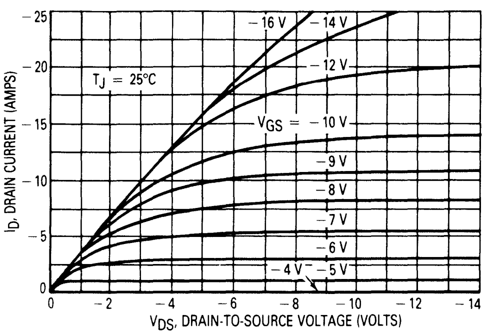


Figure 2. On-Region Characteristics

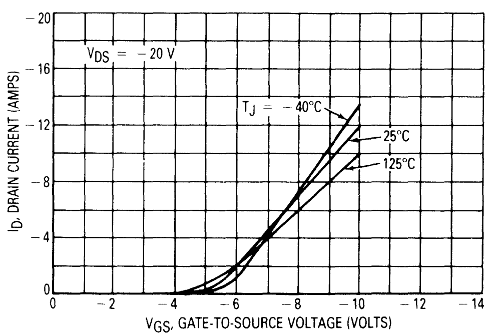


Figure 4. Transfer Characteristics

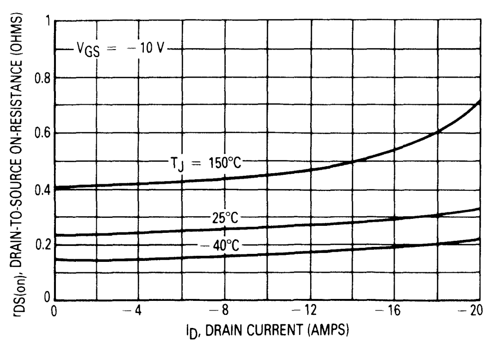


Figure 6. On-Resistance versus Drain Current

TYPICAL CHARACTERISTICS

N-CHANNEL | **P-CHANNEL**

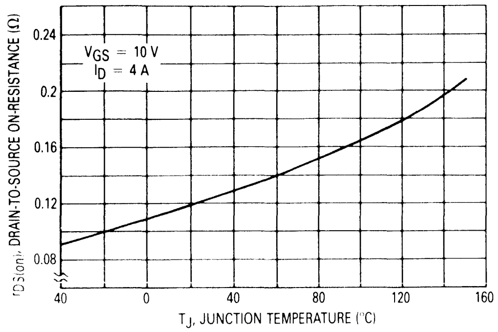


Figure 7. On-Resistance Variation with Temperature

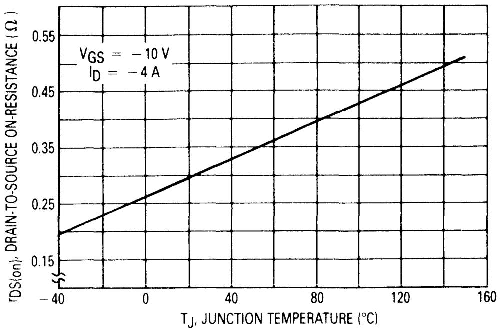


Figure 8. On-Resistance Variation with Temperature

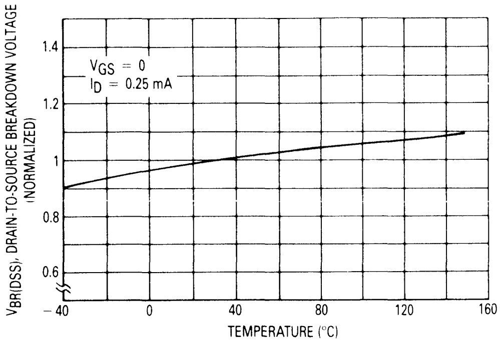


Figure 9. Drain-To-Source Breakdown Voltage Variation

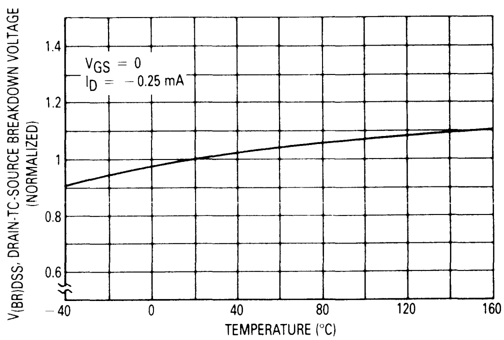


Figure 10. Drain-To-Source Breakdown Voltage Variation

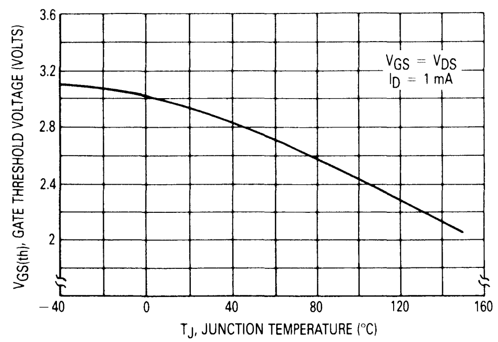


Figure 11. Gate Threshold Voltage Variation with Temperature

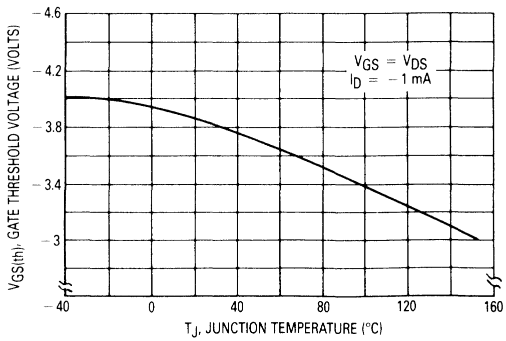


Figure 12. Gate Threshold Voltage Variation with Temperature

TYPICAL CHARACTERISTICS

N-CHANNEL | **P-CHANNEL**

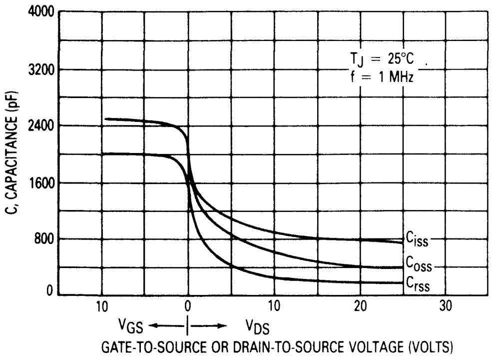


Figure 13. Capacitance Variation

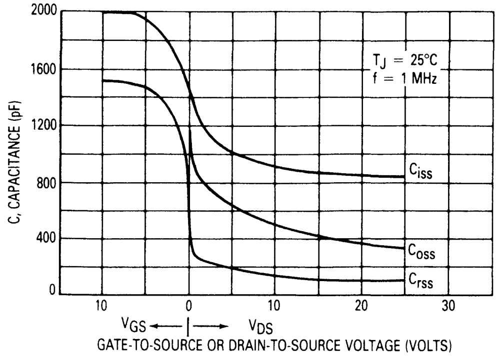


Figure 14. Capacitance Variation

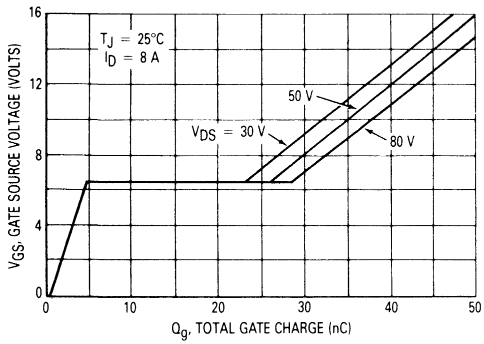


Figure 15. Stored Charge Variation

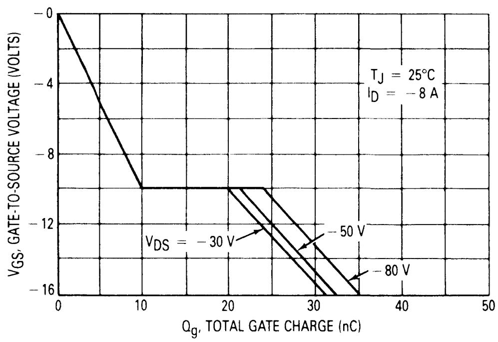


Figure 16. Stored Charge Variation

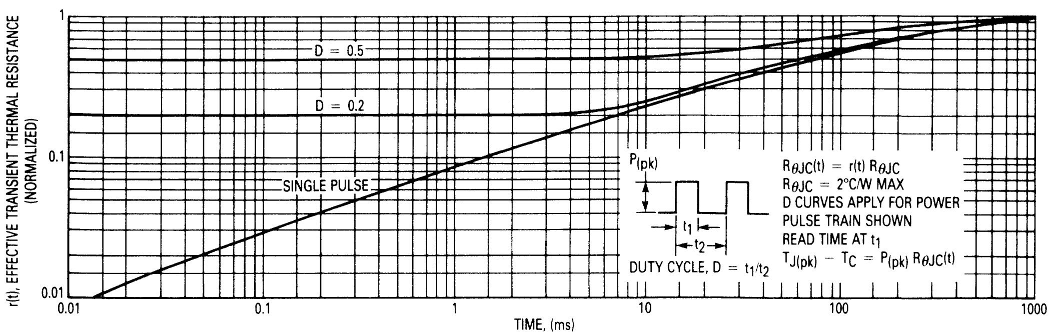


Figure 17. Thermal Response

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SAFE OPERATING AREA INFORMATION

N-CHANNEL

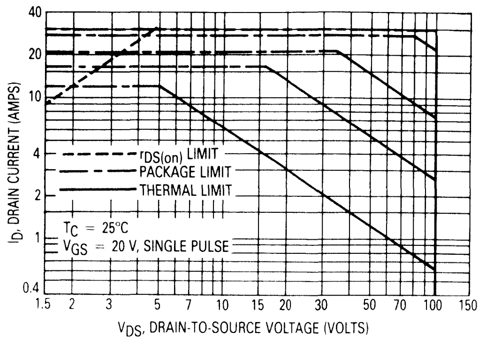


Figure 18. Maximum Rated Forward Biased Safe Operating Area

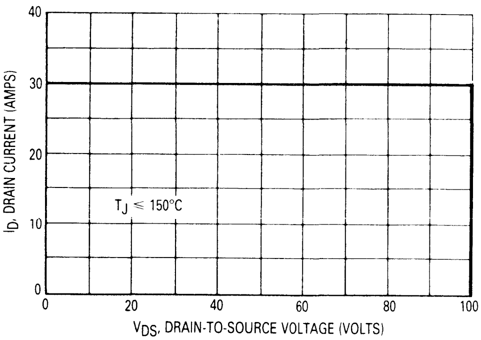


Figure 20. Maximum Rated Switching Safe Operating Area

P-CHANNEL

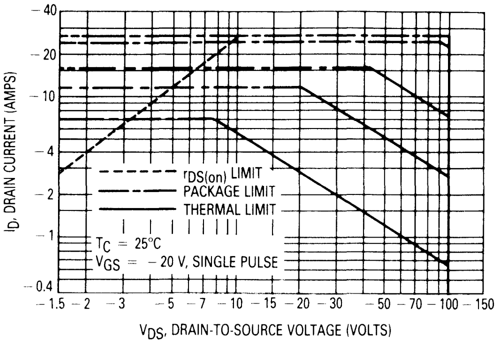


Figure 19. Maximum Rated Forward Biased Safe Operating Area

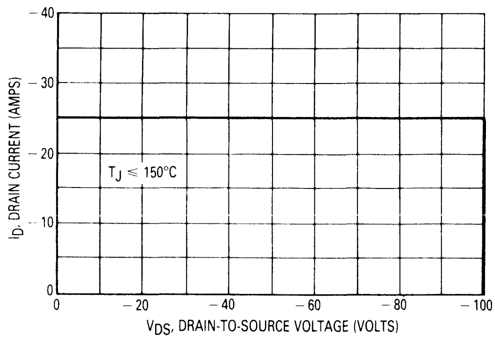


Figure 21. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figures 20 and 21 are the boundaries that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown are applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

THERMAL CONSIDERATIONS OF THE MPM3002

The MPM3002 consists of two n-channel and p-channel pairs die bonded to two separate copper leadframes. An insulating material isolates the leadframes from the aluminum case. The internal construction is shown in Figure 22 below.

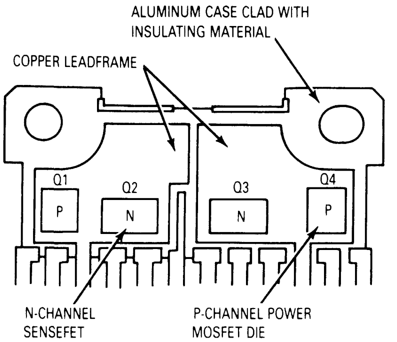


Figure 22. Internal Construction of the MPM3002

From this configuration, the simple thermal model shown in Figure 22 can be derived. Equation 3 is derived from this model. α is defined as the coupling coefficient between adjacent die on a common leadframe and β is defined as the coupling coefficient between die on separate leadframes.

EQUATION 3.

$$T_{Ji} = T_C + P_{Di}\,R_{\theta JC} + \sum_{K=1}^{4} \alpha_{ik}\,P_{Dk}\,R_{\theta JC} + \sum_{K=1}^{4} \beta_{ik}\,P_{Dk}\,R_{\theta JC}$$

α and β values for different die combinations are listed in the maximum ratings. As an example of how the equation is used, assume that devices Q1 and Q3 are dissipating 10 watts each at a case temperature of 25°C, then calculate the junction temperature of Q1 and Q4.

FROM EQUATION 3,

$$T_{J1} = T_C + P_{D1}R_{\theta JC} + \beta_{13}\,P_{D3}R_{\theta JC}$$
$$= 25 + (10)(2) + (0.01)(10)(2) = 47°C$$

and

$$T_{J4} = T_C + \alpha_{43}P_{D3}R_{\theta JC} + \beta_{41}\,P_{D1}R_{\theta JC}$$
$$= 25 + (0.5)(10)(2) + (0.01)(10)(2) = 37°C.$$

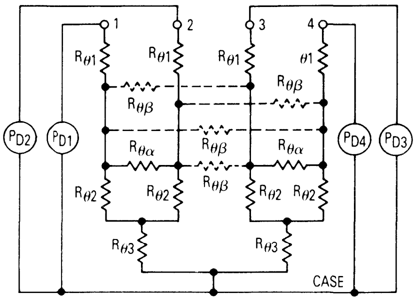


Figure 23. Thermal Model of the MPM3002

$R_{\theta 1}$ = junction to leadframe thermal resistance
$R_{\theta 2}$ = leadframe to isolator thermal resistance
$R_{\theta 3}$ = isolator to case thermal resistance
$R_{\theta \alpha}$ = coupling thermal resistance between adjacent die on common leadframe
$R_{\theta \beta}$ = coupling thermal resistance between die on separate leadframes
$R_{\theta JC} = R_{\theta 1} + R_{\theta 2} + R_{\theta 3}$

Table 1. Thermal Coupling Coefficients

α = coupling coefficient between adjacent die on same leadframe
β = coupling coefficient between die on separate leadframes

A: α coefficient values:

$\alpha_{11} = \alpha_{22} = \alpha_{33} = \alpha_{44} = 0$
$\alpha_{13} = \alpha_{31} = \alpha_{23} = \alpha_{32} = \alpha_{14} = \alpha_{41} = \alpha_{24} = \alpha_{42} = 0$
$\alpha_{12} = \alpha_{21} = \alpha_{34} = \alpha_{43} = 0.5$

B: β coefficient values

$\beta_{11} = \beta_{22} = \beta_{33} = \beta_{44} = 0$
$\beta_{12} = \beta_{21} = \beta_{34} = \beta_{43} = 0$
$\beta_{13} = \beta_{31} = \beta_{23} = \beta_{32} = \beta_{14} = \beta_{41} = \beta_{24} = \beta_{42} = 0.01$

USING SENSEFETs

Assuming a fully switched on SENSEFET, current sensing can be modeled with the simple resistor divider network shown in Figure 24. In this model, r_b is the bulk drain resistance, $r_{m(on)}$ is the active mirror on-resistance, $r_{a(on)}$ is the power section's active on-resistance and r_w is the source wire bond resistance. Using values for $r_{a(on)}$ and $r_{m(on)}$ from the electrical characteristics table; V_{SENSE}, R_{SENSE}, and drain current may be calculated from the following sensing equations.

SENSING EQUATIONS:

1. $V_{SENSE} = I_D\, r_{a(on)}\, R_{SENSE}/[R_{SENSE} + r_{m(on)}]$
2. $R_{SENSE} = V_{SENSE}\, r_{m(on)}/[I_D\, r_{a(on)} - V_{SENSE}]$
3. $I_D = V_{SENSE}\, (R_{SENSE} + r_{m(on)})/r_{a(on)}\, R_{SENSE}$
4. $n = I_D/I_{SENSE}$; where $R_{SENSE} = 0$
5. $r_{a(on)} = r_{m(on)}/n$

Shown in Figure 25 is the variation of sense voltage, V_{SENSE} with drain current. When designing with SENSEFETs there are several factors to keep in mind.

They are described as follows:

- Maximum Sense Voltage: The maximum sense voltage that can appear at the mirror terminal is $(r_{a(on)}/r_{a(on)} + r_b) \times V_{DS(on)}$. This ratio is called the mirror compliance ratio, K_{MC}, and defines the upper boundary for sense voltage.
- Accuracy: Accurate current sensing is based upon the inherent matching of $r_{m(on)}$ with the power section's active on-resistance, $r_{a(on)}$. When $R_{SENSE} = 0$, matching and current sensing accuracy are within ±3%. As R_{SENSE} is increased, sensing accuracy is reduced since mirror current becomes dependent on the ratio of internal on-resistance to an external R_{SENSE}. From a practical point of view, relatively good sensing accuracy (±10%) is maintained up to $R_{SENSE} = r_{m(on)}/2$. As R_{SENSE} is increased beyond $r_{m(on)}$, sensing accuracy decreases rapidly.
- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop errors in this kind of an application is a first order design consideration. Internal wire bond resistance, contact resistance, and external wiring resistance are all significant. Therefore, it is important to reference sense voltage measurement circuitry to the Kelvin pin rather than power ground. In addition, referencing gate drive to the Kelvin pin rather than power ground will provide faster switching speeds.
- Noise Suppression: Switching noise is also a first order design issue. Layout, therefore, is critical. In addition, a single pole RC filter between R_{SENSE} and the current sensing circuitry's input terminals is often desirable. A 1 μsec time constant is generally long enough to provide adequate noise suppression and short enough to provide adequate protection during overloads. An illustration is provided in Figure 26.
- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET is likely due to excessive power dissipation. By syncing current limiting to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Parasitic Diode: In addition to the power section's usual source-drain diode, there is a mirror-drain diode in the sense cells. Like the source-drain diode, the mirror-drain diode conducts during the reverse-mode operation, however, current sense characteristics are defined only in the forward-mode operation.
- Reverse Recovery: In bridge circuits, when a SENSEFET's source-drain diode is commutated a voltage spike is produced at the mirror. This spike is short since it lasts only for the drain-source diode's reverse recovery time. However, its amplitude can be an order of magnitude larger than normal sense voltages and produce unwanted overcurrent trips. Blanking, filtering, or other suppression techniques may be required in some applications.

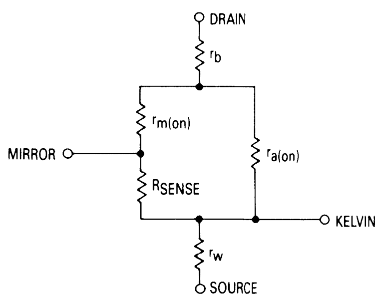


Figure 24. SENSEFET Model

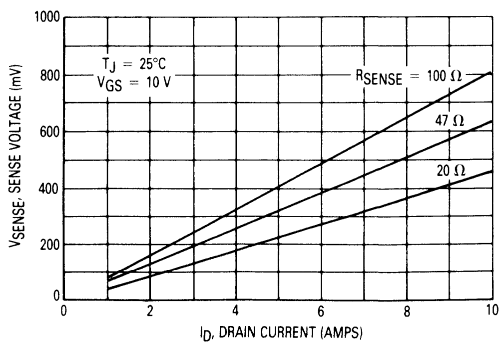


Figure 25. Sense Voltage versus Drain Current

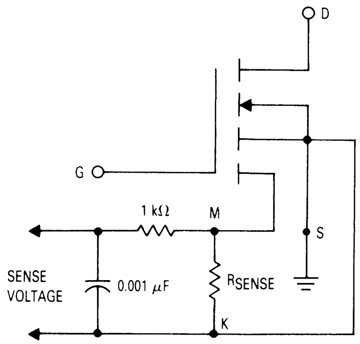
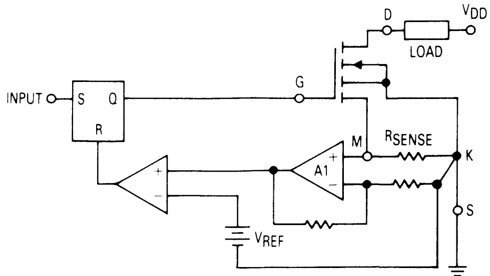


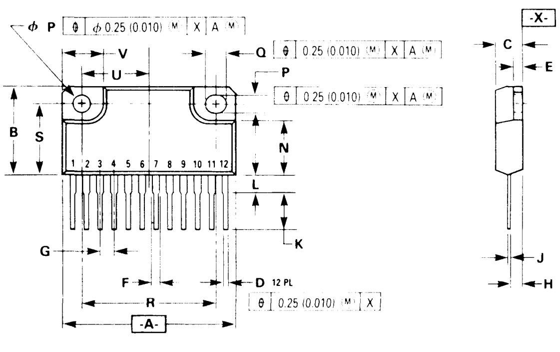
Figure 26. SENSEFET with Noise Suppression



Set A1 gain to match sense voltage to V_{REF} at max I_D.

Figure 27. Typical Current Sensing with a SENSEFET

OUTLINE DIMENSIONS



CASE 806-02

STYLE 3:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. GATE
5. MIRROR
6. KELVIN
7. SOURCE
8. MIRROR
9. GATE
10. DRAIN
11. GATE
12. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.30	31.70	1.230	1.250
B	15.80	16.20	0.622	0.638
C	4.98	5.20	0.196	0.205
D	0.69	0.99	0.027	0.390
E	1.48	1.82	0.058	0.072
F	0.69	1.01	0.027	0.040
G	2.54 BSC		0.100 BSC	
H	2.09	2.31	0.082	0.091
J	0.38	0.71	0.015	0.028
K	6.10	6.98	0.240	0.275
L	3.56	4.06	0.140	0.160
N	9.66	10.41	0.380	0.410
P	3.10	3.30	0.122	0.130
Q	3.69	3.91	0.145	0.154
R	24.38 BSC		0.960 BSC	
S	13.00 BSC		0.512 BSC	
U	12.20 BSC		0.480 BSC	
V	7.37	7.74	0.290	0.305

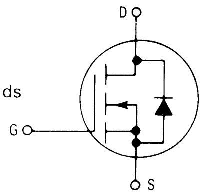
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD1N40

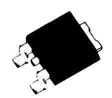
Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

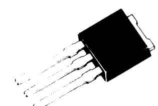
- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 5 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix



TMOS POWER FET
1 AMPERE
$r_{DS(on)}$ = 5 OHMS
400 VOLTS

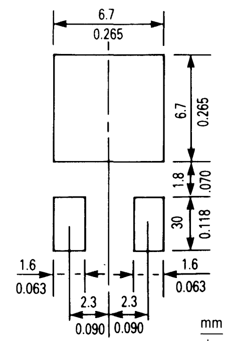


CASE 369A-04
TO-252
MTD1N40



CASE 369-03
TO-251
MTD1N40-1

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	1 3	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	400	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	 — —	 0.2 1	mAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$r_{DS(on)}$	—	5	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1 Adc) (I_D = 0.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 6.5 5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 0.5 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	300	pF
Output Capacitance		C_{oss}	—	30	
Reverse Transfer Capacitance		C_{rss}	—	10	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	35	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	9 (Typ)	11	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	2 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

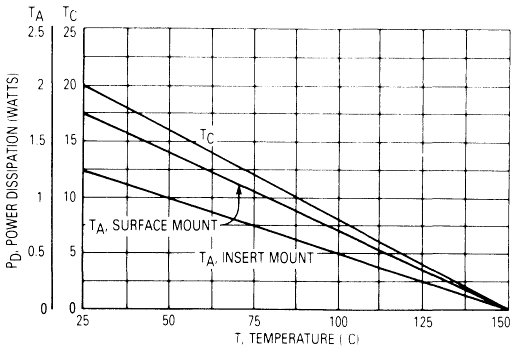


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

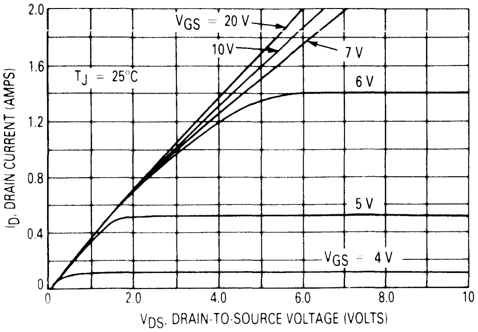


Figure 2. On-Region Characteristics

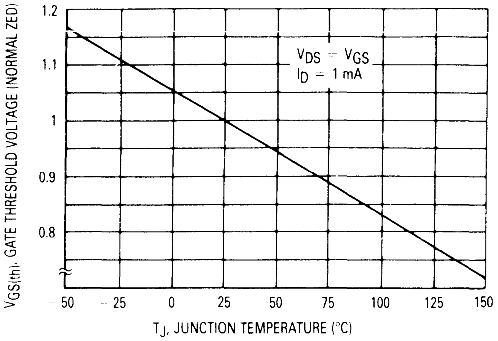


Figure 3. Gate-Threshold Voltage Variation With Temperature

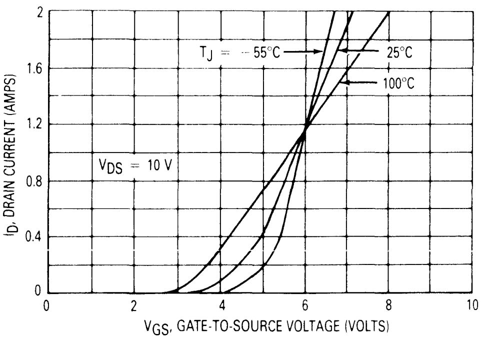


Figure 4. Transfer Characteristics

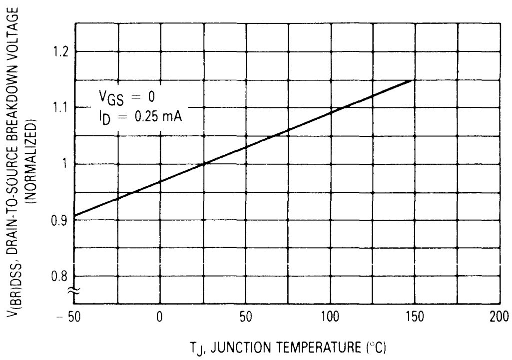


Figure 5. Breakdown Voltage Variation With Temperature

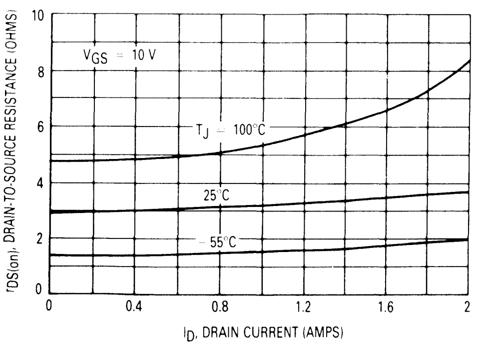


Figure 6. On-Resistance versus Drain Current

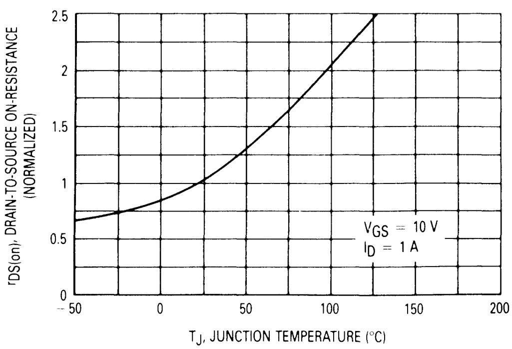


Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

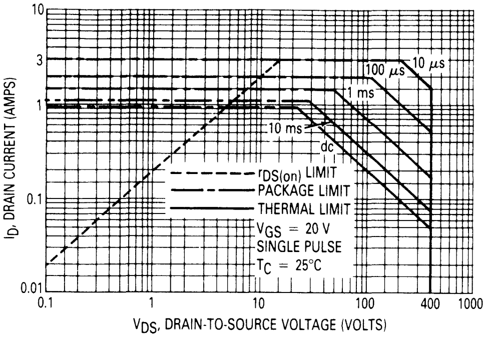


Figure 8. Maximum Rated Forward Biased Safe Operating Area

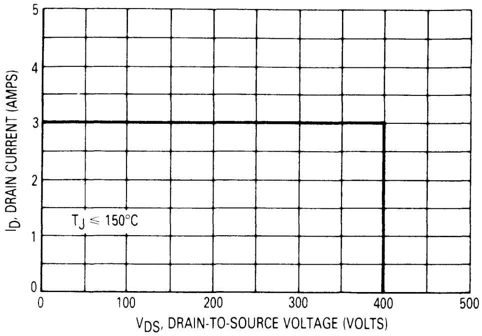


Figure 9. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

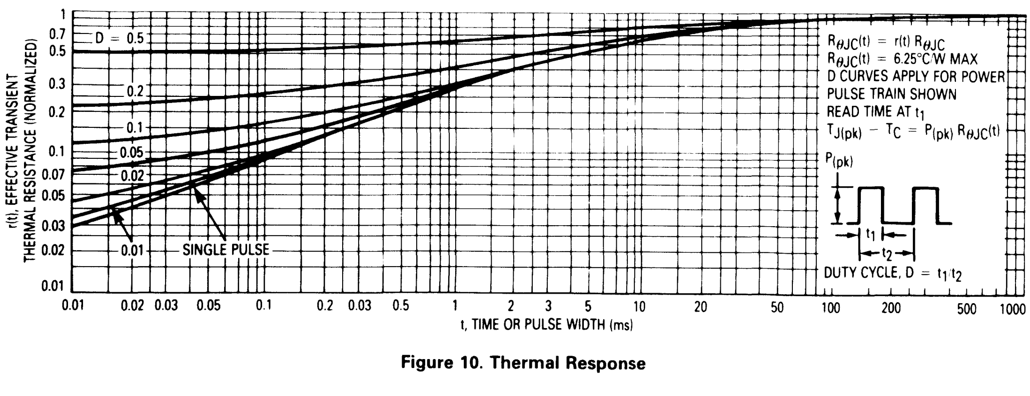


Figure 10. Thermal Response

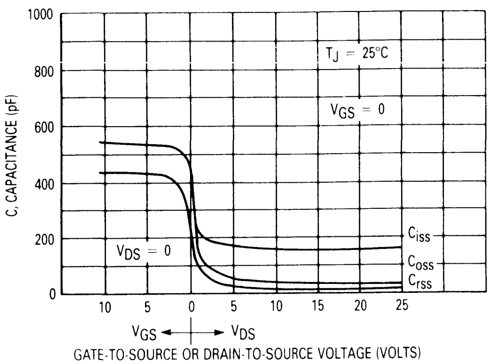


Figure 11. Capacitance Variation

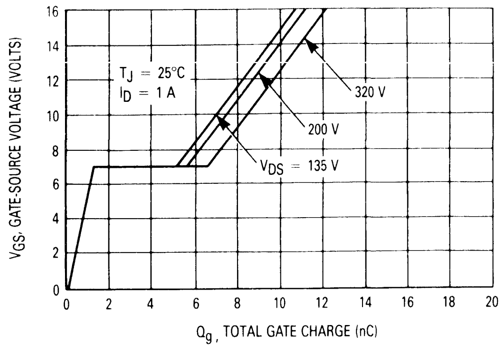


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

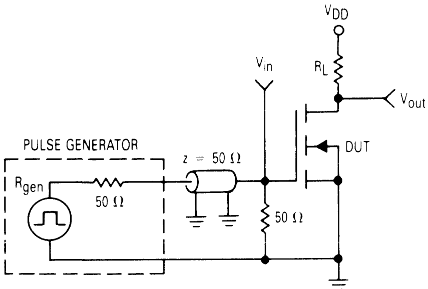


Figure 13. Switching Test Circuit

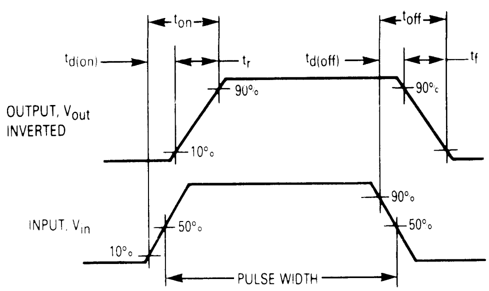
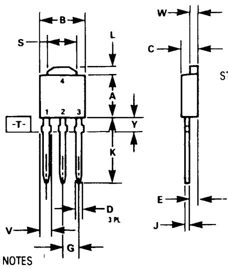


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 369-03
TO-251
MTD1N40-1

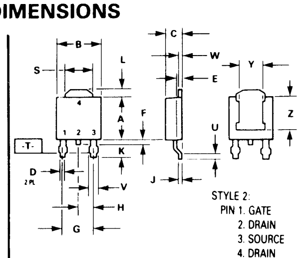


STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04
TO-252
MTD1N40



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD2N20

Designer's Data Sheet

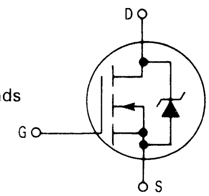
Power Field Effect Transistor

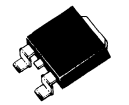
N-Channel Enhancement-Mode
Silicon Gate TMOS
DPAK for Surface Mount or Insertion Mount

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 1.5 OHMS
200 VOLTS

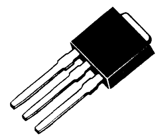
These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 1.5 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix





CASE 369A-04
MTD2N20



CASE 369-03
MTD2N20-1

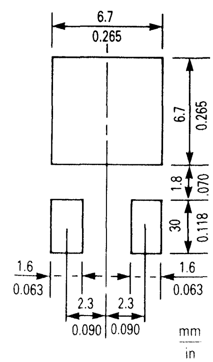
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 11	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	5	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	°C/W

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

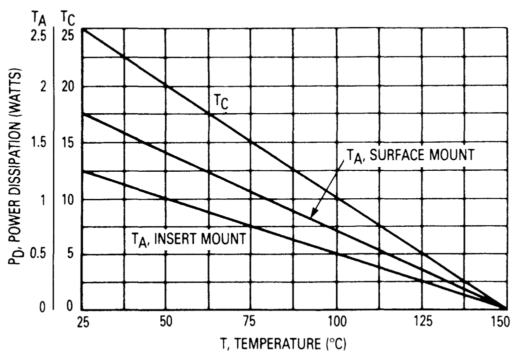
3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (T_J = 125°C)		I_{DSS}	— —	1 10	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 125°C)		$V_{GS(th)}$	2 1.3	4.5 3.8	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	1.5	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3 2.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	220 (Typ)	—	pF
Output Capacitance		C_{oss}	60 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	10 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 1 A, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	12 (Typ)	—	ns
Rise Time		t_r	18 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	35 (Typ)	—	
Fall Time		t_f	18 (Typ)	—	
Total Gate Charge	(V_{DS} = 160 V, I_D = 2 A, V_{GS} = 10 V) See Figure 12	Q_g	6.4 (Typ)	12	nC
Gate-Source Charge		Q_{gs}	1.2 (Typ)	—	
Gate-Drain Charge		Q_{gd}	3 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	I_S = 2 A, V_{GS} = 0	V_{SD}	1.1 (Typ)	1.8	Vdc
Forward Turn-On Time	I_S = 2 A, dI_S/dt = 400 A/μs V_R = 50 V	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	60 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Figure 1. Power Derating



TYPICAL ELECTRICAL CHARACTERISTICS

Figure 2. On-Region Characteristics

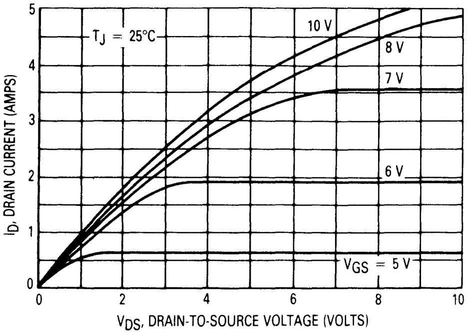


Figure 3. Gate-Threshold Voltage Variation With Temperature

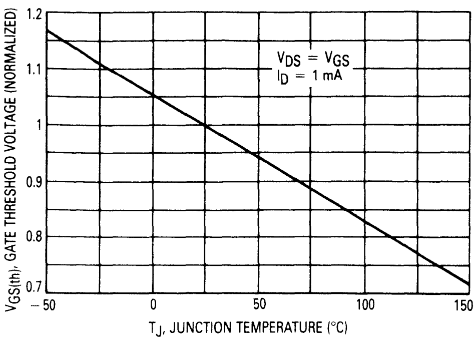


Figure 4. Transfer Characteristics

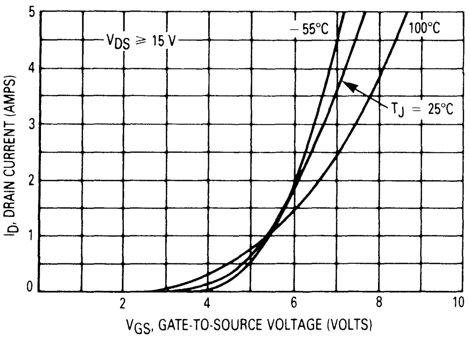


Figure 5. Breakdown Voltage Variation With Temperature

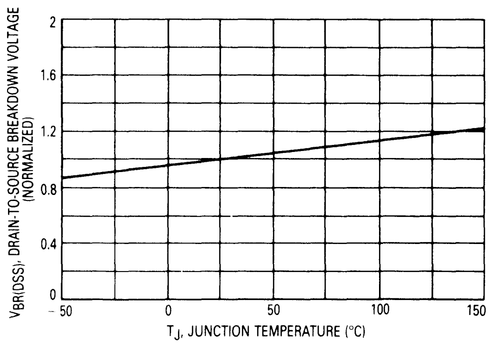


Figure 6. On-Resistance versus Drain Current

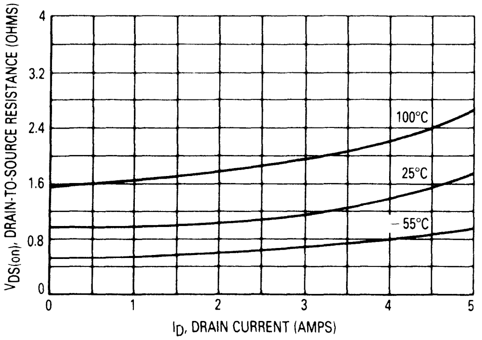


Figure 7. On-Resistance Variation With Temperature

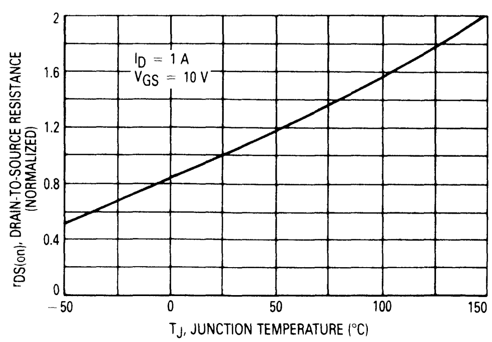


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Figure 8. Maximum Rated Forward Biased Safe Operating Area

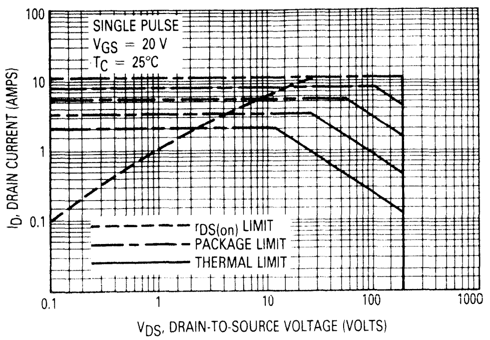
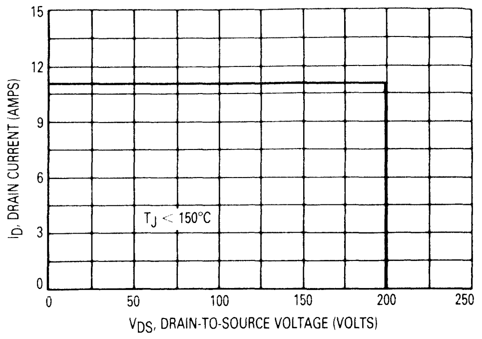


Figure 9. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 10. Thermal Response

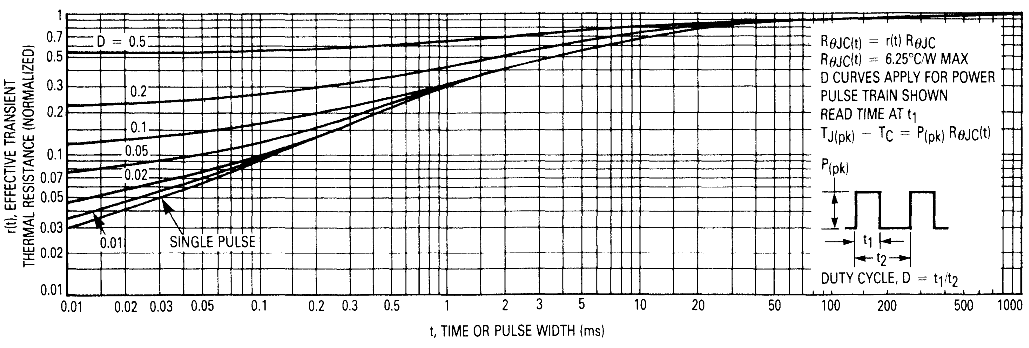


Figure 11. Capacitance Variation

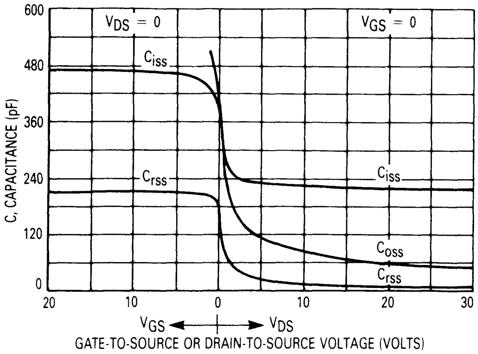
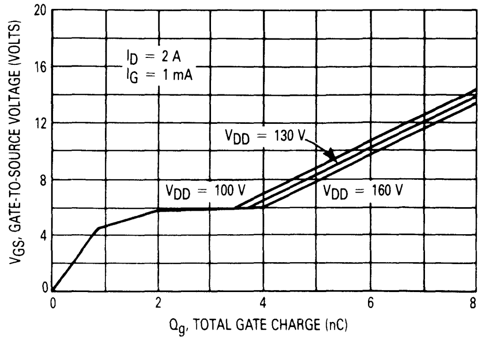


Figure 12. Gate Charge versus Gate-to-Source Voltage



RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

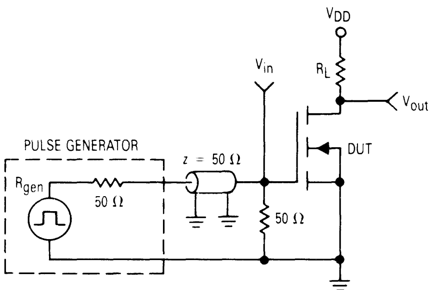
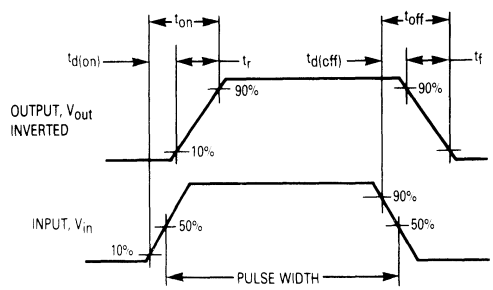
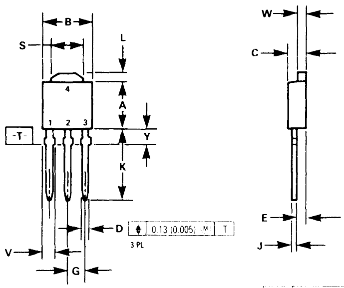


Figure 14. Switching Waveforms



OUTLINE DIMENSIONS

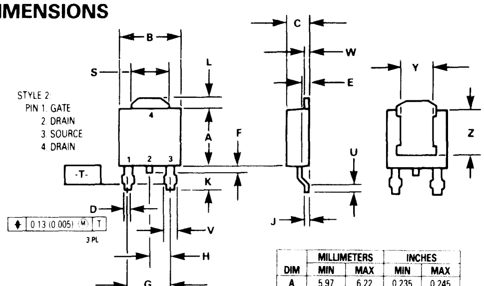


STYLE 2
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE
2 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
3 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369-03
MTD2N20-1



STYLE 2
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 SURFACE "T" IS BOTH A DATUM AND A SEATING PLANE
2 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
3 CONTROLLING DIMENSION INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

CASE 369A-04
MTD2N20

3

Figure 15. Switching Time versus Gate-to-Source Resistance

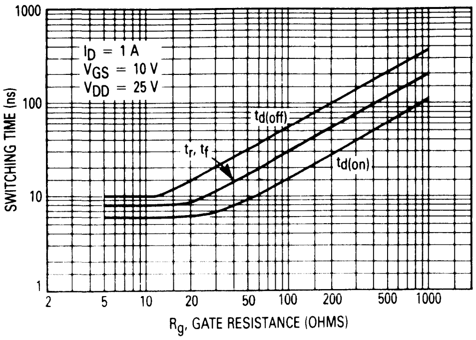


Figure 16. Diode Switching Waveform

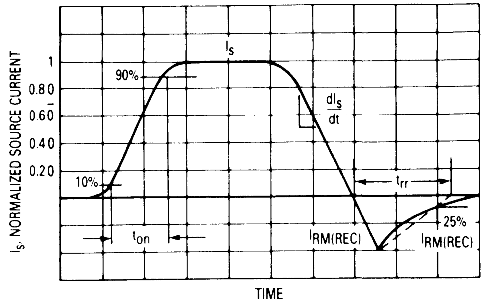
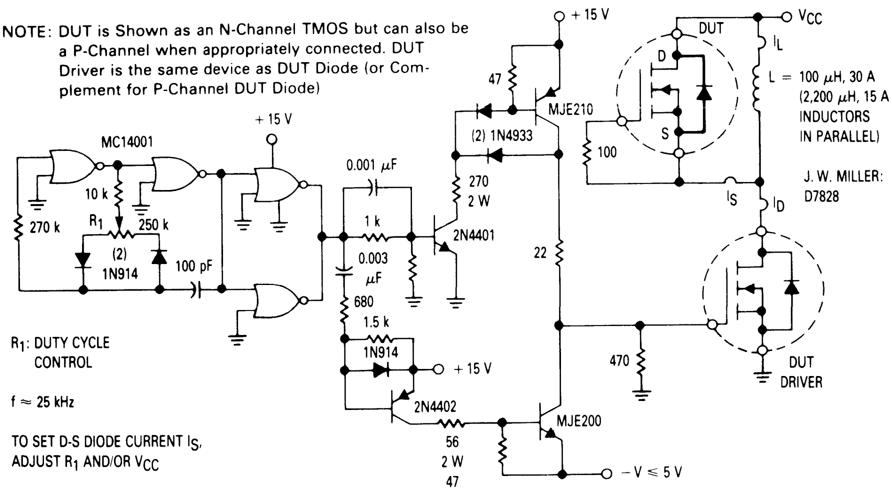


Figure 17. TMOS Diode Switching Test Circuit

NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)



R_1: DUTY CYCLE CONTROL

f ≈ 25 kHz

TO SET D-S DIODE CURRENT I_S, ADJUST R_1 AND/OR V_{CC}

MTD2N50

Designer's Data Sheet

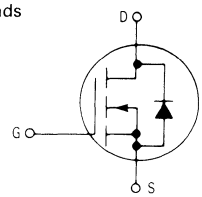
Power Field Effect Transistor

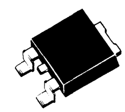
N-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

TMOS POWER FET
2 AMPERES
$r_{DS(on)}$ = 4 OHMS
500 VOLTS

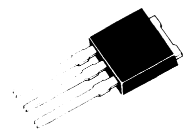
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 4 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix





CASE 369A-04
TO-252
MTD2N50



CASE 369-03
TO-251
MTD2N50-1

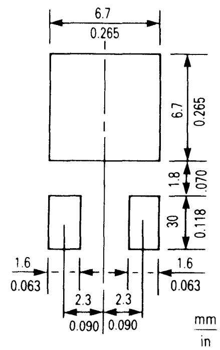
MAXIMUM RATINGS

Rating	Symbol	MTD2N50	Unit
Drain-Source Voltage	V_{DSS}	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 4	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	°C/W

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	500	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.2	mAdc
T_J = 125°C			—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	4	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 2 Adc)			—	10	
(I_D = 1 Adc, T_J = 100°C)			—	8	
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	
Reverse Transfer Capacitance		C_{rss}	—	50	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	60	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	17 (Typ)	25	nC
Gate-Source Charge		Q_{gs}	9 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

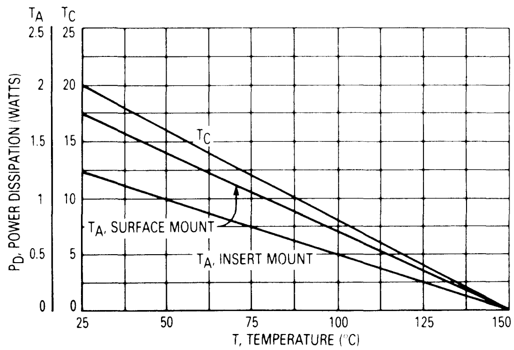


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

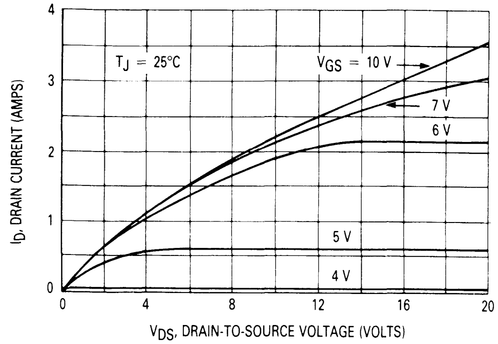


Figure 2. On-Region Characteristics

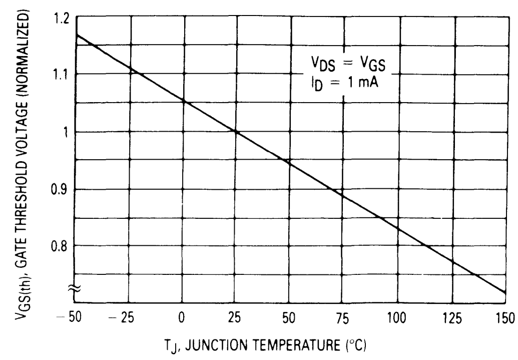


Figure 3. Gate-Threshold Voltage Variation With Temperature

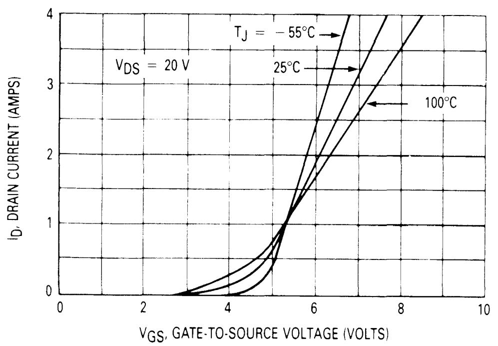


Figure 4. Transfer Characteristics

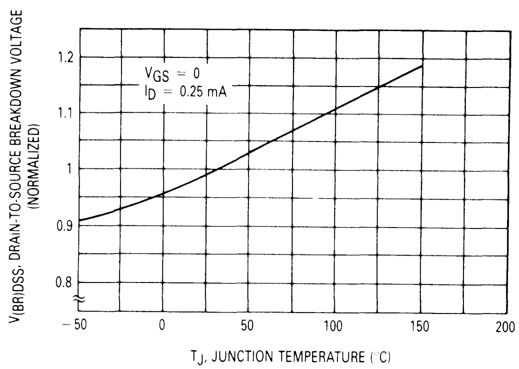


Figure 5. Breakdown Voltage Variation With Temperature

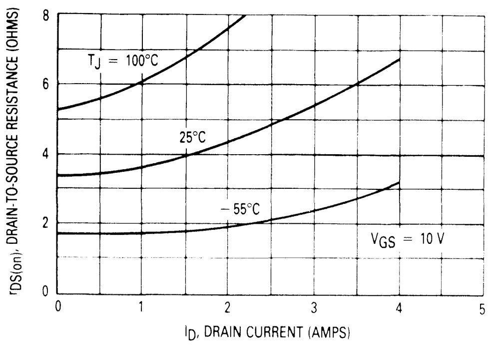


Figure 6. On-Resistance versus Drain Current

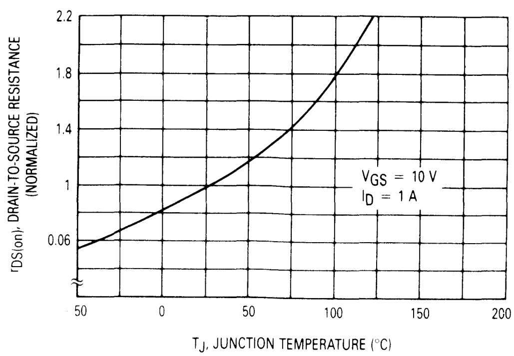


Figure 7. On-Resistance Variation With Temperature

3

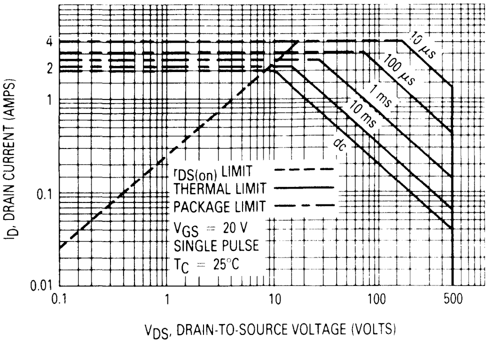


Figure 8. Maximum Rated Forward Biased Safe Operating Area

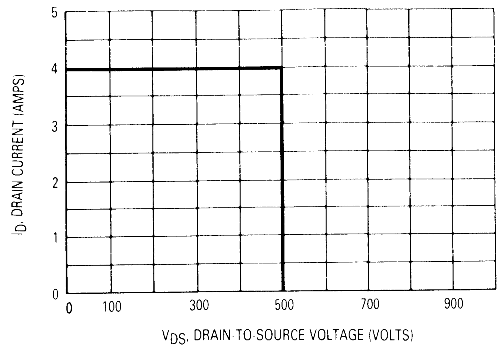


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

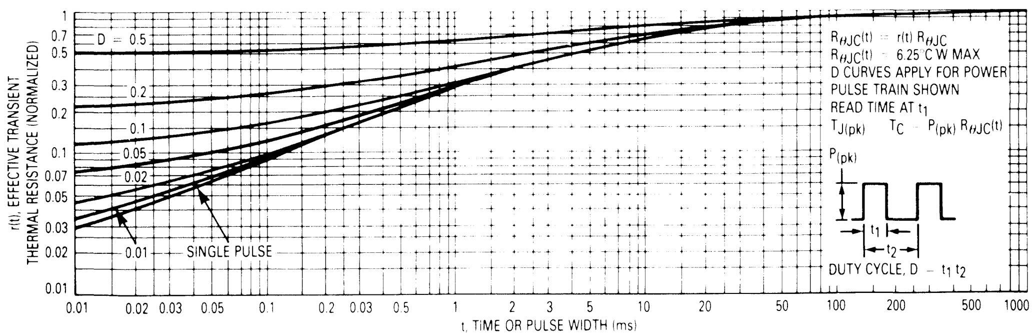


Figure 10. Thermal Response

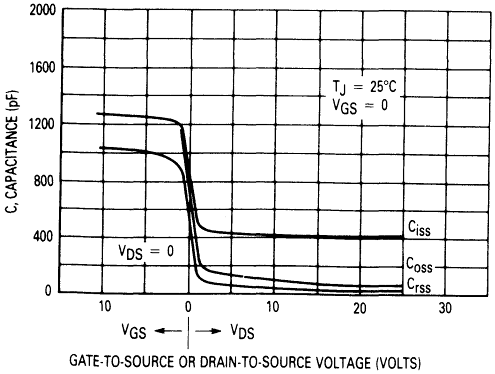


Figure 11. Capacitance Variation

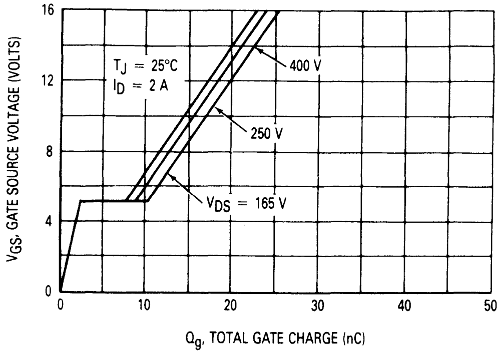


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

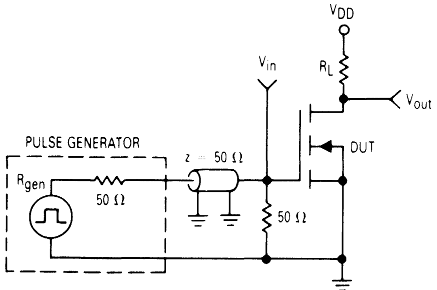


Figure 13. Switching Test Circuit

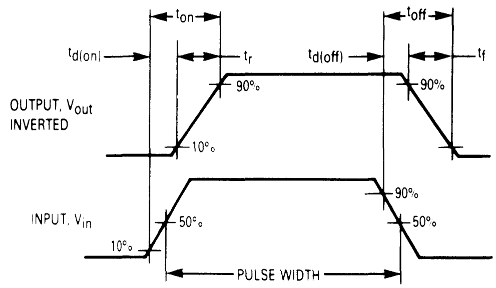
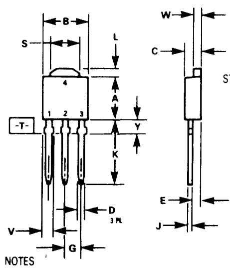


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

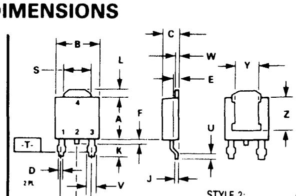


STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 369-03
TO-251
MTD2N50-1

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. ⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 369A-04
TO-252
MTD2N50

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. ⌖ 0.13 (0.005) Ⓜ T
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4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD4N20

Advance Information

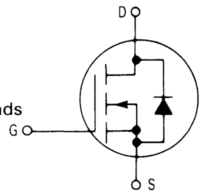
Power Field Effect Transistor

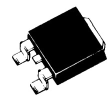
N-Channel Enhancement-Mode
Silicon Gate TMOS
DPAK for Surface Mount
or Insertion Mount

TMOS POWER FET
4 AMPERES
$r_{DS(on)}$ = 0.7 OHM
200 VOLTS

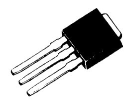
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.7 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix





CASE 369A-04
TO-252
MTD4N20



CASE 369-03
TO-251
MTD4N20-1

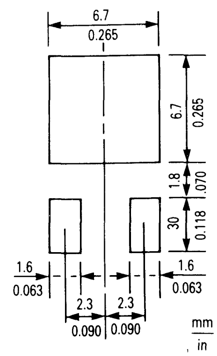
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	4 12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	 — —	 10 100	μAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	0.7	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4 Adc) (I_D = 2 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 3.4 2.9	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	700	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	9 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

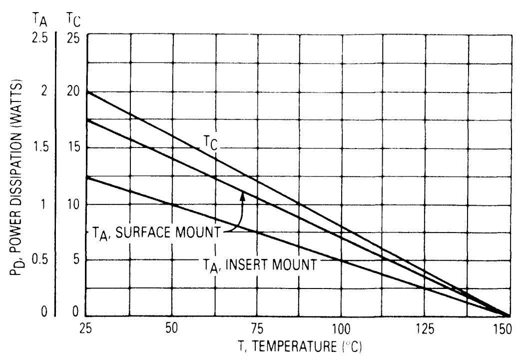


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

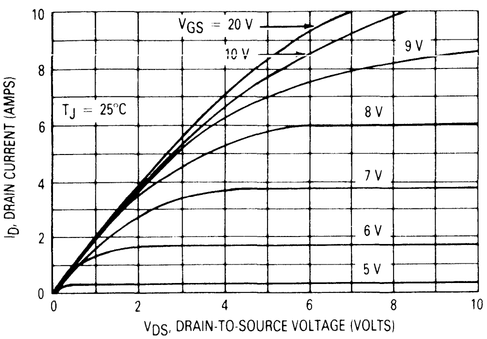


Figure 2. On-Region Characteristics

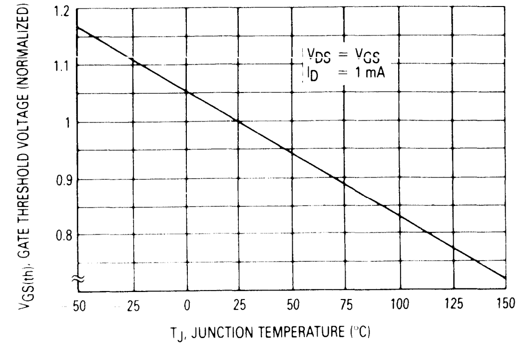
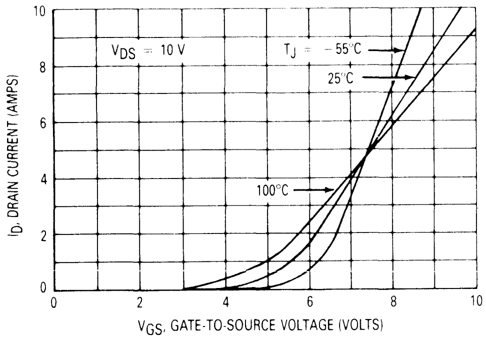


Figure 3. Gate-Threshold Voltage Variation With Temperature



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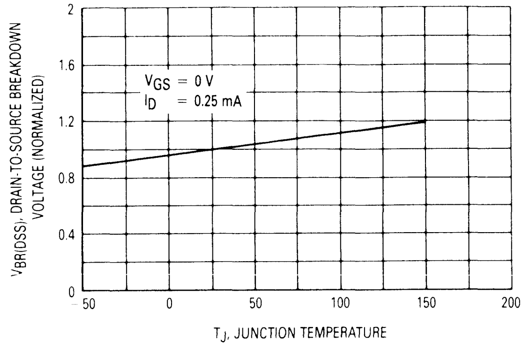

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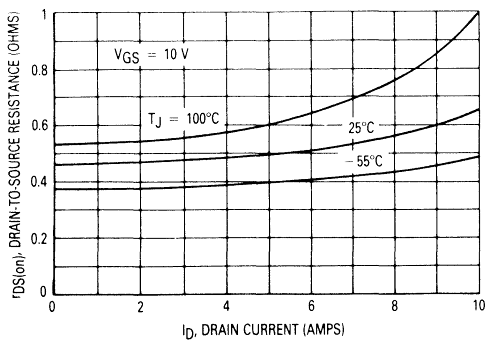

Figure 6. On-Resistance versus Drain Current

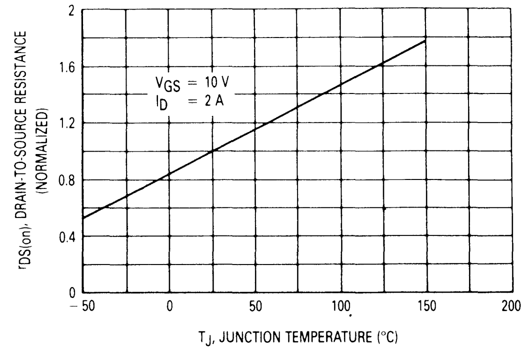

Figure 7. On-Resistance Variation With Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

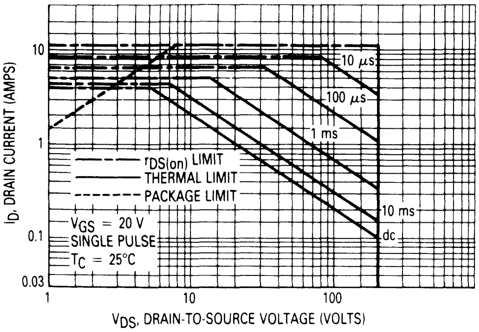

Figure 8. Maximum Rated Forward Biased Safe Operating Area

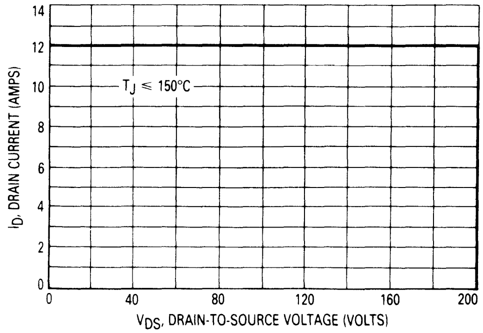

Figure 9. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

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$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

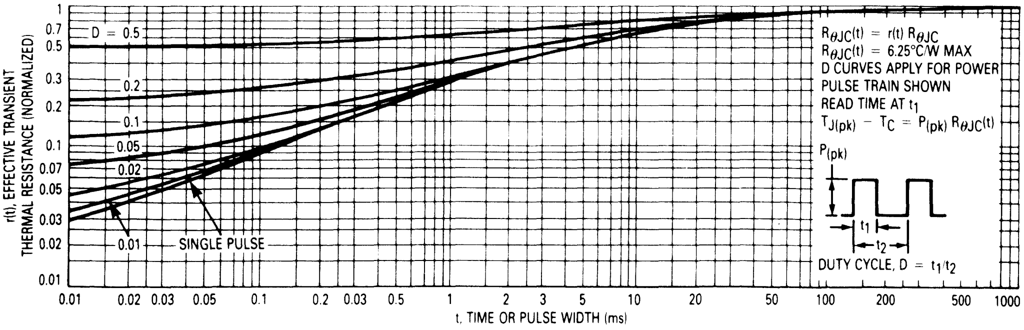


Figure 10. Thermal Response

3

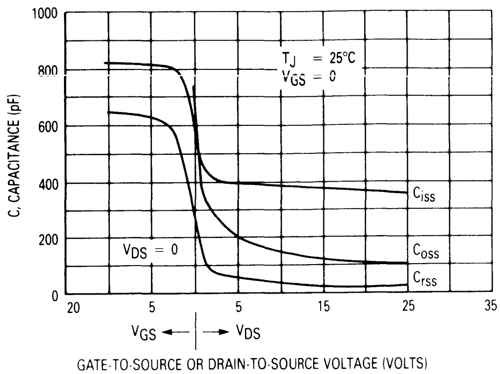


Figure 11. Capacitance Variation

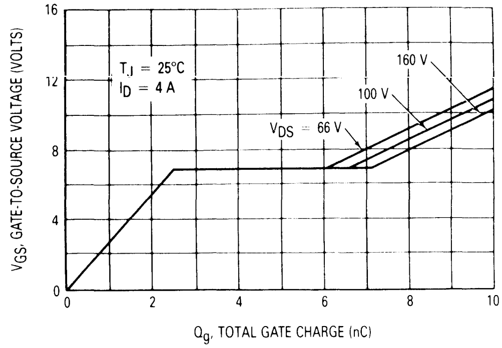


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

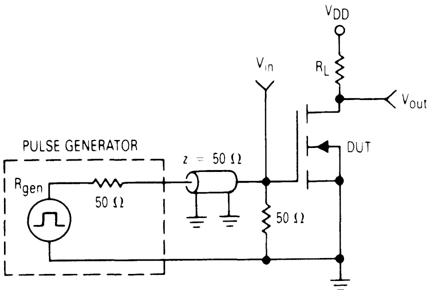


Figure 13. Switching Test Circuit

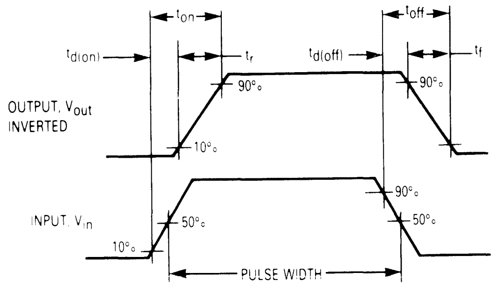
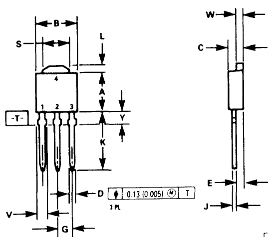


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
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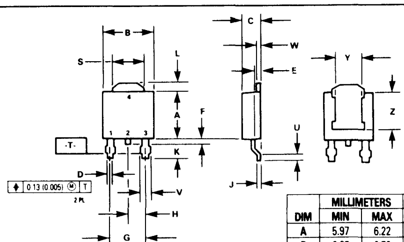
Y	1.91	2.28	0.075	0.090

CASE 369-03
TO-251
MTD4N20-1



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A SEATING PLANE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
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F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

CASE 369A-04
TO-252
MTD4N20

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD4P05
MTD4P06

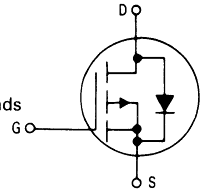
Designer's Data Sheet

Power Field Effect Transistors

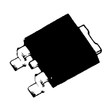
P-Channel Enhancement Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

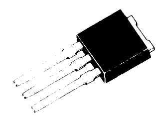
- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.3 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix



TMOS POWER FETs
4 AMPERES
$r_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS

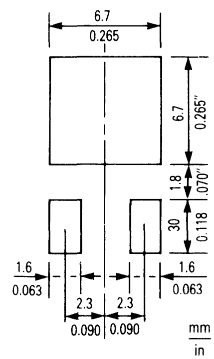


CASE 369A-04
TO-252
MTD4P05
MTD4P06



CASE 369-03
TO-251
MTD4P05-1
MTD4P06-1

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MTD4P05	MTD4P06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	4 14		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01		Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTD4P05 MTD4P06	$V_{(BR)DSS}$	 50 60	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	 — —	 0.2 1	mAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4 Adc) (I_D = 2 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2.4 2.4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 12	C_{iss}	—	700	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 10, 14 and 15	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f	—	70	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 13	Q_g	12 (Typ)	16	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.8 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

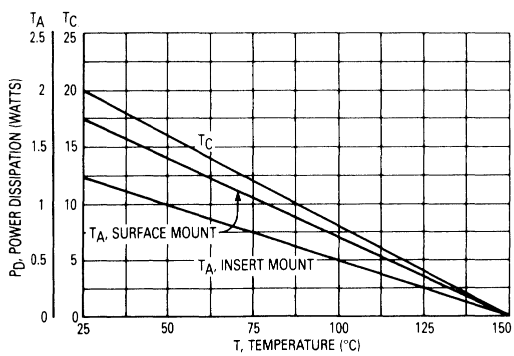


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

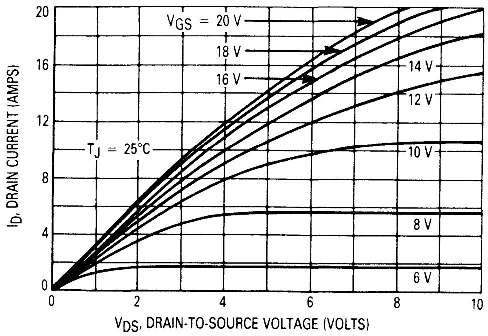


Figure 2. On-Region Characteristics

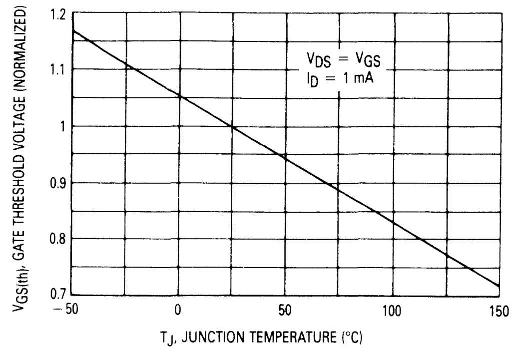


Figure 3. Gate-Threshold Voltage Variation With Temperature

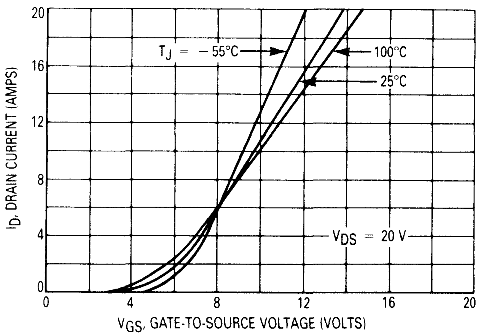


Figure 4. Transfer Characteristics

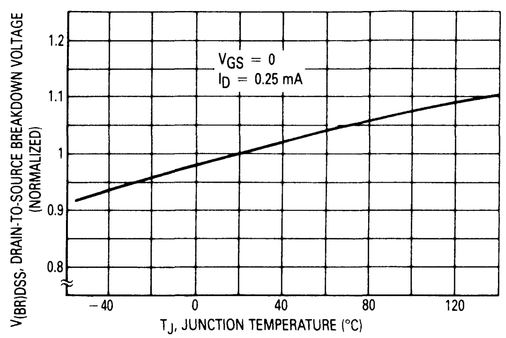


Figure 5. Breakdown Voltage Variation With Temperature

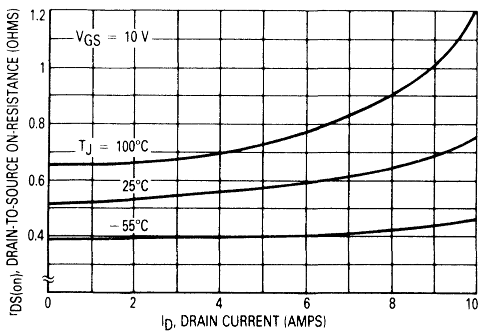


Figure 6. On-Resistance versus Drain Current

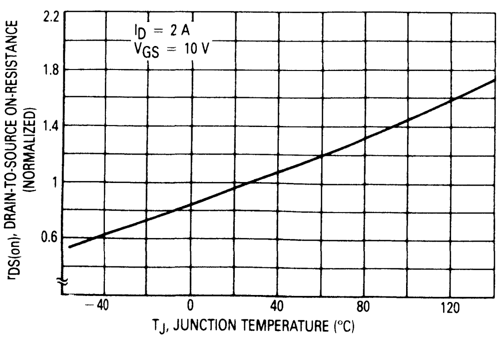


Figure 7. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

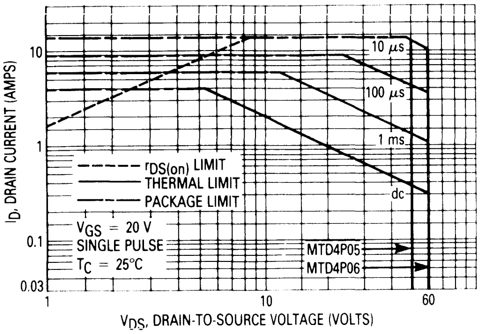


Figure 8. Maximum Rated Forward Bias Safe Operating Area

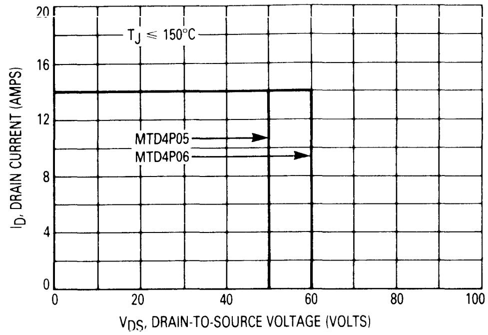


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

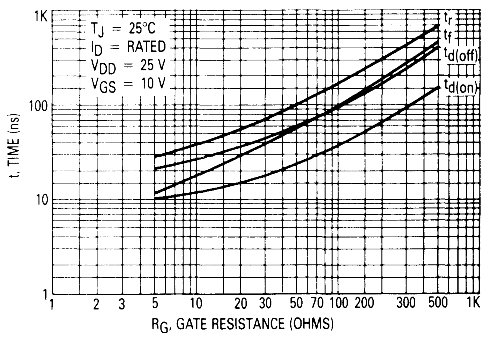


Figure 10. Resistive Switching Time Variation With Gate Resistance

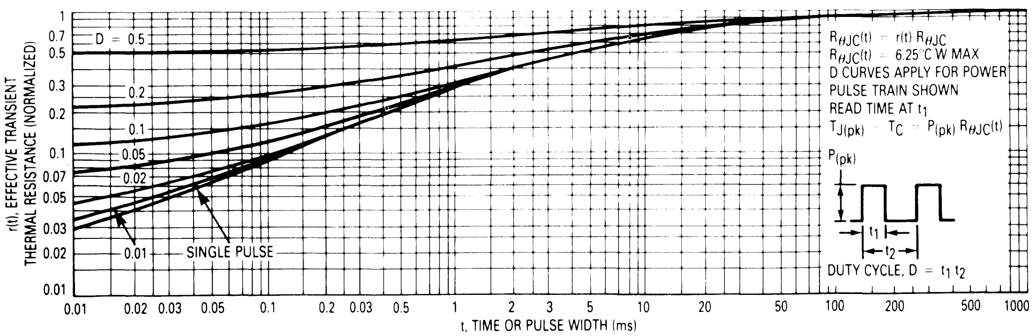


Figure 11. Thermal Response

TYPICAL CHARACTERISTICS

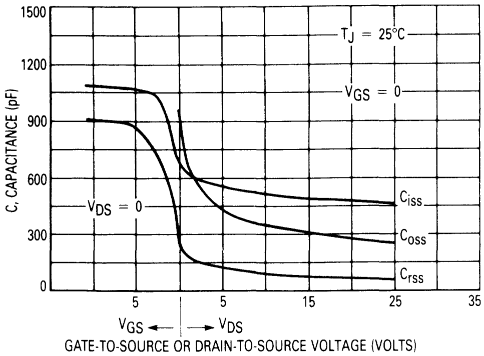


Figure 12. Capacitance Variation

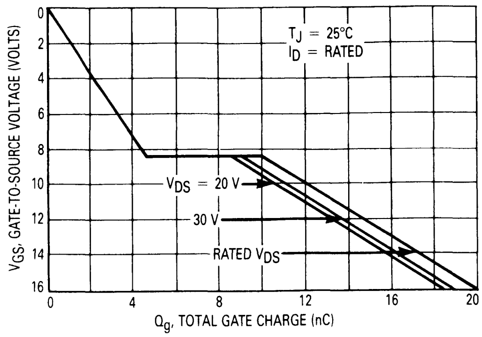


Figure 13. Gate Charge versus Gate-To-Source Voltage

3

RESISTIVE SWITCHING

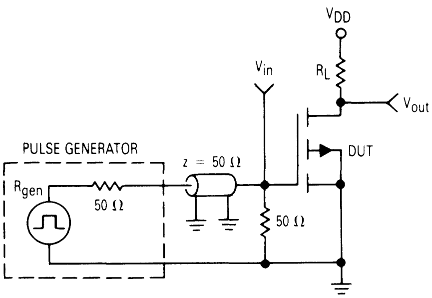


Figure 14. Switching Test Circuit

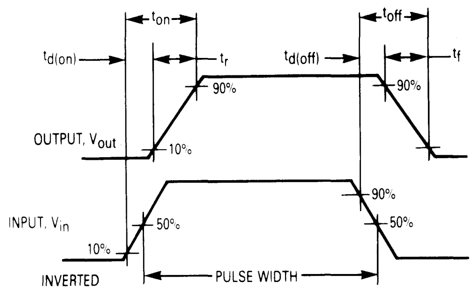
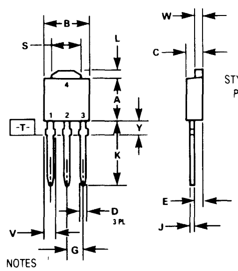


Figure 15. Switching Waveforms

OUTLINE DIMENSIONS

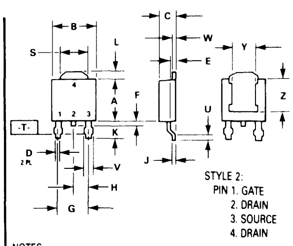


CASE 369-03
TO-251
MTD4P05-1 • MTD4P06-1

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. ⊕ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH



CASE 369A-04
TO-252
MTD4P05 • MTD4P06

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. ⊕ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

Designer's Data Sheet

Power Field Effect Transistors

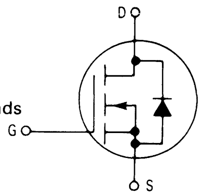
N-Channel Enhancement Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

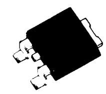
MTD5N05
MTD5N06

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 0.4 OHM
50 and 60 VOLTS

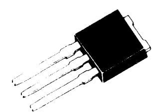
These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.4 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix





CASE 369A-04
MTD5N05
MTD5N06



CASE 369-03
MTD5N05-1
MTD5N06-1

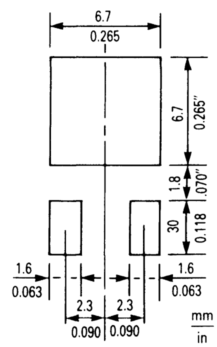
MAXIMUM RATINGS

Rating	Symbol	MTD5N05	MTD5N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	5 14		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01		Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	°C/W

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTD5N05 MTD5N06	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	— —	0.2 1	mAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2.4 2	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	300	pF
Output Capacitance		C_{oss}	—	160	
Reverse Transfer Capacitance		C_{rss}	—	50	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	6 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	3 (Typ)	—	
Gate-Drain Charge		Q_{gd}	3 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	2 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

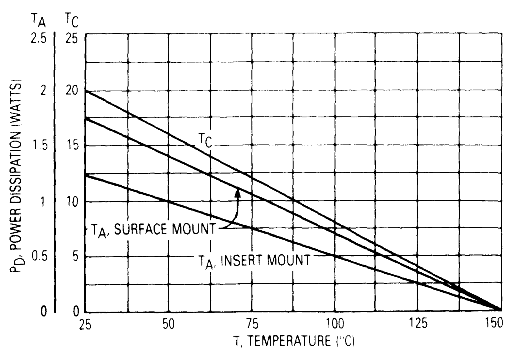


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

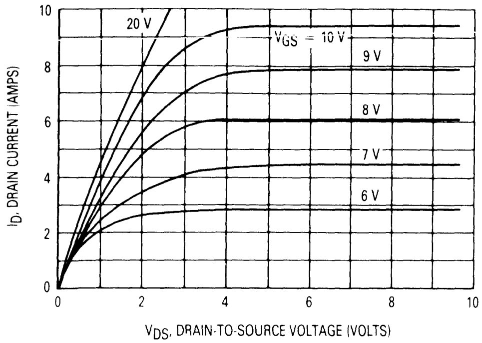


Figure 2. On-Region Characteristics

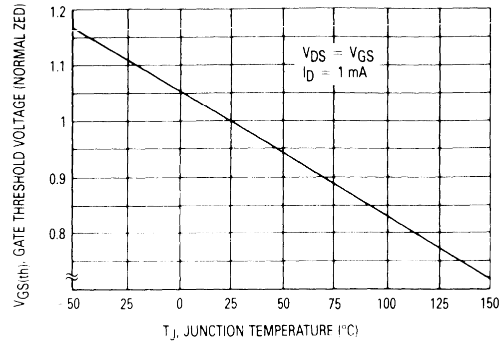


Figure 3. Gate-Threshold Voltage Variation With Temperature

3

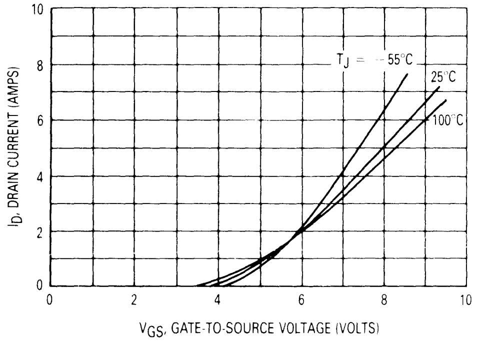


Figure 4. Transfer Characteristics

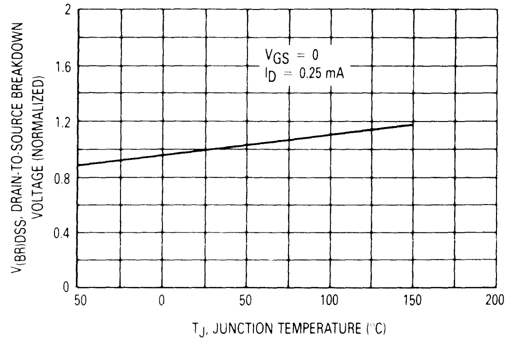


Figure 5. Breakdown Voltage Variation With Temperature

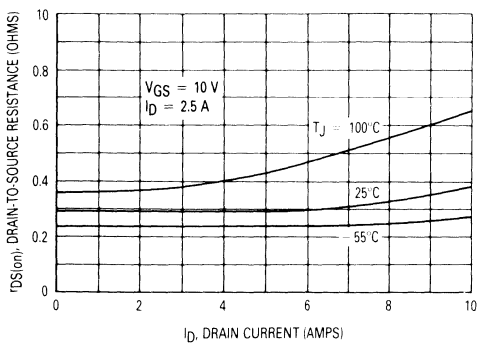


Figure 6. On-Resistance versus Drain Current

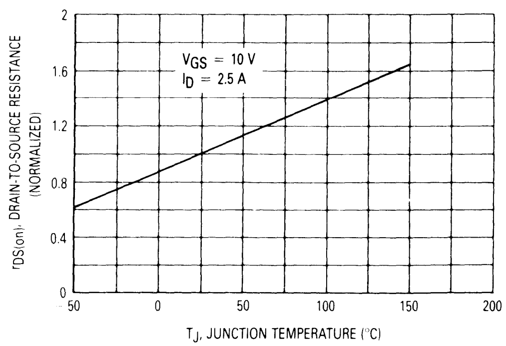


Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

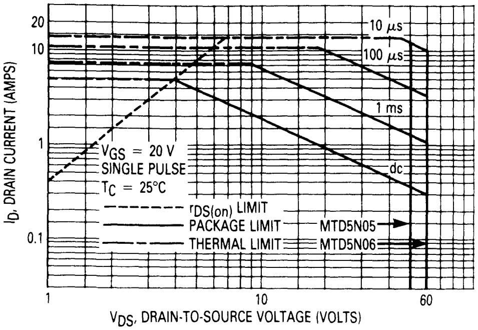


Figure 8. Maximum Rated Forward Biased Safe Operating Area

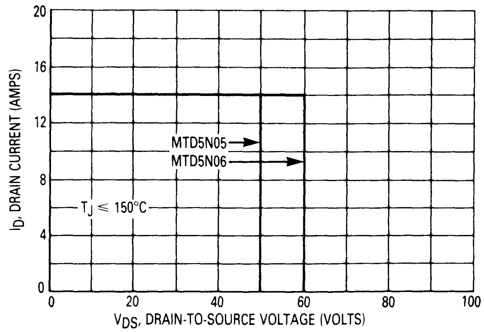


Figure 9. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

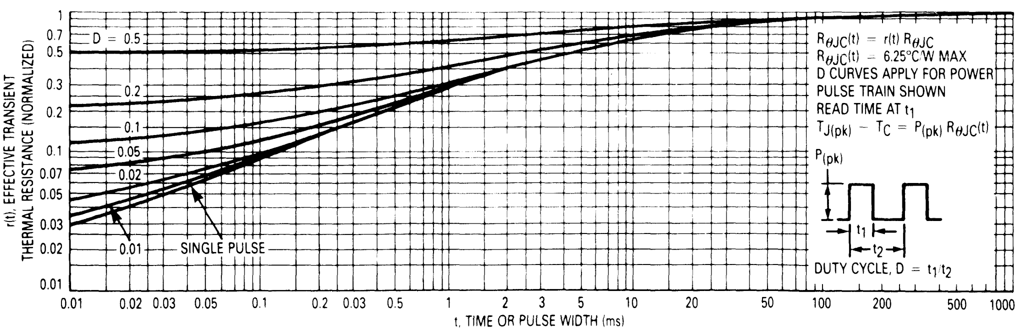


Figure 10. Thermal Response

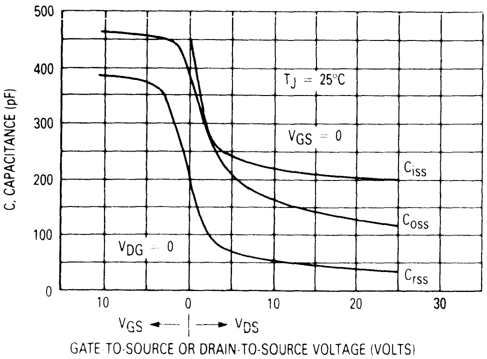


Figure 11. Capacitance Variation

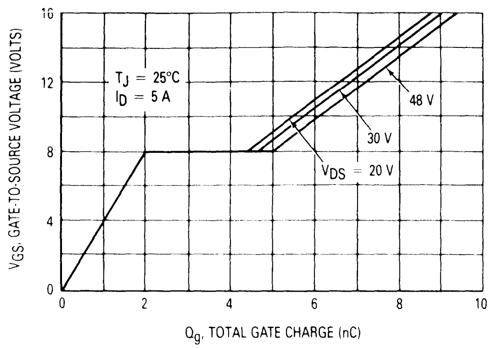


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

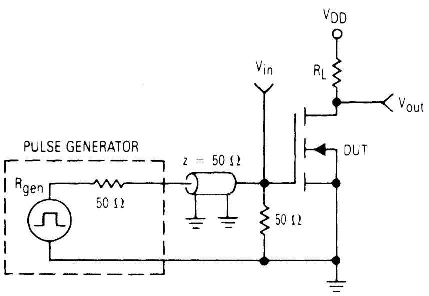


Figure 13. Switching Test Circuit

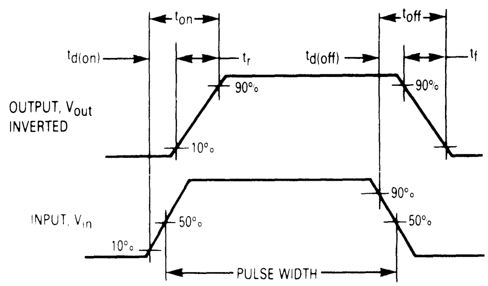
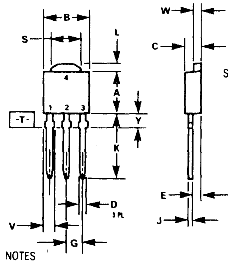


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 369-03
MTD5N05-1, MTD5N06-1

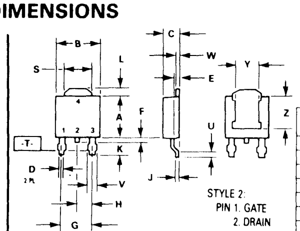


STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
| ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369A-04
MTD5N05, MTD5N06



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
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2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
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D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

MTD6N08
MTD6N10

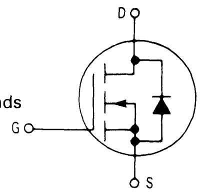
Designer's Data Sheet

Power Field Effect Transistor

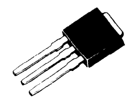
N-Channel Enhancement-Mode
Silicon Gate TMOS
DPAK for Surface Mount
or Insertion Mount

These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

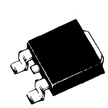
- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.25 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4 V max
- Surface Mount Package on 16 mm Tape
- Available With Long Leads, Add -1 Suffix



TMOS POWER FETs
6 AMPERES
$r_{DS(on)}$ = 0.25 OHM
80 and 100 VOLTS

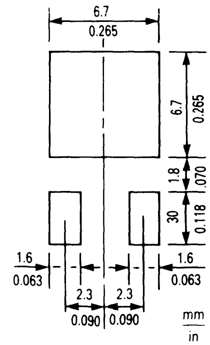


CASE 369-03
TO-251
MTD6N08-1
MTD6N10-1



CASE 369A-04
TO-252
MTD6N08
MTD6N10

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	MTD6N08	MTD6N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	6 20		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16		Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01		Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case	$R_{\theta JC}$	6.25	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTD6N08 MTD6N10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	— —	10 100	μAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	0.25	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc) (I_D = 3 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 1.6 1.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 3 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	13 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.7 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	100 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

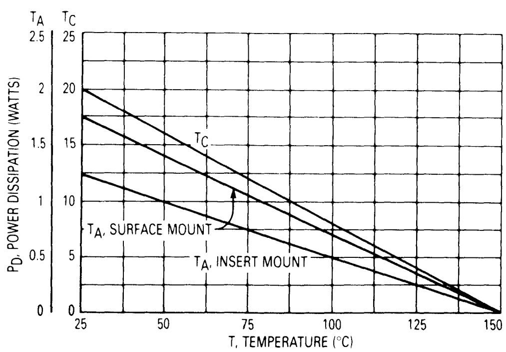


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

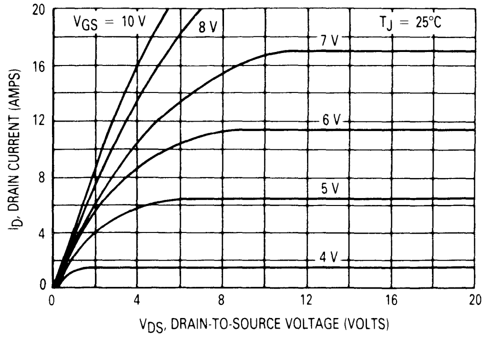


Figure 2. On-Region Characteristics

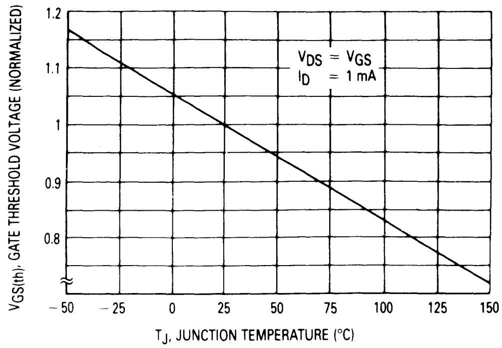


Figure 3. Gate-Threshold Voltage Variation With Temperature

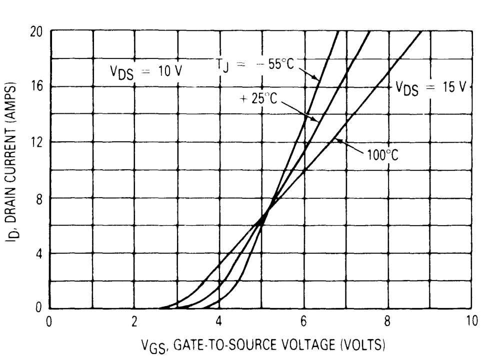


Figure 4. Transfer Characteristics

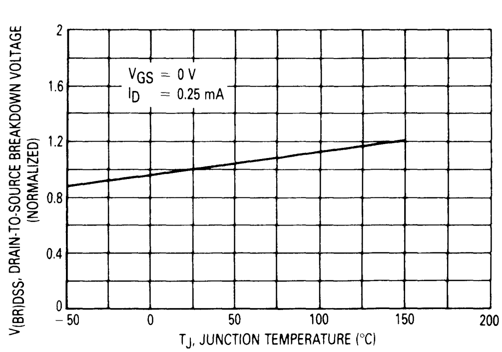


Figure 5. Breakdown Voltage Variation With Temperature

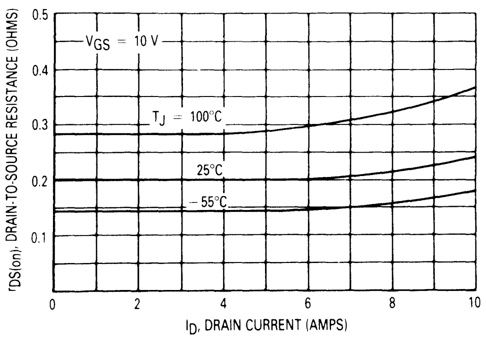


Figure 6. On-Resistance versus Drain Current

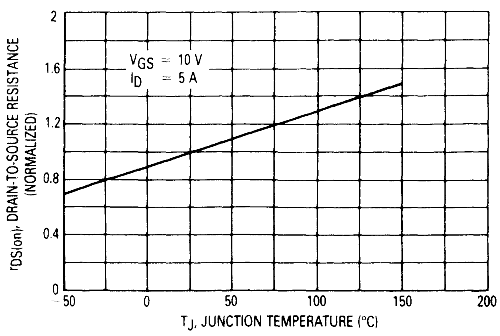


Figure 7. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

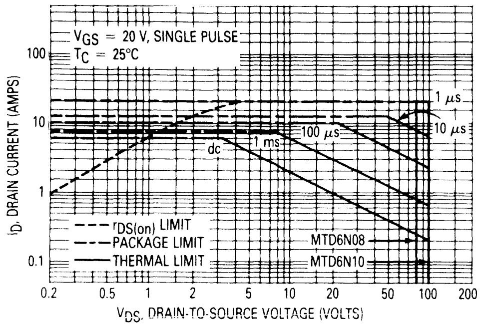


Figure 8. Maximum Rated Forward Biased Safe Operating Area

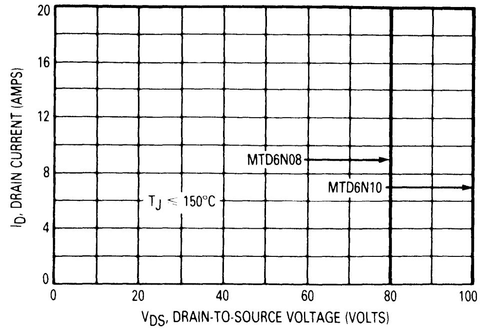


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

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The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

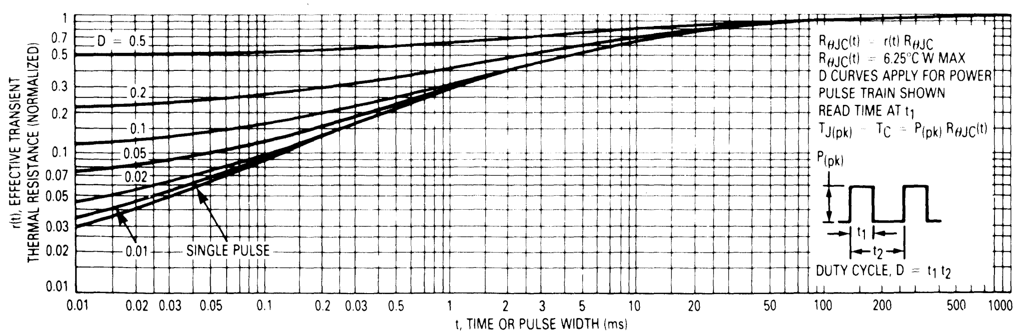
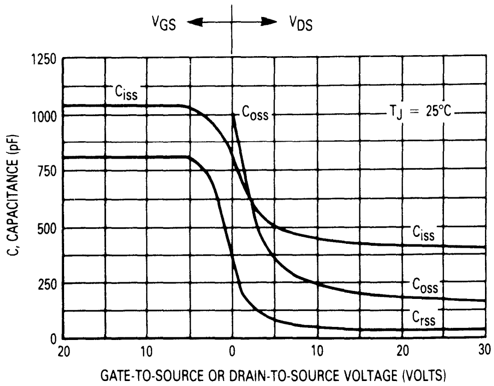


Figure 10. Thermal Response



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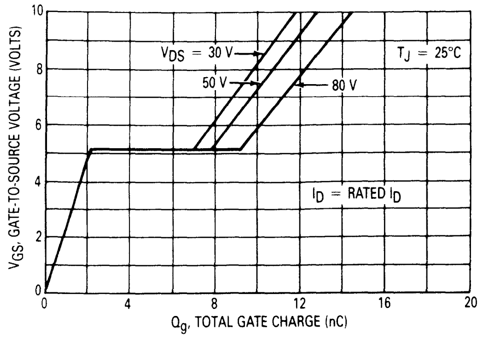


Figure 12. Gate Charge versus Gate-To-Source Voltage

3

RESISTIVE SWITCHING

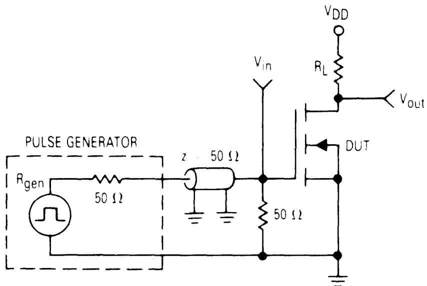


Figure 13. Switching Test Circuit

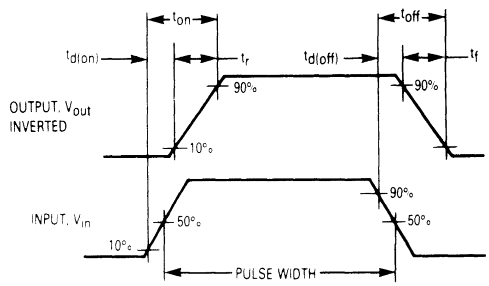
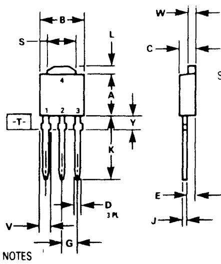


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 369-03 TO-251 MTD6N08-1, MTD6N10-1



STYLE 2:
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2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
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0.13 (0.005) Ⓜ T
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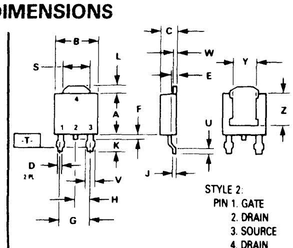
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369A-04 TO-252 MTD6N08, MTD6N10



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S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

3

MTD6N15

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

TMOS

TMOS POWER FET
6 AMPERES
$r_{DS(on)}$ = 0.3 OHM
150 VOLTS

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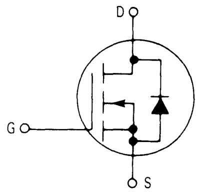
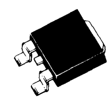
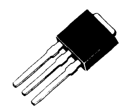


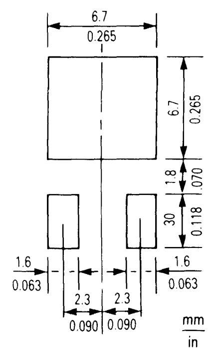


CASE 369A-04
TO-252
MTD6N15



CASE 369-03
TO-251
MTD6N15-1

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	6 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) T_J = 125°C	I_{DSS}	— —	10 100	μAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc) (I_D = 3 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 1.8 1.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 3 A)		g_{FS}	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	120	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 3 A, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	15 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 6 A, di/dt = 25 A/µs V_{GS} = 0)	V_{SD}	1.3 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

3

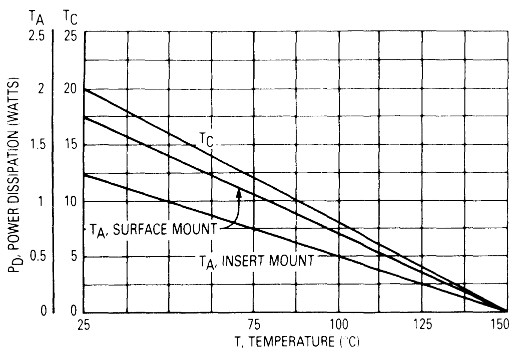


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

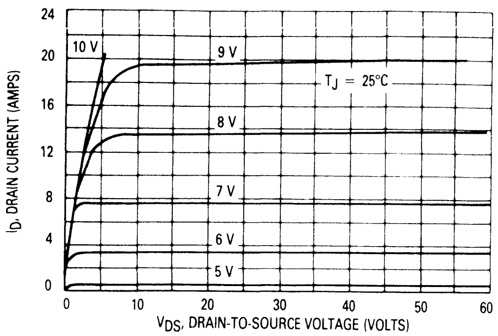


Figure 2. On-Region Characteristics

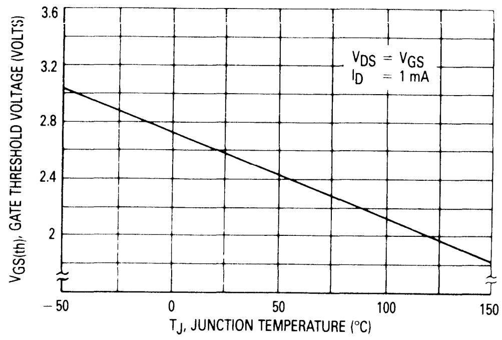


Figure 3. Gate-Threshold Voltage Variation With Temperature

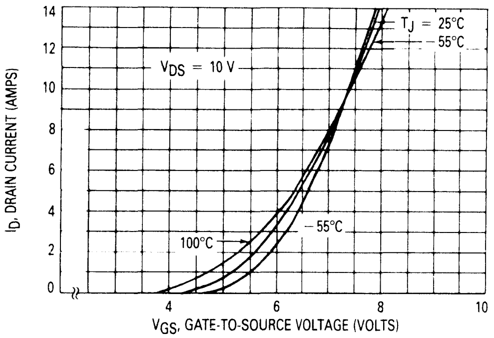


Figure 4. Transfer Characteristics

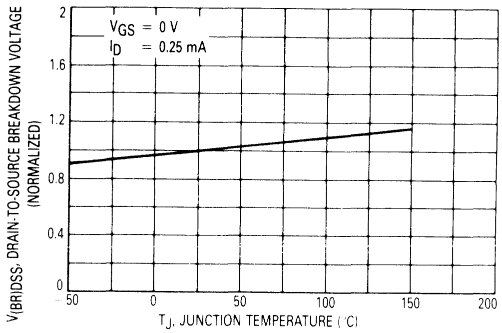


Figure 5. Breakdown Voltage Variation With Temperature

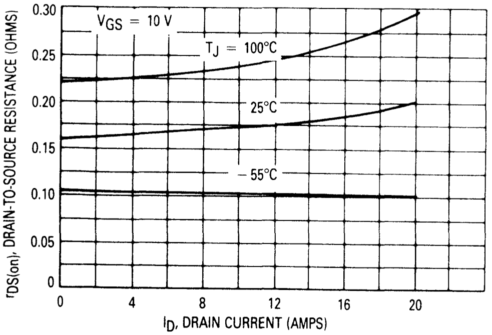


Figure 6. On-Resistance versus Drain Current

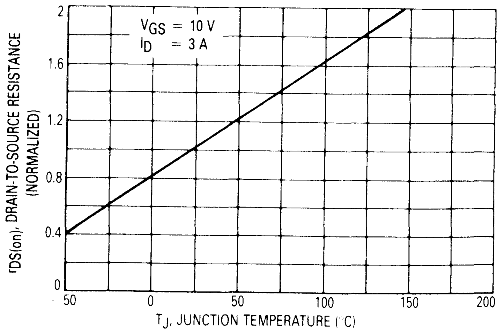


Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

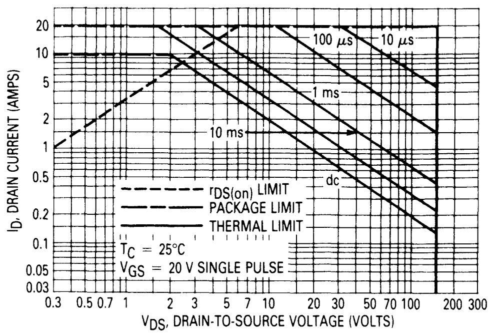


Figure 8. Maximum Rated Forward Biased Safe Operating Area

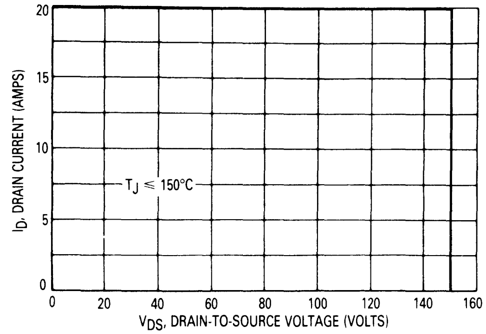


Figure 9. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

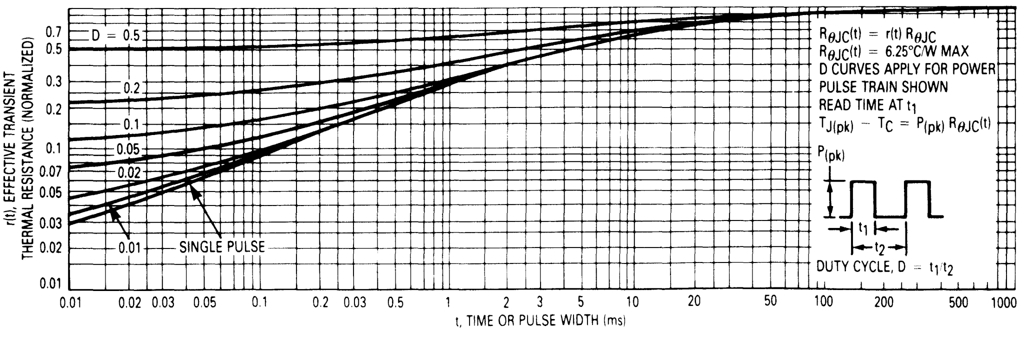


Figure 10. Thermal Response

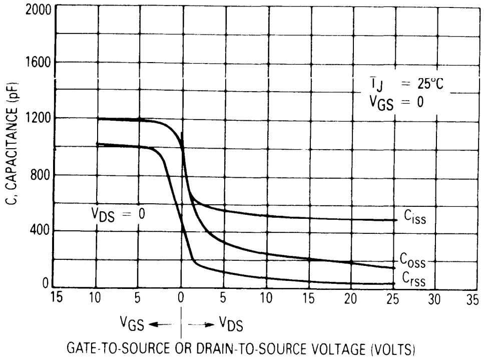


Figure 11. Capacitance Variation

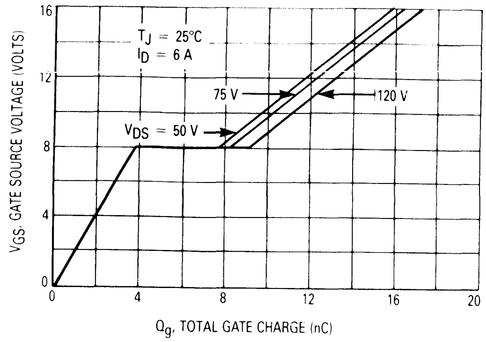


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

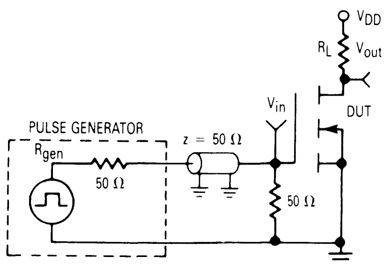


Figure 13. Switching Test Circuit

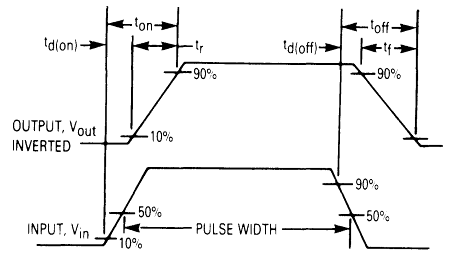
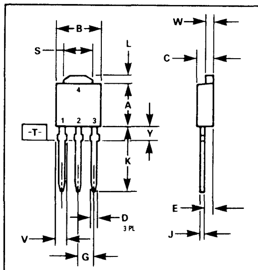


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 369-03
TO-251
MTD6N15-1

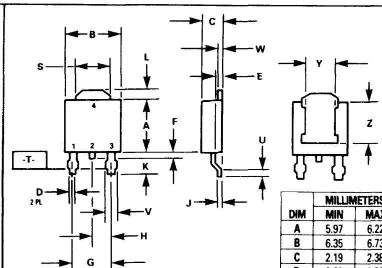


STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369A-04
TO-252
MTD6N15



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER. | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD10N05E

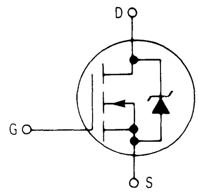
Designer's Data Sheet
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode
DPAK for Surface Mount or Insertion Mount

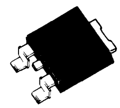
TMOS POWER FETs
10 AMPERES
$r_{DS(on)}$ = 0.1 OHM
50 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

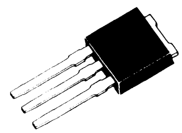
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.
- Available With Long Leads, Add -1 Suffix

TMOS™





CASE 369A-04
TO-252
MTD10N05E



CASE 369-03
TO-251
MTD10N05E-1

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

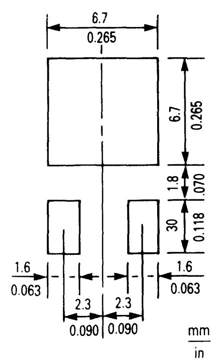
Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leqq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 24	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W
Maximum Device Temperature for Soldering Purposes (for 5 seconds maximum)	T_L	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C) °C)		I_{DSS}	— —	10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.1	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc) (I_D = 5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	1.1 0.9	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)		g_{FS}	4.5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain-to-Source Avalanche Energy See Figures 16 and 17 (I_D = 24 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 10 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 10 μs, Duty Cycle ≤ 1%) (I_D = 4 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 10 μs, Duty Cycle ≤ 1%)		W_{DSR}	— — —	5 6 2.5	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 14	C_{iss}	—	850	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 18	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	90	
Turn-Off Delay Time		$t_{d(off)}$	—	45	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 15	Q_g	14 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_{FM} = 0.5 Rated I_D, dI_S/dt = 100 A/μs, V_{GS} = 0)	V_{SD}	1 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	50 (Typ)	—	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

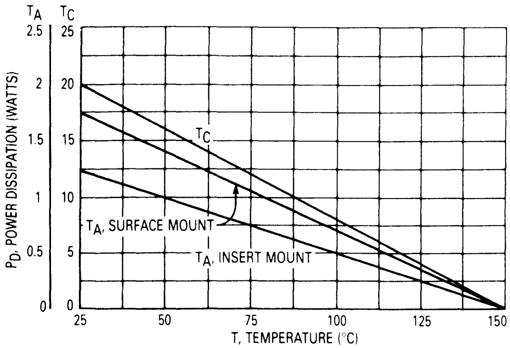

Figure 1. Power Derating

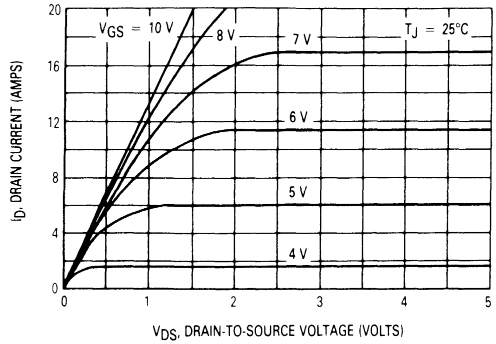

Figure 2. On-Region Characteristics

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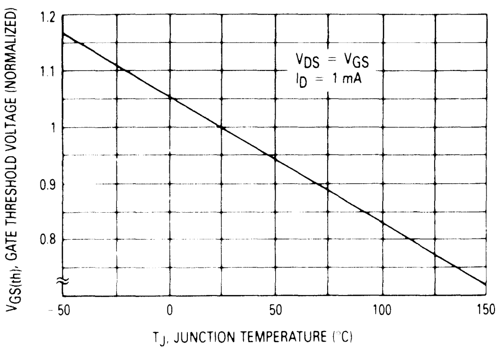


Figure 3. Gate-Threshold Voltage Variation With Temperature

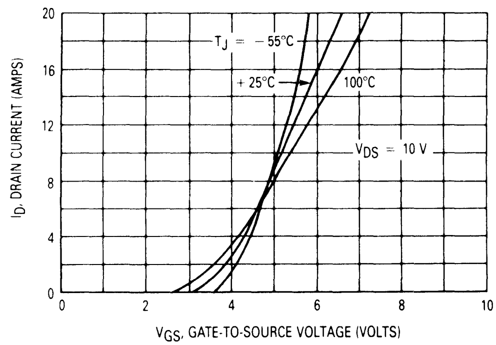


Figure 4. Transfer Characteristics

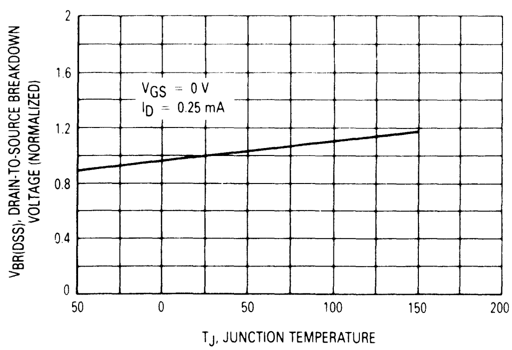


Figure 5. Breakdown Voltage Variation With Temperature

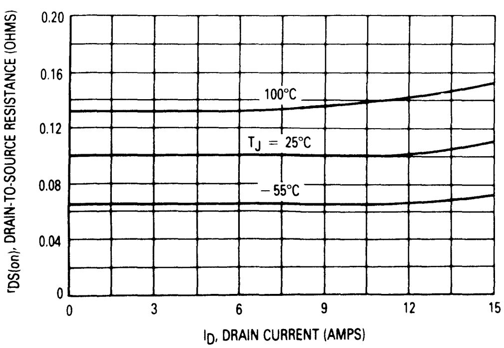


Figure 6. On-Resistance versus Drain Current

SAFE OPERATING AREA INFORMATION

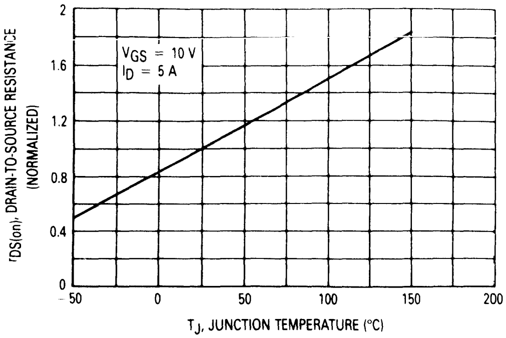


Figure 7. On-Resistance Variation With Temperature

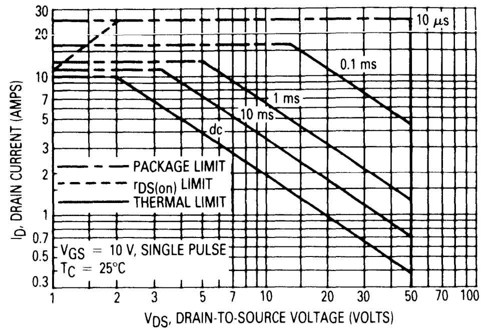


Figure 8. Maximum Rated Forward Biased Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

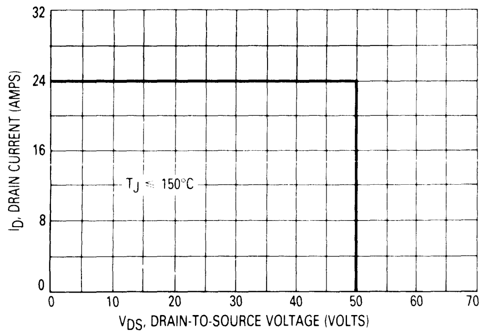


Figure 9. Maximum Rated Switching Safe Operating Area

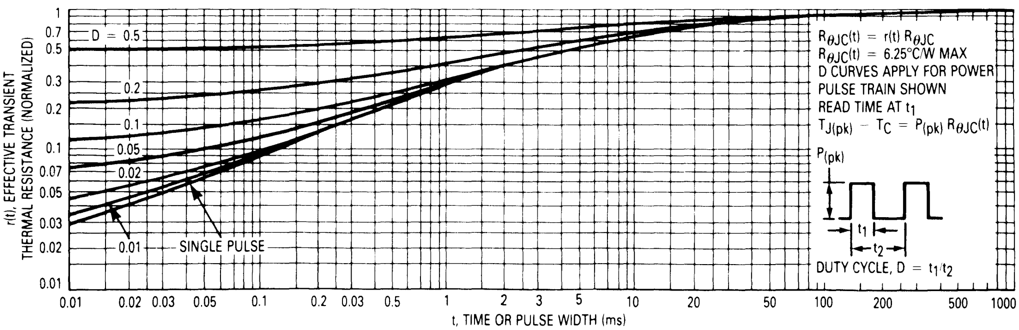


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

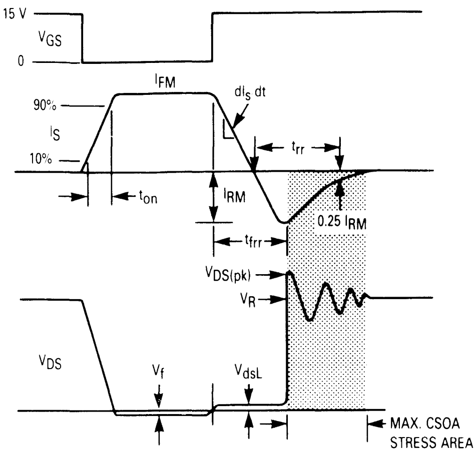


Figure 11. Commutating Waveforms

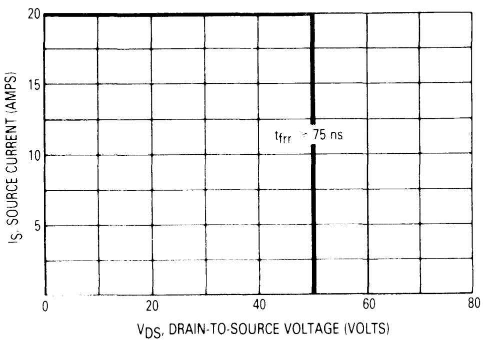


Figure 12. Commutating Safe Operating Area (CSOA)

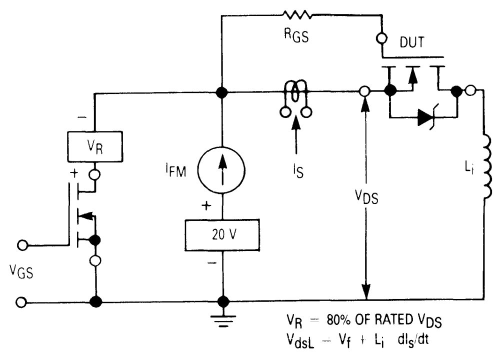


Figure 13. Commutating Safe Operating Area Test Circuit

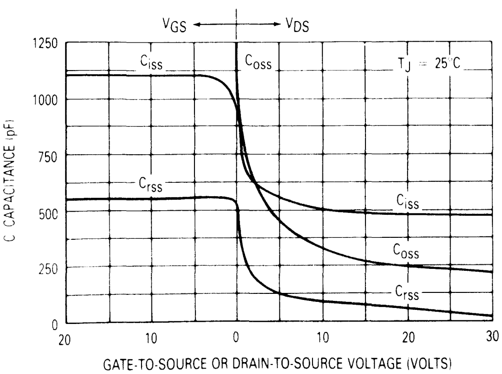


Figure 14. Capacitance Variation

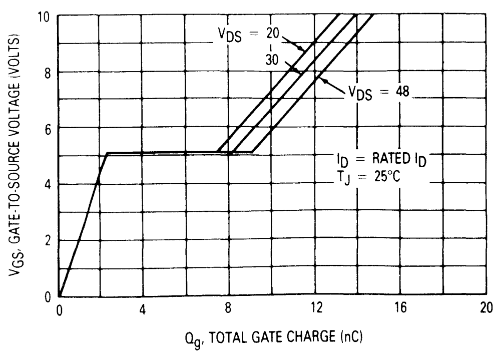


Figure 15. Gate-Charge versus Gate-to-Source Voltage

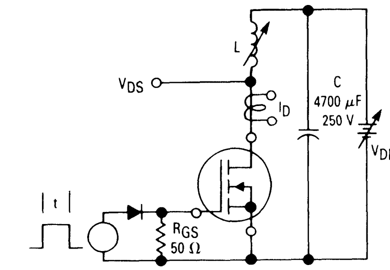
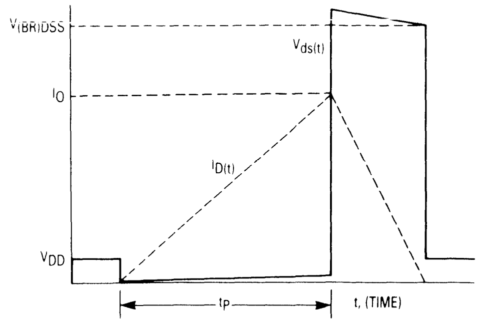


Figure 16. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 17. Unclamped Inductive Switching Waveforms

RESISTIVE SWITCHING

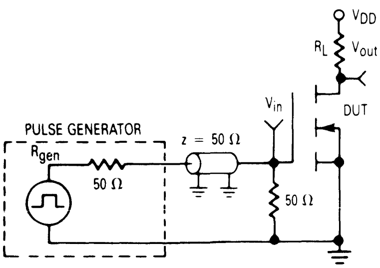


Figure 18. Switching Test Circuit

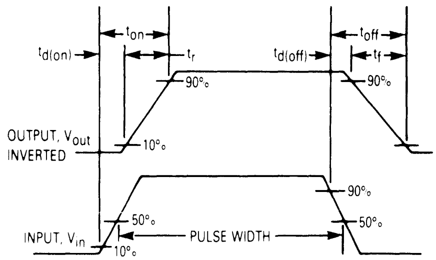
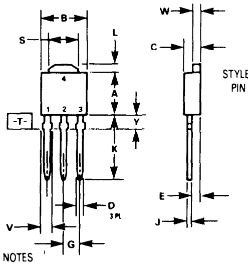


Figure 19. Switching Waveforms

OUTLINE DIMENSIONS

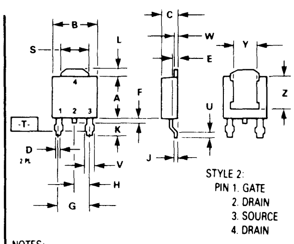


STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 369-03
TO-251
MTD10N05E1

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 369A-04
TO-252
MTD10N05E

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

NOTES:
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2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
   | ⌖ | 0.13 (0.005) Ⓜ | T |
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

MTD2955

Designer's Data Sheet

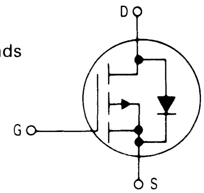
Power Field Effect Transistor

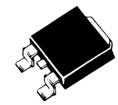
P-Channel Enhancement-Mode Silicon Gate TMOS DPAK for Surface Mount or Insertion Mount

TMOS POWER FET
12 AMPERES
$r_{DS(on)}$ = 0.3 OHM
60 VOLTS

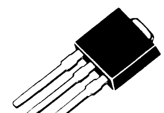
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.3 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4.0 V max
- Surface Mount Package Available on 16 mm Tape
- Available With Long Leads, Add -1 Suffix



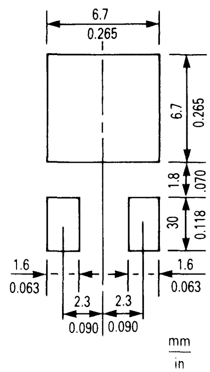


CASE 369A-04
MTD2955



CASE 369-03
MTD2955-1

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.67	°C/W
— Junction to Ambient — Junction to Ambient (1)	$R_{\theta JA}$	100 71.4	

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

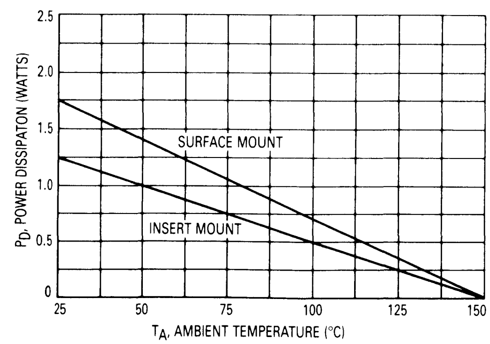
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(T_J = 125°C)			—	80	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	2.0	4.5	Vdc
(T_J = 100°C)			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc)		$V_{DS(on)}$	—	3.9	Vdc
(I_D = 6.0 Adc, T_J = 100°C)			—	3.2	
Forward Transconductance (V_{DS} = 10 V, I_D = 6.0 A)		g_{FS}	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 13	C_{iss}	600 (Typ)	—	pF
Output Capacitance		C_{oss}	300 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	135 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6.0 A, R_g = 50 ohms) See Figures 10, 14 and 15	$t_{d(on)}$	10 (Typ)	—	ns
Rise Time		t_r	75 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	75 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 12 A, V_{GS} = 10 V) See Figure 12	Q_g	26 (Typ)	45	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	I_S = 12 A, V_{GS} = 0	V_{SD}	3.0 (Typ)	3.8	Vdc
Forward Turn-On Time	I_S = 12 A, dI_S/dt = 100 A/μs, V_R = 30 V	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	110 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Figure 1. Power Derating



TYPICAL ELECTRICAL CHARACTERISTICS

Figure 2. On-Region Characteristics

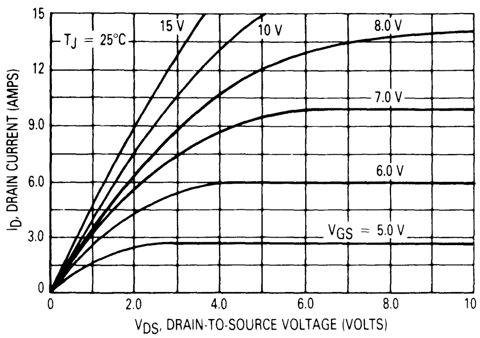


Figure 3. Gate Threshold Variation With Temperature

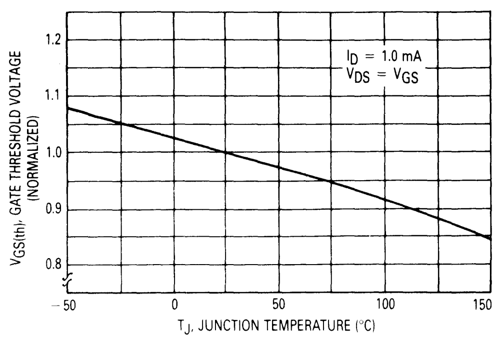


Figure 4. Transfer Characteristics

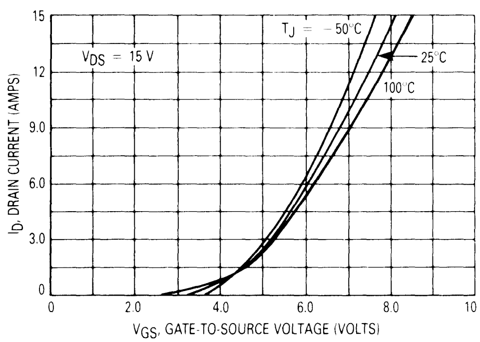


Figure 5. Breakdown Voltage Variation With Temperature

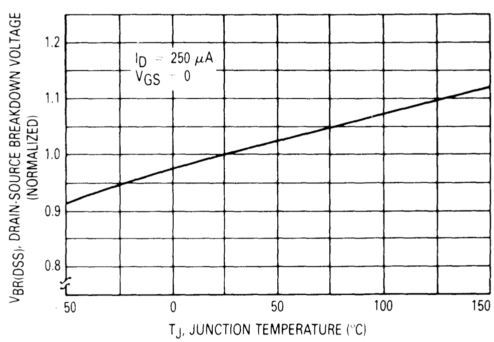


Figure 6. On-Resistance Variation With Drain Current

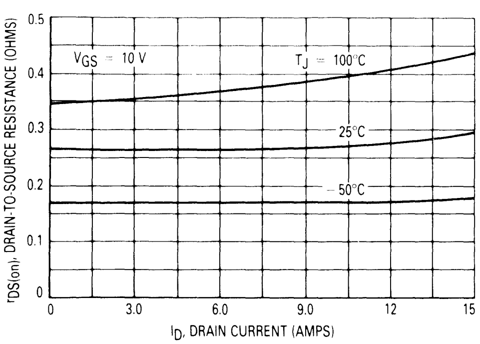
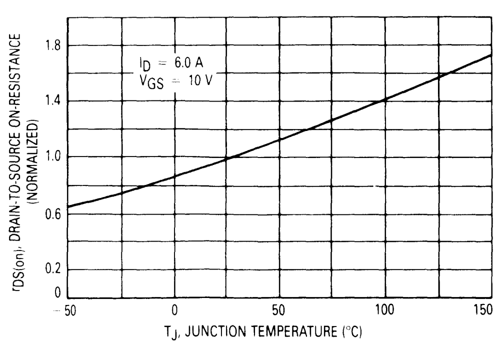


Figure 7. On-Resistance Variation With Temperature



3

Figure 8. Maximum Rated Forward Biased Safe Operating Area

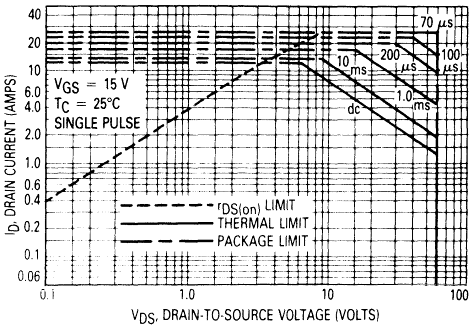
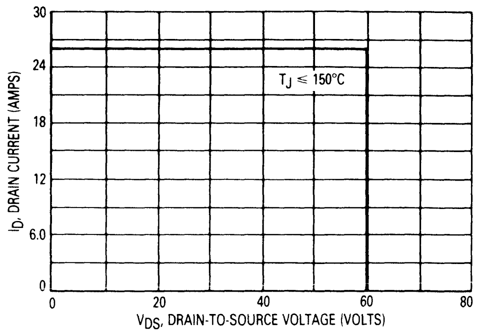


Figure 9. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 10. Resistive Switching Time versus Gate Resistance

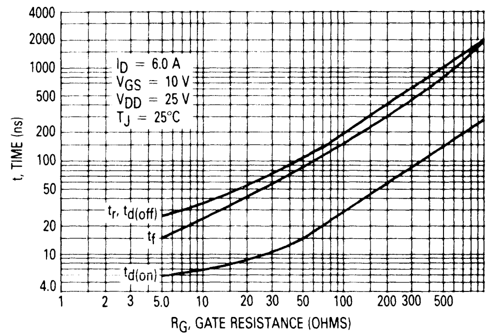


Figure 11. Thermal Response

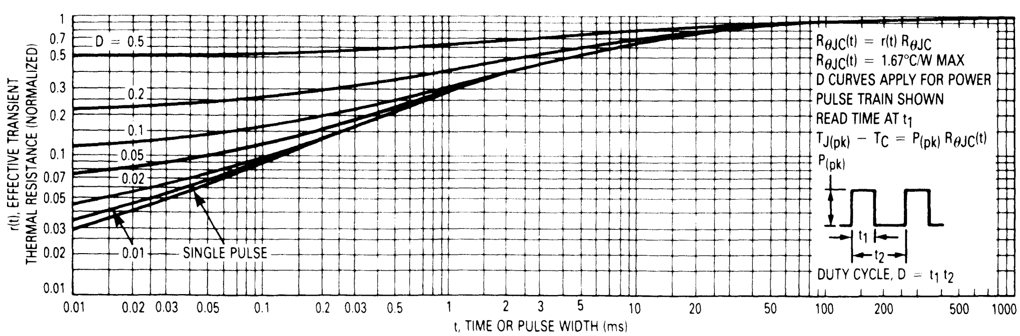


Figure 12. Gate Charge versus Gate-To-Charge Voltage

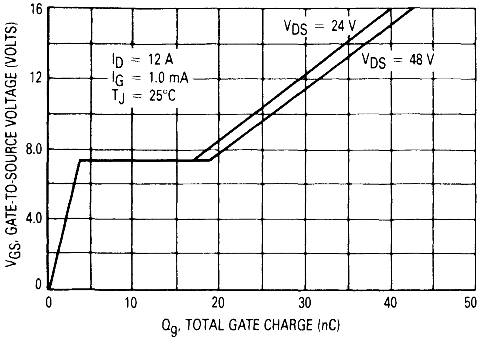
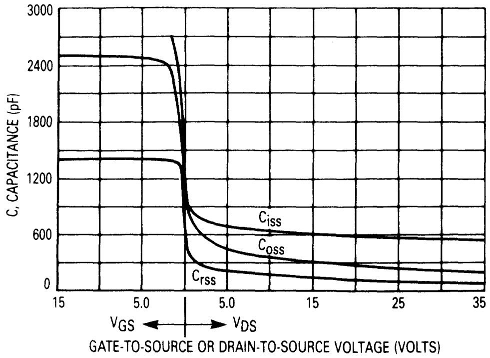


Figure 13. Capacitance Variation With Voltage



3

RESISTIVE SWITCHING

Figure 14. Switching Test Circuit

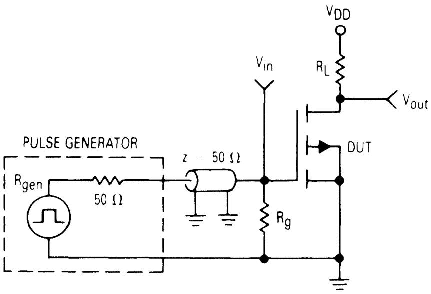
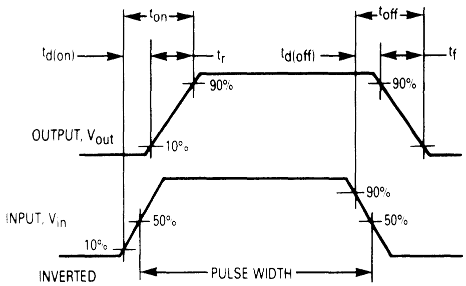
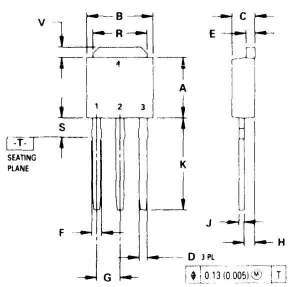


Figure 15. Switching Waveforms



OUTLINE DIMENSIONS

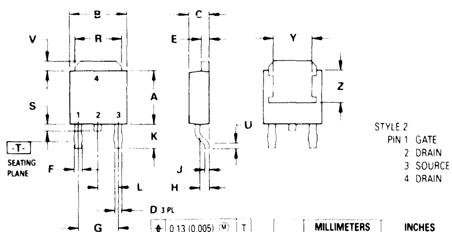


STYLE 2
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	0.94	0.033	0.037
F	0.77	1.14	0.030	0.045
G	2.29 BSC		0.090 BSC	
H	0.97	1.06	0.038	0.042
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
R	5.21	5.46	0.205	0.215
S	1.91	2.28	0.075	0.090
V	0.89	1.27	0.035	0.050

CASE 369-03
MTD2955-1



STYLE 2
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
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2. CONTROLLING DIMENSION: INCH.

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G	4.58 BSC		0.180 BSC	
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J	0.46	0.58	0.018	0.023
K	2.60	2.89	0.102	0.114
L	2.29 BSC		0.090 BSC	
R	5.21	5.46	0.205	0.215
S	0.64	0.88	0.025	0.035
U	0.51	—	0.020	—
V	0.89	1.27	0.035	0.050
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

CASE 369A-04
MTD2955

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD3055E

Designer's Data Sheet

TMOS IV N-Channel Enhancement-Mode

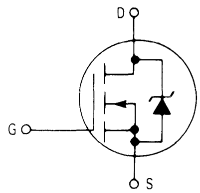
Power Field Effect Transistor
DPAK for Surface or Insertion Mount

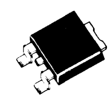
TMOS POWER FET
8 AMPERES
$r_{DS(on)}$ = 0.15 OHM
60 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

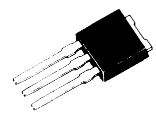
TMOS™

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.
- Available With Long Leads, Add -1 Suffix



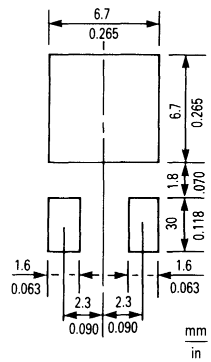


CASE 369A-04
TO-252
MTD3055E



CASE 369-03
TO-251
MTD3055E-1

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	MTD3055E	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W
Maximum Device Temperature for Soldering Purposes (for 5 seconds maximum)	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 80	μA

(1) These ratings are applicable when surface mounted on the minimum pad size recommended.

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)				
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 1.3 1	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)	g_{FS}	4	—	mhos
DRAIN-TO-SOURCE AVALANCHE STRESS CAPABILITY				
Unclamped Inductive Switching Energy — See Figures 16 and 17 (I_D = 20 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 8 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 3.2 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)	W_{DSR}	 — — —	 3 10 4	mJ
DYNAMIC CHARACTERISTICS				
Input Capacitance — (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 14	C_{iss}	—	500	pF
Output Capacitance	C_{oss}	—	300	
Reverse Transfer Capacitance	C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time — (V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figure 18	$t_{d(on)}$	—	20	ns
Rise Time	t_r	—	60	
Turn-Off Delay Time	$t_{d(off)}$	—	65	
Fall Time	t_f	—	65	
Total Gate Charge — (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 15	Q_g	12 (Typ)	17	nC
Gate-Source Charge	Q_{gs}	6.5 (Typ)	—	
Gate-Drain Charge	Q_{gd}	5.5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage — (I_{FM} = 0.5 Rated I_D, dI_S/dt = 100 A/μs, V_{GS} = 0)	V_{SD}	1.7 (Typ)	2.5	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	50 (Typ)	90	ns

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

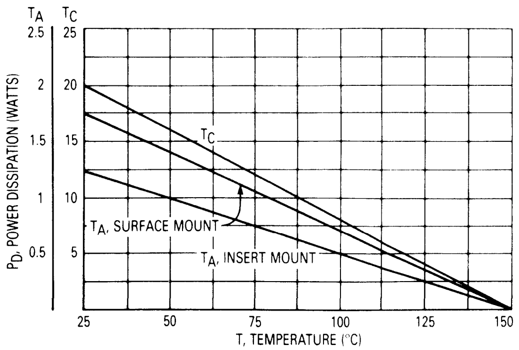


Figure 1. Power Derating

3

TYPICAL ELECTRICAL CHARACTERISTICS

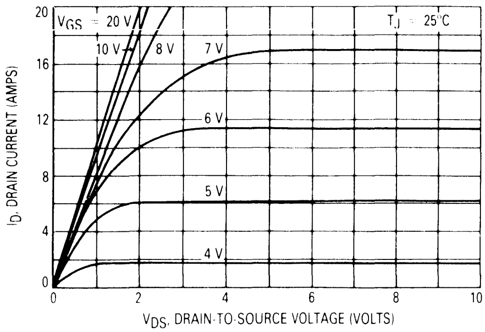


Figure 2. On-Region Characteristics

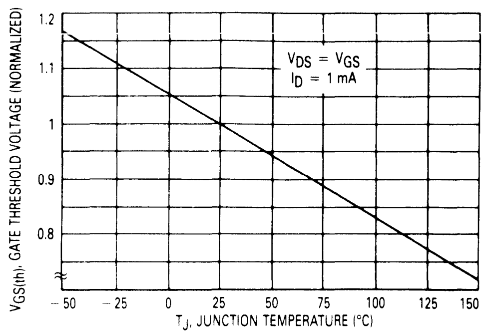


Figure 3. Gate-Threshold Voltage Variation With Temperature

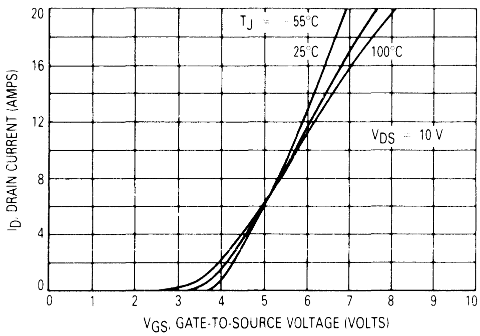


Figure 4. Transfer Characteristics

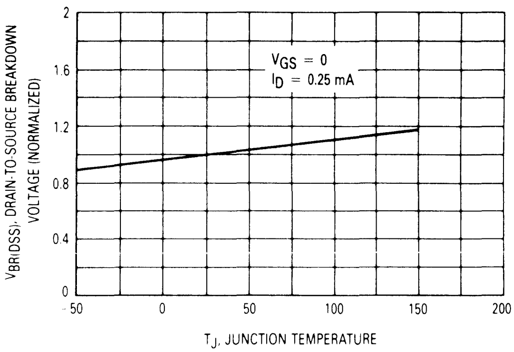


Figure 5. Breakdown Voltage Variation With Temperature

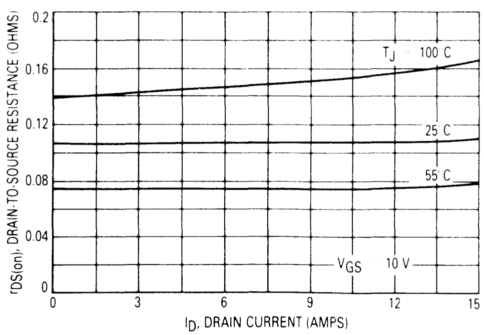


Figure 6. On-Resistance versus Drain Current

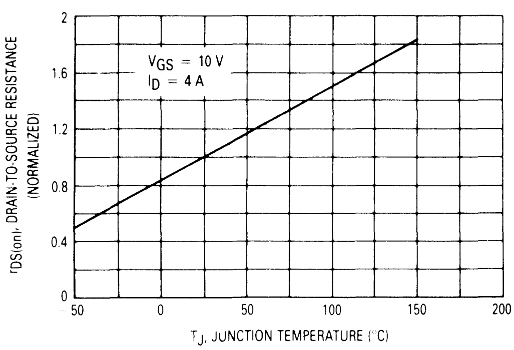


Figure 7. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

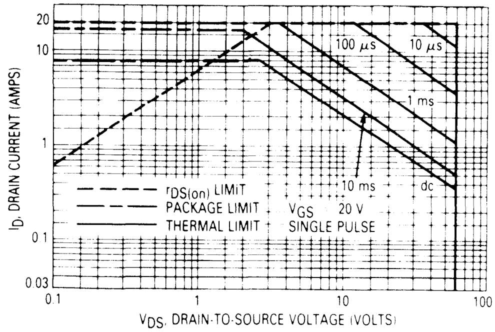


Figure 8. Maximum Rated Forward Biased Safe Operating Area

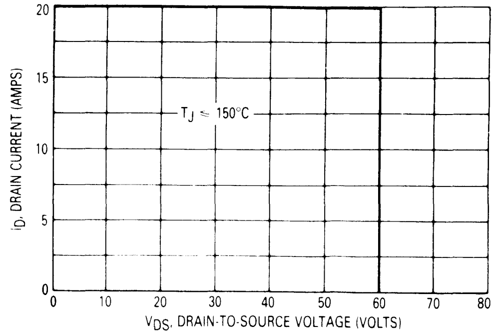


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

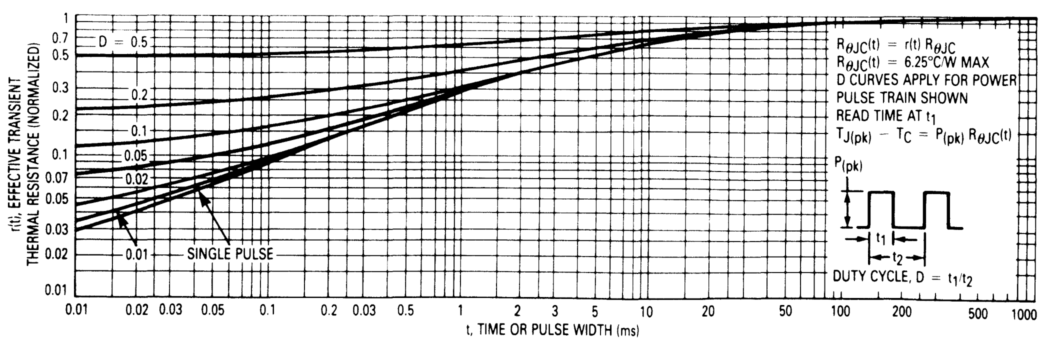


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

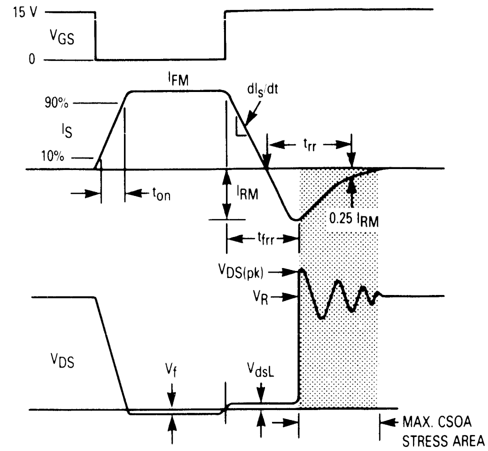


Figure 11. Commutating Waveforms

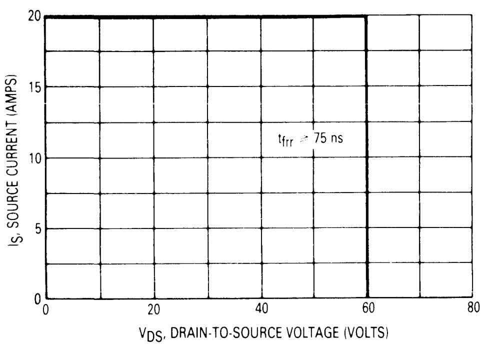


Figure 12. Commutating Safe Operating Area (CSOA)

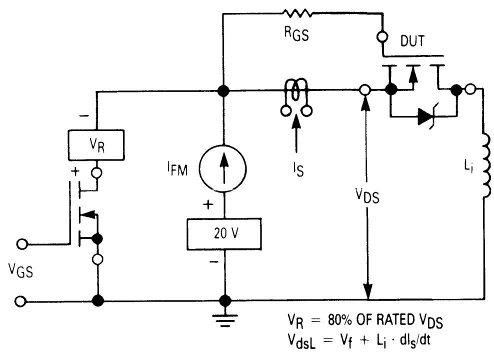


Figure 13. Commutating Safe Operating Area Test Circuit

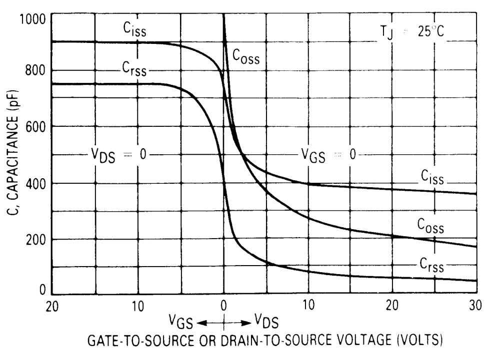


Figure 14. Capacitance Variation

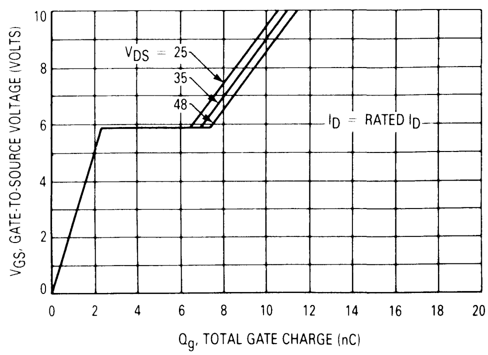


Figure 15. Gate-Charge versus Gate-to-Source Voltage

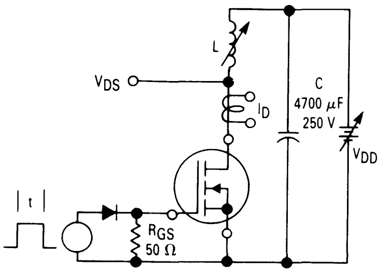
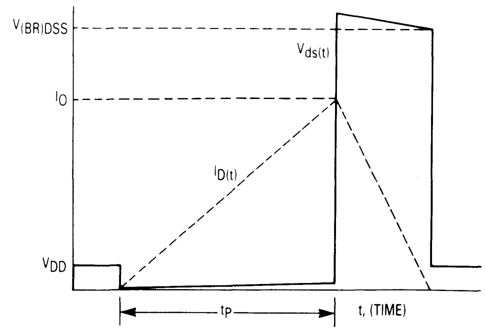


Figure 16. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 17. Unclamped Inductive Switching Waveforms

RESISTIVE SWITCHING

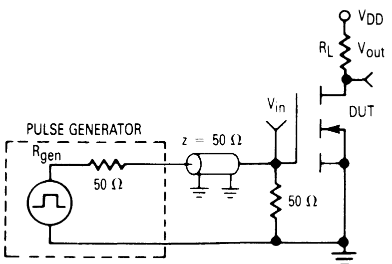


Figure 18. Switching Test Circuit

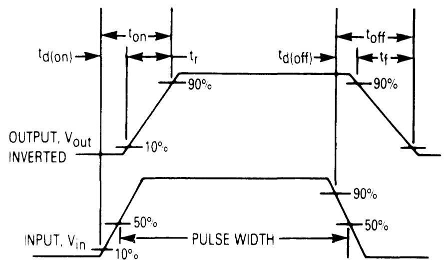
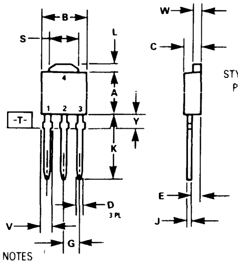


Figure 19. Switching Waveforms

OUTLINE DIMENSIONS

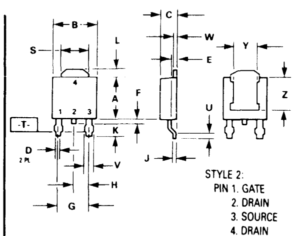


STYLE 2:
PIN 1. GATF
2. DRAIN
3. SOURCE
4. DRAIN

CASE 369-03
TO-251
MTD3055E-1

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER.
⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE.
2. POSITIONAL TOLERANCE FOR "D" DIAMETER
⌖ 0.13 (0.005) Ⓜ T
3. DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH

CASE 369A-04
TO-252
MTD3055E

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

3

3

MTD3055EL

Designer's Data Sheet

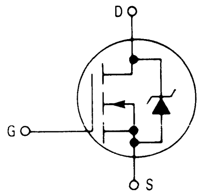
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

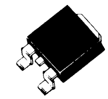
TMOS POWER MOSFET
LOGIC LEVEL
12 AMPERES
$r_{DS(on)}$ = 0.18 OHM
60 VOLTS

This advanced E-FET is a TMOS power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

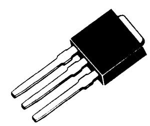
- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at 150°C
- Available With Long Leads, Add 1 Suffix

TMOS™





CASE 369A-04
MTD3055EL



CASE 369-03
MTD3055EL1

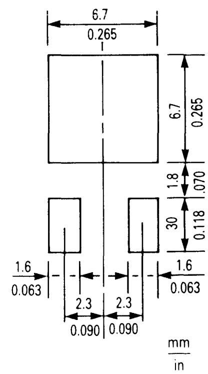
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	− 65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0) (V_{DS} = 60 V, V_{GS} = 0, T_J = 150°C)	I_{DSS}	— —	1 50	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 150°C	$V_{GS(th)}$	1 0.6	2 1.6	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 150°C)	$V_{DS(on)}$	 — —	 2.4 1.95	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)	g_{FS}	5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 13 and 14 (I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%) (I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)	W_{DSR}	 — — —	 18 35 16	mJ
DYNAMIC CHARACTERISTICS				
Input Capacitance — V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15	C_{iss}	400 (Typ) 1000 (Typ)	— —	pF
Reverse Transfer Capacitance — V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15	C_{rss}	30 (Typ) 660 (Typ)	— —	pF
Output Capacitance — V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 15	C_{oss}	175 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)				
Turn-On Delay Time — (V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms, R_{GS} = 50 ohms)	$t_{d(on)}$	20 (Typ)	—	ns
Rise Time	t_r	95 (Typ)	—	
Turn-Off Delay Time	$t_{d(off)}$	38 (Typ)	—	
Fall Time	t_f	50 (Typ)	—	
Total Gate Charge — (V_{DS} = 48 V, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 16 and 17	Q_g	7.2 (Typ)	17	nC
Gate-Source Charge	Q_{gs}	2 (Typ)	—	
Gate-Drain Charge	Q_{gd}	4 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS				
Forward On-Voltage — (I_S = 12 A, V_{GS} = 0)	V_{SD}	1.04 (Typ)	1.18	Vdc
Forward Turn-On Time — (I_S = 26 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	55 (Typ)	—	ns

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

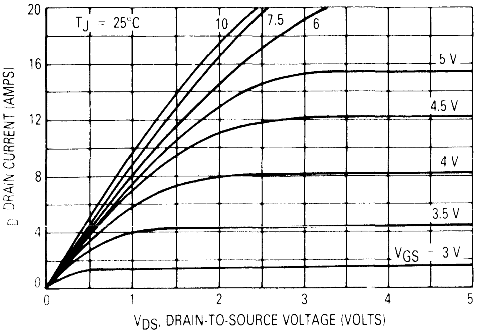


Figure 2. Gate-Threshold Voltage Variation With Temperature

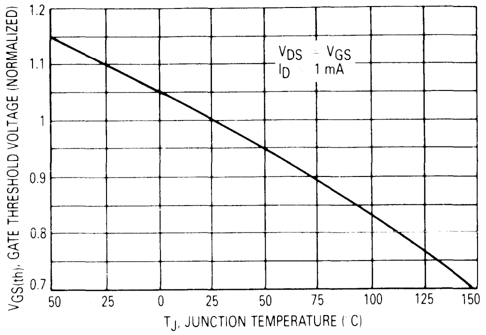


Figure 3. Transfer Characteristics

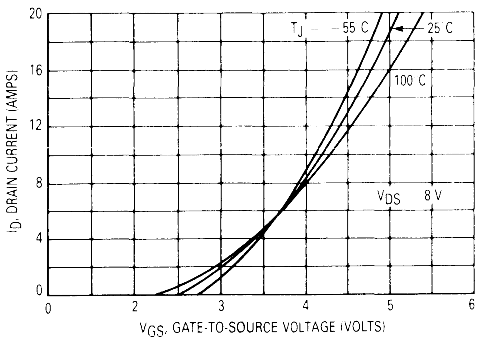


Figure 4. On-Resistance versus Drain Current

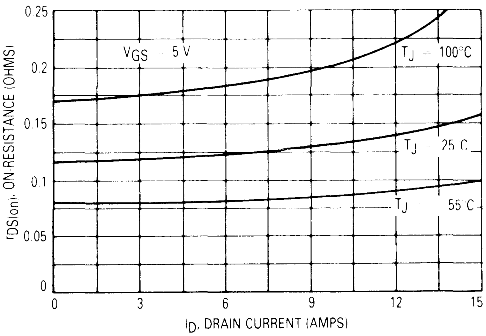


Figure 5. On-Resistance versus Gate-to-Source Voltage

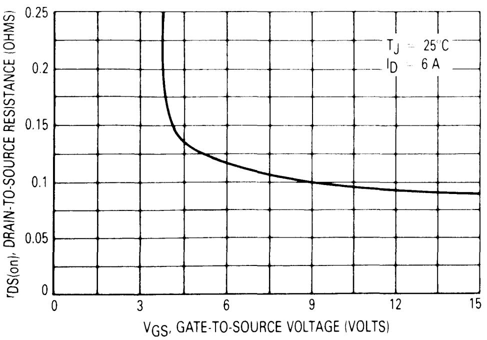


Figure 6. On-Resistance Variation With Temperature

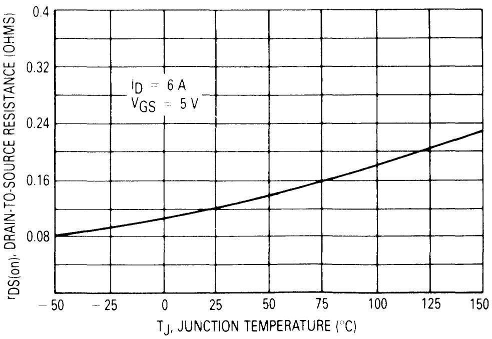


Figure 7. Breakdown Voltage Variation With Temperature

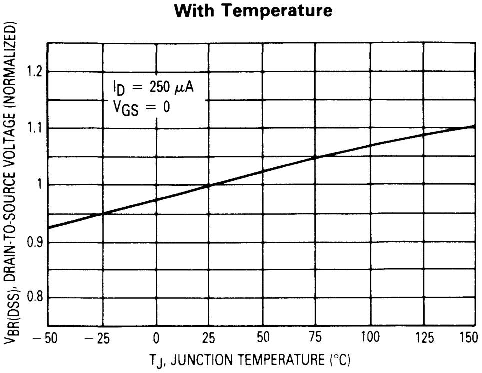
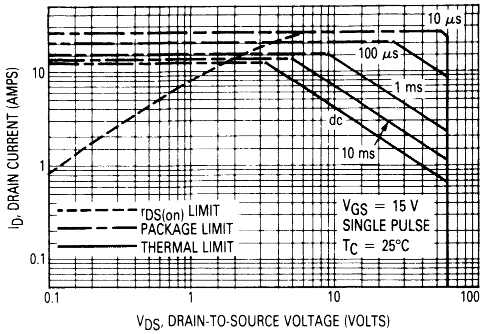


Figure 8. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

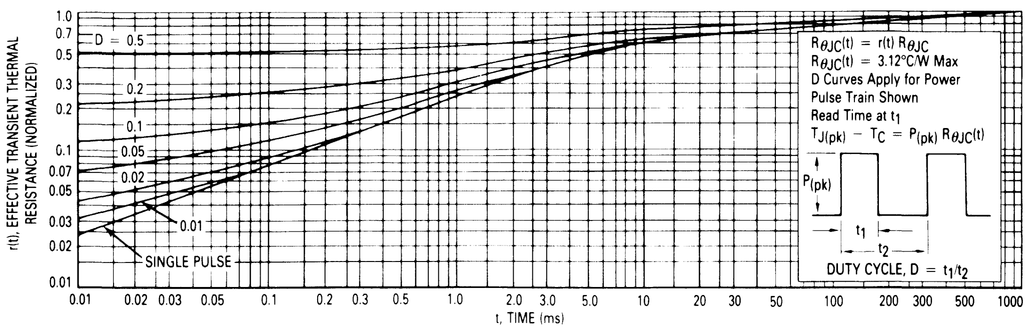
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

The switching safe operating area fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. This is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 11 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

Figure 11. Commutating Safe Operating Area (CSOA)

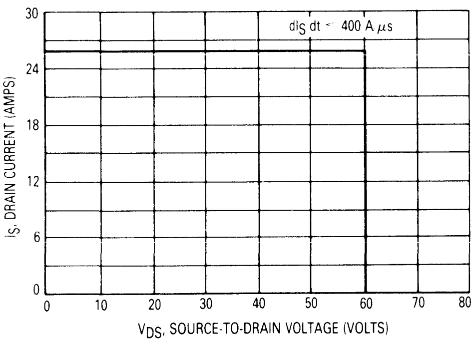


Figure 13. Unclamped Inductive Switching Test Circuit

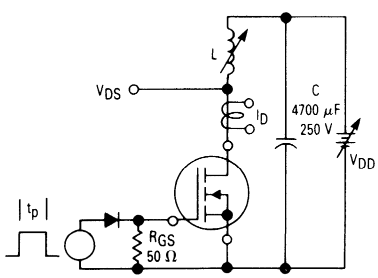


Figure 10. Commutating Waveforms

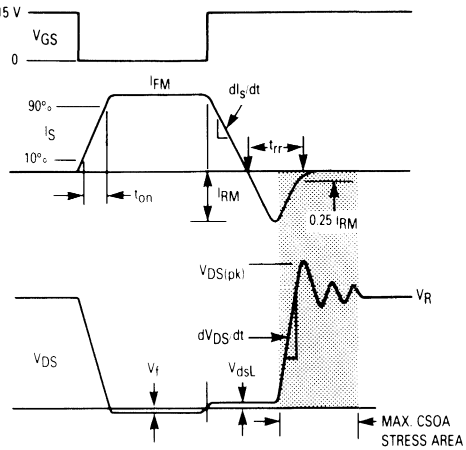


Figure 12. Commutating Safe Operating Area Test Circuit

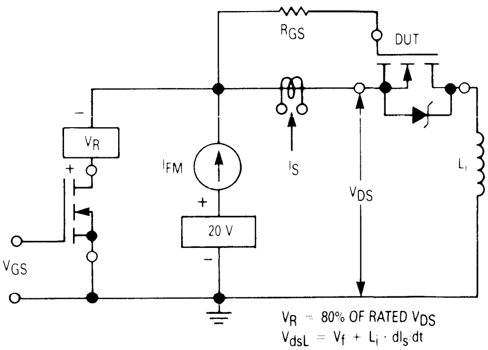
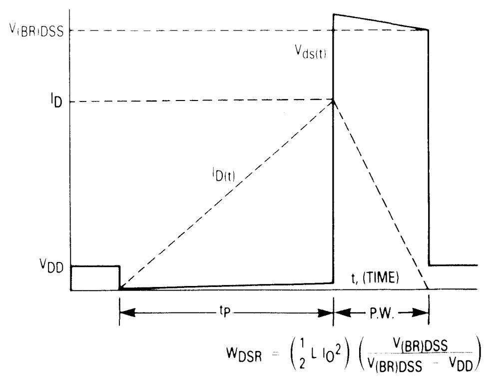


Figure 14. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_D^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

3

Figure 15. Capacitance Variation

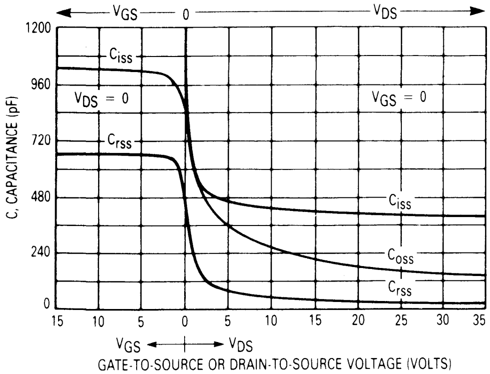


Figure 16. Gate Charge versus Gate-to-Source Voltage

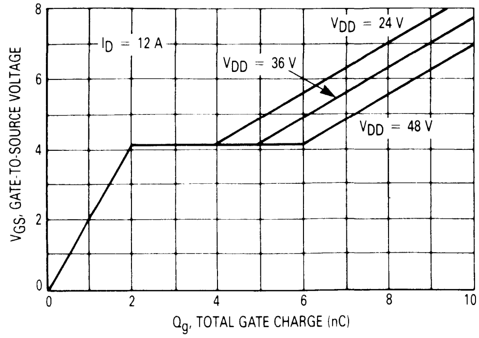
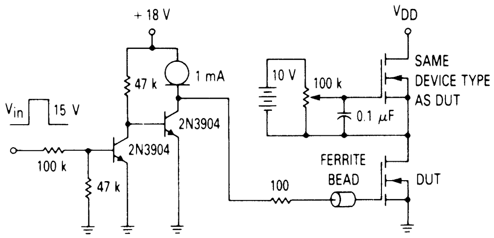
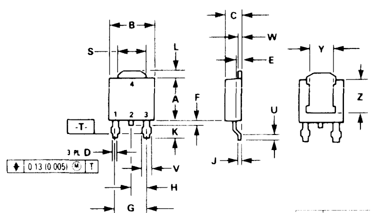


Figure 17. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS

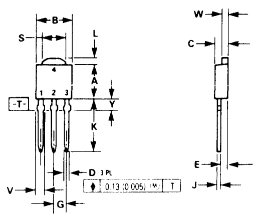


STYLE 2
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1. SURFACE "T" IS BOTH A DATUM AND A SEATING PLANE
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
3. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.97	1.06	0.038	0.042
F	0.64	0.88	0.025	0.035
G	4.58 BSC		0.180 BSC	
H	2.29 BSC		0.090 BSC	
J	6.46	0.58	0.018	0.023
K	2.59	2.89	0.102	0.114
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
U	0.51	—	0.020	—
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	4.32	—	0.170	—
Z	3.69	—	0.145	—

CASE 369A-04
MTD3055EL



STYLE 2
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. SURFACE "T" IS BOTH A DATUM AND A MOUNTING SURFACE
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
3. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.64	0.88	0.025	0.035
E	0.97	1.06	0.038	0.042
G	2.29 BSC		0.090 BSC	
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
L	0.89	1.27	0.035	0.050
S	5.21	5.46	0.205	0.215
V	0.77	1.14	0.030	0.045
W	0.84	0.94	0.033	0.037
Y	1.91	2.28	0.075	0.090

CASE 369-03
MTD3055EL1

3

MTH5N95
MTH5N100
MTM5N95
MTM5N100

Designer's Data Sheet

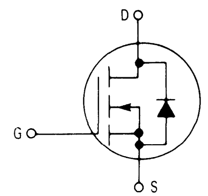
Power Field Effect Transistor

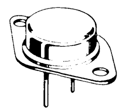
N-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 3 OHMS
950 and 1000 VOLTS

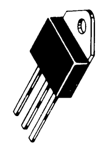
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM5N95
MTM5N100
CASE 1-06
TO-204AA



MTH5N95
MTH5N100
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 5N95	MTH or MTM 5N100	Unit
Drain-Source Voltage	V_{DSS}	950	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	950	1000	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 5 17		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH/MTM5N95 / MTH/MTM5N100	$V_{(BR)DSS}$	950 / 1000	— / —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) / (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— / —	0.2 / 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) / T_J = 100°C	$V_{GS(th)}$	2 / 1.5	4.5 / 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$r_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) / (I_D = 2.5 Adc, T_J = 100°C)	$V_{DS(on)}$	— / —	15 / 12.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	2600	pF
Output Capacitance	C_{oss}	—	350	
Reverse Transfer Capacitance	C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	70	ns
Rise Time	t_r	—	250	
Turn-Off Delay Time	$t_{d(off)}$	—	500	
Fall Time	t_f	—	200	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	110 (Typ)	140	nC
Gate-Source Charge	Q_{gs}	60 (Typ)	—	
Gate-Drain Charge	Q_{gd}	50 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) / (Measured from the drain lead 0.25″ from package to center of die)	L_d	4 (Typ) / 5 (Typ)	— / —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

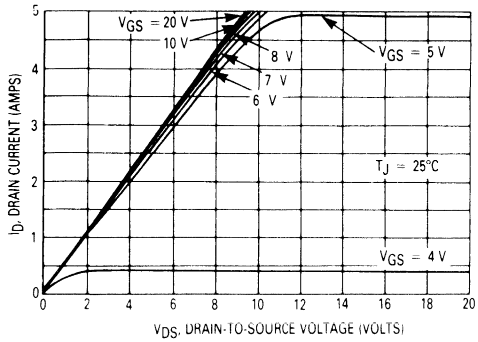


Figure 1. On-Region Characteristics

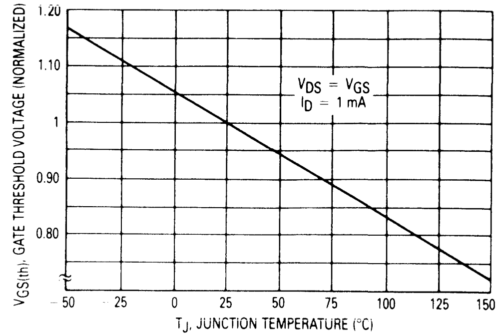


Figure 2. Gate-Threshold Voltage Variation With Temperature

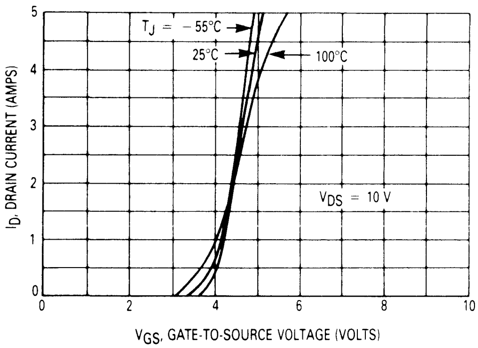


Figure 3. Transfer Characteristics

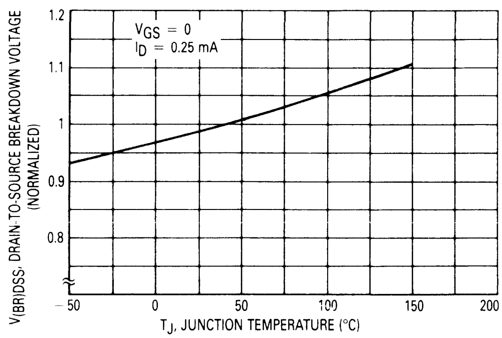


Figure 4. Breakdown Voltage Variation With Temperature

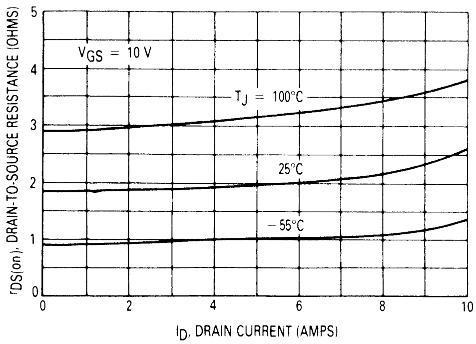


Figure 5. On-Resistance versus Drain Current

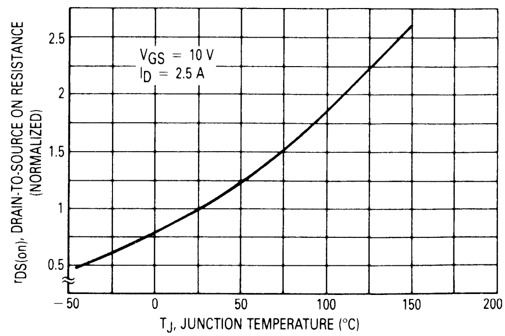


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

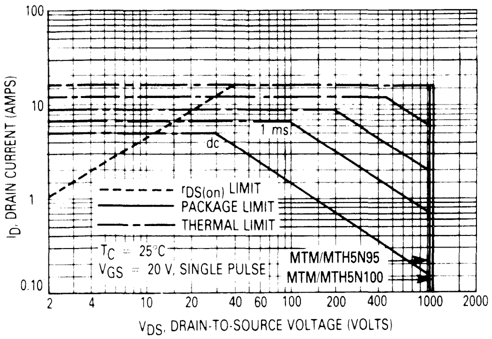


Figure 7. Maximum Rated Forward Biased Safe Operating Area

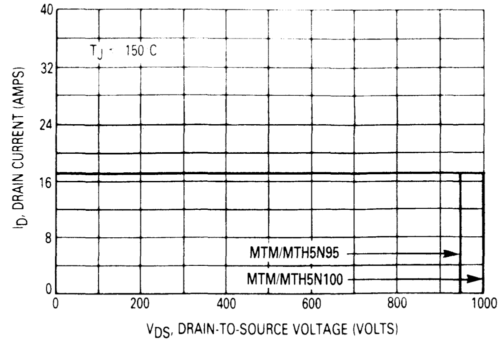


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

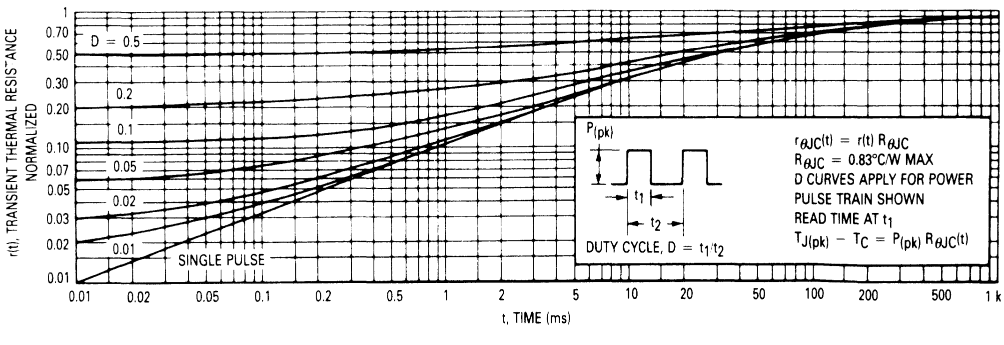


Figure 9. Thermal Response

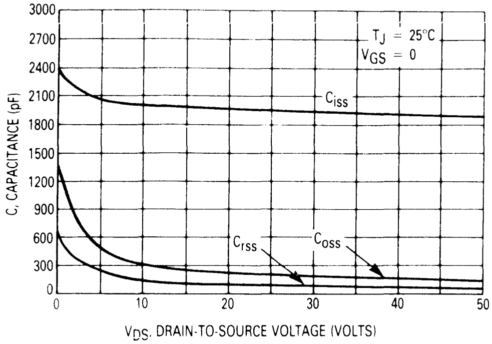


Figure 10. Capacitance Variation

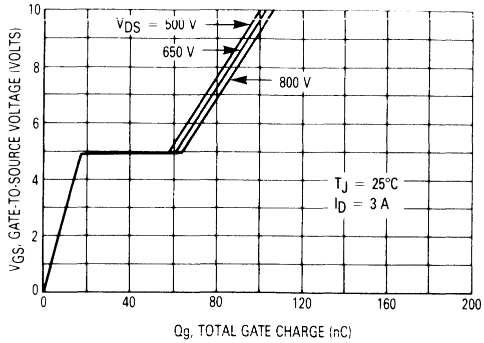


Figure 11. Gate Charge versus Gate-To-Source Voltage

3

RESISTIVE SWITCHING

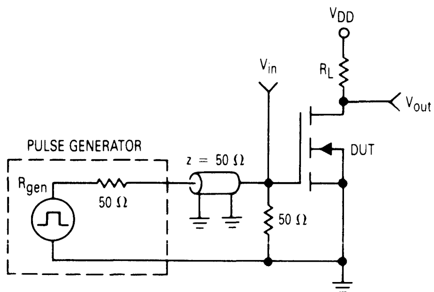


Figure 12. Switching Test Circuit

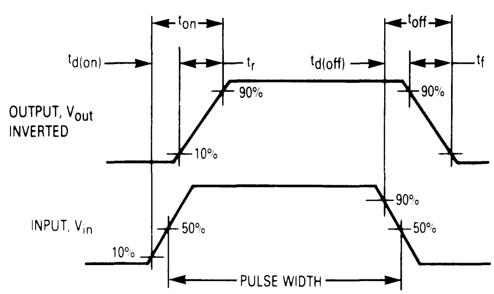
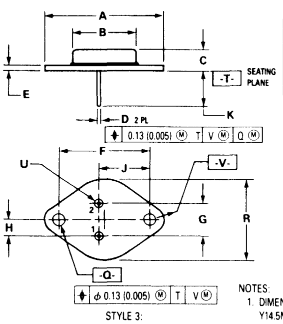


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

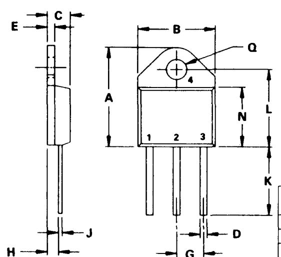


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MTH6N55
MTH6N60
MTM6N60

Designer's Data Sheet

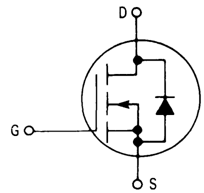
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

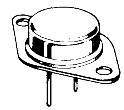
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

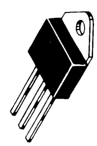
TMOS POWER FETs
6 AMPERES
$r_{DS(on)}$ = 1.2 OHMS
550 and 600 VOLTS



3



MTM6N60
CASE 1-06
TO-204AA



MTH6N55
MTH6N60
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH6N55	MTH6N60 MTM6N60	Unit
Drain-Source Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current Continuous Pulsed	I_D I_{DM}	6 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH6N55 MTH6N60, MTM6N60	$V_{(BR)DSS}$	 550 600	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	1.2	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc)		$V_{DS(on)}$	—	9	Vdc
(I_D = 3 Adc, T_J = 100°C)			—	7.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 3 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	55 (Typ)	65	nC
Gate-Source Charge		Q_{gs}	25 (Typ)	—	
Gate-Drain Charge		Q_{gd}	30 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond part)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance		L_d			nH
(Measured from screw on tab to center of die)			4 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

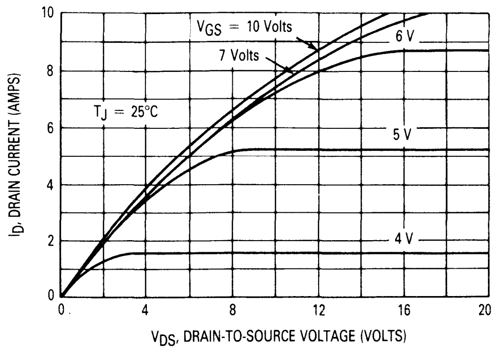


Figure 1. On-Region Characteristics

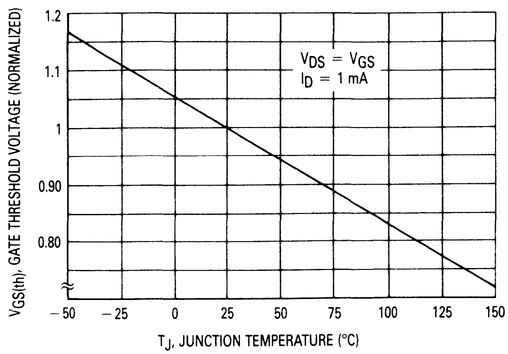


Figure 2. Gate-Threshold Voltage Variation With Temperature

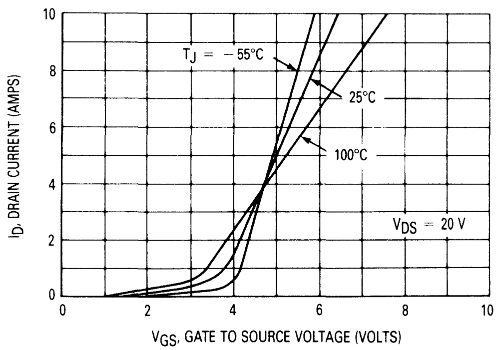


Figure 3. Transfer Characteristics

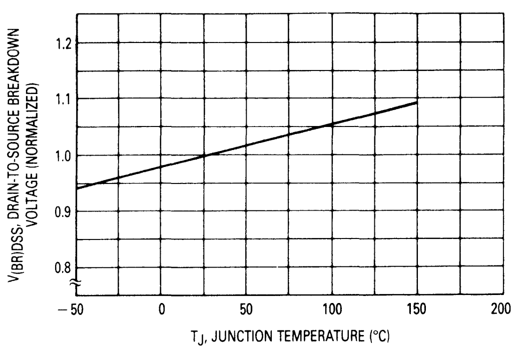


Figure 4. Breakdown Voltage Variation With Temperature

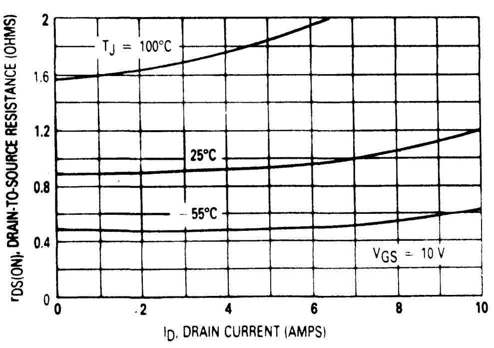


Figure 5. On-Resistance versus Drain Current

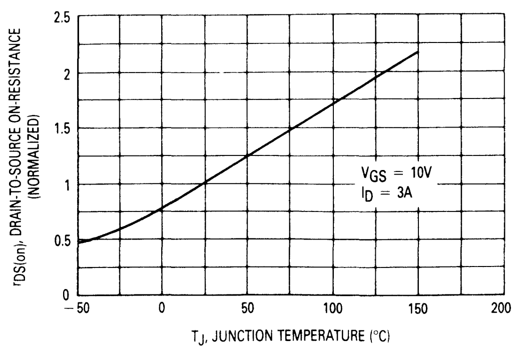


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

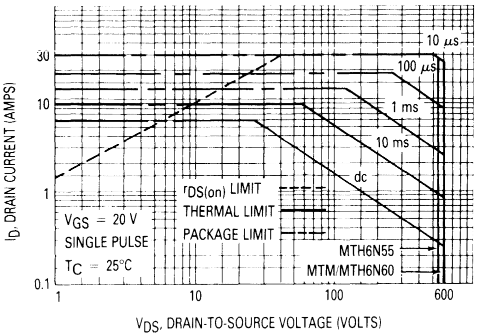


Figure 7. Maximum Rated Forward Biased Safe Operating Area

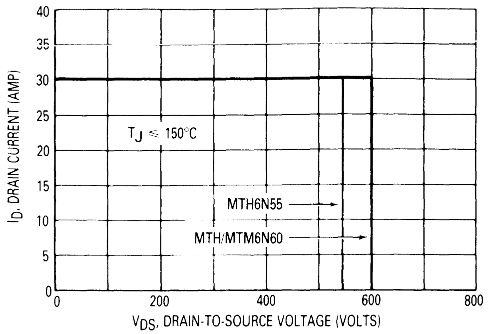


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

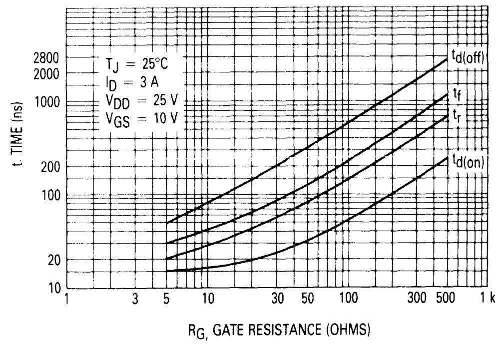


Figure 9. Resistive Switching Time Variation versus Gate Resistance

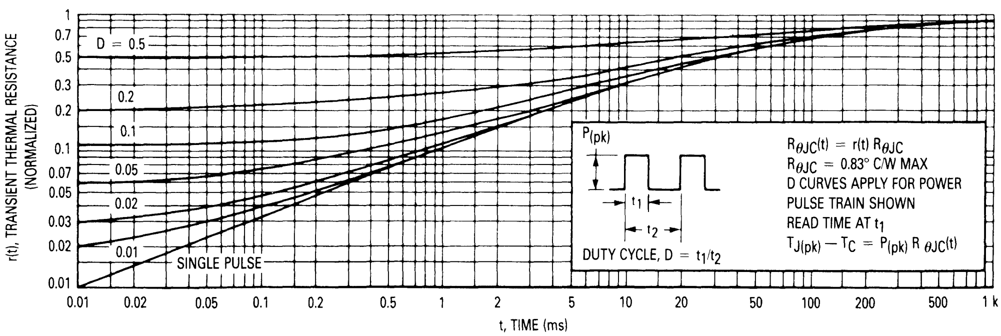


Figure 10. Thermal Response

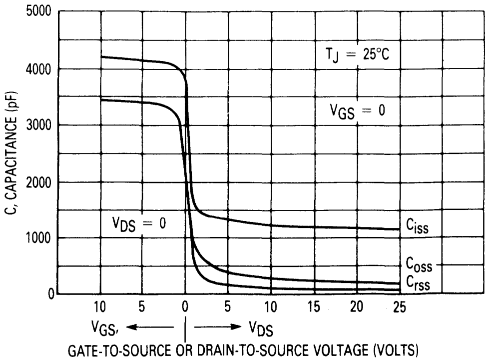


Figure 11. Capacitance Variation

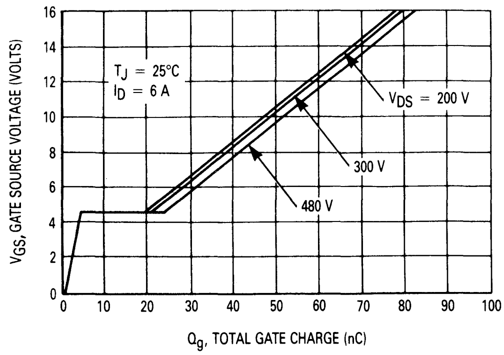


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

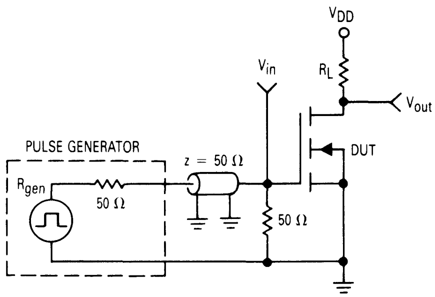


Figure 13. Switching Test Circuit

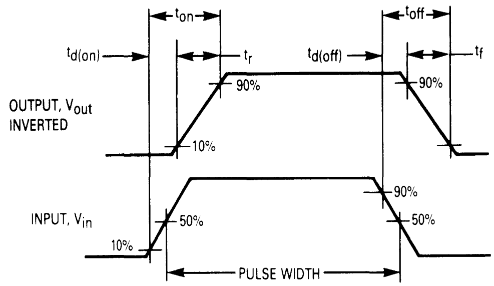
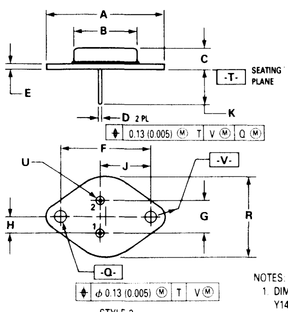


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

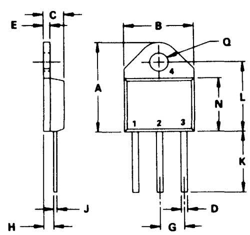


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH6N85
MTH6N90
MTM6N85
MTM6N90

Designer's Data Sheet

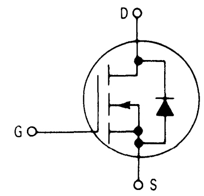
Power Field Effect Transistor

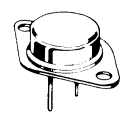
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
6 AMPERES
$r_{DS(on)}$ = 3 OHMS
850 and 900 VOLTS

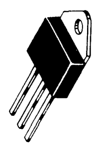
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM6N85
MTM6N90
CASE 1-06
TO-204AA



MTH6N85
MTH6N90
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 6N85	MTH or MTM 6N90	Unit
Drain-Source Voltage	V_{DSS}	850	900	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	850	900	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 6 22		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTH/MTM6N85	$V_{(BR)DSS}$	850	—	Vdc
	MTH/MTM6N90		900	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc)		$V_{DS(on)}$	—	18	Vdc
(I_D = 3 Adc, T_J = 100°C)			—	14.4	
Forward Transconductance (V_{DS} = 15 V, I_D = 3 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	2600	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	70	ns
Rise Time		t_r	—	200	
Turn-Off Delay Time		$t_{d(off)}$	—	500	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	110 (Typ)	140	nC
Gate-Source Charge		Q_{gs}	60 (Typ)	—	
Gate-Drain Charge		Q_{gd}	50 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	(Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

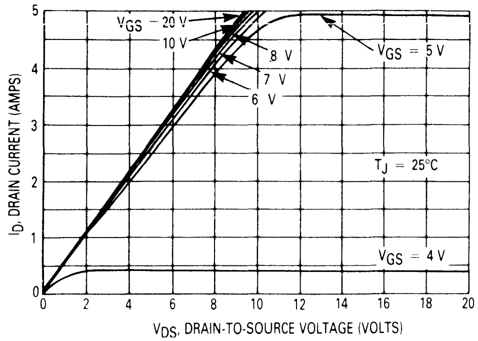


Figure 1. On-Region Characteristics

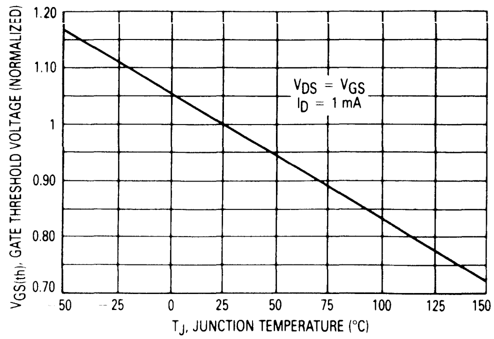


Figure 2. Gate-Threshold Voltage Variation With Temperature

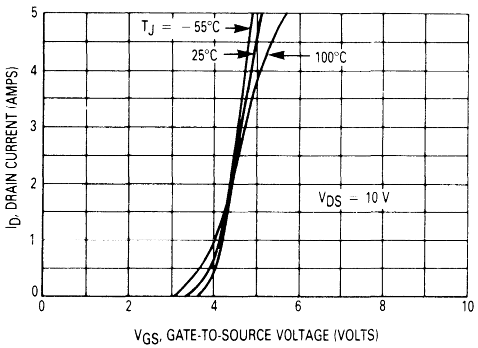


Figure 3. Transfer Characteristics

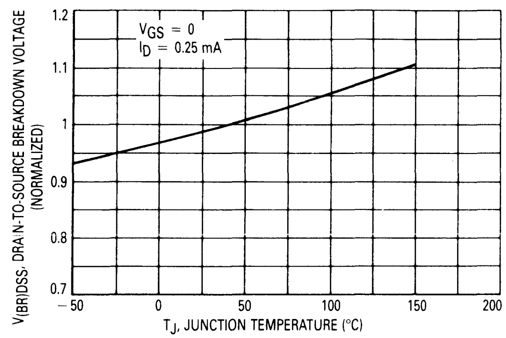


Figure 4. Breakdown Voltage Variation With Temperature

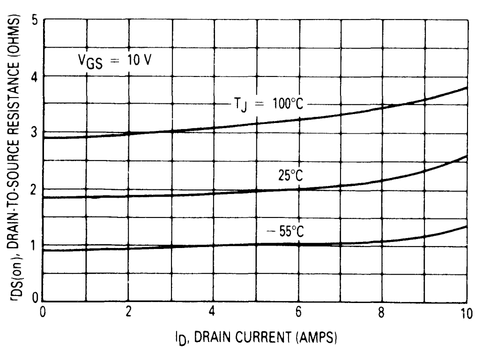


Figure 5. On-Resistance versus Drain Current

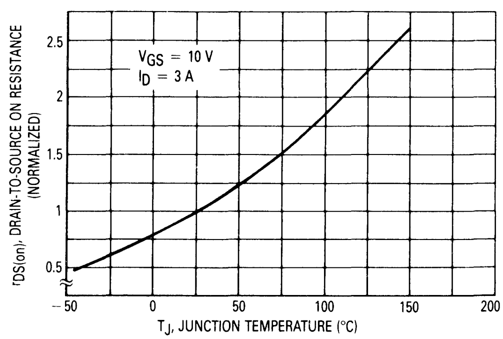


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

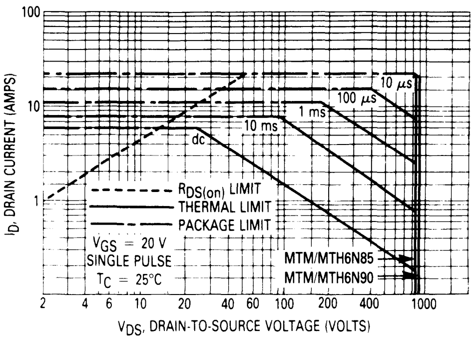


Figure 7. Maximum Rated Forward Biased Safe Operating Area

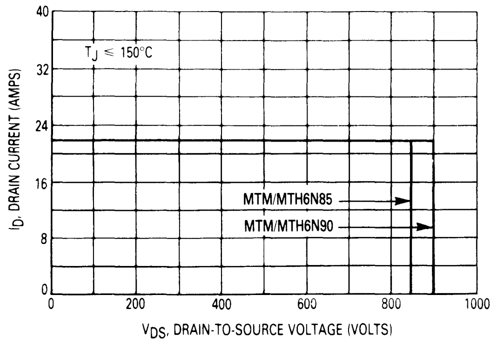


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

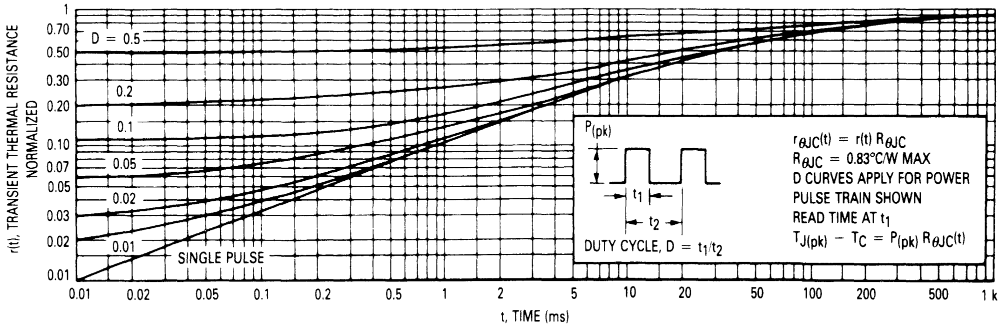


Figure 9. Thermal Response

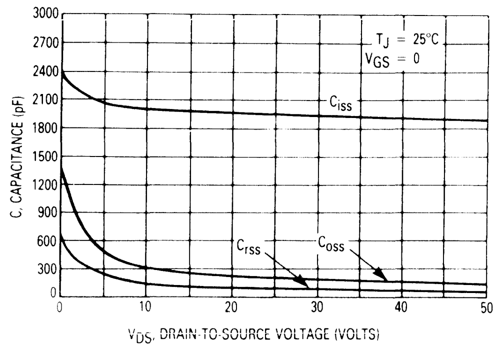


Figure 10. Capacitance Variation

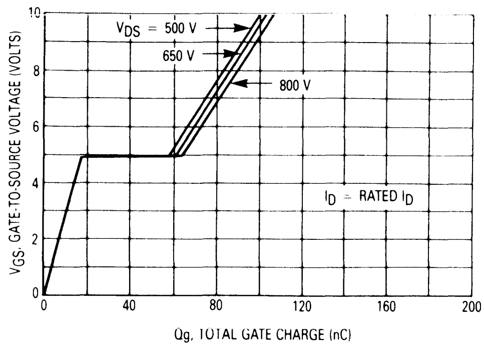


Figure 11. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

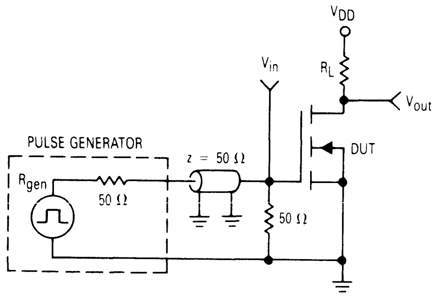


Figure 12. Switching Test Circuit

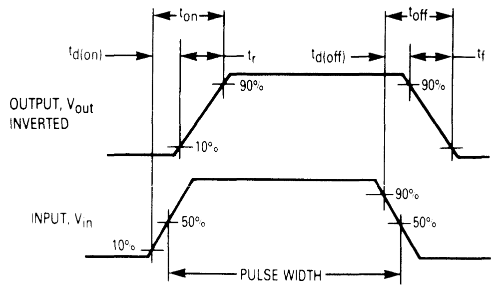
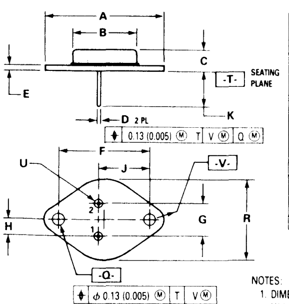


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

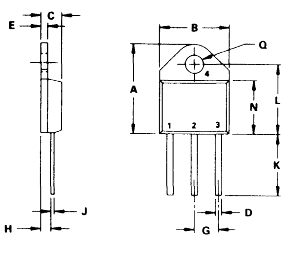


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 340-02
TO-218AC



STYLE 2
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MTH6N100

Designer's Data Sheet

Power Field Effect Transistor

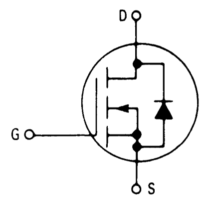
N-Channel Enhancement-Mode Silicon Gate TMOS

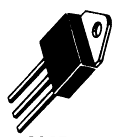
TMOS POWER FETs
6 AMPERES
$r_{DS(on)}$ = 2 OHMS
1000 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Similar To IRFPG50

TMOS™





CASE 340-02
TO-218AC

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	1000	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	6 24	Adc
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	1000	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0) (V_{DS} = 1000 Vdc, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4 3.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	2	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc) (I_D = 3 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	15 12	Vdc
Forward Transconductance (V_{DS} = 20 V, I_D = 3 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	2000 (Typ)	—	pF
Output Capacitance		C_{oss}	175 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	100 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 3 Amps R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	55 (Typ)	—	ns
Rise Time		t_r	175 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	440 (Typ)	—	
Fall Time		t_f	180 (Typ)	—	
Total Gate Charge	(V_{DS} = 800 V, I_D = 6 Amps, V_{GS} = 10 V) See Figures 11 and 12	Q_g	110 (Typ)	140	nC
Gate-Source Charge		Q_{gs}	17 (Typ)	—	
Gate-Drain Charge		Q_{gd}	50 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 6 Amps, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time	(I_S = 6 A, dI_S/dt = 100 A/μs, V_R = 70 V) See Figures 15 and 16	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

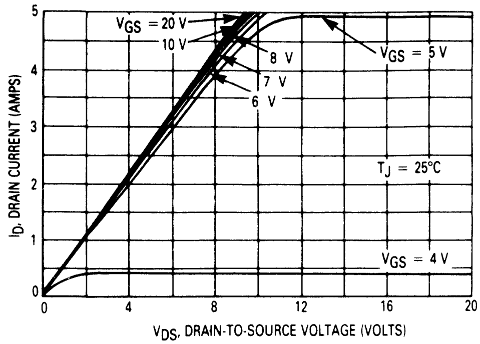


Figure 2. Gate-Threshold Voltage Variation With Temperature

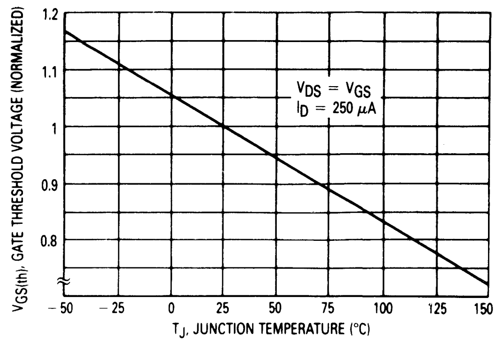


Figure 3. Transfer Characteristics

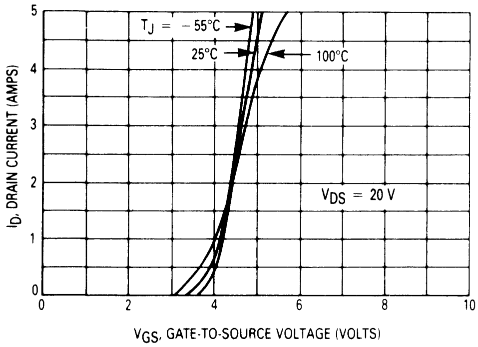


Figure 4. Breakdown Voltage Variation With Temperature

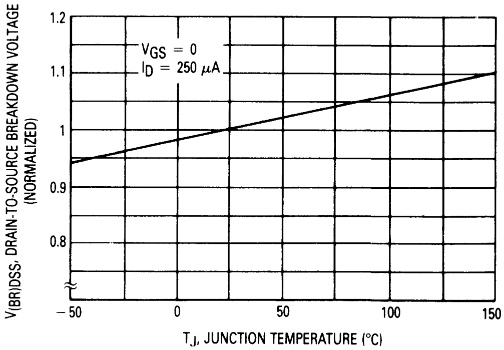


Figure 5. On-Resistance versus Drain Current

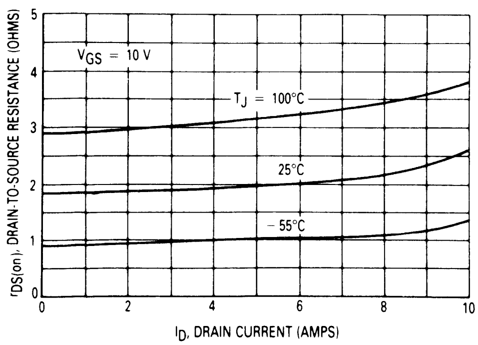
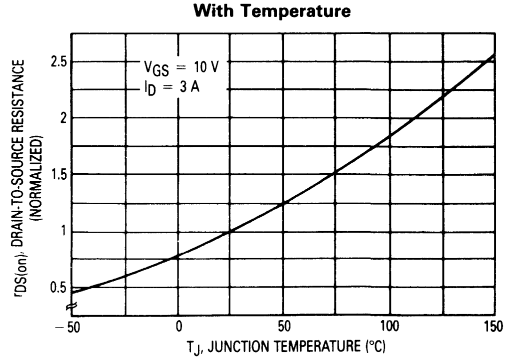


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

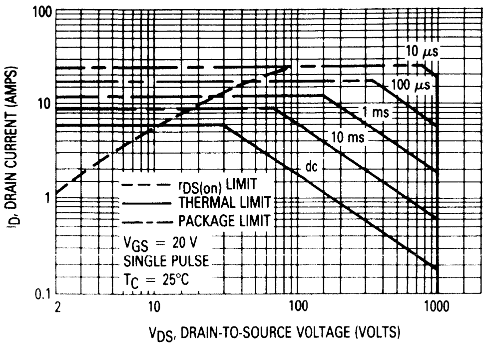
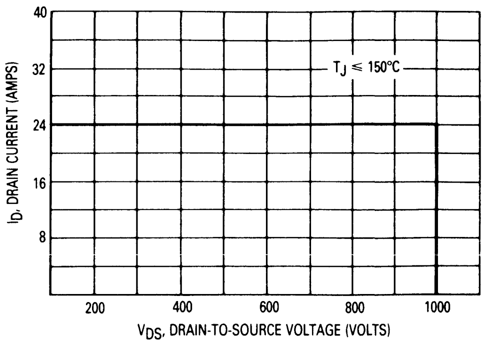


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response

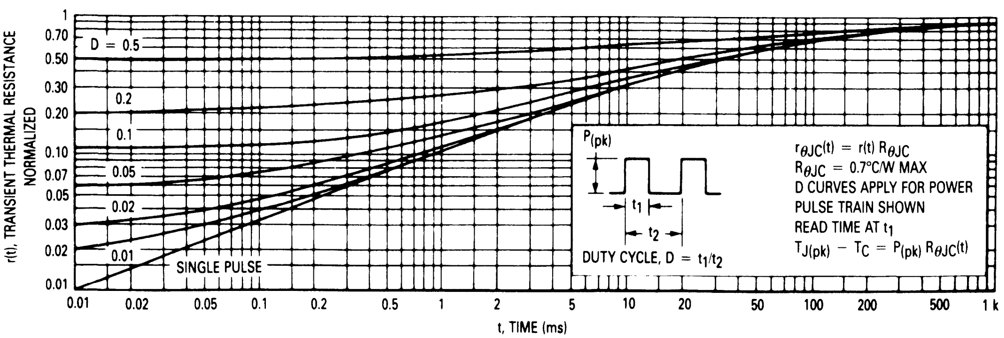


Figure 10. Capacitance Variation

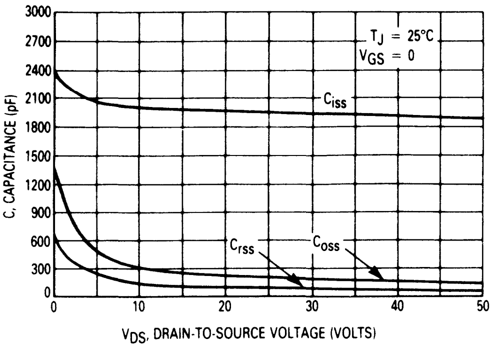
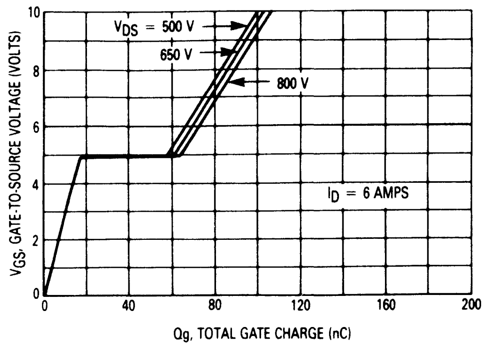


Figure 11. Gate Charge versus Gate-to-Source Voltage



RESISTIVE SWITCHING

Figure 12. Gate Charge Test Circuit

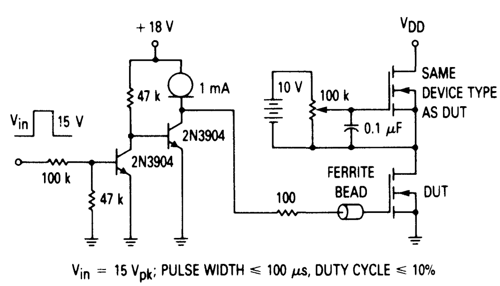


Figure 13. Switching Test Circuit

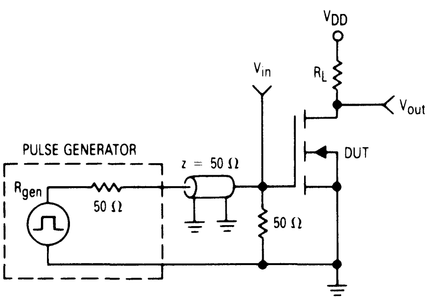


Figure 14. Switching Waveforms

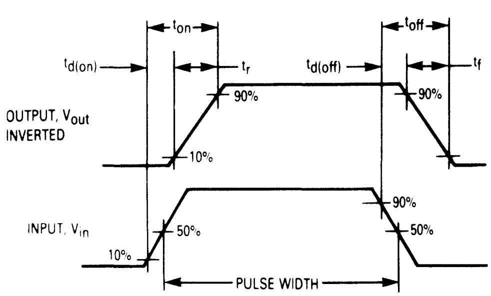


Figure 15. Diode Switching Waveform

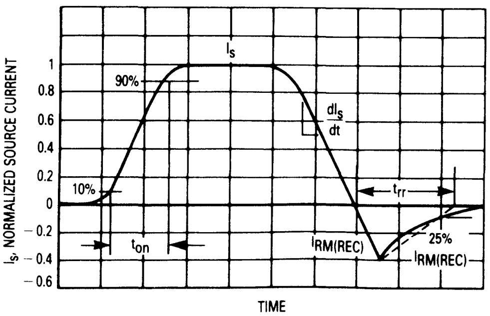
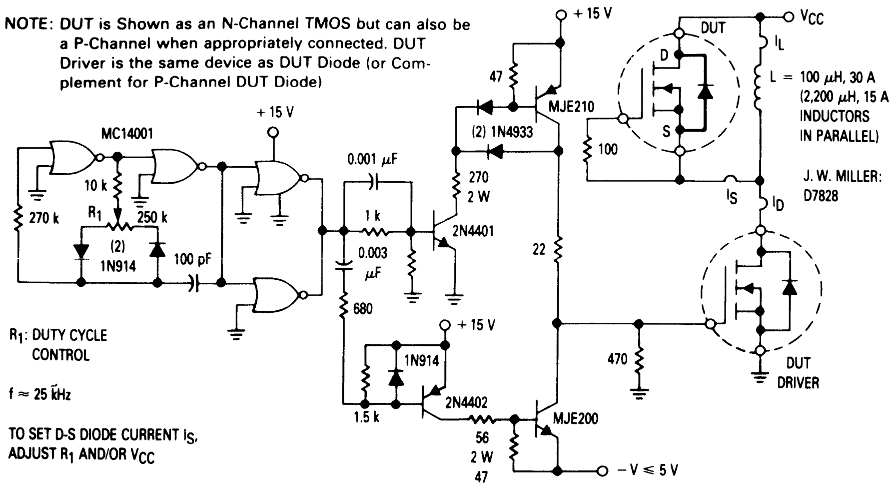
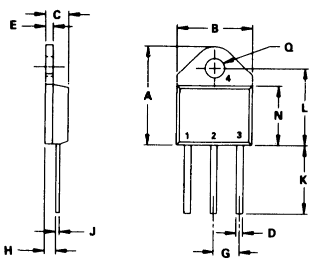


Figure 16. TMOS Diode Switching Test Circuit



OUTLINE DIMENSIONS

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MTH7N45
MTH7N50
MTM7N45
MTM7N50

Designer's Data Sheet

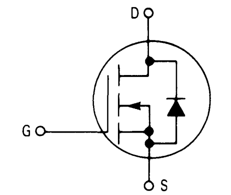
Power Field Effect Transistor

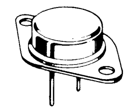
N-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
7 AMPERES
$r_{DS(on)}$ = 0.8 OHM
450 and 500 VOLTS

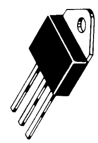
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM7N45
MTM7N50
CASE 1-06
TO-204AA



MTH7N45
MTH7N50
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 7N45	MTH or MTM 7N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50$ μs)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	7 40		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH7N45, MTM7N45 MTH7N50, MTM7N50	$V_{(BR)DSS}$	 450 500	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$r_{DS(on)}$	—	0.8	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7 Adc)		$V_{DS(on)}$	—	7	Vdc
(I_D = 3.5 Adc, T_J = 100°C)			—	5.6	
Forward Transconductance (V_{DS} = 10 V, I_D = 3.5 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	55 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	32 (Typ)	—	
Gate-Drain Charge		Q_{gd}	23 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	280 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	(5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

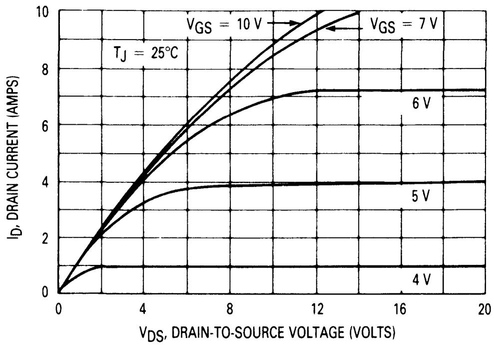


Figure 1. On-Region Characteristics

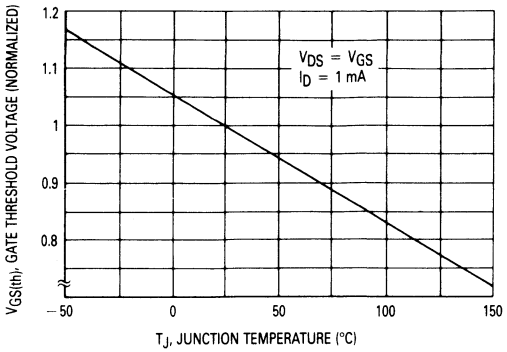


Figure 2. Gate-Threshold Voltage Variation With Temperature

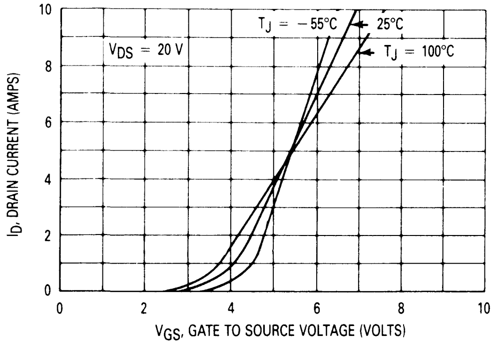


Figure 3. Transfer Characteristics

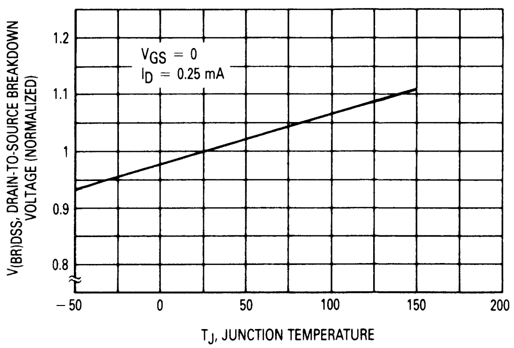


Figure 4. Breakdown Voltage Variation With Temperature

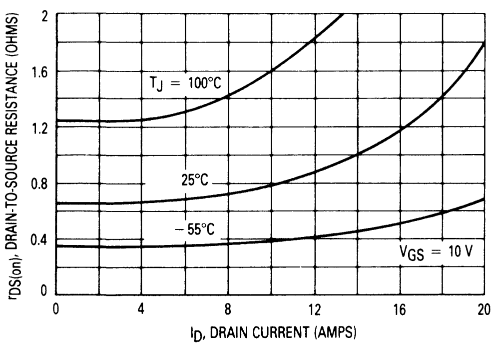


Figure 5. On-Resistance versus Drain Current

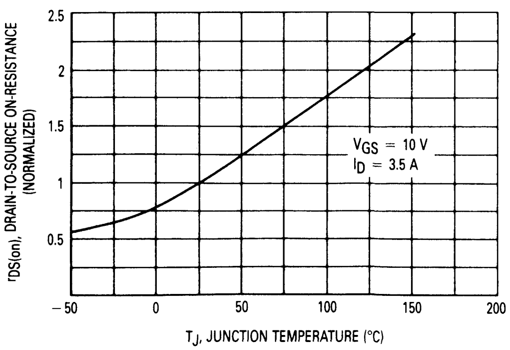


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

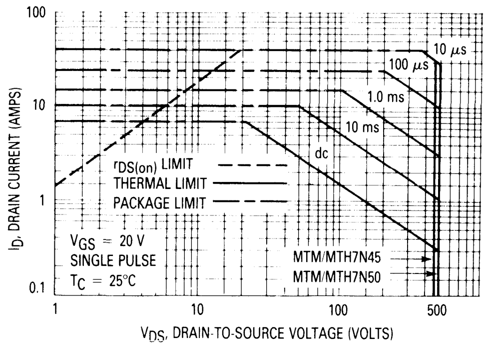


Figure 7. Maximum Rated Forward Biased Safe Operating Area

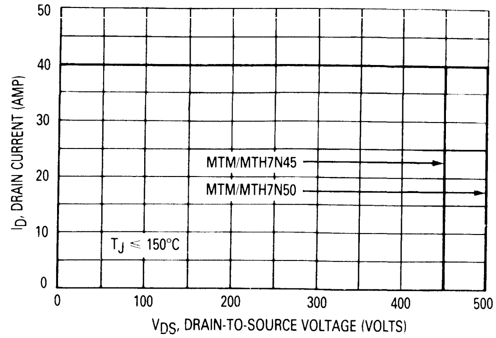


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

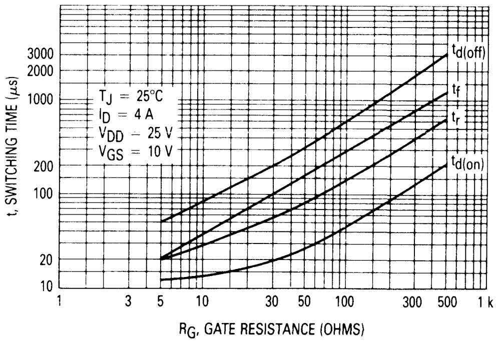


Figure 9. Resistive Switching Time Variation versus Gate Resistance

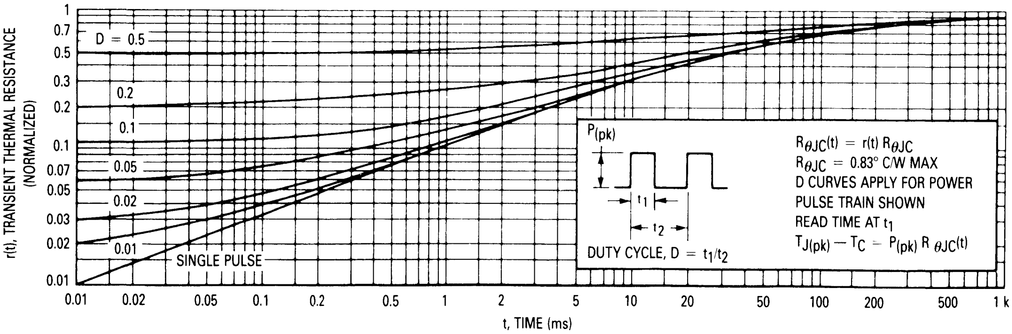


Figure 10. Thermal Response

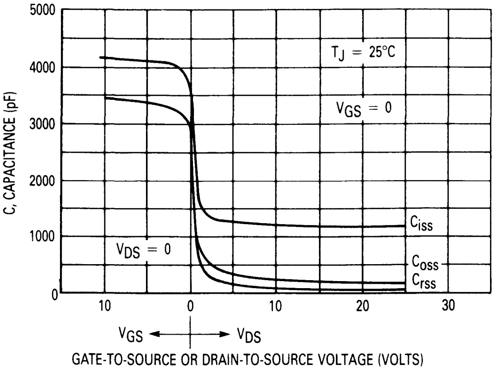


Figure 11. Capacitance Variation

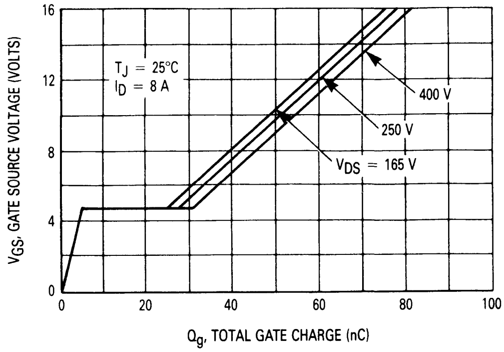


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

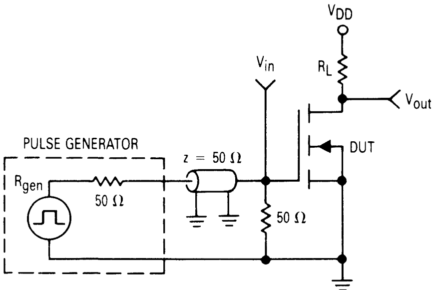


Figure 13. Switching Test Circuit

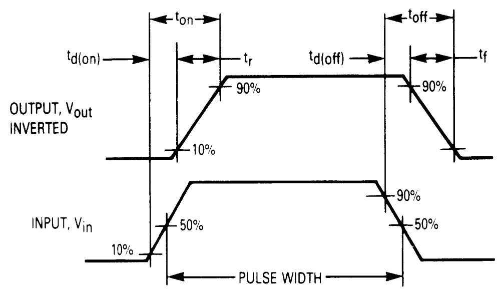
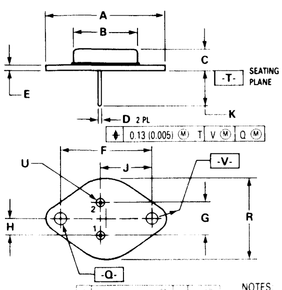


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

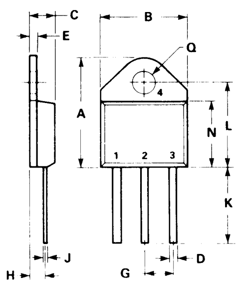
CASE 1-06
TO-204AA



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

CASE 340-02
TO-218AC

MTH8N35
MTH8N40
MTM8N35
MTM8N40

Designer's Data Sheet

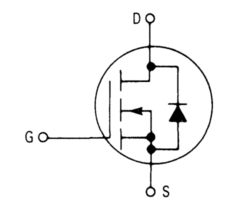
Power Field Effect Transistor

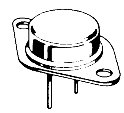
N-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.55 OHM
350 and 400 VOLTS

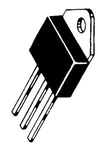
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM8N35
MTM8N40
CASE 1-06
TO-204AA



MTH8N35
MTH8N40
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 8N35	MTH or MTM 8N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 48		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH8N35, MTM8N35 MTH8N40, MTM8N40	$V_{(BR)DSS}$	 350 400	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.55	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc)		$V_{DS(on)}$	—	5.3	Vdc
(I_D = 4 Adc, T_J = 100°C)			—	4.4	
Forward Transconductance (V_{DS} = 10 V, I_D = 4 A)		g_{FS}	3	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11.	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	55 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	32 (Typ)	—	
Gate-Drain Charge		Q_{gd}	23 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	280 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	(5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

3

TYPICAL ELECTRICAL CHARACTERISTICS

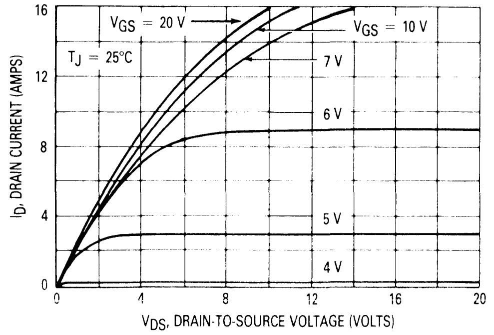


Figure 1. On-Region Characteristics

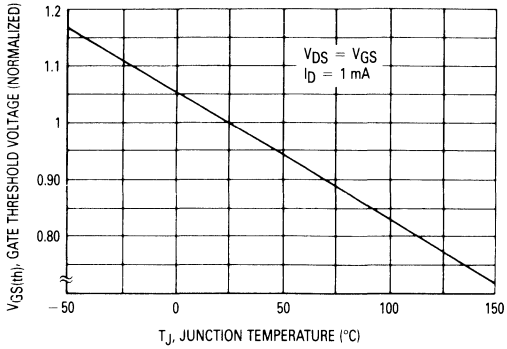


Figure 2. Gate-Threshold Voltage Variation With Temperature

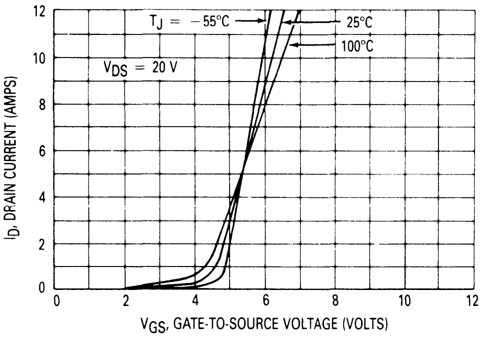


Figure 3. Transfer Characteristics

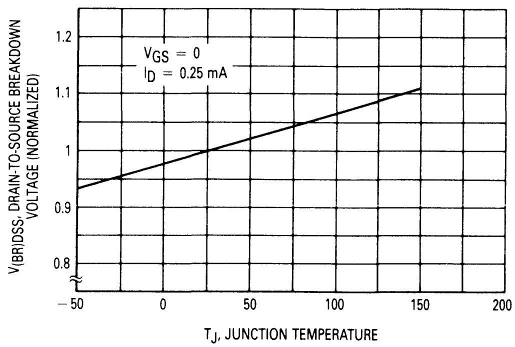


Figure 4. Breakdown Voltage Variation With Temperature

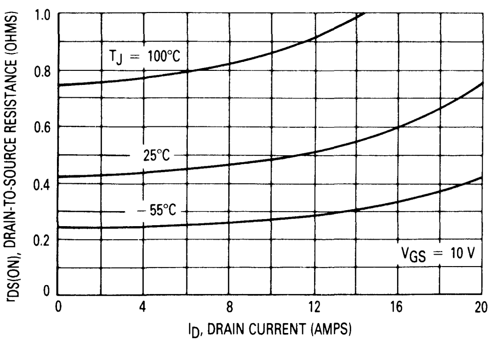


Figure 5. On-Resistance versus Drain Current

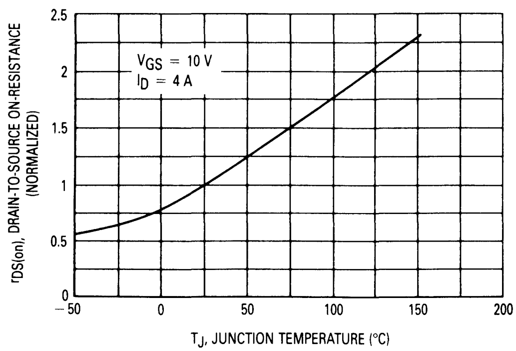


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

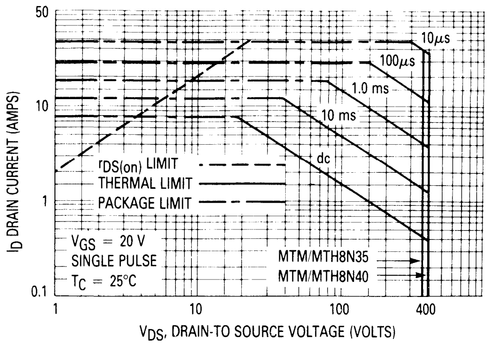


Figure 7. Maximum Rated Forward Biased Safe Operating Area

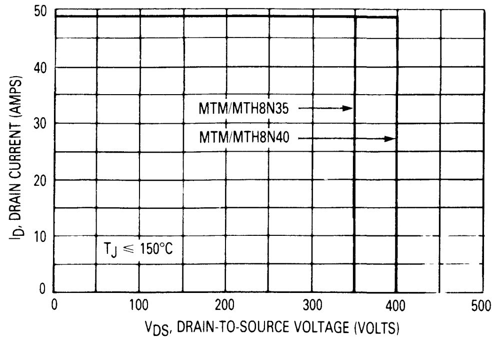


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

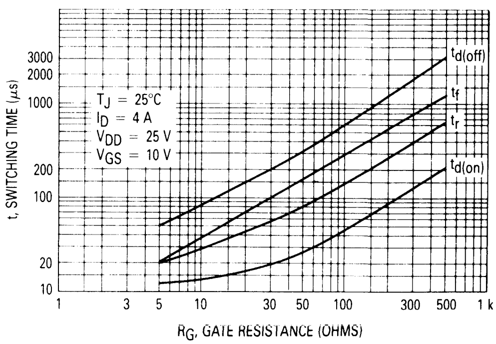


Figure 9. Resistive Switching Time Variation versus Gate Resistance

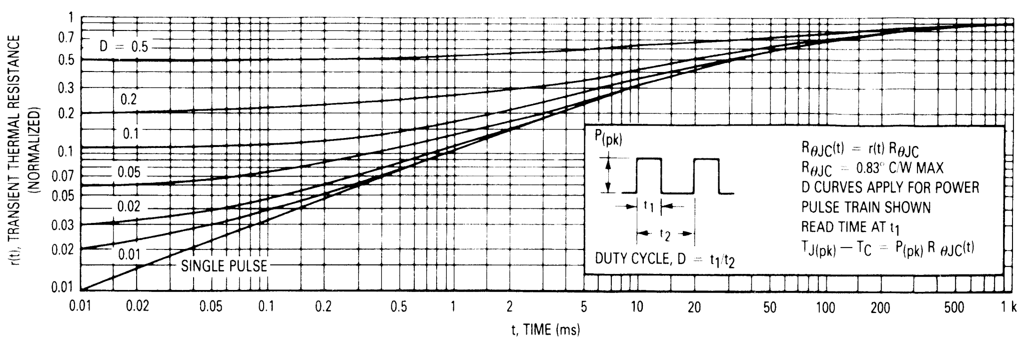


Figure 10. Thermal Response

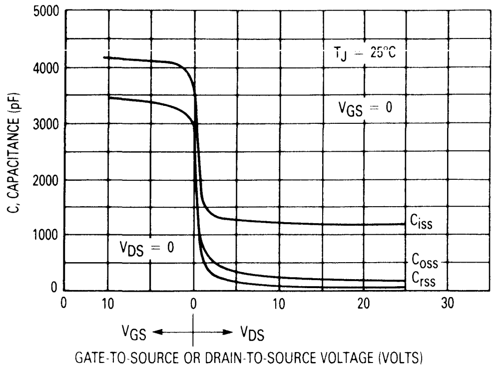


Figure 11. Capacitance Variation

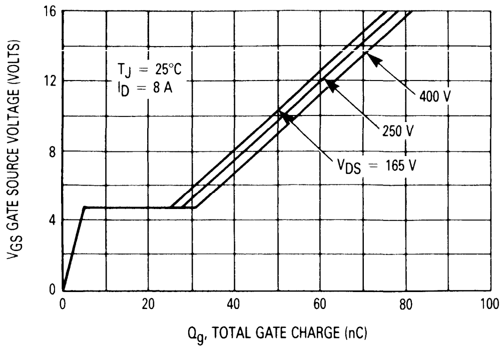


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

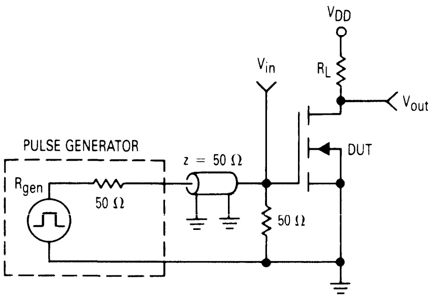


Figure 13. Switching Test Circuit

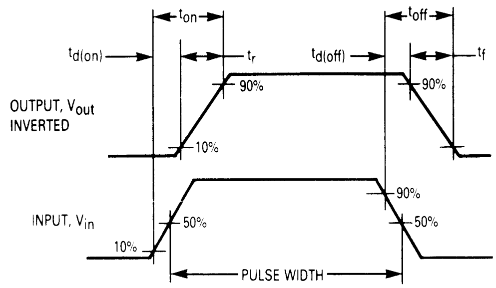
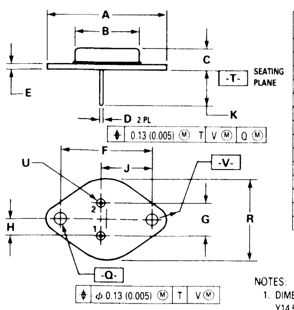


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

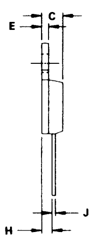


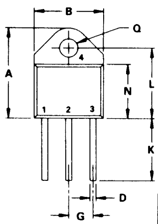
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 340-02
TO-218AC





STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MTH8N55
MTH8N60
MTM8N60

Designer's Data Sheet

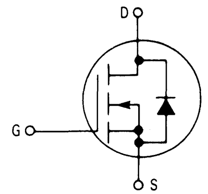
Power Field Effect Transistor

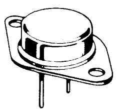
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

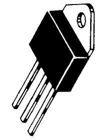
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.5 OHM
550 and 600 VOLTS





MTM8N60
CASE 1-06
TO-204AA



MTH8N55
MTH8N60
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH8N55	MTH8N60 MTM8N60	Unit
Drain-Source Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 41		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH8N55 MTH8N60, MTM8N60	$V_{(BR)DSS}$	 550 600	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.5	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc)		$V_{DS(on)}$	—	5	Vdc
(I_D = 4 Adc, T_J = 100°C)			—	4	
Forward Transconductance (V_{DS} = 10 V, I_D = 4 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	2300	pF
Output Capacitance		C_{oss}	—	425	
Reverse Transfer Capacitance		C_{rss}	—	180	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	70	ns
Rise Time		t_r	—	160	
Turn-Off Delay Time		$t_{d(off)}$	—	430	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	127 (Typ)	150	nC
Gate-Source Charge		Q_{gs}	62 (Typ)	—	
Gate-Drain Charge		Q_{gd}	65 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

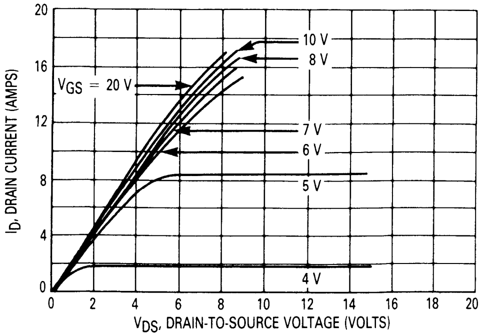


Figure 1. On-Region Characteristics

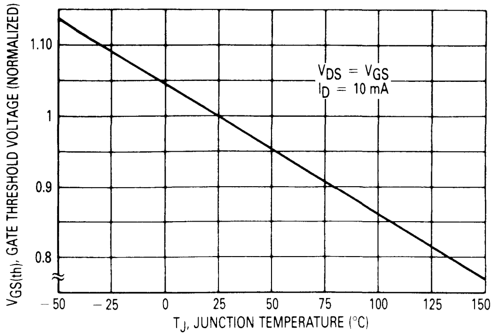


Figure 2. Gate-Threshold Voltage Variation With Temperature

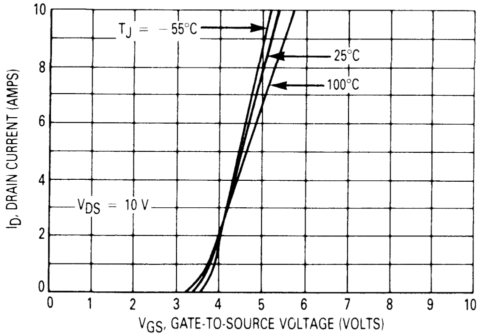


Figure 3. Transfer Characteristics

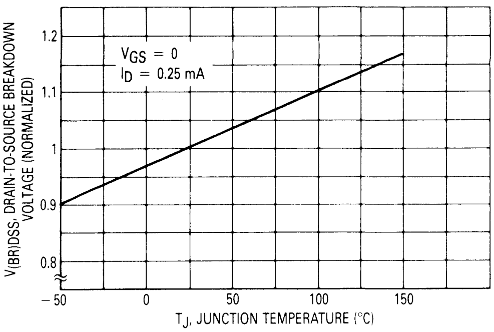


Figure 4. Breakdown Voltage Variation With Temperature

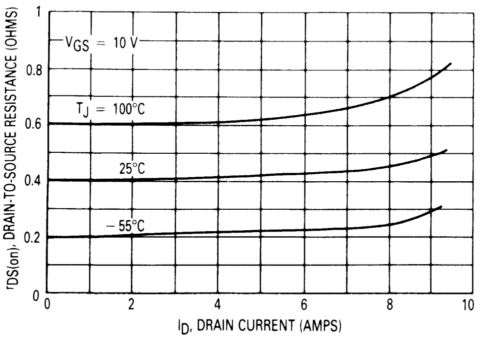


Figure 5. On-Resistance versus Drain Current

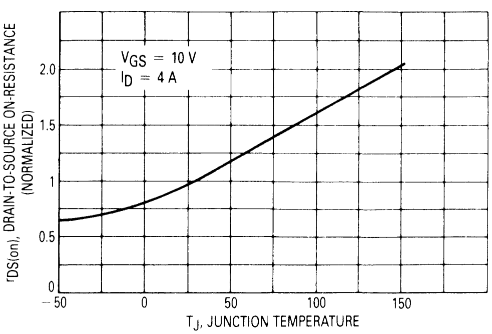


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

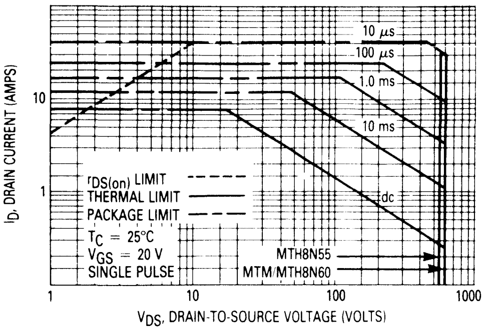


Figure 7. Maximum Rated Forward Biased Safe Operating Area

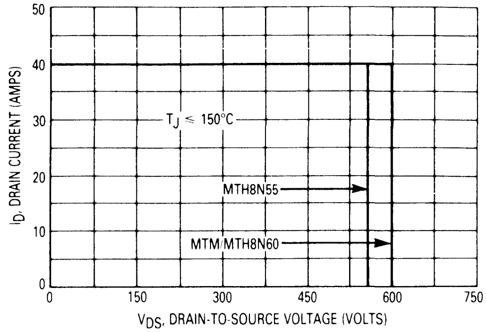


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

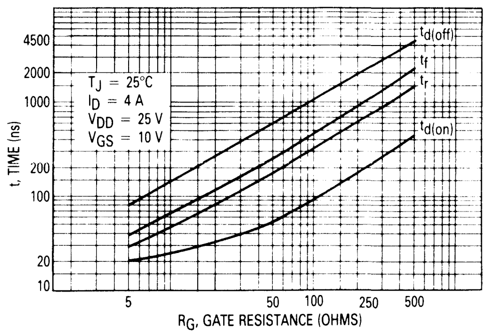


Figure 9. Resistive Switching Time Variation With Gate Resistance

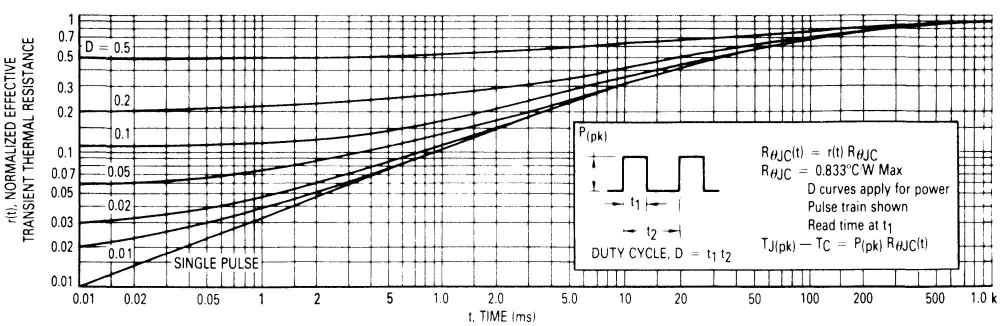


Figure 10. Thermal Response

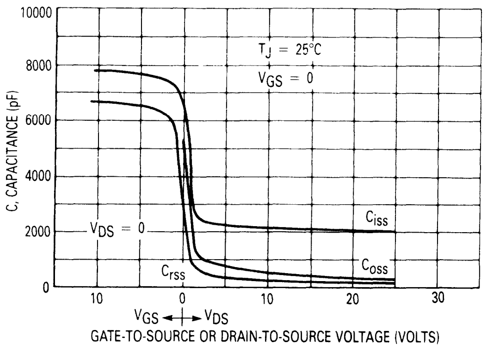


Figure 11. Capacitance Variation

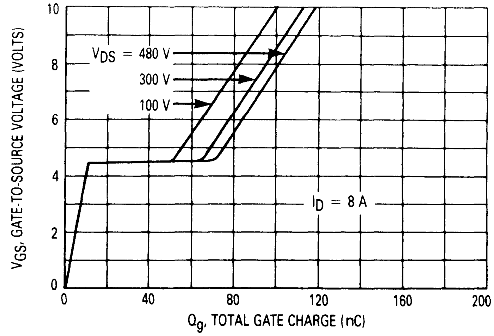


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

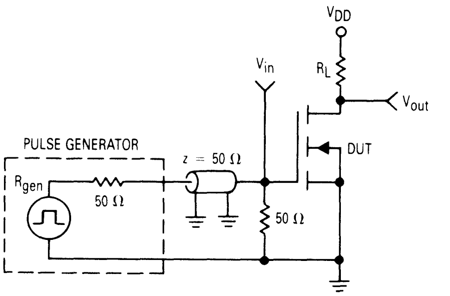


Figure 13. Switching Test Circuit

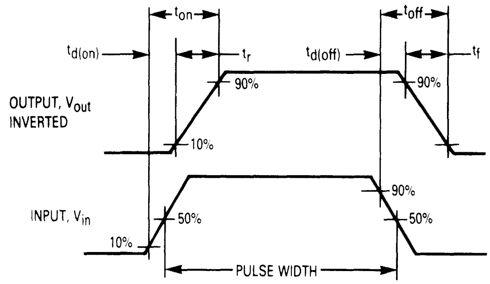
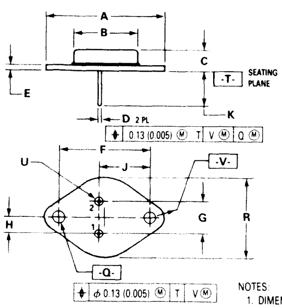


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

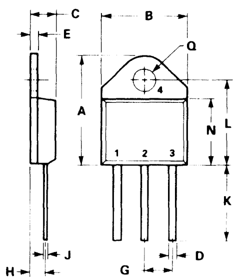
CASE 1-06
TO-204AA



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.38	0.64	0.015	0.025
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

CASE 340-02
TO-218AC

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH8N90

Designer's Data Sheet

Power Field Effect Transistor

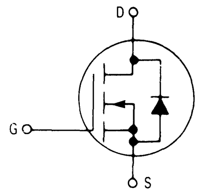
N-Channel Enhancement-Mode Silicon Gate TMOS

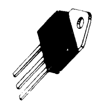
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 1.8 OHMS
900 VOLTS





CASE 340-02
TO-218AC

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	900	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	900	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 22	Adc
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	900	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	1.8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 17 15	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	3	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	2000 (Typ)	—	pF
Output Capacitance		C_{oss}	175 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	100 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 4 Amps R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	55 (Typ)	—	ns
Rise Time		t_r	175 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	440 (Typ)	—	
Fall Time		t_f	180 (Typ)	—	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 8 Amps, V_{GS} = 10 V) See Figures 11 and 14	Q_g	110 (Typ)	140	nC
Gate-Source Charge		Q_{gs}	18 (Typ)	—	
Gate-Drain Charge		Q_{gd}	50 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 8 Amps, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time	(I_S = 8 A, dI_S/dt = 100 A/μs, V_R = 70 V, See Figures 15 and 16)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 4 (Typ) 5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

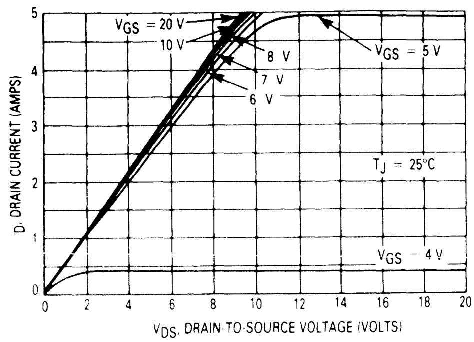


Figure 2. Gate-Threshold Voltage Variation With Temperature

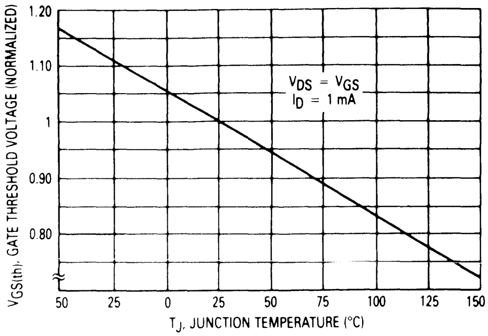


Figure 3. Transfer Characteristics

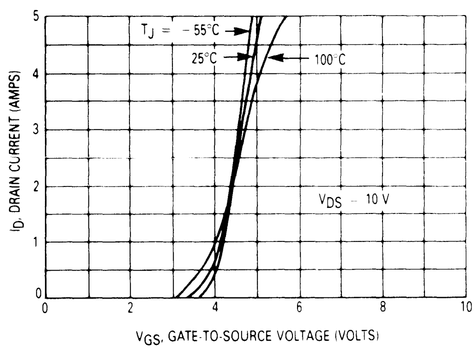


Figure 4. Breakdown Voltage Variation With Temperature

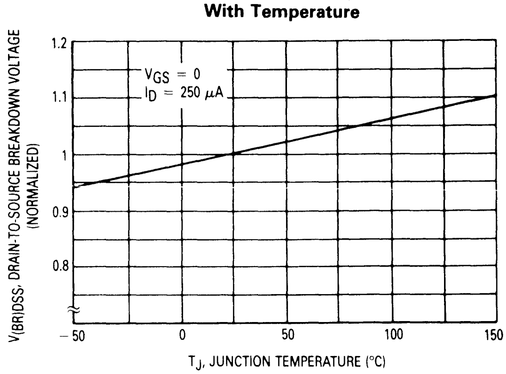


Figure 5. On-Resistance versus Drain Current

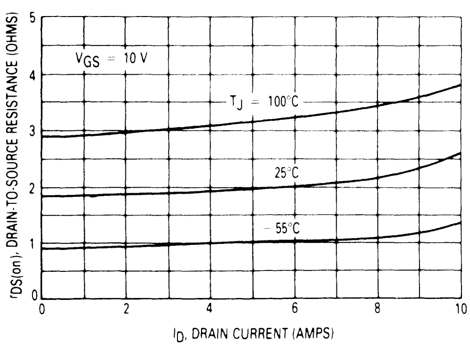
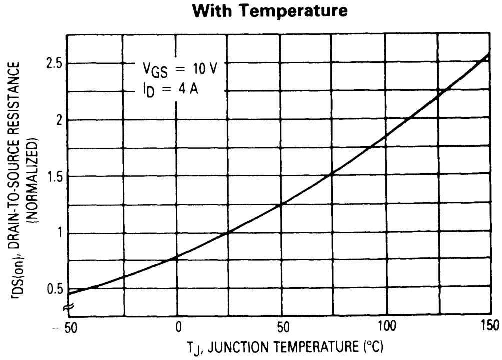


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

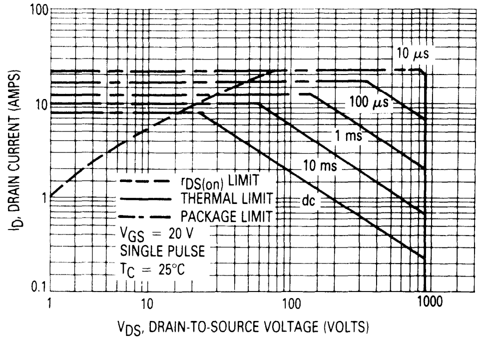
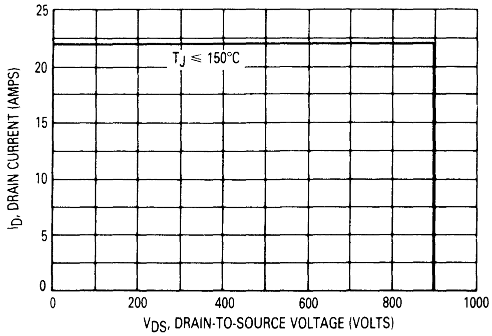


Figure 8. Maximum Rated Switching Safe Operating Area



3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response

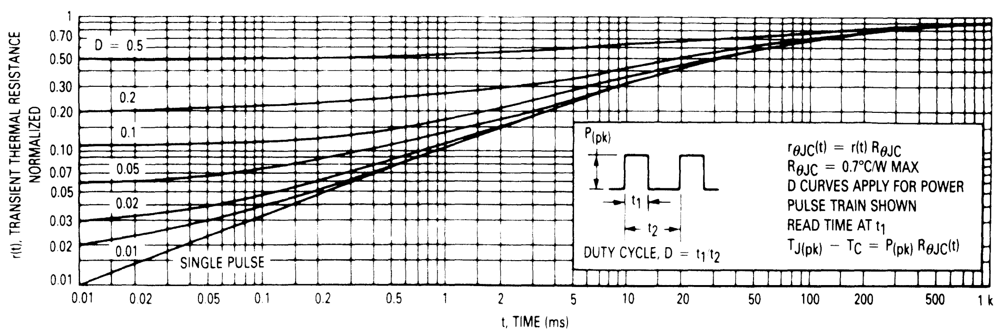


Figure 10. Capacitance Variation

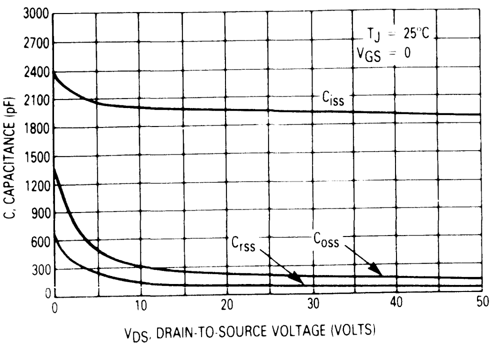
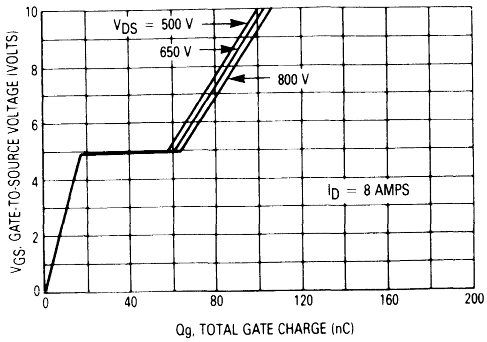


Figure 11. Gate Charge versus Gate-to-Source Voltage



RESISTIVE SWITCHING

Figure 12. Switching Test Circuit

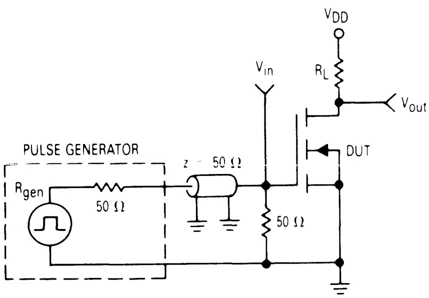


Figure 13. Switching Waveforms

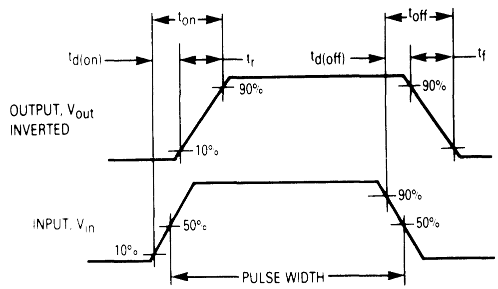
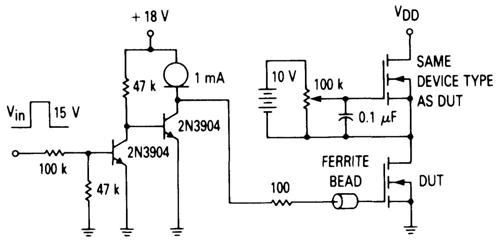


Figure 14. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 15. TMOS Diode Switching Test Circuit

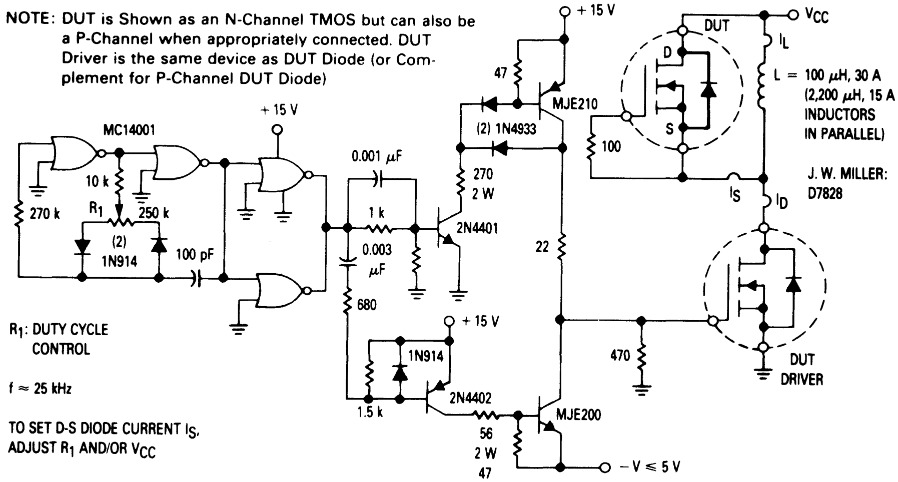
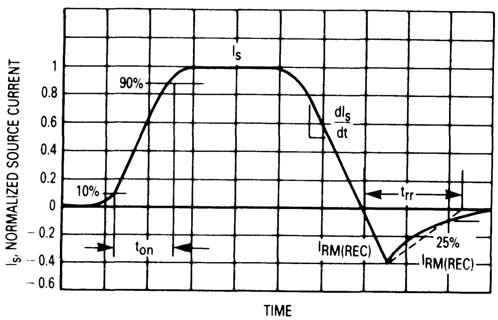
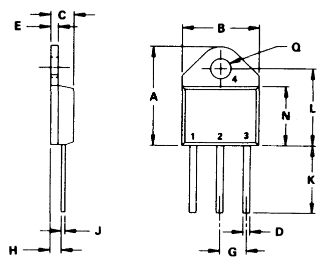


Figure 16. Diode Switching Waveform



OUTLINE DIMENSIONS

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

3

MTH8P18
MTH8P20
MTM8P18
MTM8P20

Designer's Data Sheet

Power Field Effect Transistor

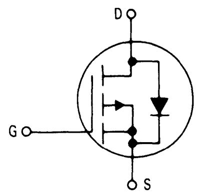
P-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.7 OHM
180 and 200 VOLTS

3

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

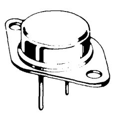


MAXIMUM RATINGS

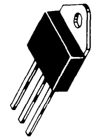
Rating	Symbol	MTH or MTM 8P18	MTH or MTM 8P20	Unit
Drain-Source Voltage	V_{DSS}	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	180	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 8 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTM8P18
MTM8P20
CASE 1-04
TO-204AA



MTH8P18
MTH8P20
CASE 340-02
TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTH/MTM8P18 MTH/MTM8P20	$V_{(BR)DSS}$	180 200	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.7	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	7 6	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	120	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 11 and 12	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	80	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	2 (Typ)	4.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	350 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

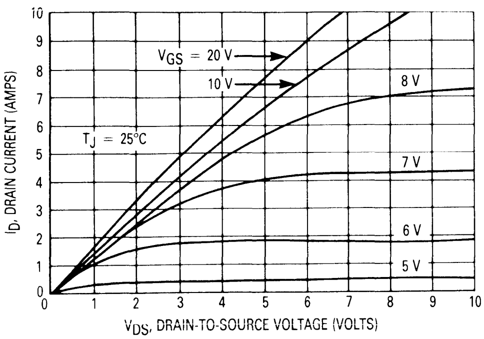


Figure 1. On-Region Characteristics

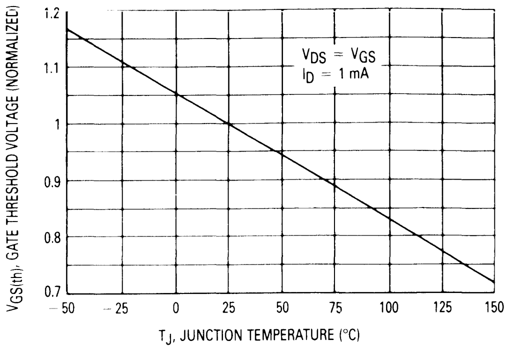


Figure 2. Gate-Threshold Voltage Variation With Temperature

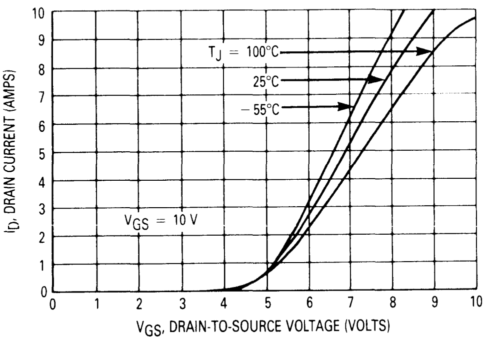


Figure 3. Transfer Characteristics

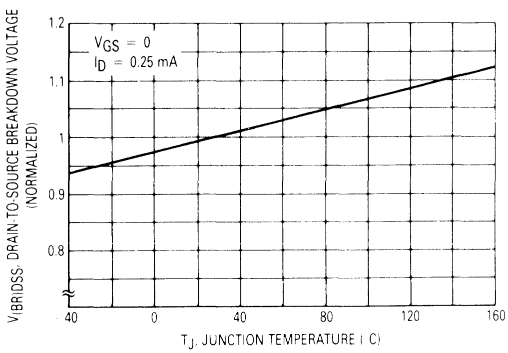


Figure 4. Breakdown Voltage Variation With Temperature

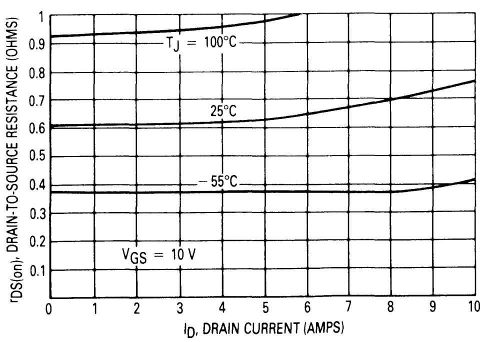


Figure 5. On-Resistance versus Drain Current

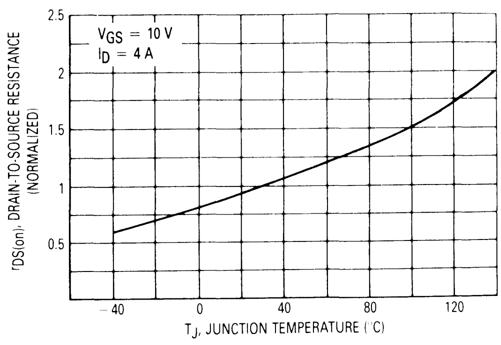


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

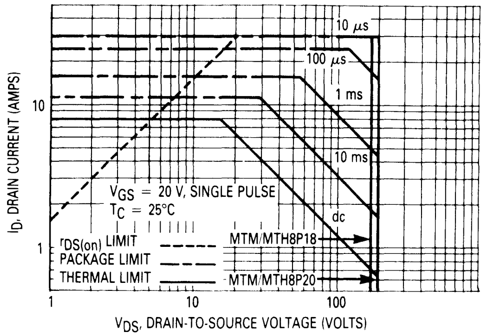


Figure 7. Maximum Rated Forward Biased Safe Operating Area

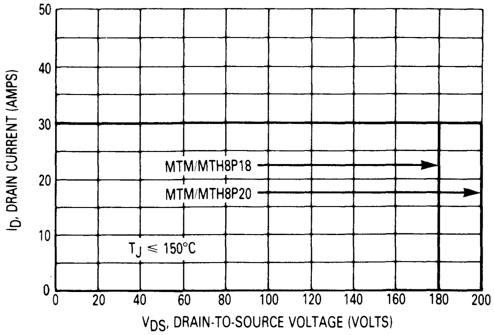


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

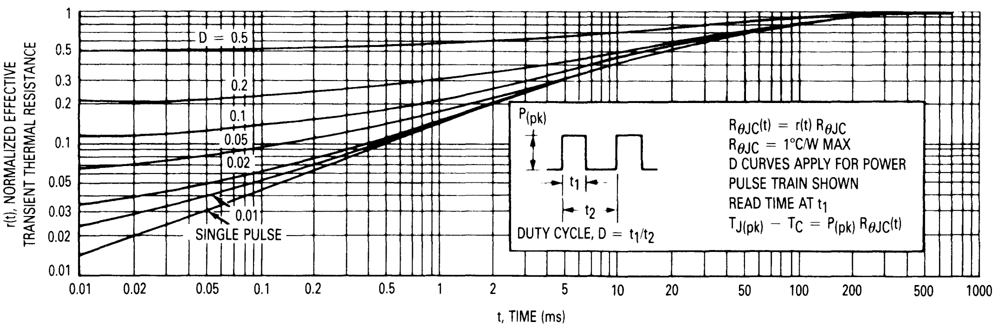


Figure 9. Thermal Response

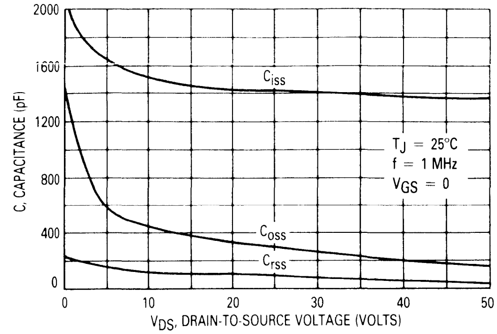


Figure 10. Capacitance Variation

RESISTIVE SWITCHING

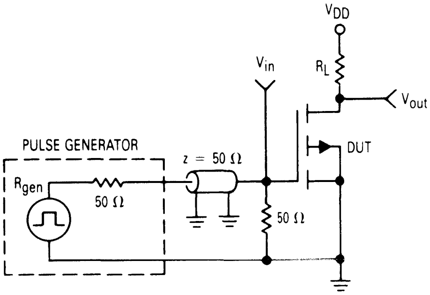


Figure 11. Switching Test Circuit

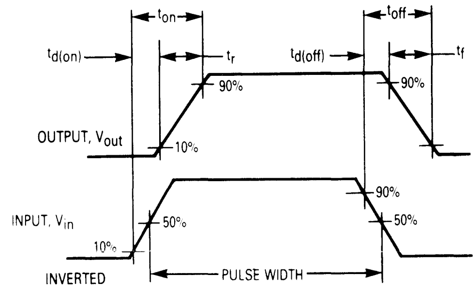
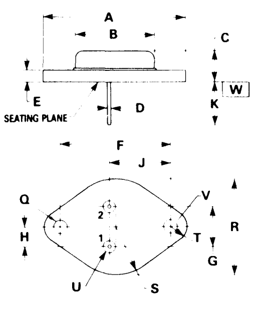


Figure 12. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-04
TO-204AA

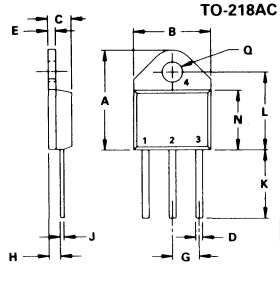


STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH13N45
MTH13N50

Designer's Data Sheet

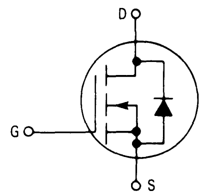
Power Field Effect Transistor

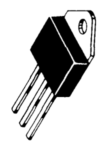
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
13 AMPERES
$r_{DS(on)}$ = 0.4 OHM
450 and 500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 340-02
TO-218AC

3

MAXIMUM RATINGS

Rating	Symbol	MTH 13N45	MTH 13N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	13 60		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH13N45 MTH13N50	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7 Adc)		$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 13 Adc) (I_D = 7 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	5.2 5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 7 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	450	
Fall Time		t_f	—	180	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	110 (Typ)	160	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

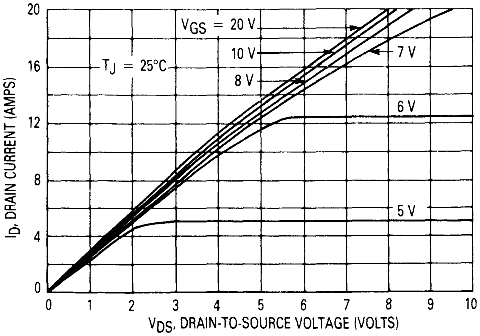

Figure 1. On-Region Characteristics

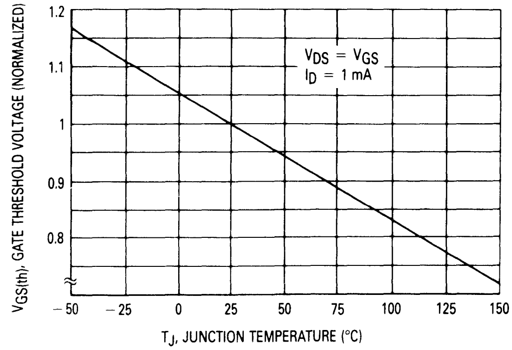

Figure 2. Gate-Threshold Voltage Variation With Temperature

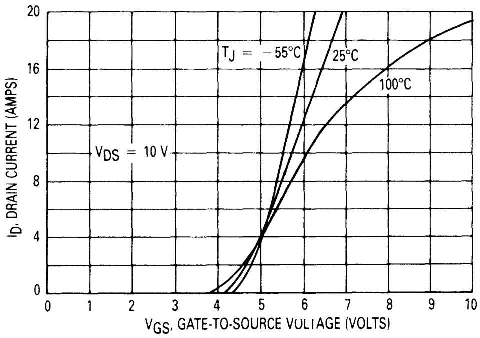

Figure 3. Transfer Characteristics

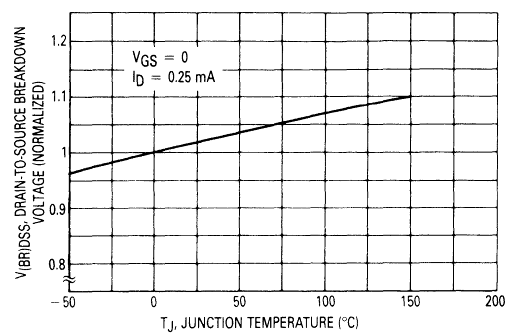

Figure 4. Breakdown Voltage Variation With Temperature

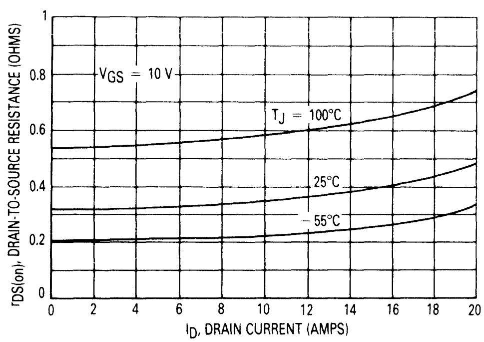

Figure 5. On-Resistance versus Drain Current

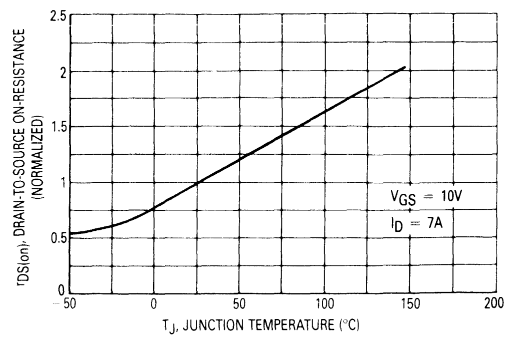

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

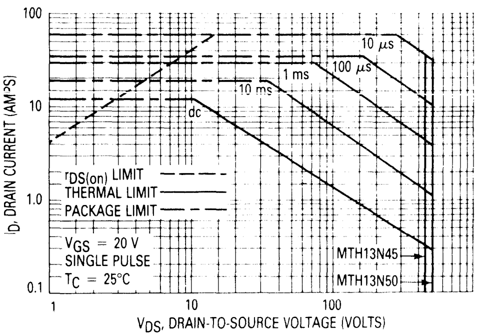

Figure 7. Maximum Rated Forward Biased Safe Operating Area

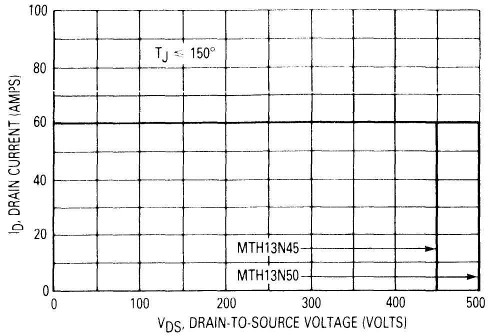

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

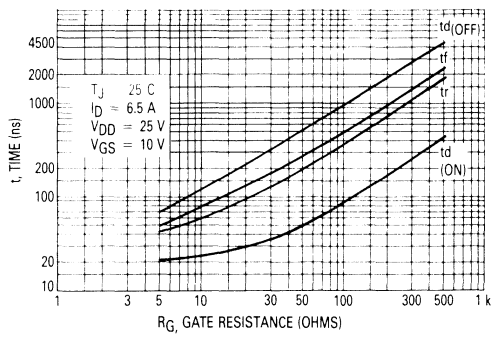

Figure 9. Resistive Switching Time Variation With Gate Resistance

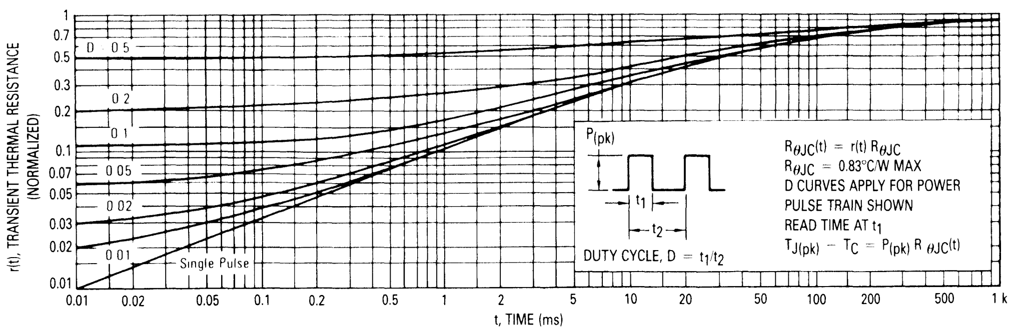

Figure 10. Thermal Response

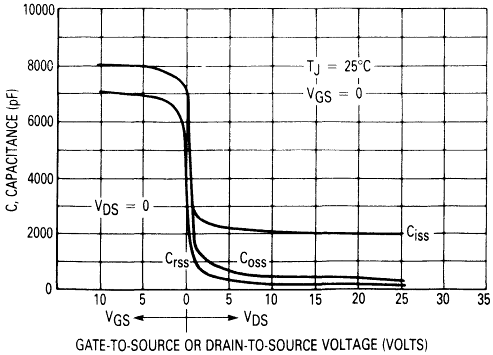

Figure 11. Capacitance Variation

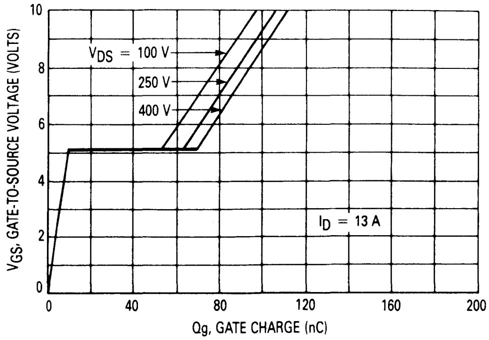

Figure 12. Gate Charge versus Gate-to-Source Voltage

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RESISTIVE SWITCHING

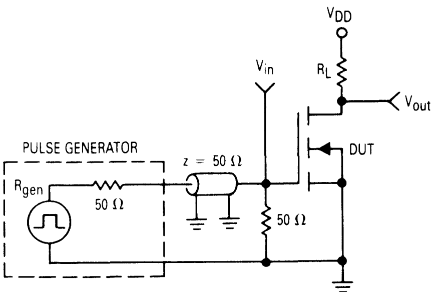


Figure 13. Switching Test Circuit

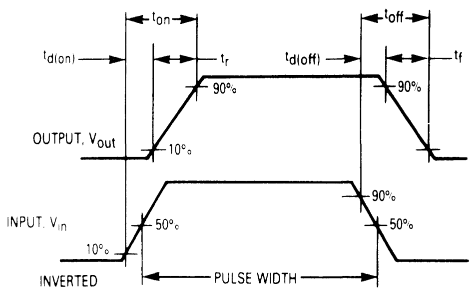
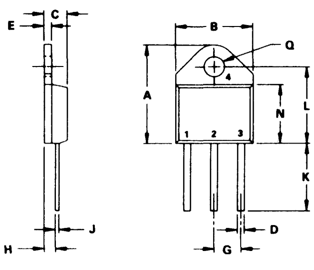


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 340-02
TO-218AC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH15N20
MTM15N20

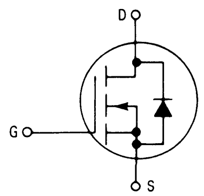
Designer's Data Sheet

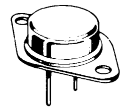
Power Field Effect Transistor

N-Channel Enhancement-Mode
Silicon Gate TMOS

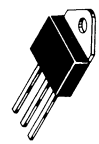
TMOS

TMOS POWER FETs
15 AMPERES
$r_{DS(on)}$ = 0.16 OHM
200 VOLTS





MTM15N20
CASE 197A-02
TO-204AE



MTH15N20
CASE 340-02
TO-218AC

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These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 15N20	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 80	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH15N20, MTM15N20	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.16	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3 2.4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	700	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	220	
Fall Time		t_f	—	250	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	60 (Typ)	75	nC
Gate-Source Charge		Q_{gs}	35 (Typ)	—	
Gate-Drain Charge		Q_{gd}	25 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	2.1	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

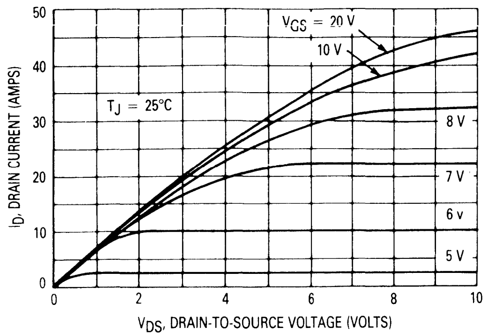

Figure 1. On-Region Characteristics

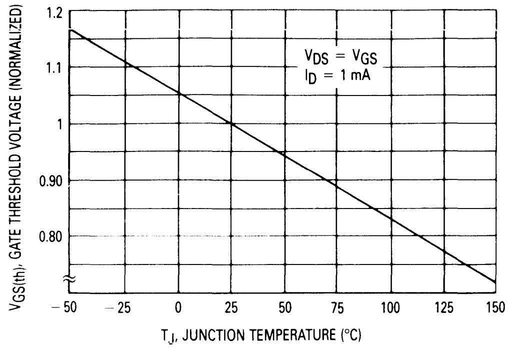

Figure 2. Gate-Threshold Voltage Variation With Temperature

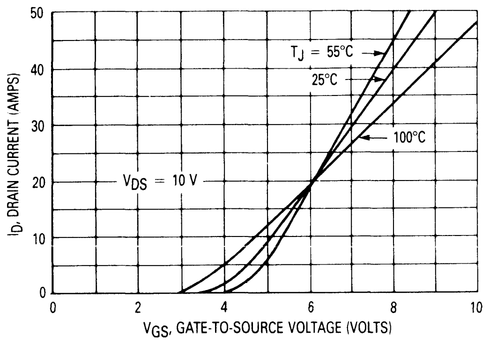

Figure 3. Transfer Characteristics

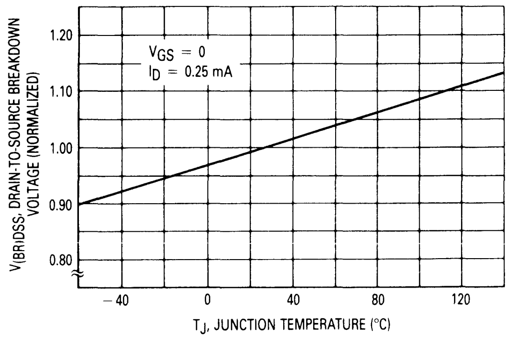

Figure 4. Breakdown Voltage Variation With Temperature

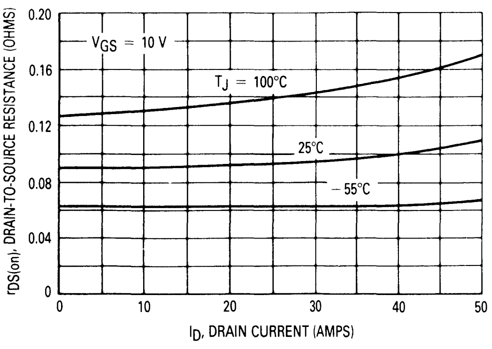

Figure 5. On-Resistance versus Drain Current

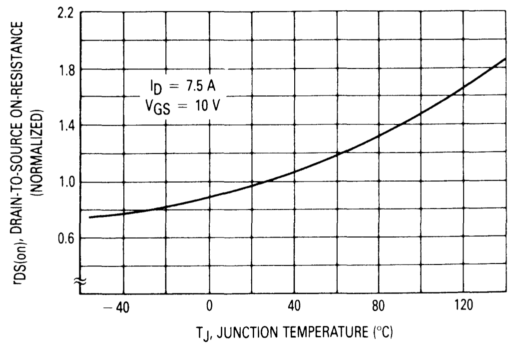

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

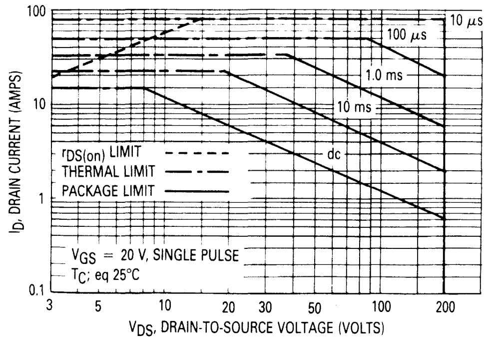

Figure 7. Maximum Rated Forward Biased Safe Operating Area

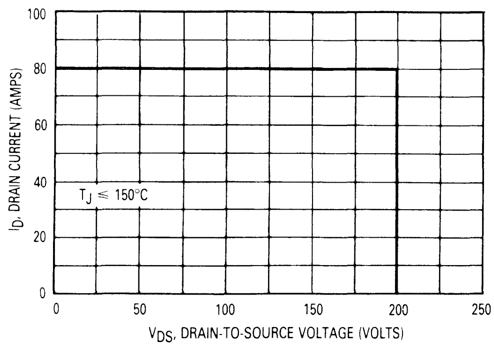

Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

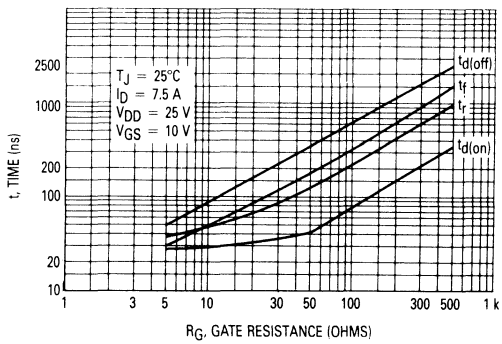


Figure 9. Resistive Switching Time Variation With Gate Resistance

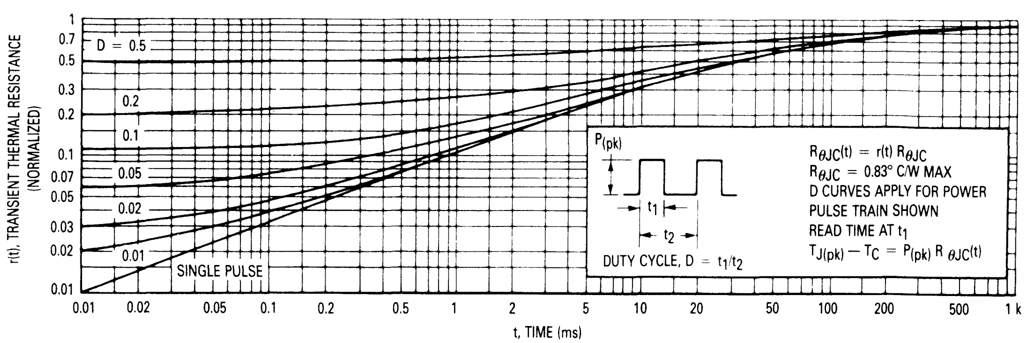


Figure 10. Thermal Response

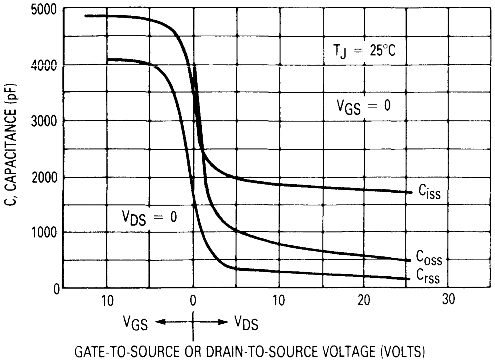


Figure 11. Capacitance Variation

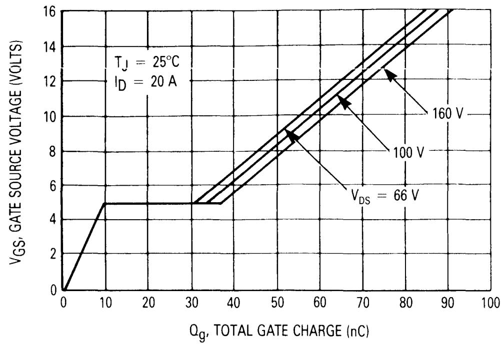


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

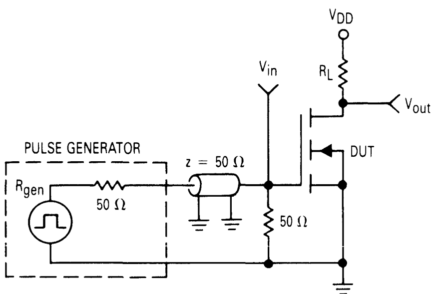


Figure 13. Switching Test Circuit

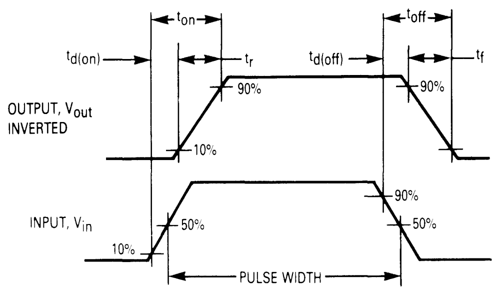
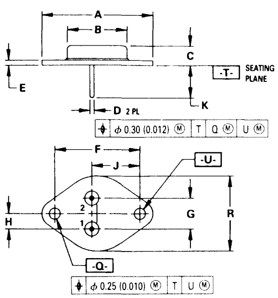


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

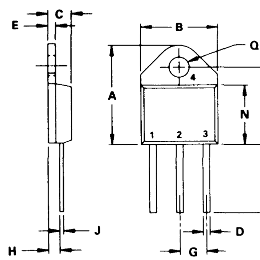


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

CASE 197A-02
TO-204AE



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

CASE 340-02
TO-218AC

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH15N35
MTH15N40

Designer's Data Sheet

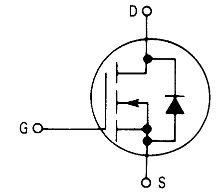
Power Field Effect Transistor

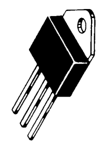
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
15 AMPERES
$r_{DS(on)}$ = 0.3 OHM
350 and 400 VOLTS





CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH 15N35	MTH 15N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 75		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	 MTH15N35 MTH15N40	$V_{(BR)DSS}$	 350 400	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 8 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc)		$V_{DS(on)}$	—	4.5	Vdc
(I_D = 8 Adc, T_J = 100°C)			—	3.5	
Forward Transconductance (V_{DS} = 10 V, I_D = 8 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	450	
Fall Time		t_f	—	180	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	110 (Typ)	160	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.3 (Typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

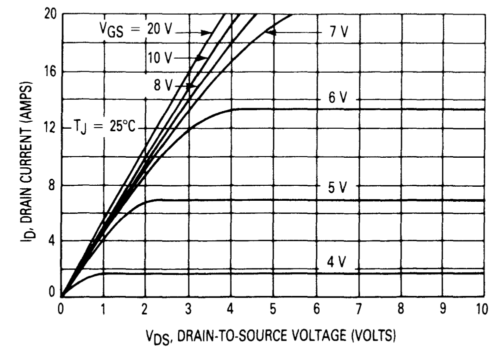


Figure 1. On-Region Characteristics

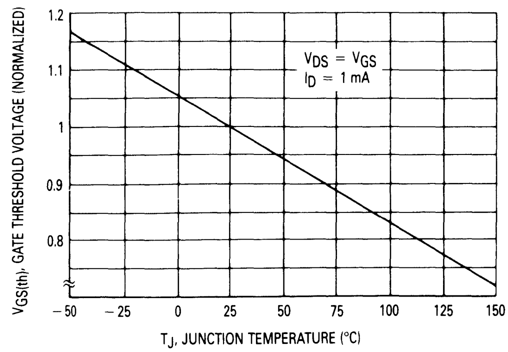


Figure 2. Gate-Threshold Voltage Variation With Temperature

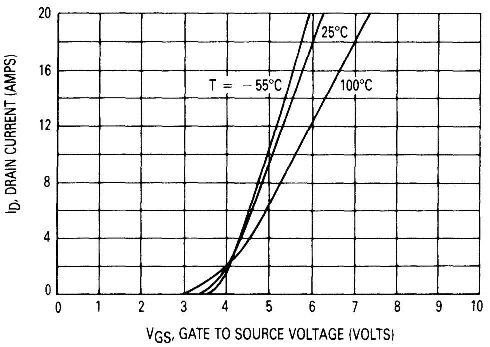


Figure 3. Transfer Characteristics

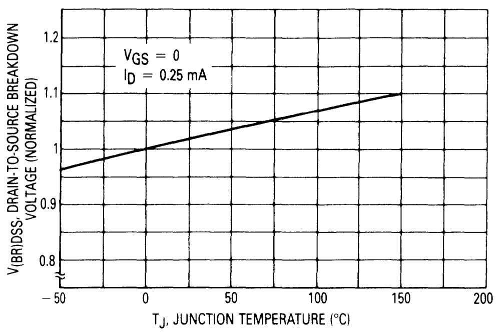


Figure 4. Breakdown Voltage Variation With Temperature

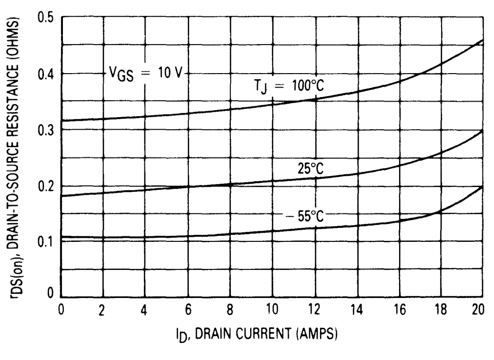


Figure 5. On-Resistance versus Drain Current

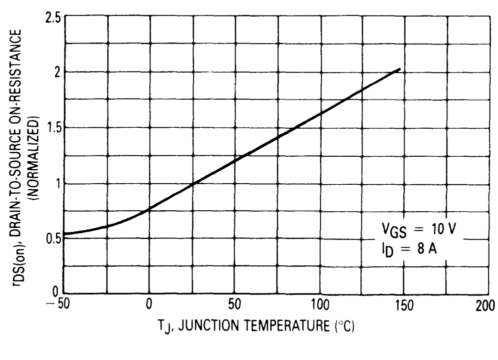


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

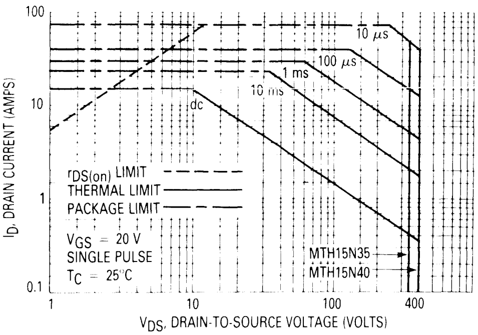


Figure 7. Maximum Rated Forward Biased Safe Operating Area

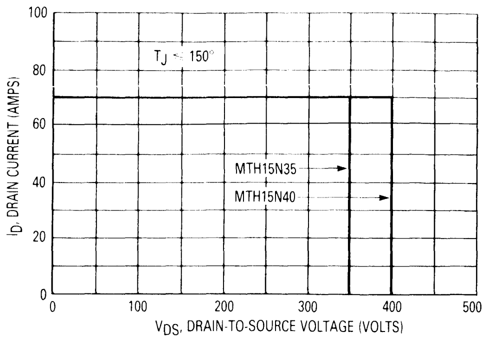


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

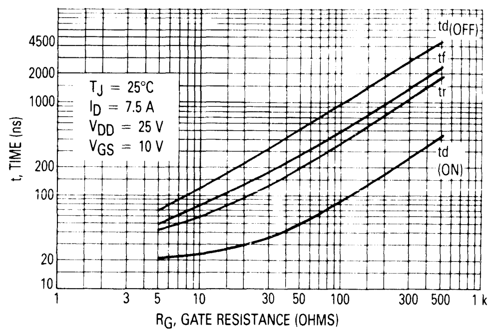


Figure 9. Resistive Switching Time Variation versus Gate Resistance

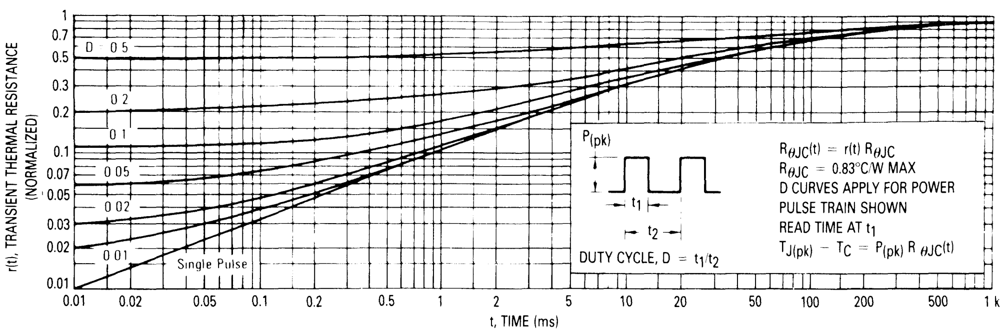


Figure 10. Thermal Response

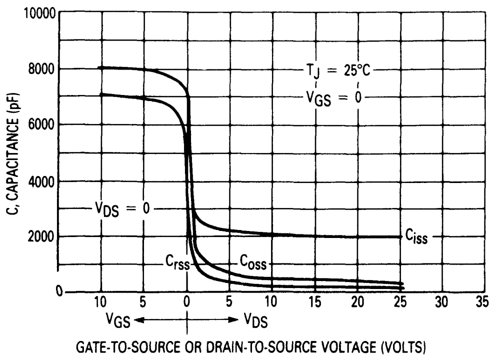


Figure 11. Capacitance Variation

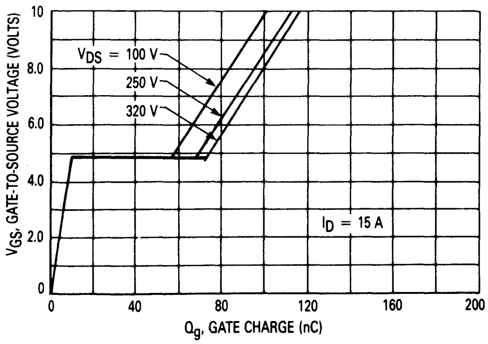


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

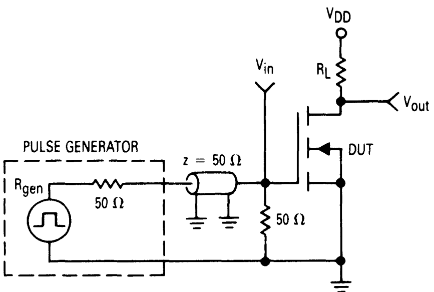


Figure 13. Switching Test Circuit

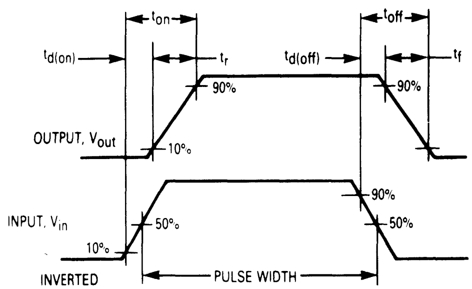
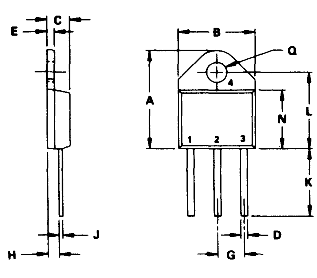


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH20N15
MTM20N15

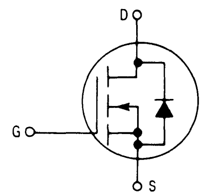
Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

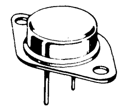
TMOS

TMOS POWER FETs
20 AMPERES
$r_{DS(on)}$ = 0.12 OHM
150 VOLTS

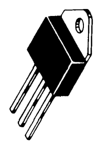


These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MTM20N15
CASE 197A-02
TO-204AE



MTH20N15
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 20N15	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	20 100	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH20N15, MTM20N15	$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.12	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc)		$V_{DS(on)}$	—	3	Vdc
(I_D = 10 Adc, T_J = 100°C)			—	2.4	
Forward Transconductance (V_{DS} = 10 V, I_D = 10 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	700	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	220	
Fall Time		t_f	—	250	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	60 (Typ)	75	nC
Gate-Source Charge		Q_{gs}	35 (Typ)	—	
Gate-Drain Charge		Q_{gd}	25 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	2.1	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

3

TYPICAL ELECTRICAL CHARACTERISTICS

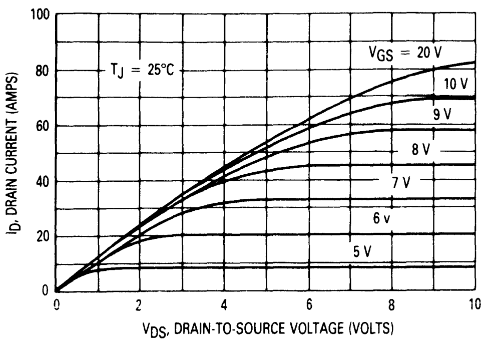


Figure 1. On-Region Characteristics

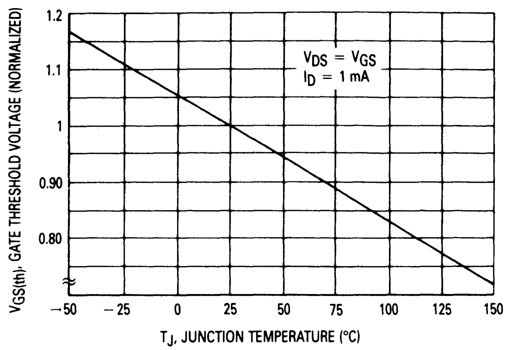


Figure 2. Gate-Threshold Voltage Variation With Temperature

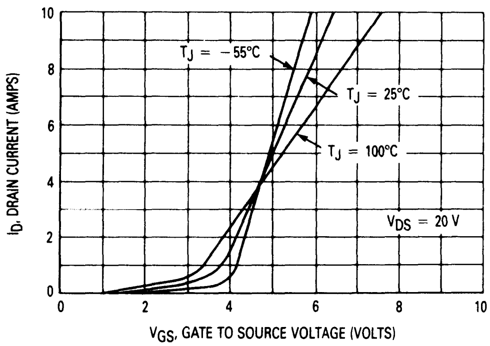


Figure 3. Transfer Characteristics

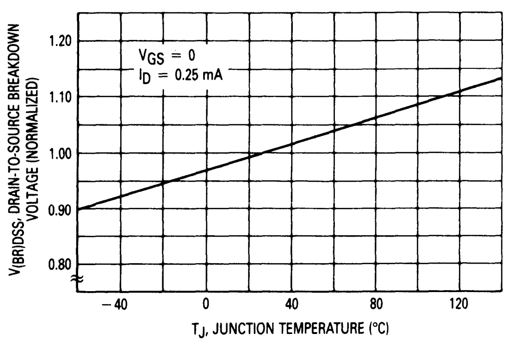


Figure 4. Breakdown Voltage Variation With Temperature

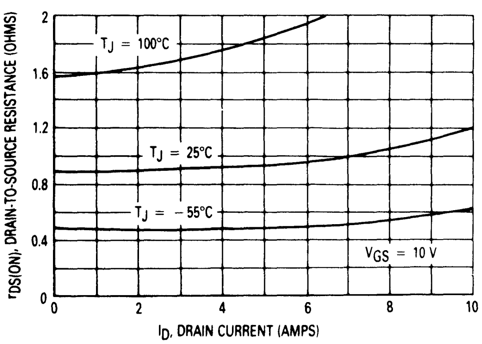


Figure 5. On-Resistance versus Drain Current

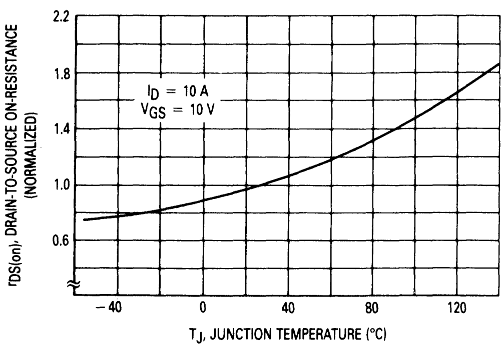


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

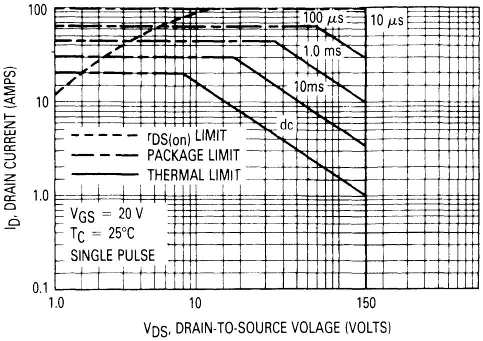


Figure 7. Maximum Rated Forward Biased Safe Operating Area

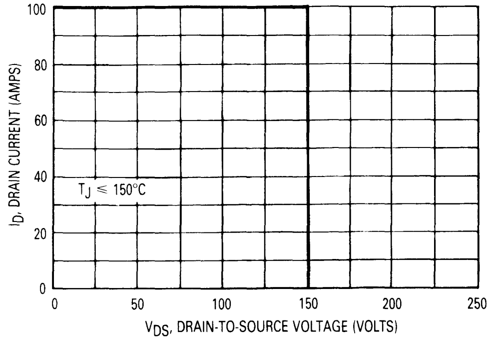


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

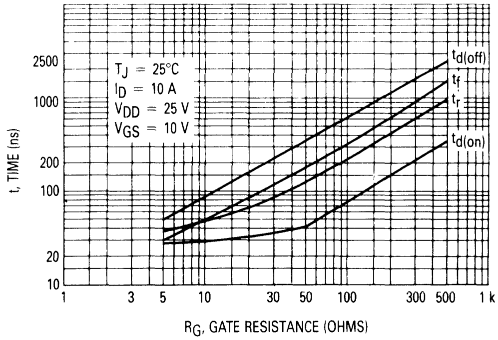


Figure 9. Resistive Switching Time Variation versus Gate Resistance

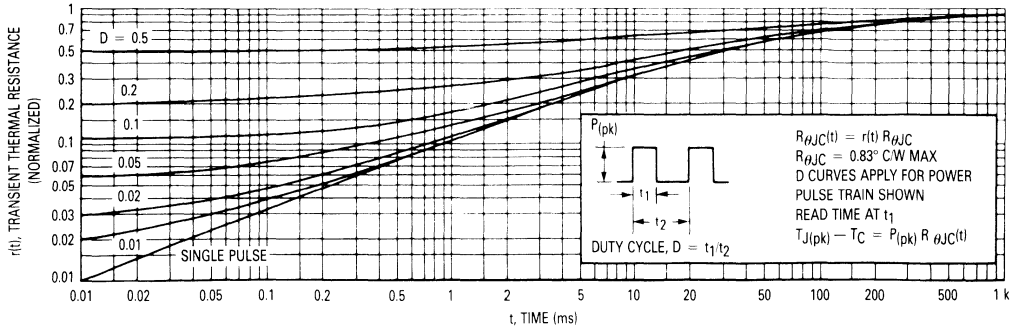


Figure 10. Thermal Response

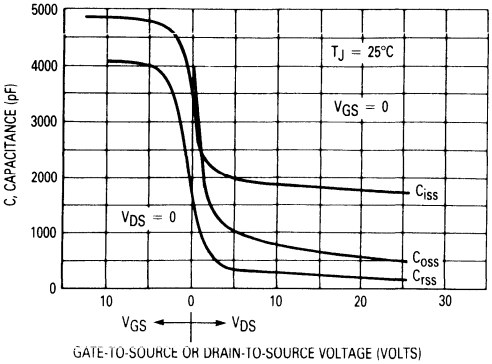


Figure 11. Capacitance Variation

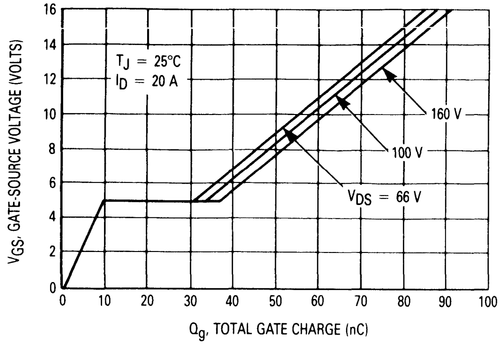


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

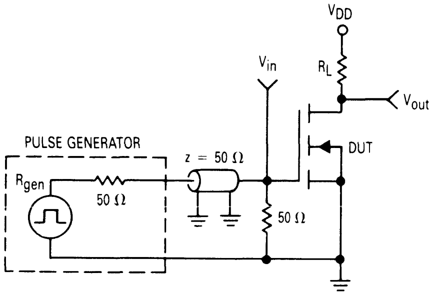


Figure 13. Switching Test Circuit

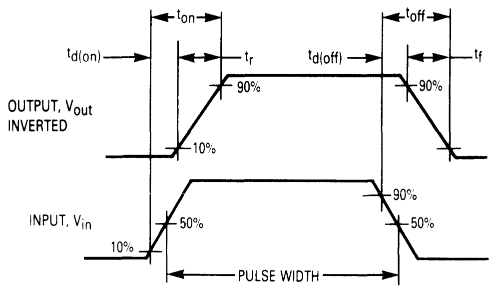
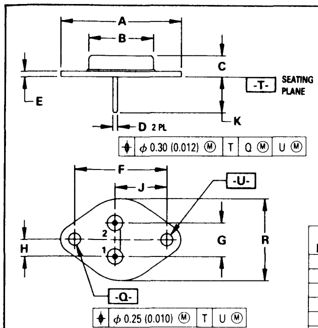


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



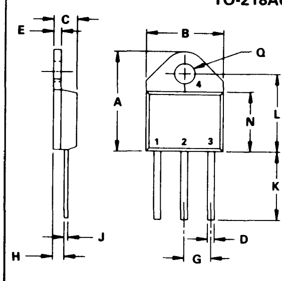
CASE 197A-02
TO-204AE

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH20P08
MTH20P10
MTM20P08
MTM20P10

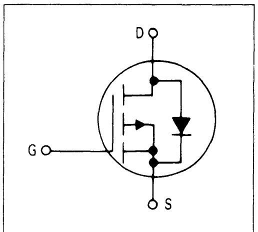
Designer's Data Sheet
Power Field Effect Transistor
P-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

TMOS POWER FETs
20 AMPERES
$r_{DS(on)}$ = 0.15 OHM
80 and 100 VOLTS



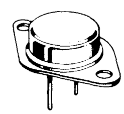
3

MAXIMUM RATINGS

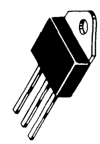
Rating	Symbol	MTM and MTH 20P08	MTM and MTH 20P10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 20 80		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTM20P08
MTM20P10
CASE 1-04
TO-204AA



MTH20P08
MTH20P10
CASE 340-02
TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH20P08, MTM20P08 MTH20P10, MTM20P10	$V_{(BR)DSS}$	 80 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)	$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 3.2 3	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 10 A)	g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	2000	pF
Output Capacitance	C_{oss}	—	950	
Reverse Transfer Capacitance	C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	45	ns
Rise Time	t_r	—	200	
Turn-Off Delay Time	$t_{d(off)}$	—	150	
Fall Time	t_f	—	150	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	52 (Typ)	75	nC
Gate-Source Charge	Q_{gs}	22 (Typ)	—	
Gate-Drain Charge	Q_{gd}	30 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.8 (Typ)	4	Vdc
Forward Turn-On Time	t_{on}	100 (Typ)	—	ns
Reverse Recovery Time	t_{rr}	350 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

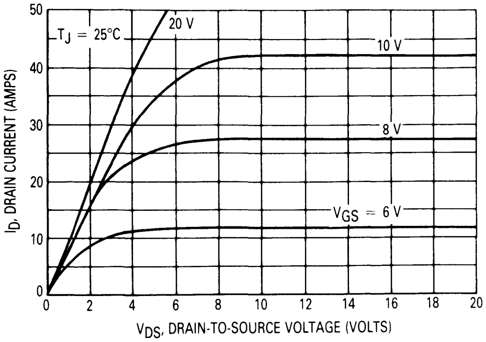


Figure 1. On-Region Characteristics

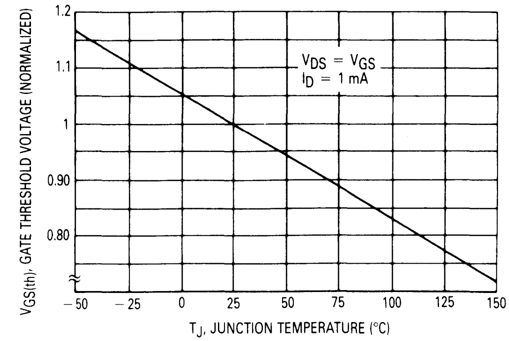


Figure 2. Gate-Threshold Voltage Variation With Temperature

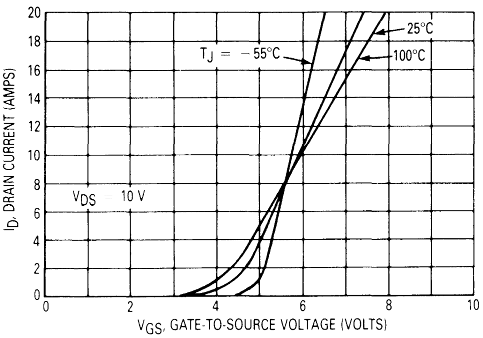


Figure 3. Transfer Characteristics

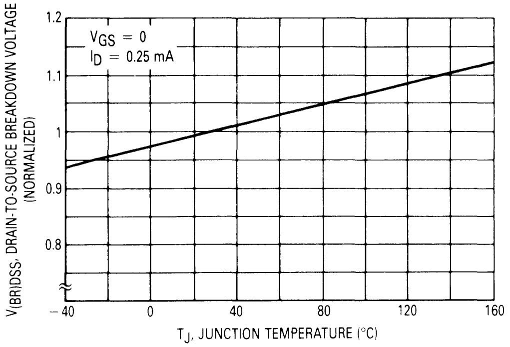


Figure 4. Breakdown Voltage Variation With Temperature

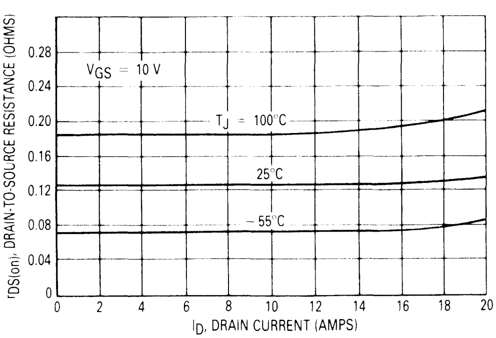


Figure 5. On-Resistance versus Drain Current

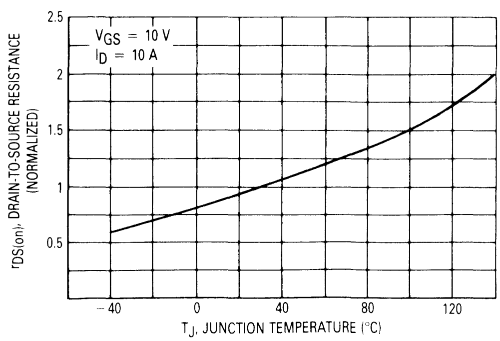


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

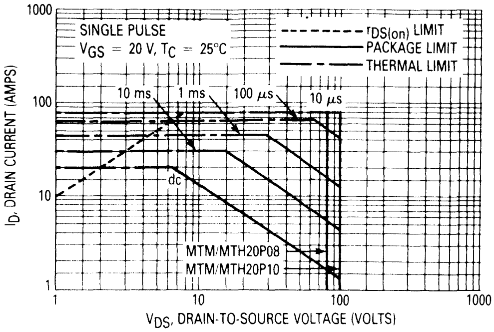


Figure 7. Maximum Rated Forward Biased Safe Operating Area

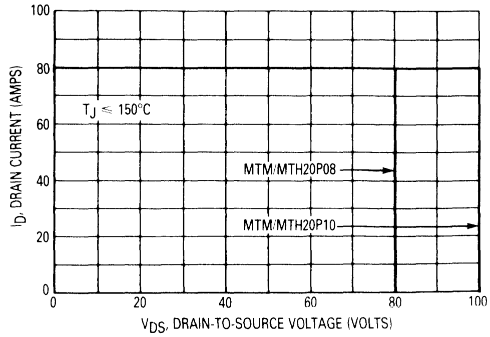


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

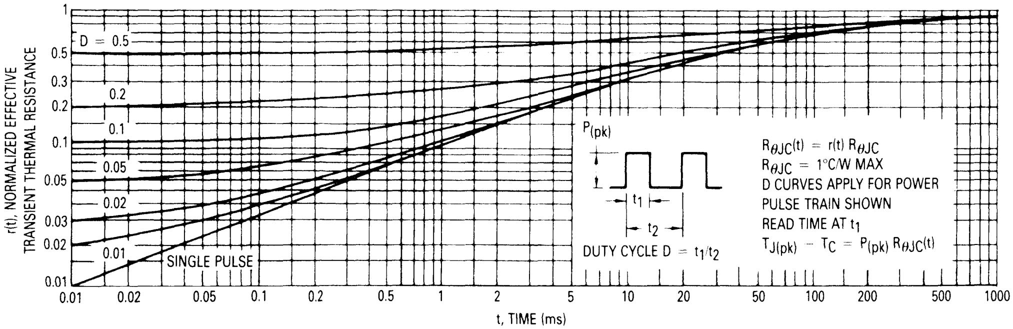


Figure 9. Thermal Response

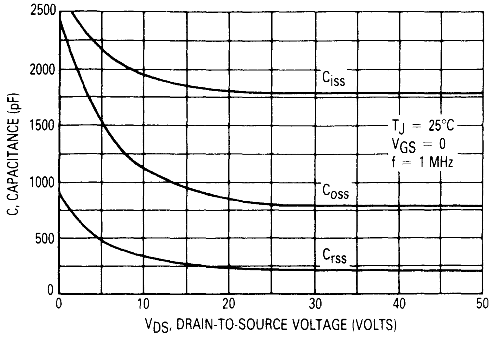


Figure 10. Capacitance Variation

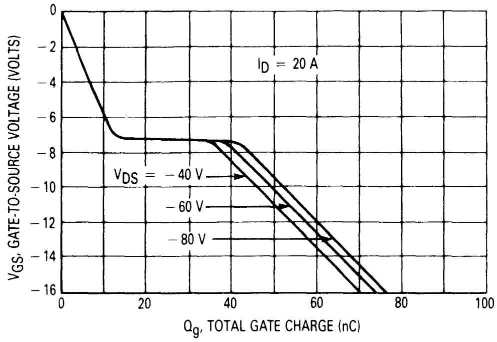


Figure 11. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

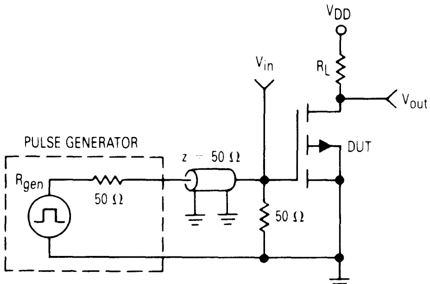


Figure 12. Switching Test Circuit

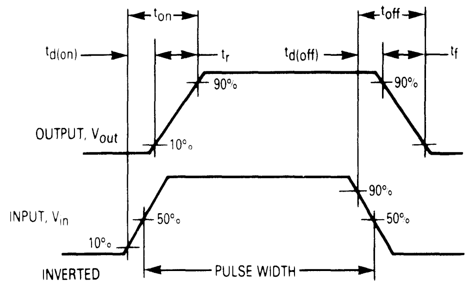
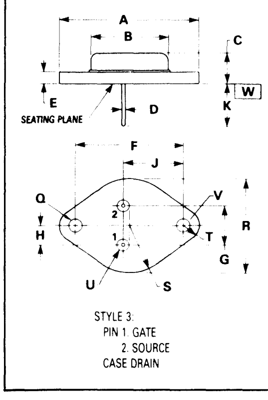


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

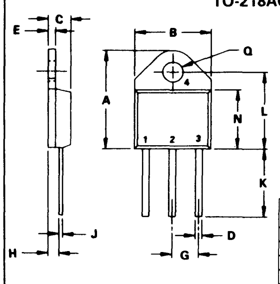
NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:

⌖	φ 0.25 (0.010) Ⓜ	W	V Ⓜ

3. POSITIONAL TOLERANCE FOR LEADS:

⌖	φ 0.30 (0.012) Ⓜ	W	V Ⓜ	Q Ⓜ

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

3

MTH25N08
MTH25N10
MTM25N10

Designer's Data Sheet

Power Field Effect Transistor

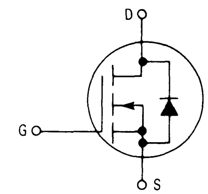
N-Channel Enhancement-Mode Silicon Gate TMOS

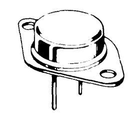
TMOS POWER FETs
AMPERES
$r_{DS(on)}$ = 0.075 OHM
80 and 100 VOLTS

3

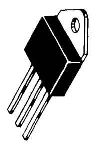
These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM25N10
CASE 197A-02
TO-204AE



MTH25N08
MTH25N10
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH25N08	MTH25N10 MTM25N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50$ μs)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 105		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS — (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH25N08 MTH25N10,MTH25N10	$V_{(BR)DSS}$	 80 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$r_{DS(on)}$	—	0.075	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 25 Adc)		$V_{DS(on)}$	—	2.25	Vdc
(I_D = 12.5 Adc, T_J = 100°C)			—	1.8	
Forward Transconductance (V_{DS} = 10 V, I_D = 12.5 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	29 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	23 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die)		L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

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TYPICAL ELECTRICAL CHARACTERISTICS

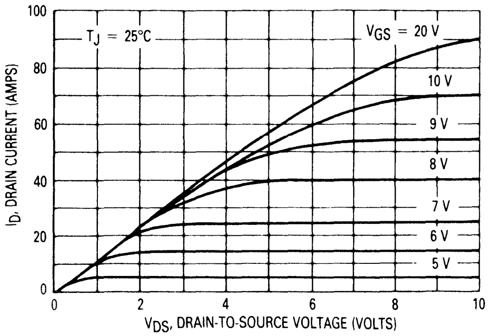


Figure 1. On-Region Characteristics

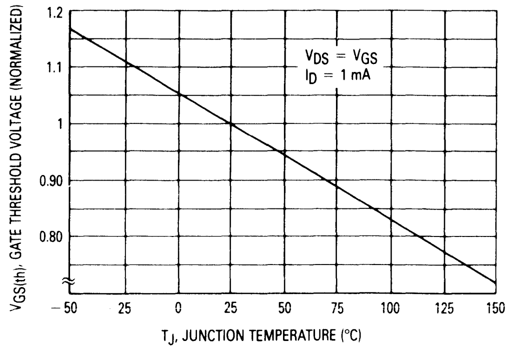


Figure 2. Gate-Threshold Voltage Variation With Temperature

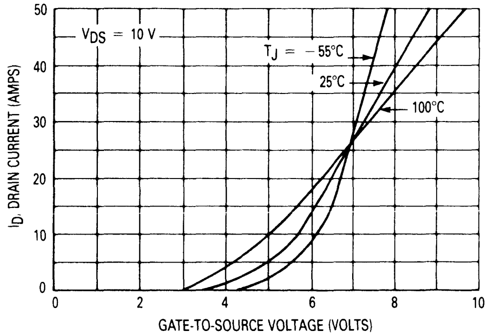


Figure 3. Transfer Characteristics

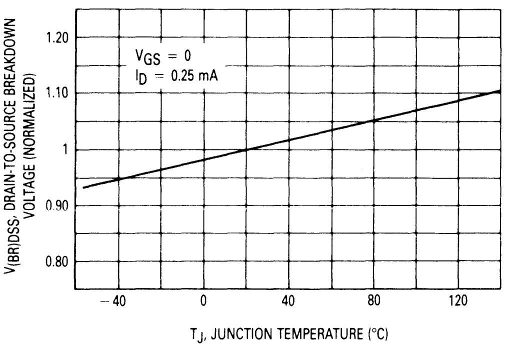


Figure 4. Breakdown Voltage Variation With Temperature

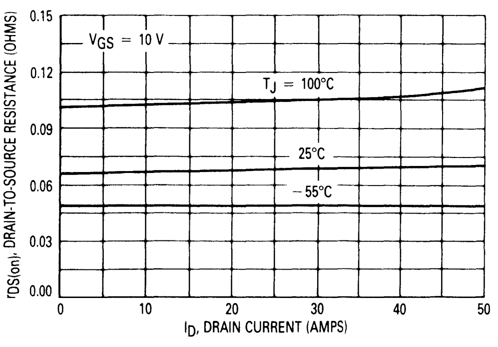


Figure 5. On-Resistance versus Drain Current

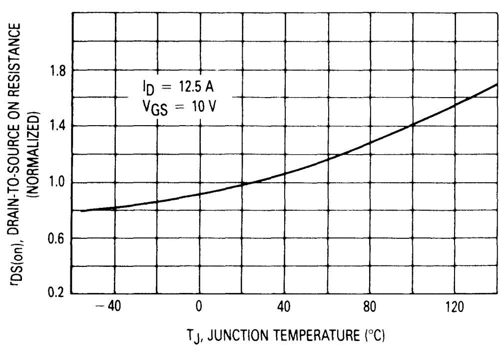


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

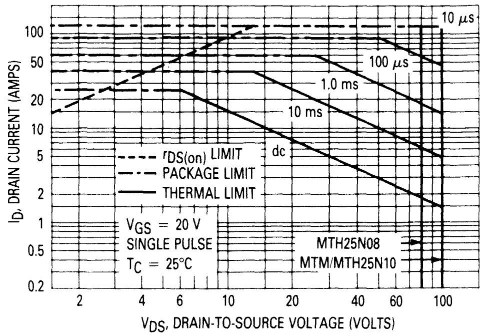


Figure 7. Maximum Rated Forward Biased Safe Operating Area

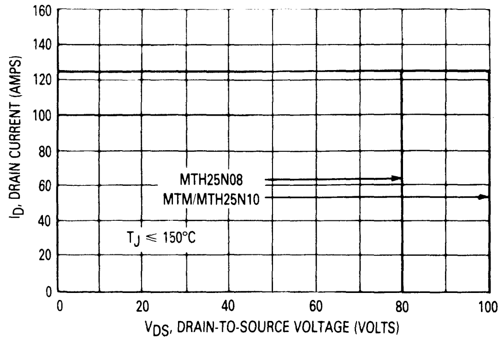


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

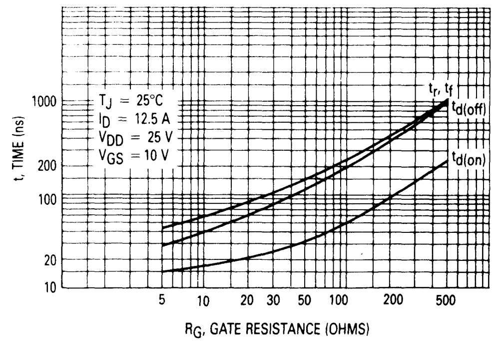


Figure 9. Resistive Switching Time Variation versus Gate Resistance

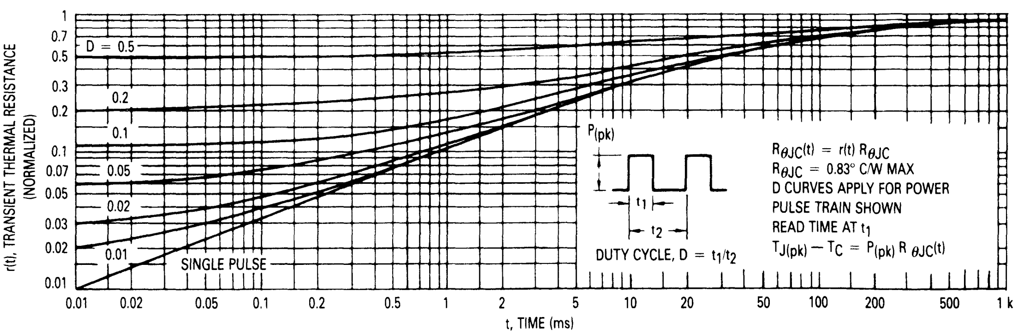


Figure 10. Thermal Response

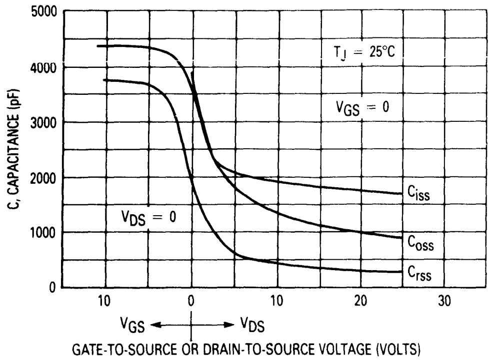


Figure 11. Capacitance Variation

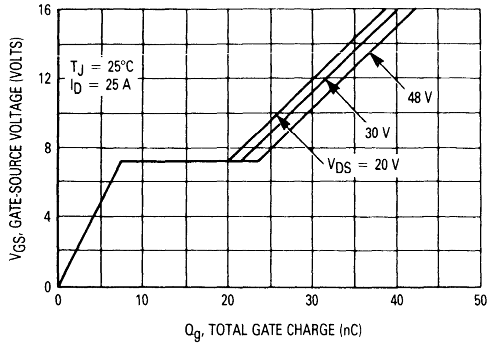


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

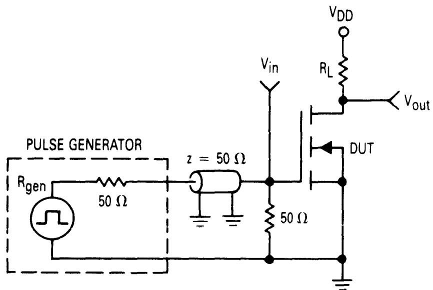


Figure 13. Switching Test Circuit

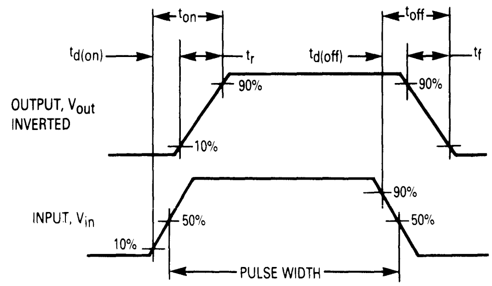
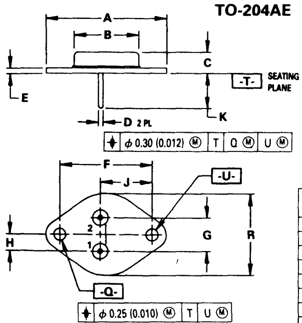


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 197A-02
TO-204AE

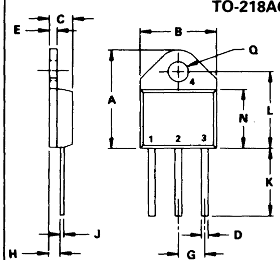


STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MTH25P05
MTH25P06
MTM25P05
MTM25P06

Designer's Data Sheet

Power Field Effect Transistor

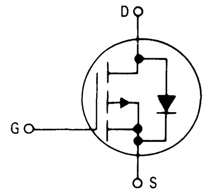
P-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
25 AMPERES
$r_{DS(on)}$ = 0.14 OHM
50 and 60 VOLTS

3

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

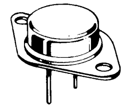


MAXIMUM RATINGS

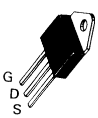
Rating	Symbol	MTM and MTH 25P05	MTM and MTH 25P06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 25 100		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTM25P05
MTM25P06
CASE 1-04
TO-204AA



MTH25P05
MTH25P06
CASE 340-02
TO-218AC

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTH25P05, MTM25P05 MTH25P06, MTM25P06	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$r_{DS(on)}$	—	0.14	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 25 Adc) (I_D = 12.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3.5 2.6	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 12.5 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	950	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	180	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	50 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	25 (Typ)	—	
Gate-Drain Charge		Q_{gd}	33 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	3.8 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	100 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	275 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

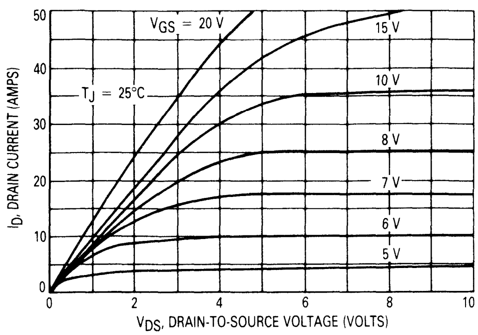

Figure 1. On-Region Characteristics

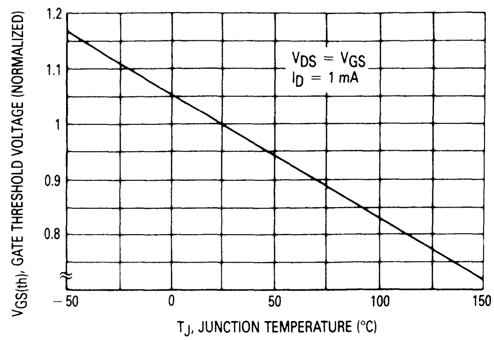

Figure 2. Gate-Threshold Voltage Variation With Temperature

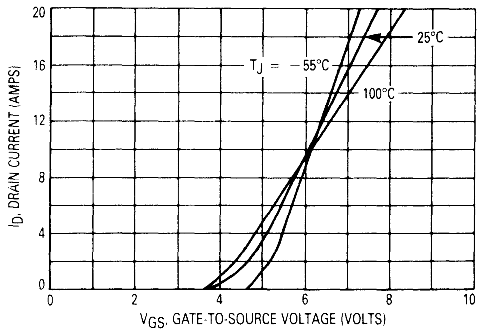

Figure 3. Transfer Characteristics

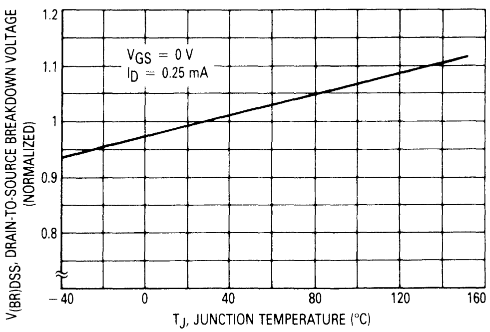

Figure 4. Breakdown Voltage Variation With Temperature

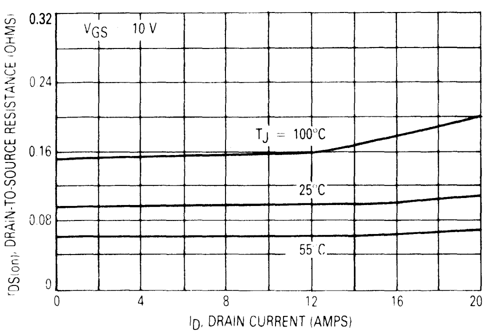

Figure 5. On-Resistance versus Drain Current

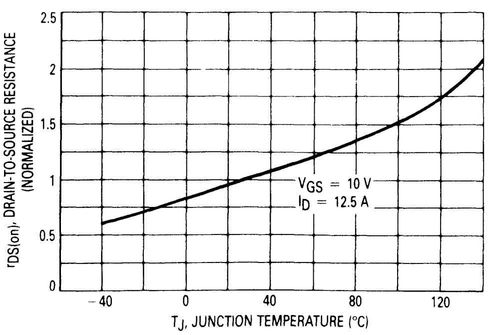

Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

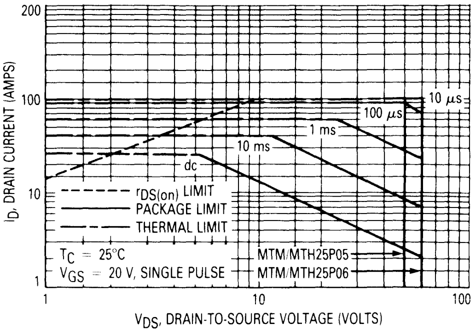


Figure 7. Maximum Rated Forward Biased Safe Operating Area

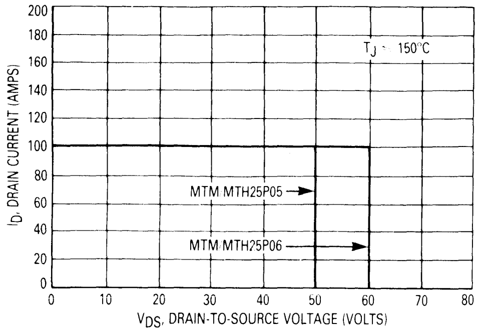


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

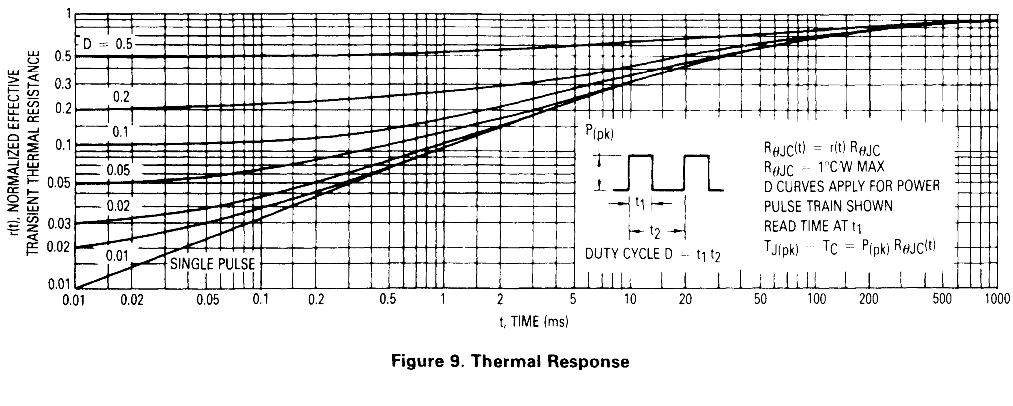


Figure 9. Thermal Response

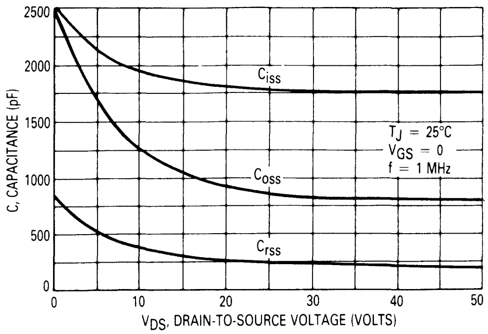


Figure 10. Capacitance Variation

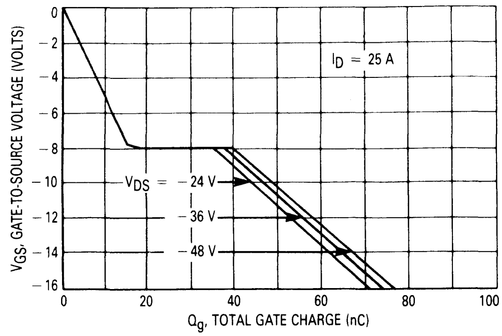


Figure 11. Gate Charge Variation

RESISTIVE SWITCHING

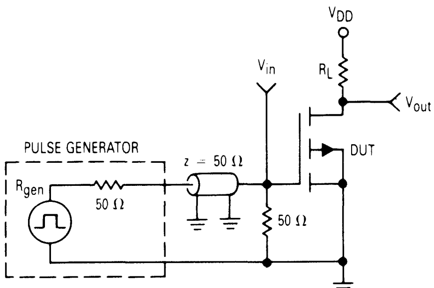


Figure 12. Switching Test Circuit

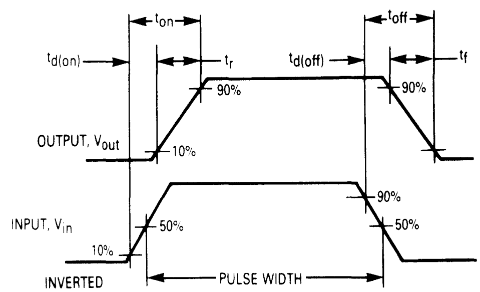
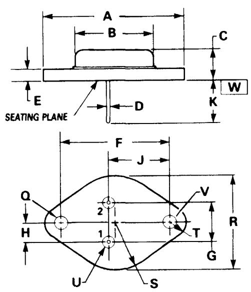


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

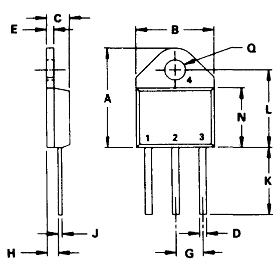
CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   | ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
   | ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

3

MTH30N20

Designer's Data Sheet

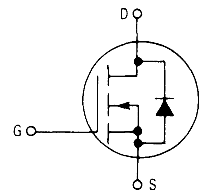
Power Field Effect Transistor

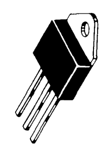
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
30 AMPERES
$r_{DS(on)}$ = 0.08 OHM
200 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 90	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH30N20	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$r_{DS(on)}$	—	0.08	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 30 Adc)		$V_{DS(on)}$	—	2.85	Vdc
(I_D = 15 Adc, T_J = 100°C)			—	1.92	
Forward Transconductance (V_{DS} = 10 V, I_D = 15 A)		g_{FS}	10	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	5500	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	85 (Typ)	95	nC
Gate-Source Charge		Q_{gs}	45 (Typ)	—	
Gate-Drain Charge		Q_{gd}	40 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			4 (Typ)	—	
(Measured from the drain lead 0.25" from package to center of die)			5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

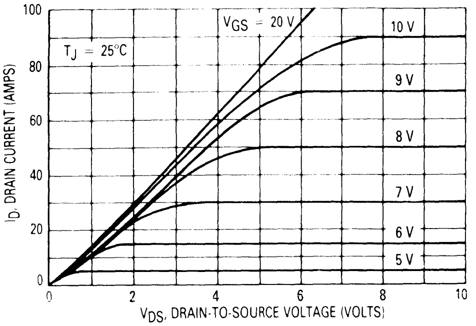


Figure 1. On-Region Characteristics

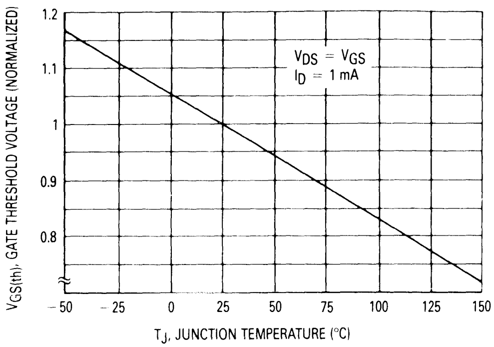


Figure 2. Gate-Threshold Voltage Variation With Temperature

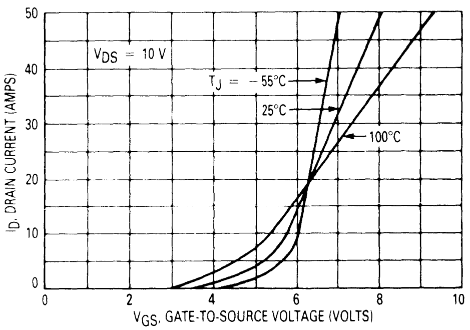


Figure 3. Transfer Characteristics

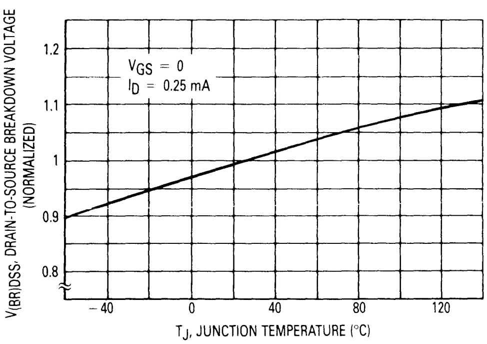


Figure 4. Breakdown Voltage Variation With Temperature

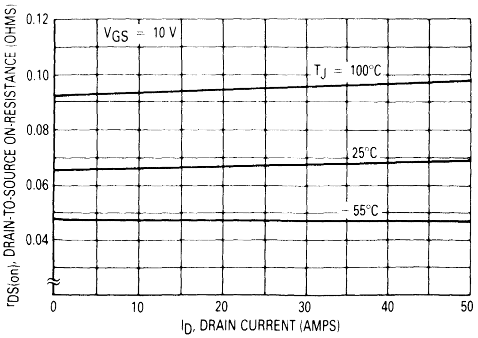


Figure 5. On-Resistance versus Drain Current

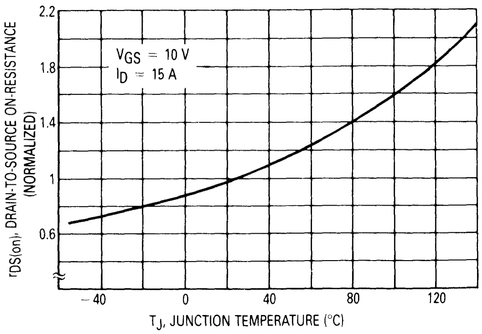


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

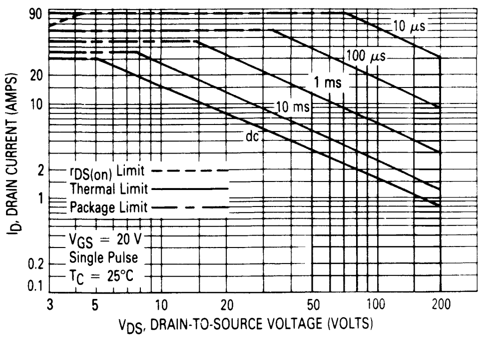


Figure 7. Maximum Rated Forward Biased Safe Operating Area

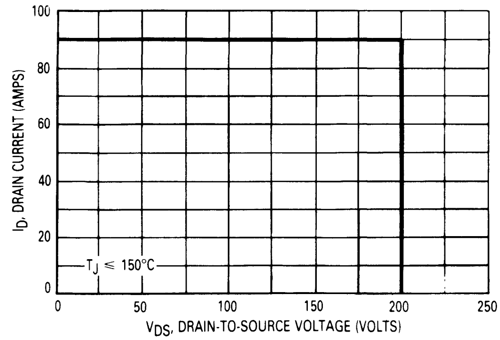


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

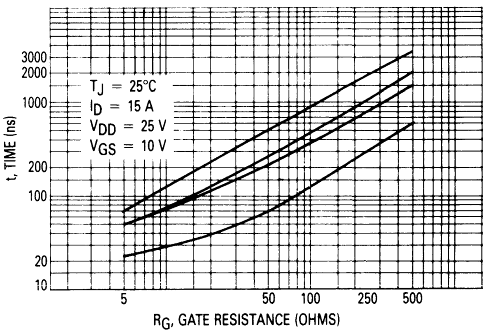


Figure 9. Resistive Switching Time Variation versus Gate Resistance

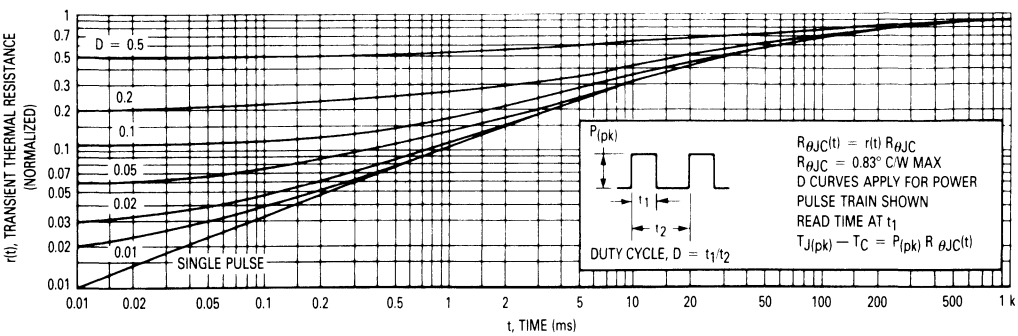


Figure 10. Thermal Response

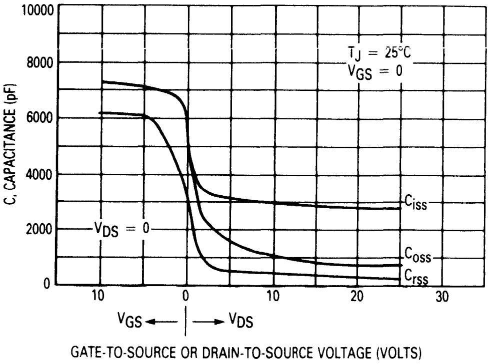


Figure 11. Capacitance Variation

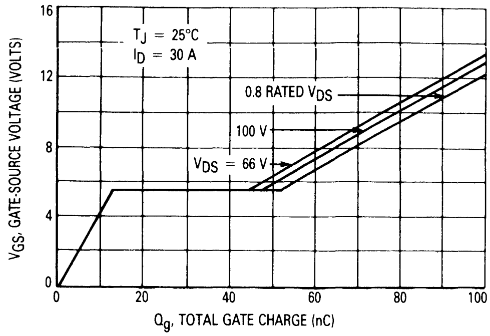


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

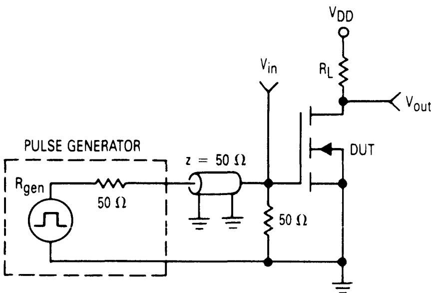


Figure 13. Switching Test Circuit

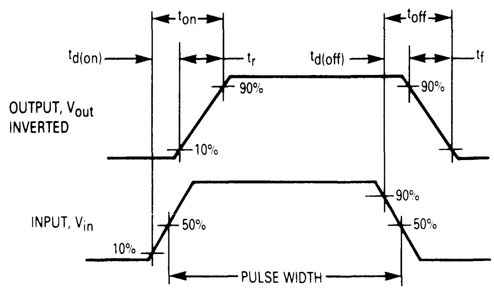
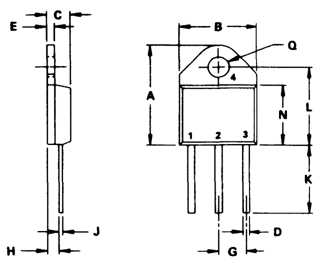


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH30N25

Designer's Data Sheet

Power Field Effect Transistor

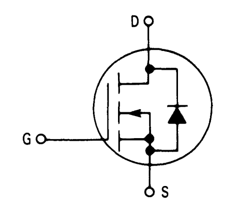
N-Channel Enhancement-Mode Silicon Gate TMOS

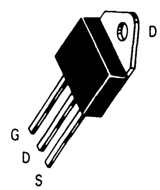
TMOS POWER FET
30 AMPERES
$r_{DS(on)}$ = 0.14 OHM
250 VOLTS

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Electrically Similar to IRFP254

TMOS™





CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 100	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DSS} = 250 V, V_{GS} = 0) (T_J = 125°C)	I_{DSS}	 — —	 10 500	μA

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit Curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 250 μA, V_{DS} = V_{GS}) (T_J = 125°C)		$V_{GS(th)}$	2 1.4	4 3.4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$r_{DS(on)}$	—	0.14	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 30 Adc) (I_D = 15 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	5.1 3.9	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 15 A)		g_{FS}	11	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0 f = 1 MHz)	C_{iss}	3200 (Typ)	—	pF
Output Capacitance		C_{oss}	515 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	90 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 1 and 2 R_{GS} = 5.6 Ω	$t_{d(on)}$	30 (Typ)	—	ns
Rise Time		t_r	55 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	65 (Typ)	—	
Fall Time		t_f	38 (Typ)	—	
TOTAL GATE CHARGE					
Total Gate Charge	V_{DS} = 200 V I_D = 30 A V_{GS} = 10 V	Q_g	80 (Typ)	130	nC
Gate-Source Charge		Q_{gs}	15 (Typ)	—	
Gate-Drain Charge		Q_{gd}	35 (Typ)	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	I_S = 30 A, V_{GS} = 0	V_{SD}	—	1.8	Vdc
Forward Turn-On Time	I_S = 30 A, V_R = 30 V dI_S/dt = 100 A/μs	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	280 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

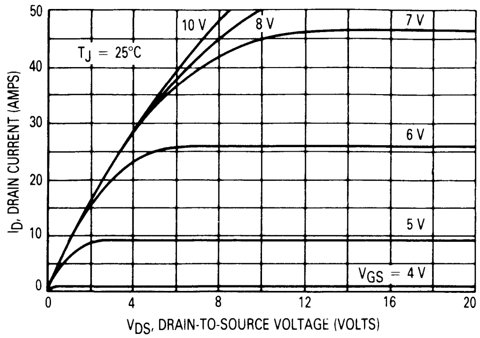


Figure 2. Gate Threshold Voltage Variation With Temperature

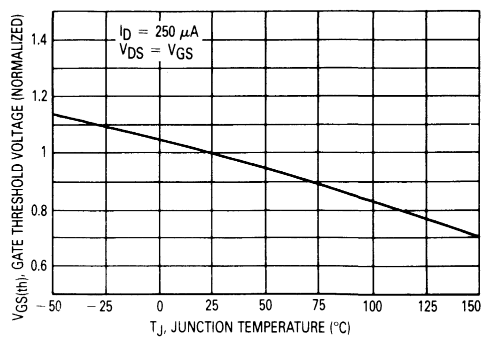


Figure 3. Transfer Characteristics

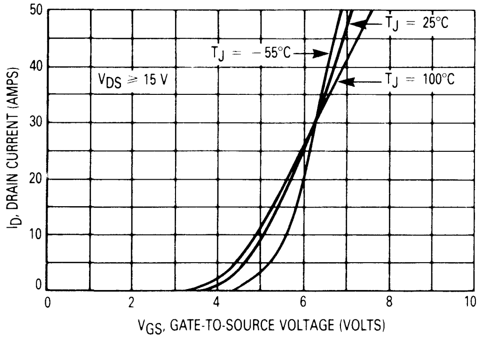


Figure 4. Breakdown Voltage Variation With Temperature

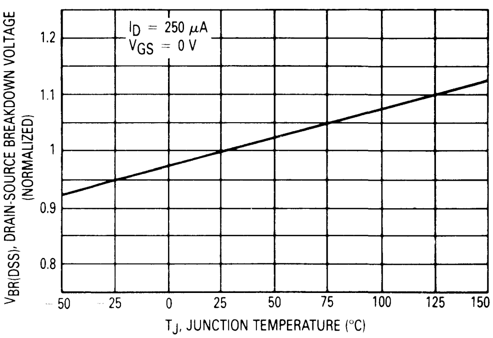


Figure 5. On-Resistance Variation With Drain Current

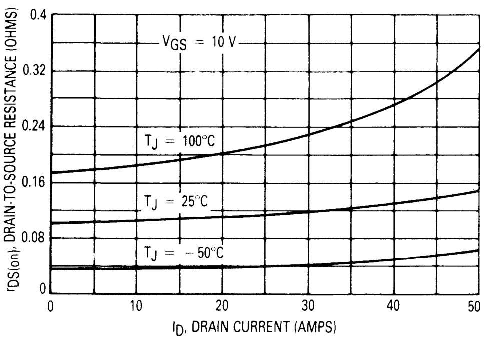
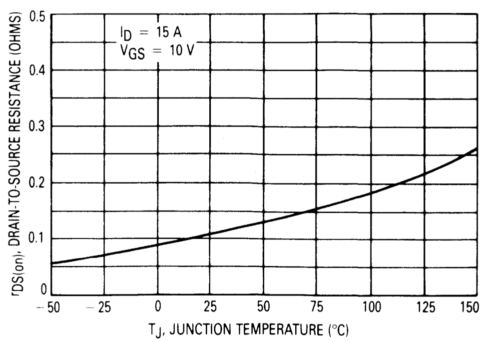


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

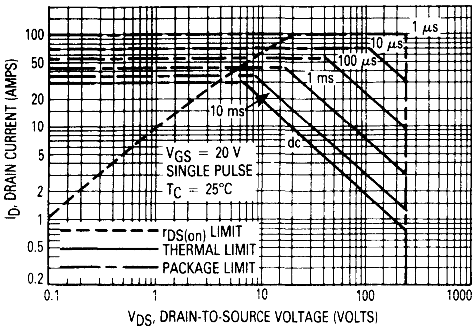
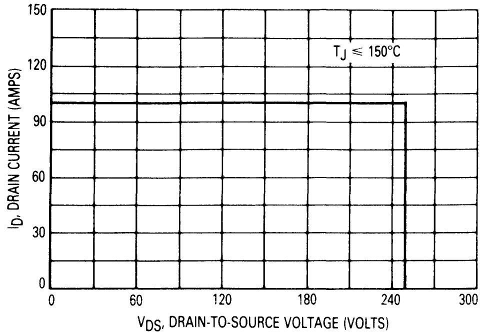


Figure 8. Maximum Rated Switching Safe Operating Area



3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response

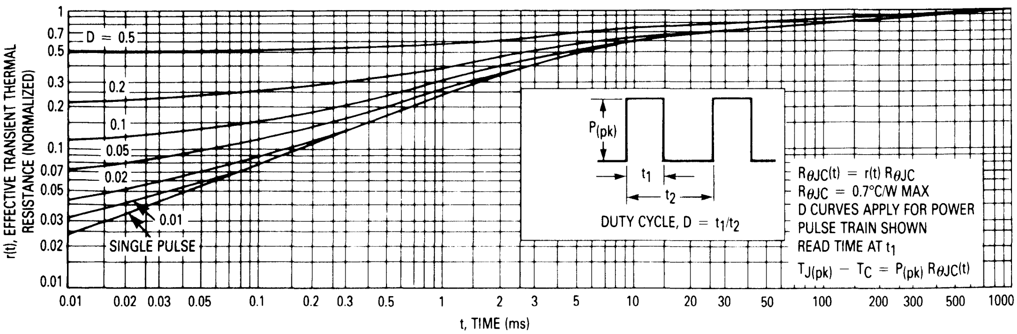


Figure 10. Capacitance Variation With Voltage

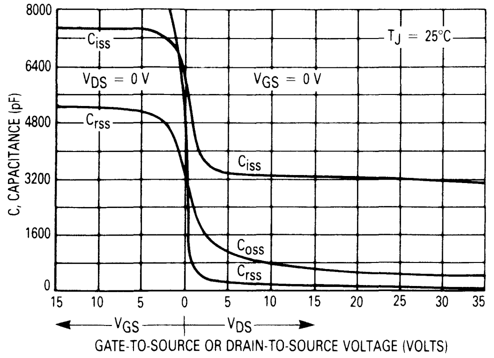


Figure 11. Gate Charge versus Gate-to-Source Voltage

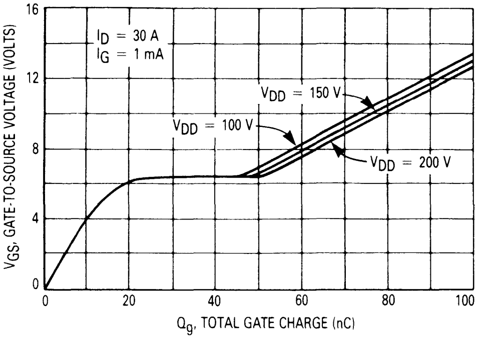
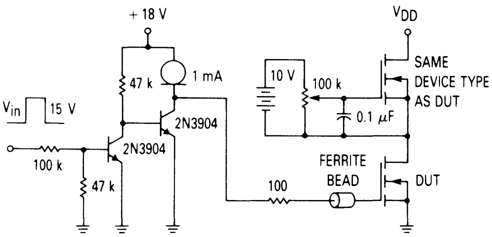


Figure 12. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 13. Switching Test Circuit

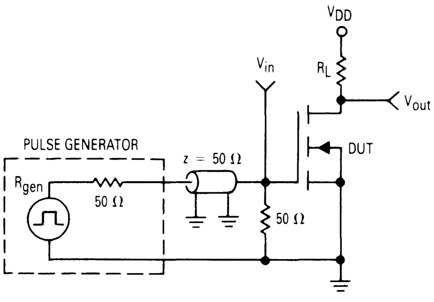
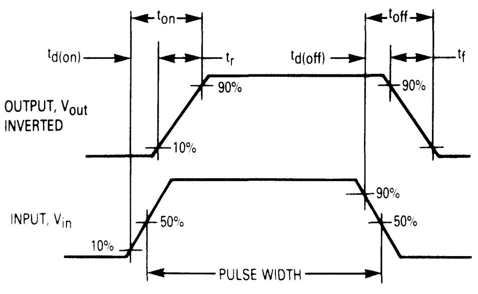
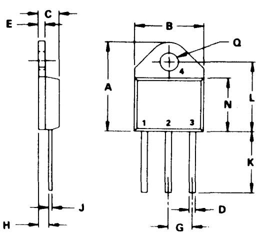


Figure 14. Switching Waveforms



OUTLINE DIMENSIONS



CASE 340-02
TO-218AC

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

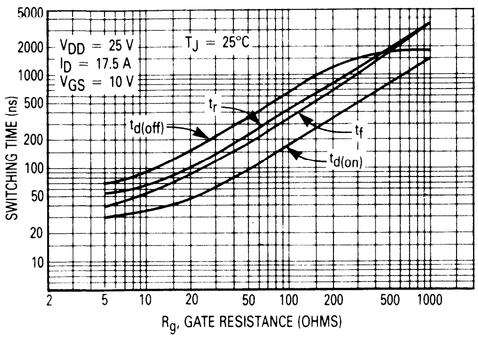


Figure 15. Switching Time versus Gate Resistance

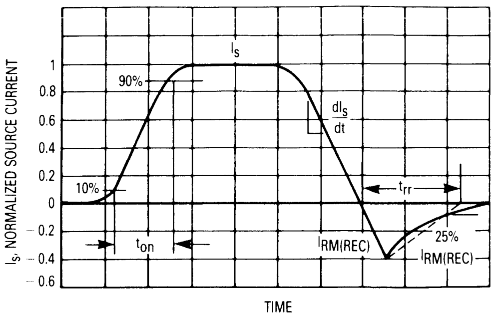
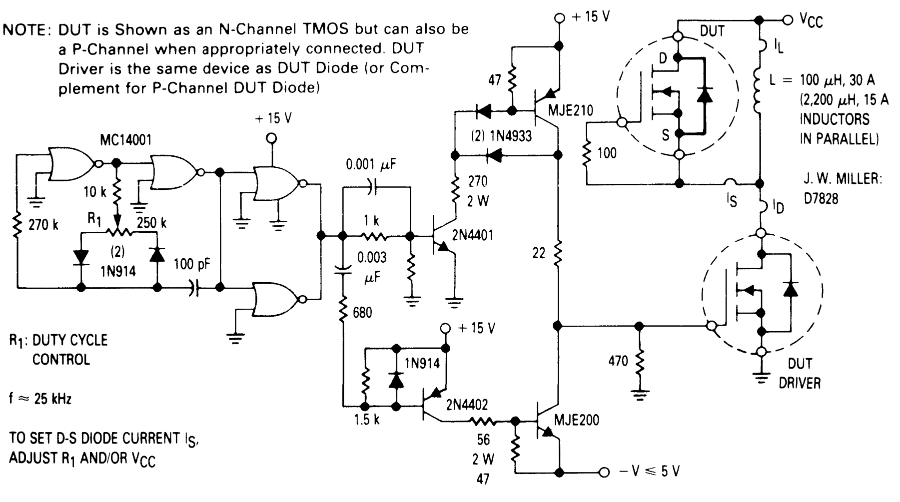


Figure 16. Diode Switching Waveform

Figure 17. TMOS Diode Switching Test Circuit

NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)



R1: DUTY CYCLE CONTROL

f ≈ 25 kHz

TO SET D-S DIODE CURRENT I_S, ADJUST R_1 AND/OR V_{CC}

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH35N05 MTH35N06 MTM35N05 MTM35N06

Designer's Data Sheet

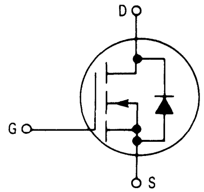
Power Field Effect Transistor

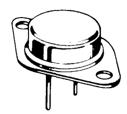
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

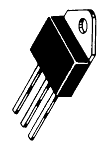
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
35 AMPERES
$r_{DS(on)}$ = 0.055 OHM
50 and 60 VOLTS





MTM35N05
MTM35N06
CASE 197A-02
TO-204AE



MTH35N05
MTH35N06
CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH or MTM 35N05	MTH or MTM 35N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	35 120		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH35N05, MTM35N05 MTH35N06, MTM35N06	$V_{(BR)DSS}$	 50 60	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 17.5 Adc)		$r_{DS(on)}$	—	0.055	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 35 Adc) (I_D = 17.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	2.3 1.9	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 17.5 A)		g_{FS}	8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	29 (Typ)		nC
Gate-Source Charge		Q_{gs}	23 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

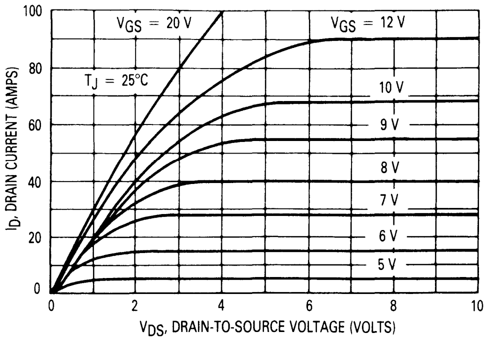


Figure 1. On-Region Characteristics

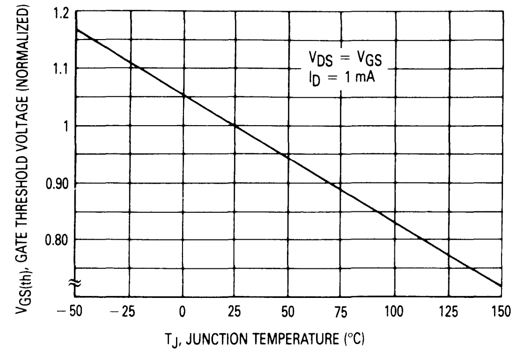


Figure 2. Gate-Threshold Voltage Variation With Temperature

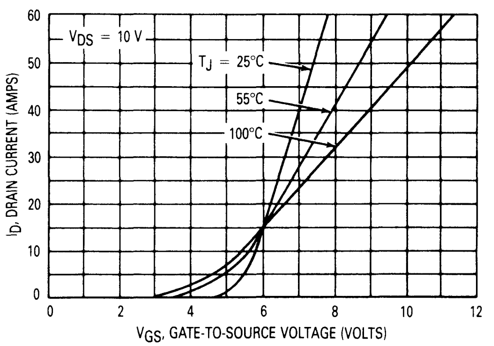


Figure 3. Transfer Characteristics

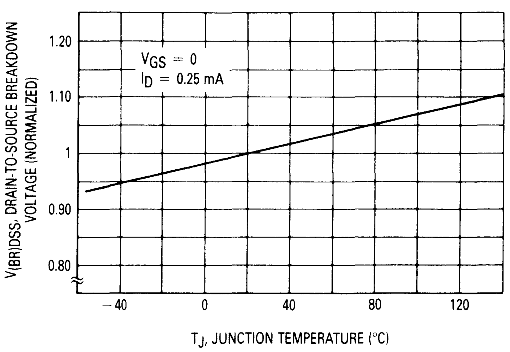


Figure 4. Breakdown Voltage Variation With Temperature

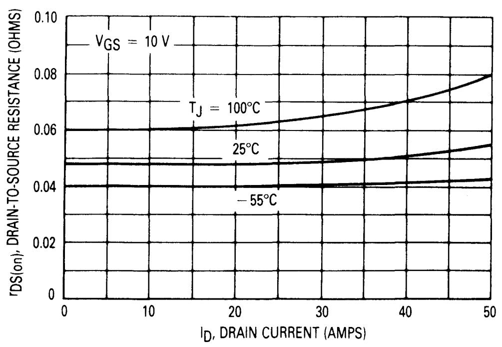


Figure 5. On-Resistance versus Drain Current

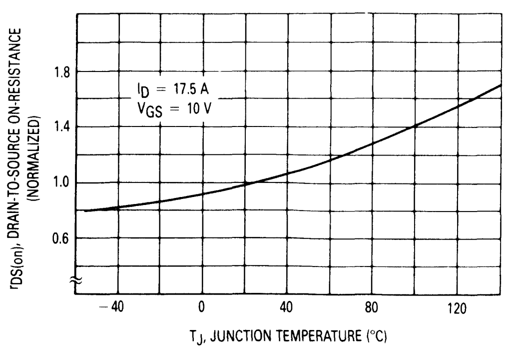


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

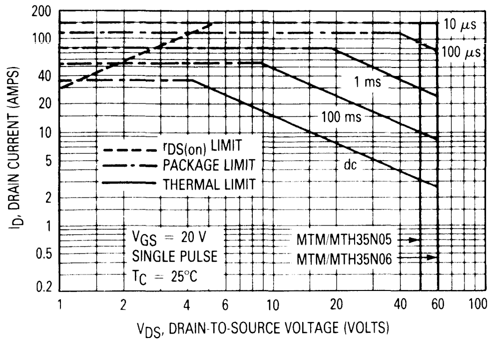


Figure 7. Maximum Rated Forward Biased Safe Operating Area

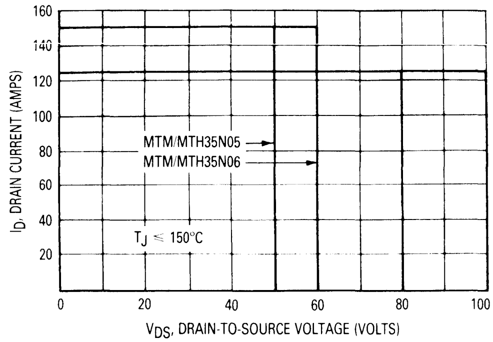


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

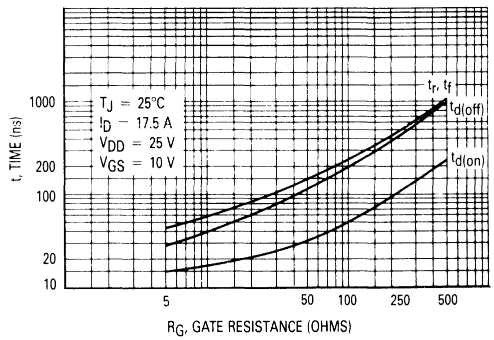


Figure 9. Resistive Switching Time Variation versus Gate Resistance

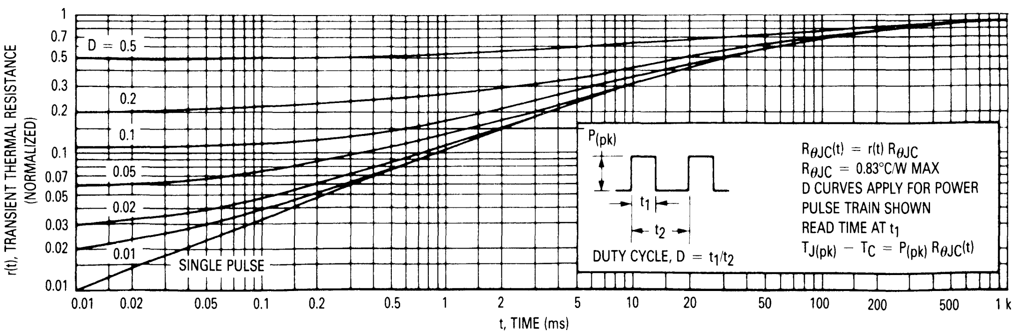


Figure 10. Thermal Response

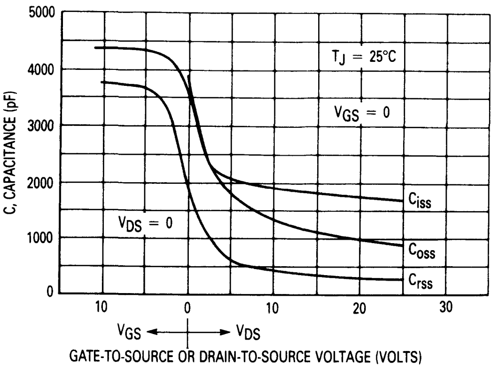


Figure 11. Capacitance Variation

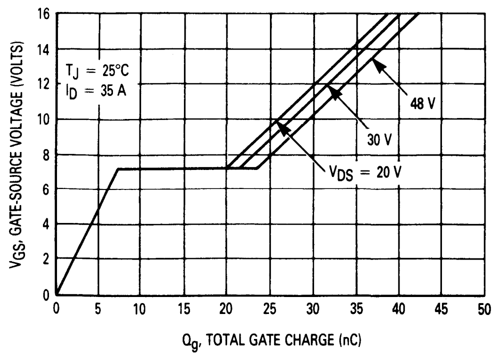


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

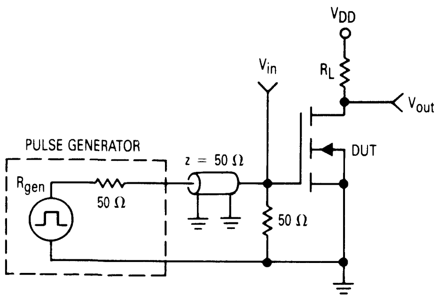


Figure 13. Switching Test Circuit

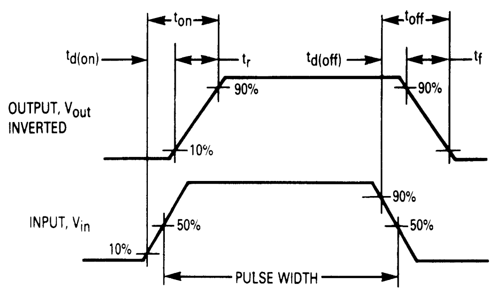
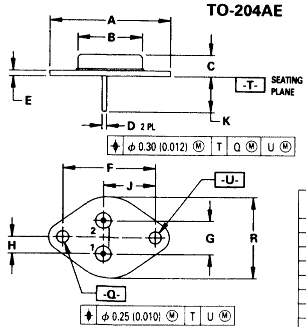


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 197A-02
TO-204AE

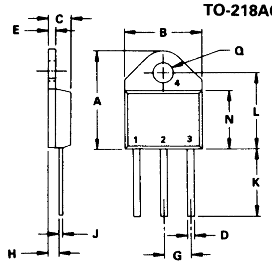


STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH35N06E
MTM35N06E

Designer's Data Sheet

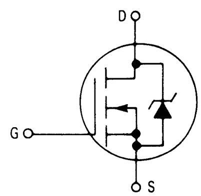
TMOS IV
Power Field Effect Transistors
N-Channel Enhancement-Mode Silicon Gate

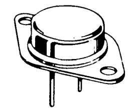
TMOS POWER FETs
35 AMPERES
$r_{DS(on)}$ = 0.055 OHM
60 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

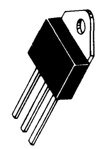
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS





MTM35N06E
CASE 197A-02
TO-204AE



MTH35N06E
CASE 340-02
TO-218AC

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	35 120	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 17.5 Adc)		$r_{DS(on)}$	—	0.055	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 35 Adc) (I_D = 17.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	2.3 1.9	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 17.5 A)		g_{FS}	14	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Inductive Switching Energy See Figures 14 and 15 (I_D = 120 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 35 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 14 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		W_{DSR}	— — —	200 500 180	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	60 (Typ)	90	nC
Gate-Source Charge		Q_{gs}	33 (Typ)	—	
Gate-Drain Charge		Q_{gd}	35 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 35 A V_{GS} = 0) dI_S/dt = 100 A/μs	V_{SD}	1.7 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-218)					
Internal Drain Inductance (Measured frrom the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

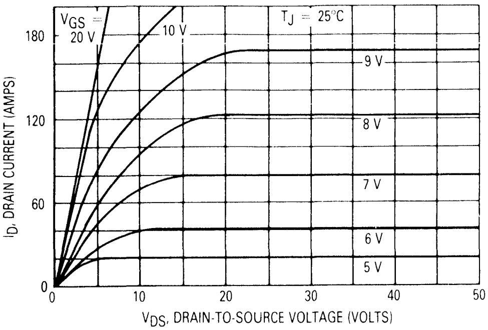


Figure 1. On-Region Characteristics

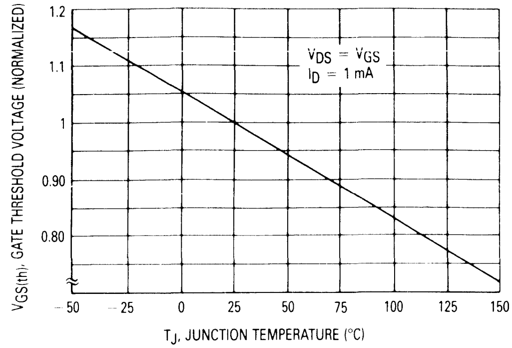


Figure 2. Gate-Threshold Voltage Variation With Temperature

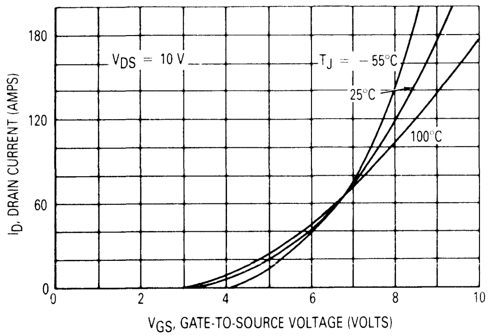


Figure 3. Transfer Characteristics

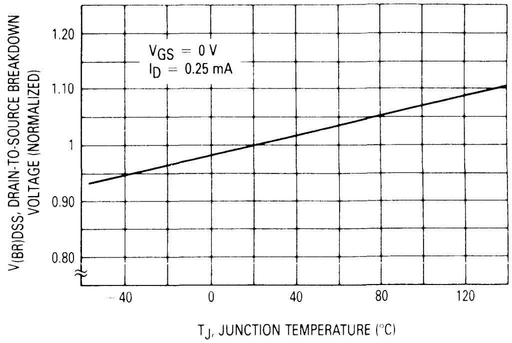


Figure 4. Breakdown Voltage Variation With Temperature

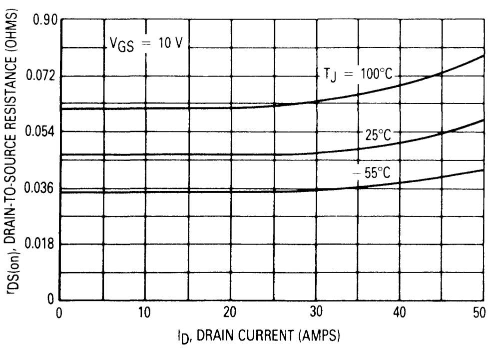


Figure 5. On-Resistance versus Drain Current

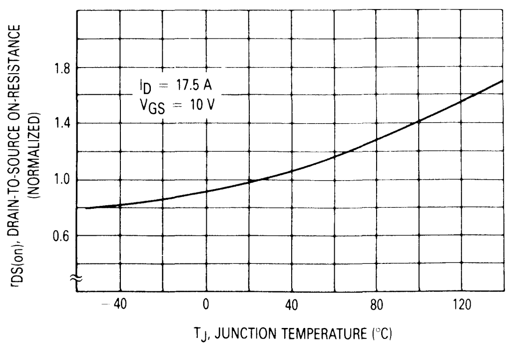


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

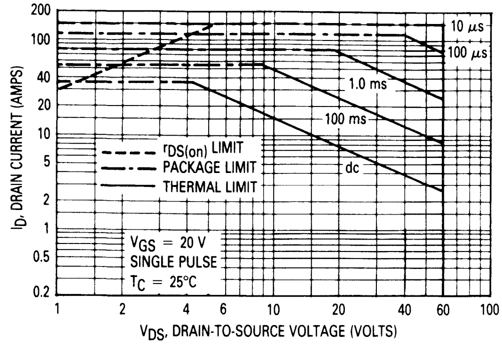


Figure 7. Maximum Rated Forward Biased Safe Operating Area

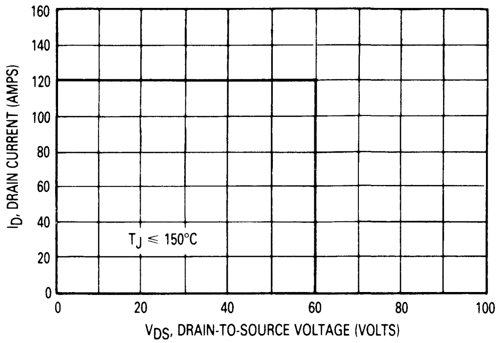


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

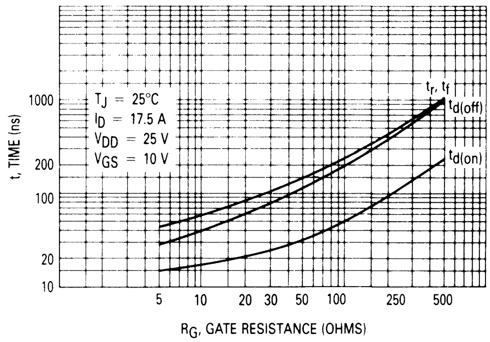


Figure 9. Resistive Switching Time Variation versus Gate Resistance

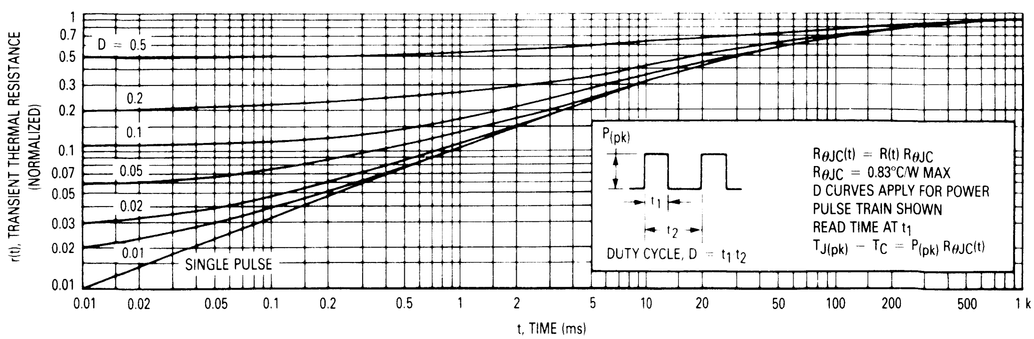


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

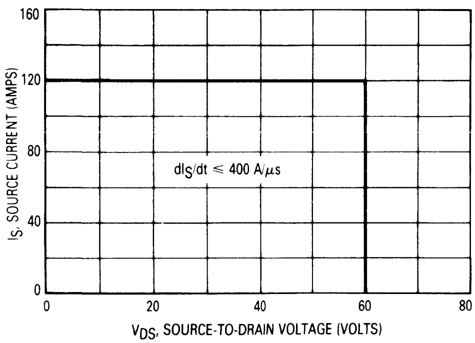


Figure 12. Commutating Safe Operating Area (CSOA)

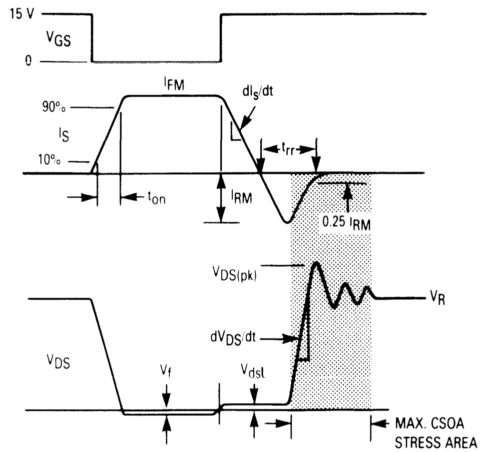


Figure 11. Commutating Waveforms

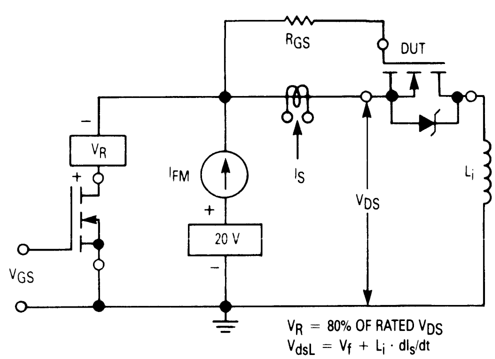


Figure 13. Commutating Safe Operating Area Test Circuit

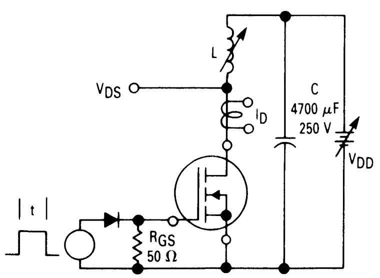
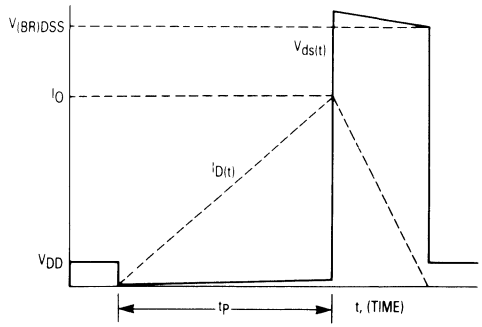


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

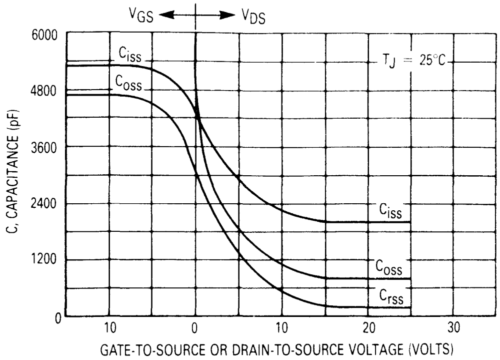


Figure 16. Capacitance Variation

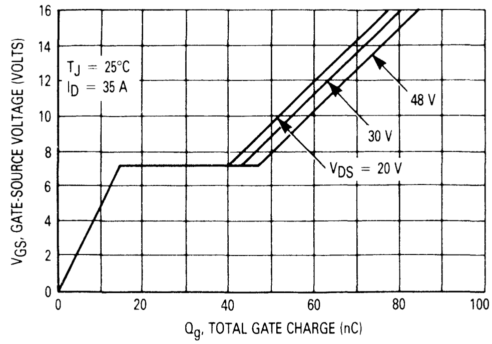
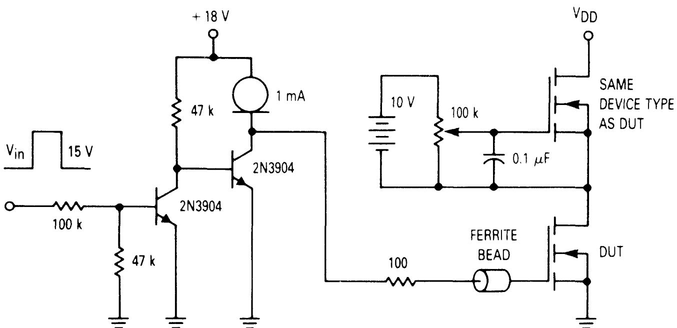


Figure 17. Gate Charge versus Gate-to-Source Voltage



$V_{in} = 15\ V_{pk}$; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

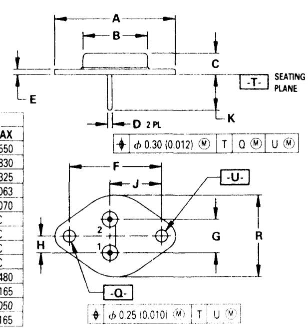
Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS

CASE 197A-02
MTM35N06E

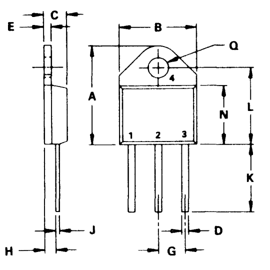
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 340-02
MTH35N06E



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTH35N15

Designer's Data Sheet

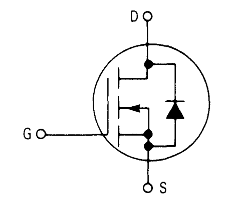
Power Field Effect Transistor

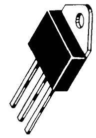
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
35 AMPERES
$r_{DS(on)}$ = 0.06 OHM
150 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	35 100	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.83 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH35N15	$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 17.5 Adc)		$r_{DS(on)}$	—	0.06	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 35 Adc) (I_D = 17.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	2.52 2.10	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 17.5 A)		g_{FS}	10	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	5500	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	85 (Typ)	95	nC
Gate-Source Charge		Q_{gs}	45 (Typ)	—	
Gate-Drain Charge		Q_{gd}	40 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	4 (Typ) 5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

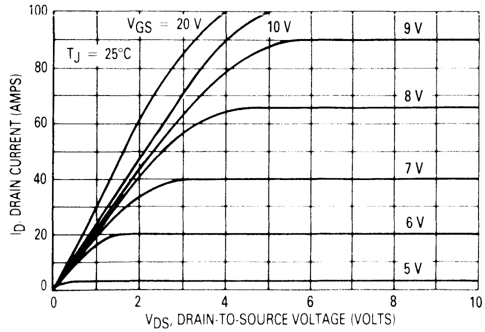


Figure 1. On-Region Characteristics

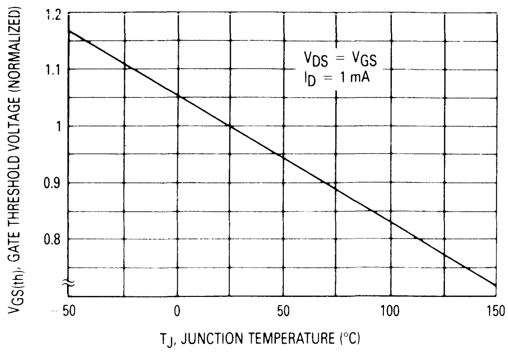
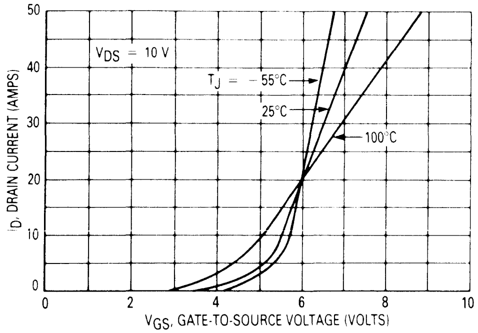


Figure 2. Gate-Threshold Voltage Variation With Temperature



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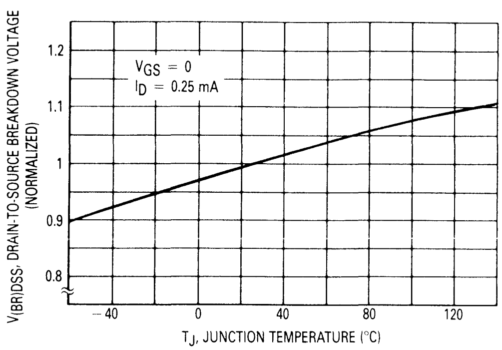

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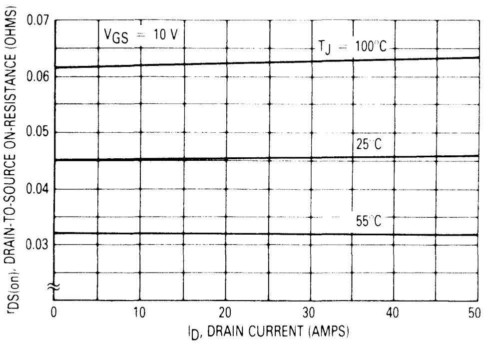

Figure 5. On-Resistance versus Drain Current

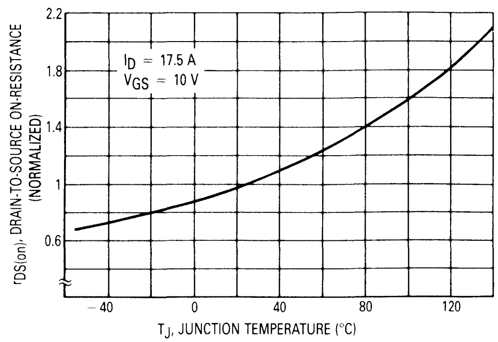

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

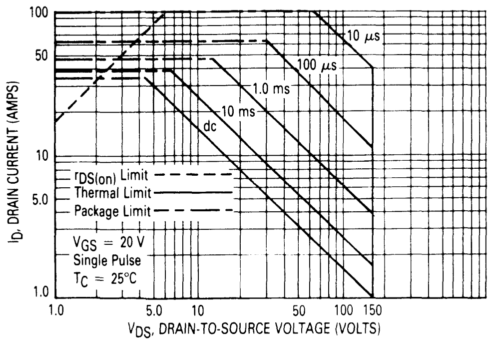

Figure 7. Maximum Rated Forward Biased Safe Operating Area

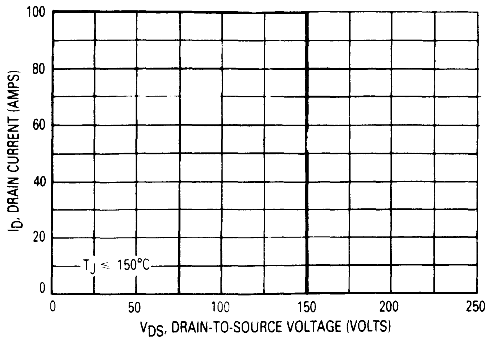

Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

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$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

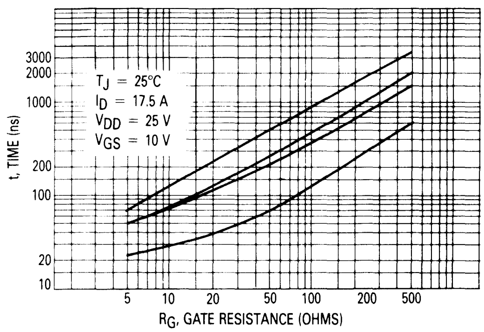


Figure 9. Resistive Switching Time Variation versus Gate Resistance

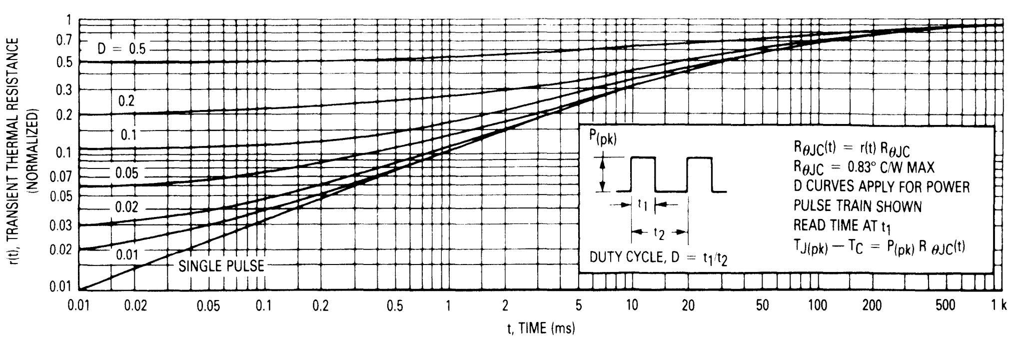


Figure 10. Thermal Response

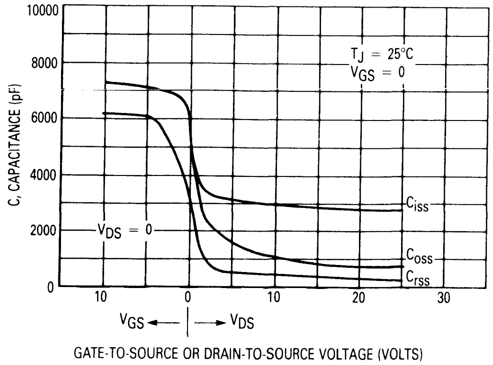


Figure 11. Capacitance Variation

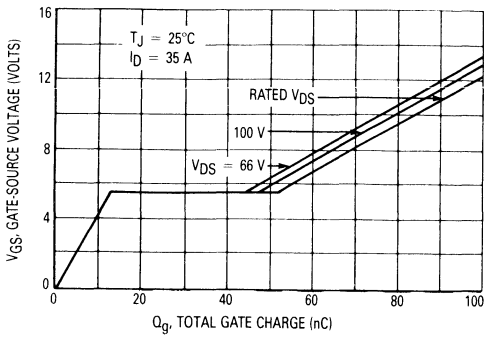


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

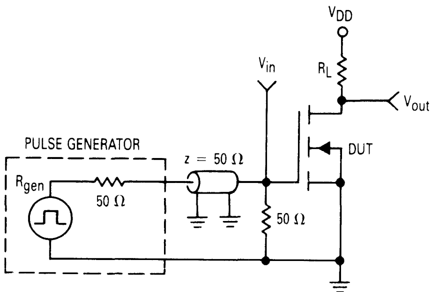


Figure 13. Switching Test Circuit

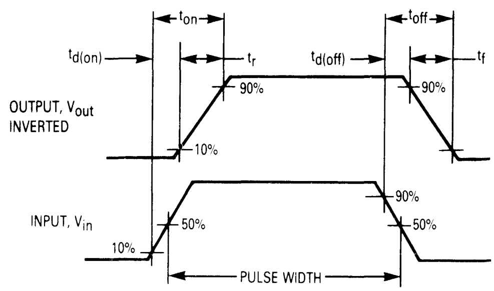
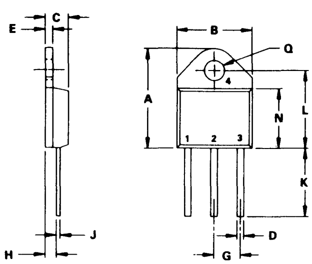


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 340-02
TO-218AC



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

MTH40N08
MTH40N10
MTH40N05
MTH40N06

Designer's Data Sheet

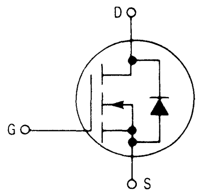
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

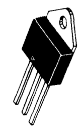
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



TMOS POWER FETs
and AMPERES
$r_{DS(on)}$ = 0.04 OHM
80 and 100 VOLTS
$r_{DS(on)}$ = 0.028 OHM
50 and 60 VOLTS

3



CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	MTH 40N05	MTH 40N06	MTH 40N08	MTH 40N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40				Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 40 140		 40 120		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.833 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTH40N05	$V_{(BR)DSS}$	50	—	Vdc
MTH40N06		60	—	
MTH40N08		80	—	
MTH40N10		100	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)	I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	500	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc) MTH40N05/06	$r_{DS(on)}$	—	0.028	Ohm
MTH40N08/10		—	0.04	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 40 Adc) MTH40N05/06	$V_{DS(on)}$	—	1.4	Vdc
(I_D = 20 Adc, T_J = 100°C) MTH40N05/06		—	1.12	
(I_D = 40 Adc) MTH40N08/10		—	2	
(I_D = 20 Adc, T_C 100°C) MTH40N08/10		—	1.6	
Forward Transconductance (V_{DS} = 15 V, I_D = 20 A)	g_{FS}	10	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 8	C_{iss}	—	5000	pF
Output Capacitance		C_{oss}	—	2500	
Reverse Transfer Capacitance		C_{rss}	—	1000	

SWITCHING CHARACTERISTICS (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 16	$t_{d(on)}$	—	100	ns
Rise Time		t_r	—	330	
Turn-Off Delay Time		$t_{d(off)}$	—	330	
Fall Time		t_f	—	360	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 Vdc) See Figure 15	Q_g	105 (Typ)	120	nC
Gate-Source Charge		Q_{gs}	74 (Typ)	—	
Gate-Drain Charge		Q_{gd}	31 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.2 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	75 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die)	L_d	4 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)		5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	10 (Typ)	—	

TYPICAL CHARACTERISTICS

MTH40N05, MTH40N06

FIGURE 1 — ON-REGION CHARACTERISTICS

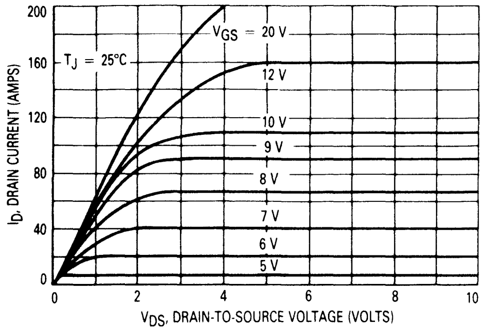


FIGURE 3 — TRANSFER CHARACTERISTICS

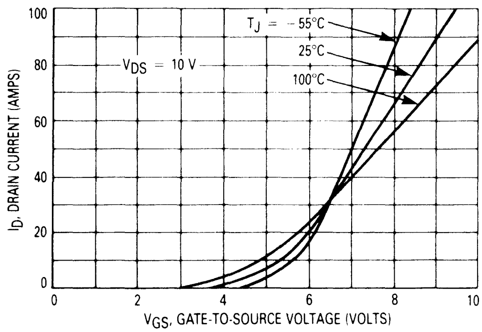
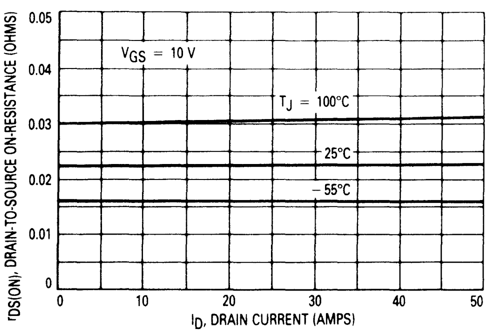


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT



MTH40N08, MTH40N10

FIGURE 2 — ON-REGION CHARACTERISTICS

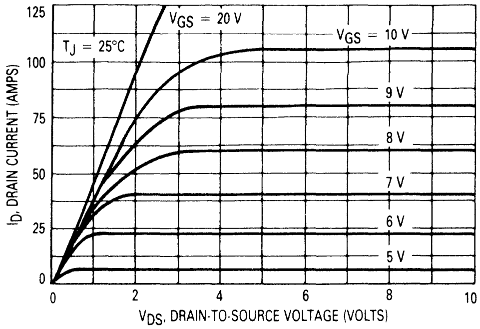


FIGURE 4 — TRANSFER CHARACTERISTICS

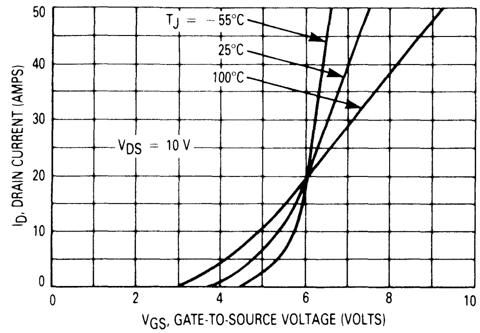
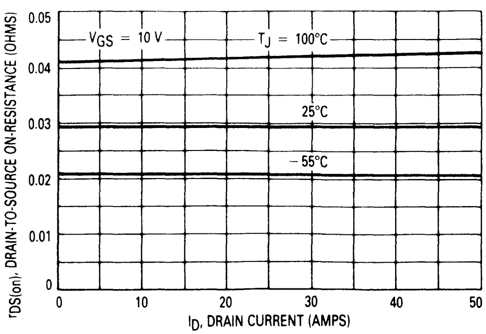


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

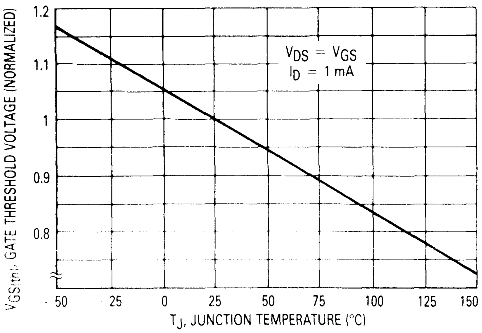


FIGURE 8 — CAPACITANCE VARIATION

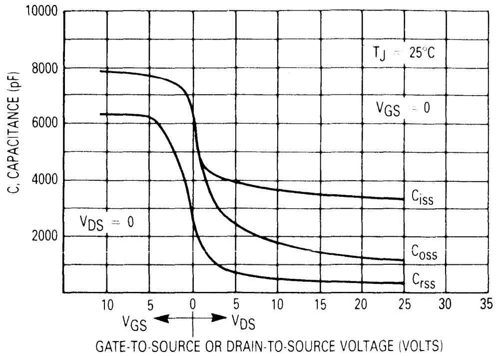


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

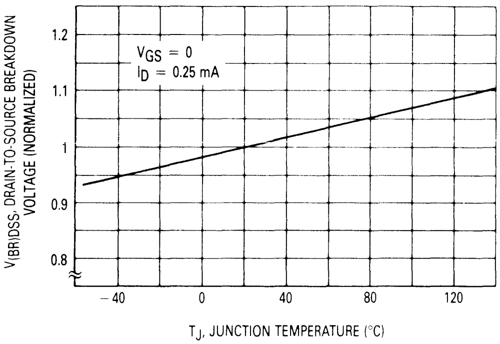


FIGURE 10 — ON-RESISTANCE VARIATION WITH TEMPERATURE

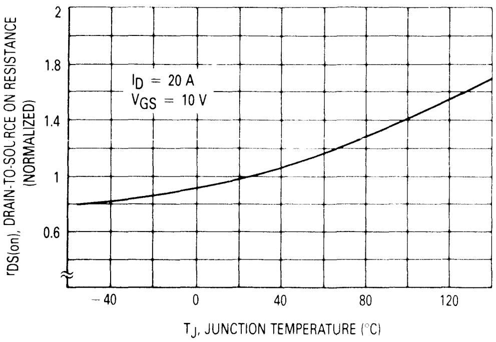
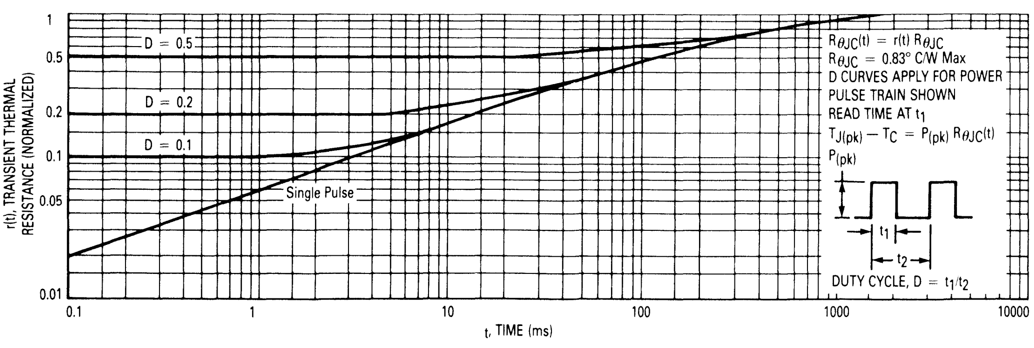


FIGURE 11 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

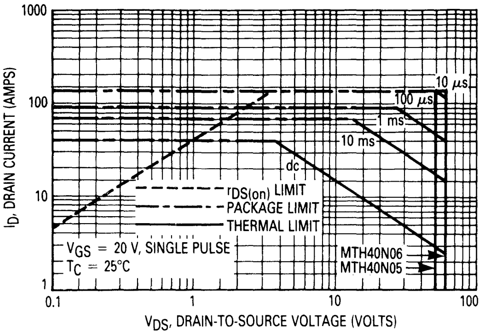
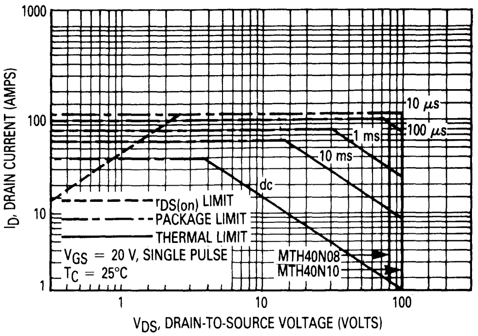


FIGURE 13 — MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

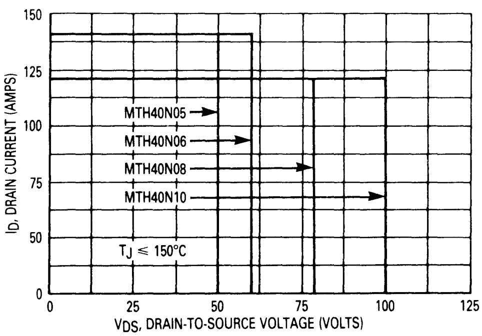


FIGURE 15 — STORED CHARGE versus GATE-TO-SOURCE VOLTAGE

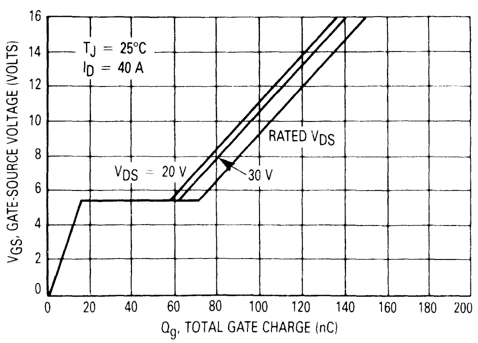
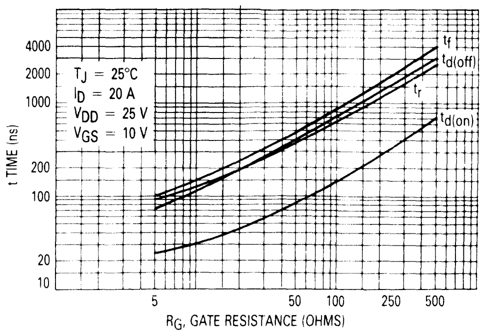


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE



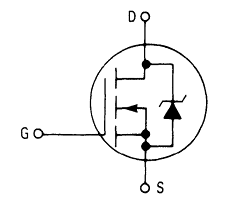
3

MTH50N05E

Designer's Data Sheet

TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

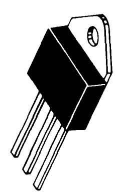
TMOS POWER FET
50 AMPERES
$r_{DS(on)}$ = 0.028 OHM
50 VOLTS



This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to IRFZ40

TMOS™



MTH50N05E
CASE 340-02
TO-218AC

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	50 160	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	80	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage	$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 250 μA)		2	4	
T_J = 100°C		1.5	3.5	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 25 Adc)	$r_{DS(on)}$	—	0.028	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 50 Adc)		—	1.4	
(I_D = 25 Adc, T_J = 100°C)		—	1.3	
Forward Transconductance (V_{DS} = 15 V, I_D = 25 A)	g_{FS}	17	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Inductive Switching Energy See Figures 14 and 15	W_{DSR}			mJ
(I_D = 160 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive)		—	60	
(I_D = 50 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 45 μs, Duty Cycle ≤ 1%)		—	135	
(I_D = 20 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 40 μs, Duty Cycle ≤ 1%)		—	50	

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1200	
Reverse Transfer Capacitance		C_{rss}	—	400	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 4.7 ohms) See Figure 9	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	70	
Fall Time		t_f	—	25	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	55 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	30 (Typ)	—	
Gate-Drain Charge		Q_{gd}	25 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = 51 A, V_{GS} = 0, dI_S/dt = 100 A/μs)	V_{DS}	1.9 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	(Typ)	250	ns

INTERNAL PACKAGE INDUCTANCE (TO-218)

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance	L_d			nH
(Measured frrom the contact screw on tab to center of die)		4 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	10 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

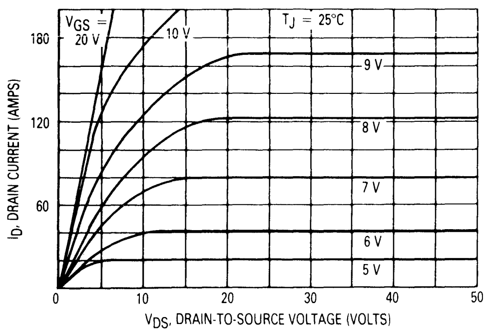


Figure 1. On-Region Characteristics

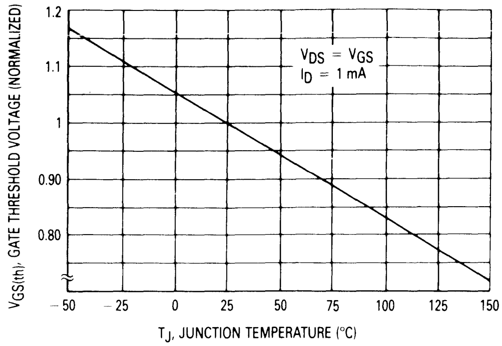


Figure 2. Gate-Threshold Voltage Variation With Temperature

3

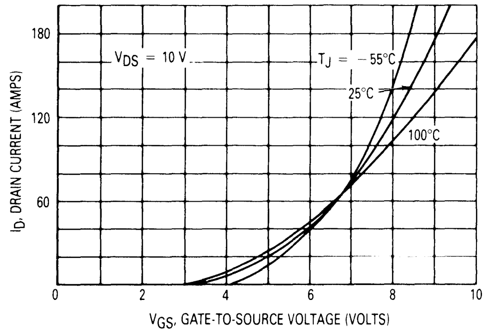


Figure 3. Transfer Characteristics

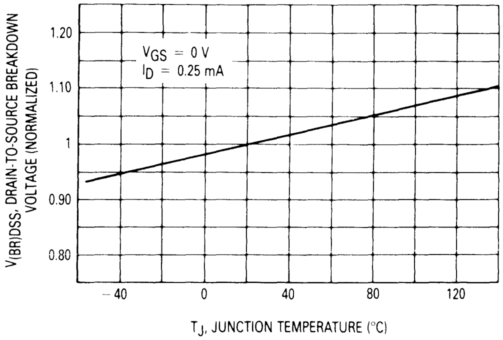


Figure 4. Breakdown Voltage Variation With Temperature

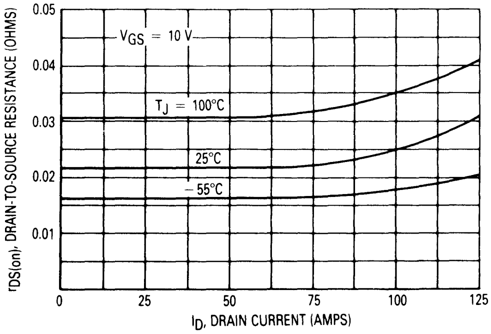


Figure 5. On-Resistance versus Drain Current

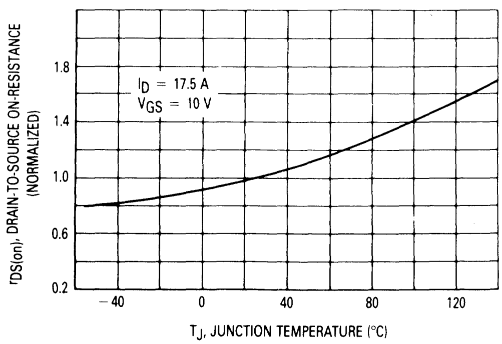


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

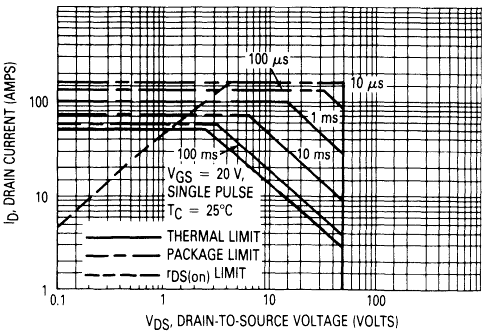


Figure 7. Maximum Rated Forward Biased Safe Operating Area

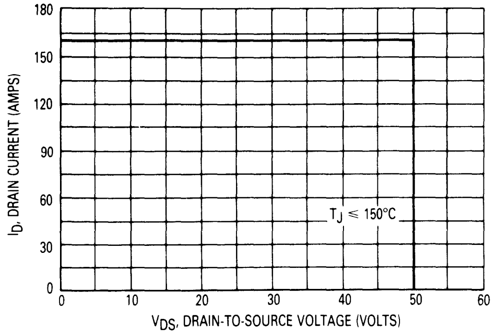


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

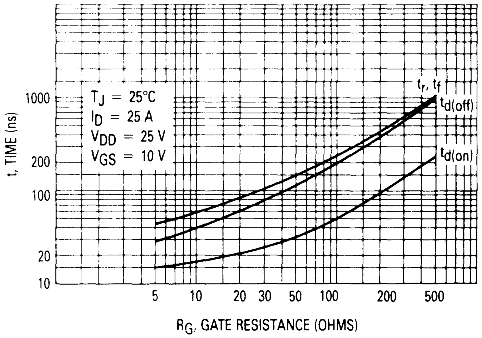


Figure 9. Resistive Switching Time Variation versus Gate Resistance

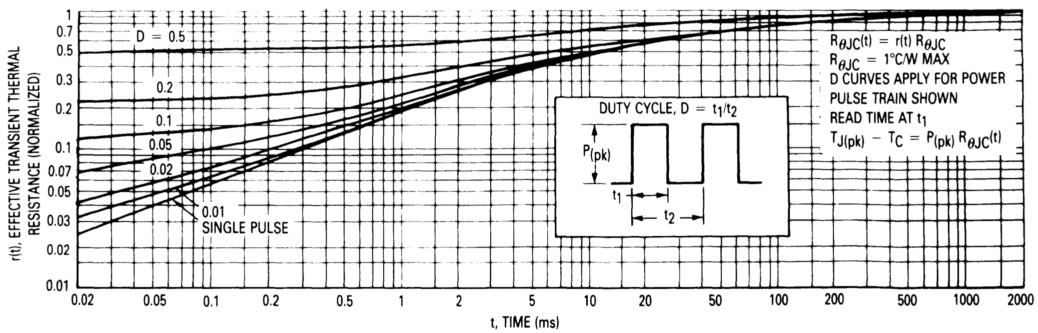


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

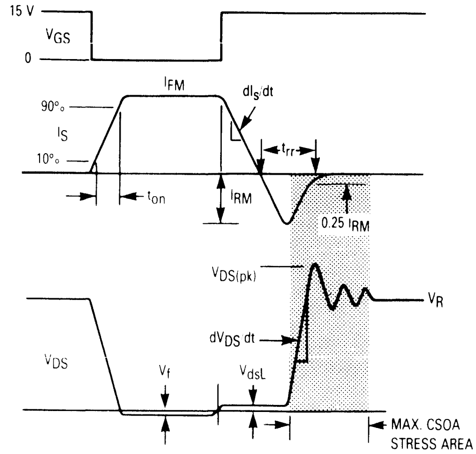


Figure 11. Commutating Waveforms

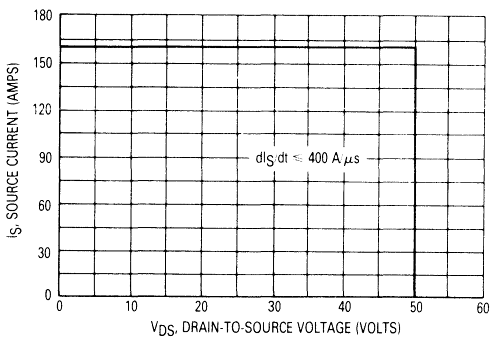


Figure 12. Commutating Safe Operating Area (CSOA)

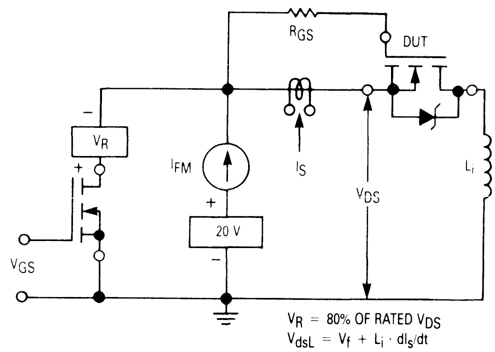


Figure 13. Commutating Safe Operating Area Test Circuit

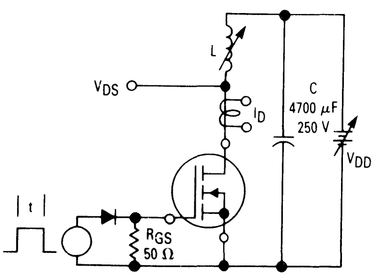
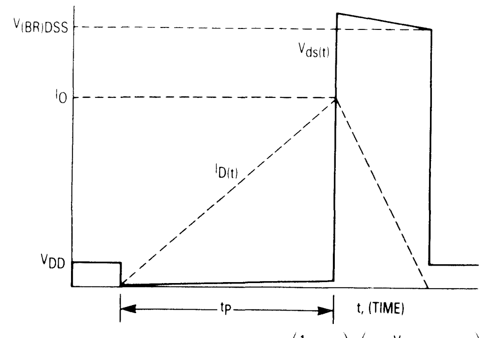


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

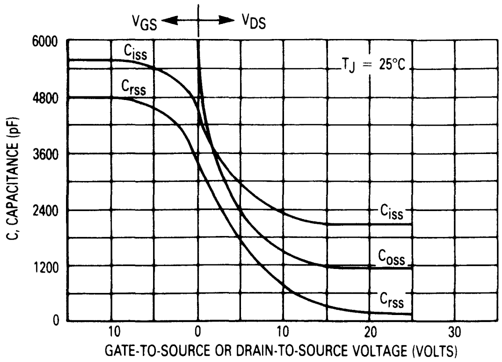


Figure 16. Capacitance Variation

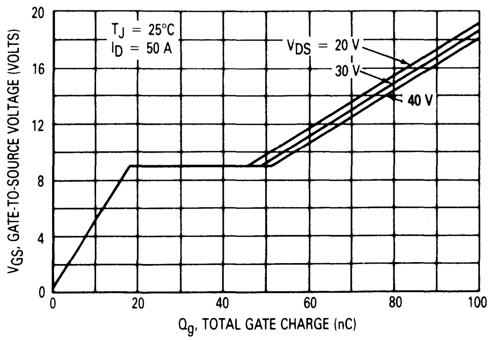
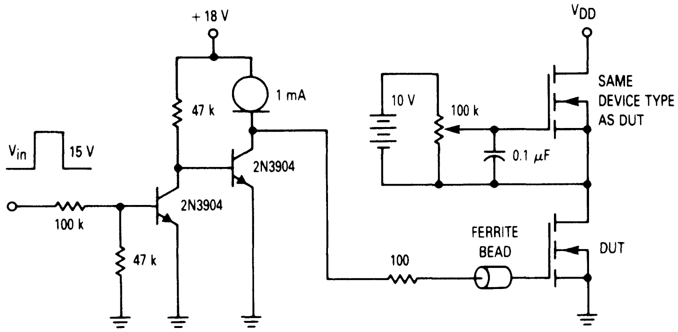


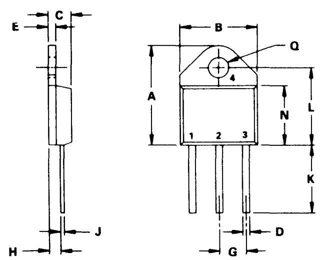
Figure 17. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

CASE 340-02

MTM1N95
MTM1N100
MTP1N95
MTP1N100

Designer's Data Sheet

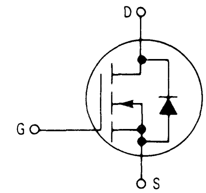
Power Field Effect Transistor

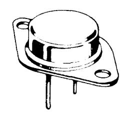
N-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

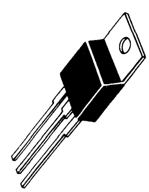
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
1 AMPERE
$r_{DS(on)}$ = 10 OHMS
950 and 1000 VOLTS





MTM1N95
MTM1N100
CASE 1-06
TO-204AA



MTP1N95
MTP1N100
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM1N95 / MTP1N95	MTM1N100 / MTP1N100	Unit
Drain-Source Voltage	V_{DSS}	950	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	950	1000	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	1 6		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient TO-204 TO-220	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 30 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM1N95/MTP1N95 MTM1N100/MTP1N100	$V_{(BR)DSS}$	 950 1000	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are give to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$r_{DS(on)}$	—	10	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 0.5 Adc)		$V_{DS(on)}$	—	5	Vdc
(I_D = 0.5 Adc, T_J = 100°C)			—	10	
Forward Transconductance (V_{DS} = 15 V, I_D = 0.5 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 125 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	33 (Typ)	37	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1 (Typ)	1.3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	725 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	nH
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

3

TYPICAL ELECTRICAL CHARACTERISTICS

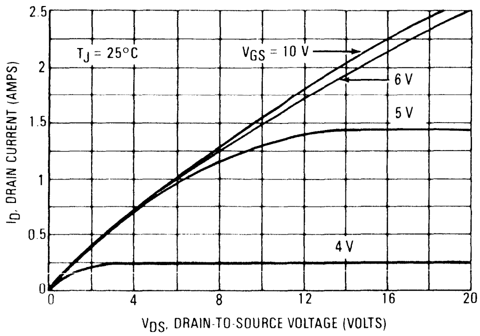


Figure 1. On-Region Characteristics

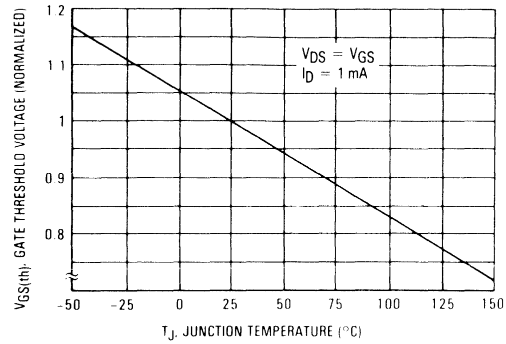


Figure 2. Gate-Threshold Voltage Variation With Temperature

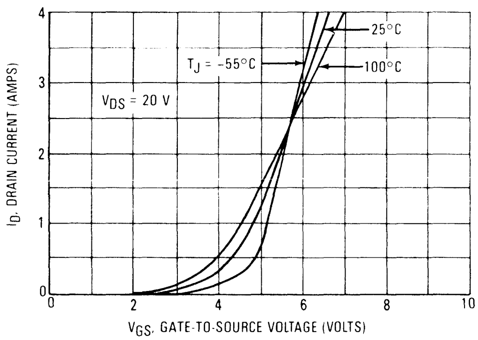


Figure 3. Transfer Characteristics

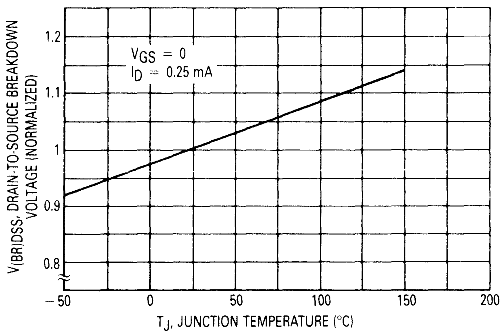


Figure 4. Breakdown Voltage Variation With Temperature

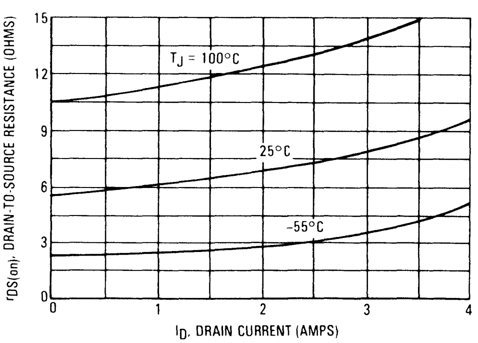


Figure 5. On-Resistance versus Drain Current

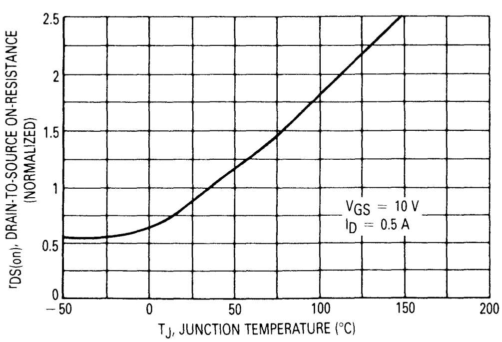


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

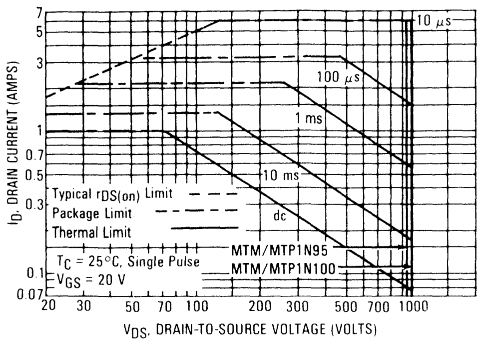


Figure 7. Maximum Rated Forward Biased Safe Operating Area

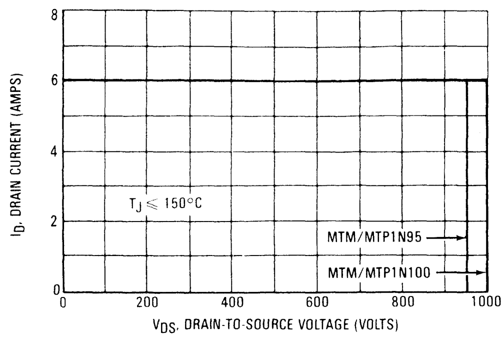


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

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The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

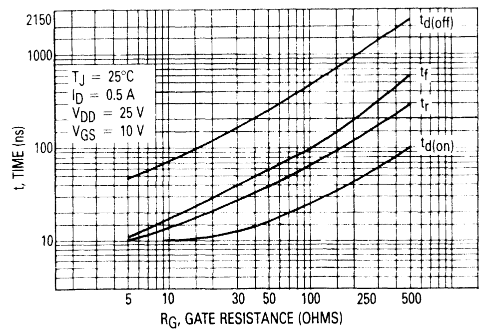


Figure 9. Resistive Switching Time Variation versus Gate Resistance

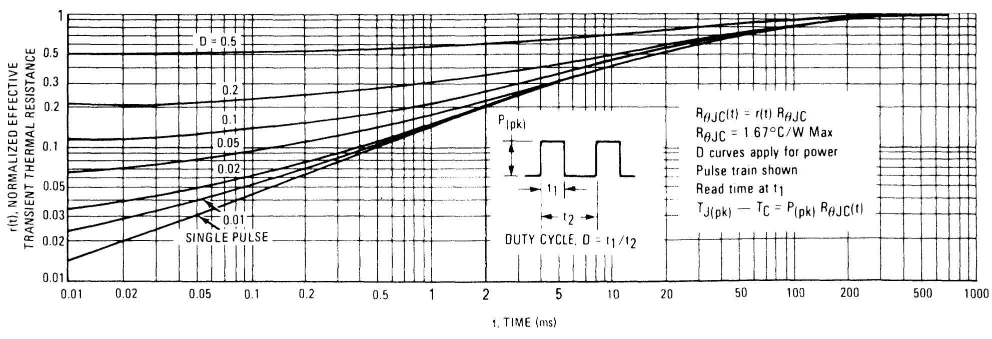


Figure 10. Thermal Response

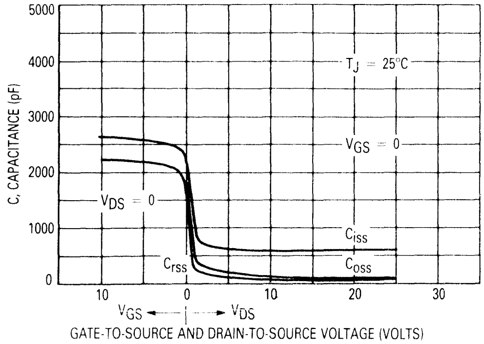


Figure 11. Capacitance Variation

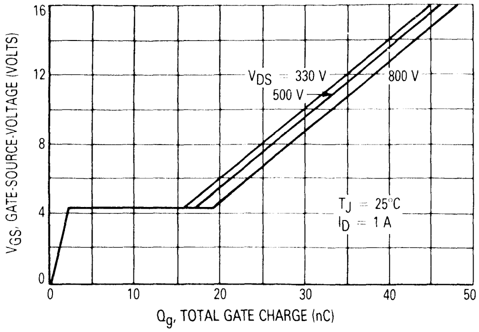


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

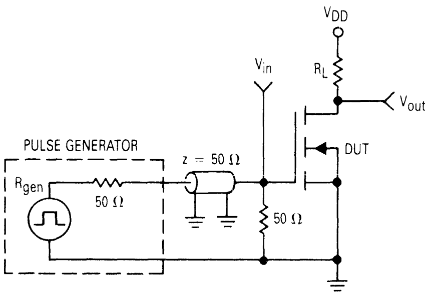


Figure 13. Switching Test Circuit

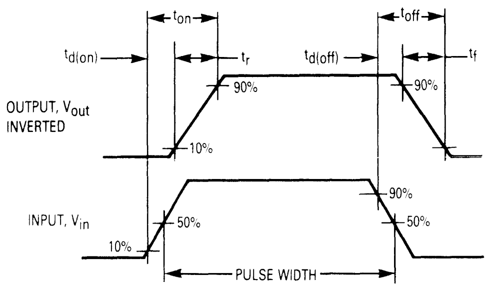
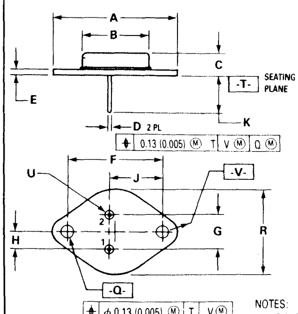


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

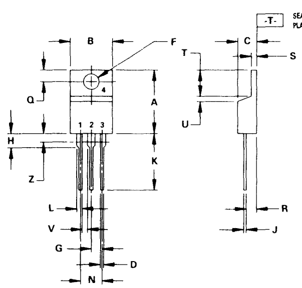
CASE 1-06
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM2N50
MTP2N45
MTP2N50

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 4 OHMS
450 and 500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
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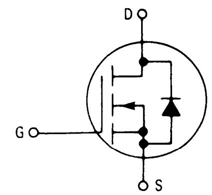
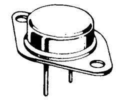
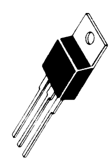




MTM2N50
CASE 1-06
TO-204AA



MTP2N45
MTP2N50
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP2N45	MTM2N50 / MTP2N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 2 7		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP2N45 / MTM/MTP2N50		$V_{(BR)DSS}$	450 / 500	— / —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) / (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— / —	0.2 / 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) / T_J = 100°C		$V_{GS(th)}$	2 / 1.5	4.5 / 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	4	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) / (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	— / —	10 / 8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	
Reverse Transfer Capacitance		C_{rss}	—	50	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	60	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	17 (Typ)	25	nC
Gate-Source Charge		Q_{gs}	9 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) / (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) / 4.5 (Typ)	— / —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

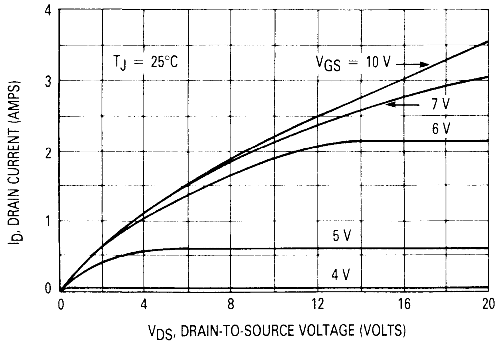


Figure 1. On-Region Characteristics

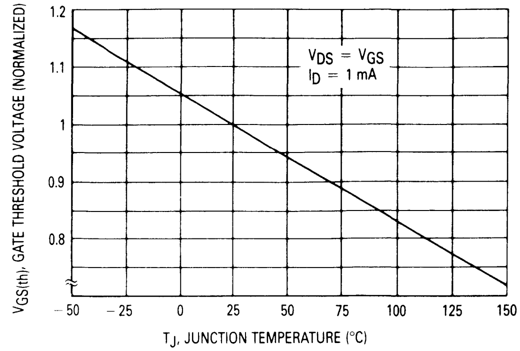


Figure 2. Gate-Threshold Voltage Variation With Temperature

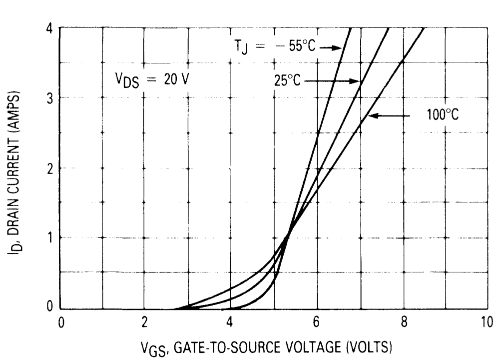


Figure 3. Transfer Characteristics

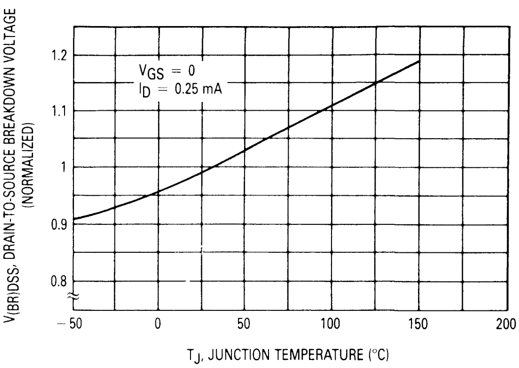


Figure 4. Breakdown Voltage Variation With Temperature

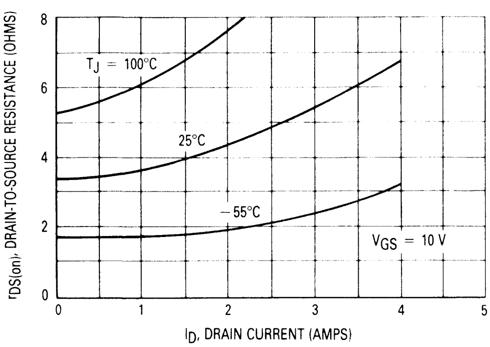


Figure 5. On-Resistance versus Drain Current

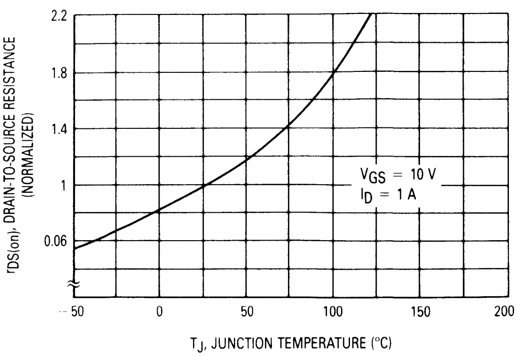


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

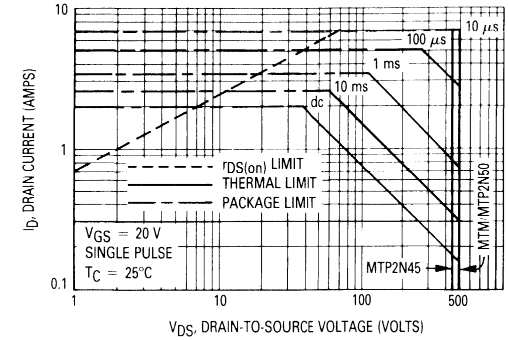


Figure 7. Maximum Rated Forward Biased Safe Operating Area

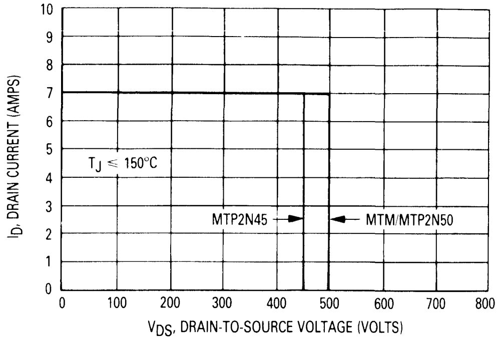


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

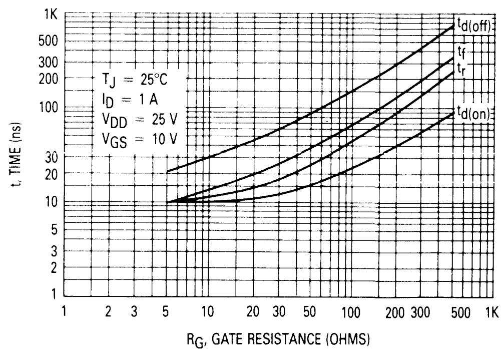


Figure 9. Resistive Switching Time Variation versus Gate Resistance

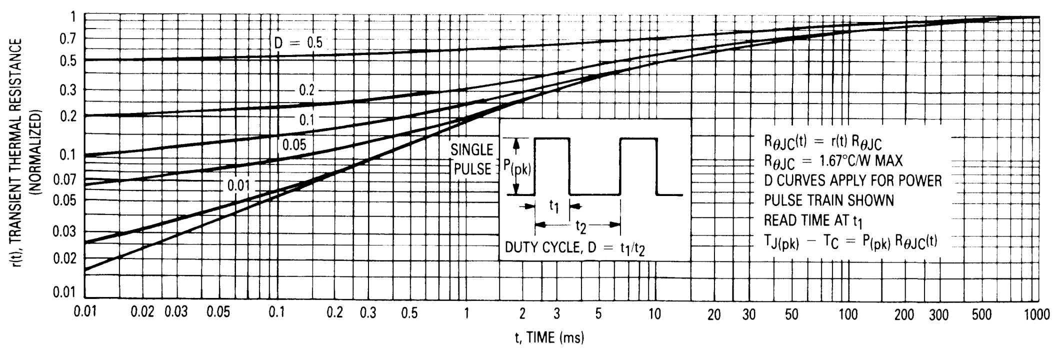


Figure 10. Thermal Response

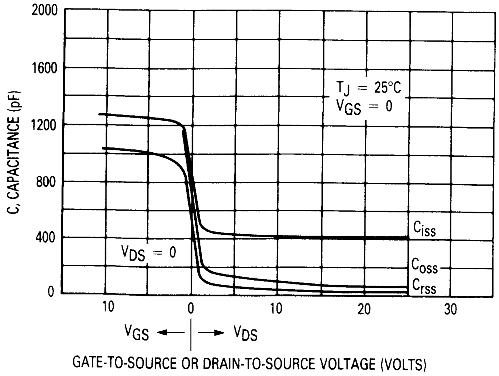


Figure 11. Capacitance Variation

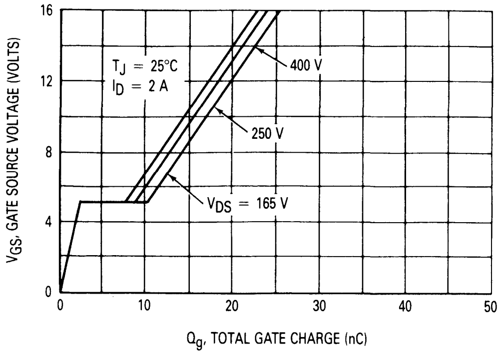


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

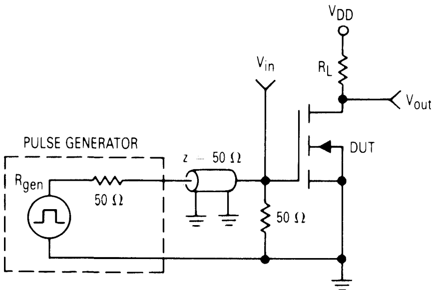


Figure 13. Switching Test Circuit

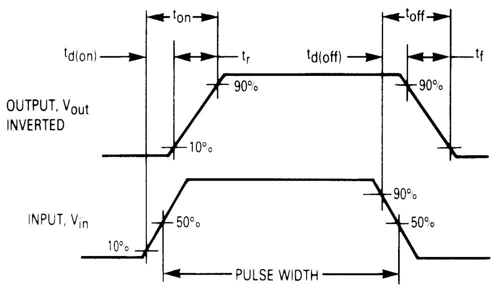
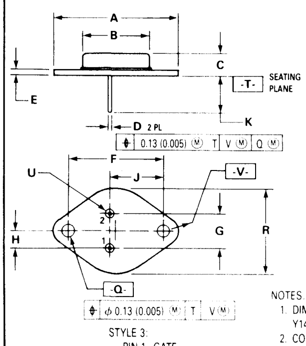


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

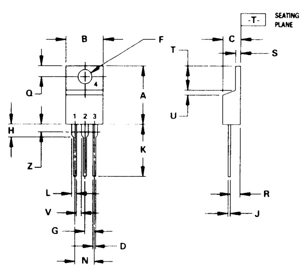


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 221A-04
TO-220AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM2N85
MTM2N90
MTP2N85
MTP2N90

Designer's Data Sheet

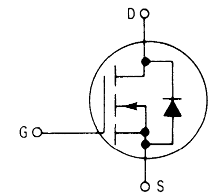
Power Field Effect Transistor

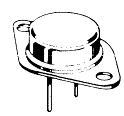
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 8 OHMS
850 and 900 VOLTS

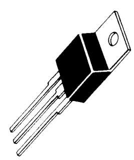
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM2N85
MTM2N90
CASE 1-06
TO-204AA



MTP2N85
MTP2N90
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM2N85 MTP2N85	MTM2N90 MTP2N90	Unit
Drain-Source Voltage	V_{DSS}	850	900	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	850	900	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 7		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Max	Unit
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP2N85		$V_{(BR)DSS}$	850	—	Vdc
MTM/MTP2N90			900	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc)		$V_{DS(on)}$	—	20	Vdc
(I_D = 1 Adc, T_J = 100°C)			—	16	
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	33 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	420 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

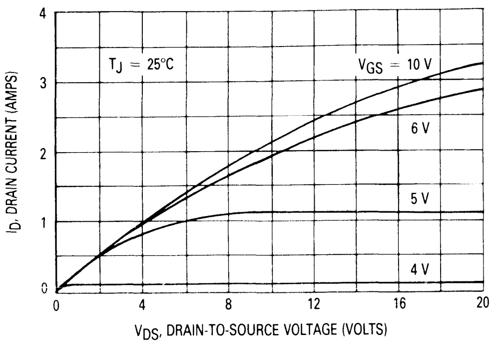


Figure 1. On-Region Characteristics

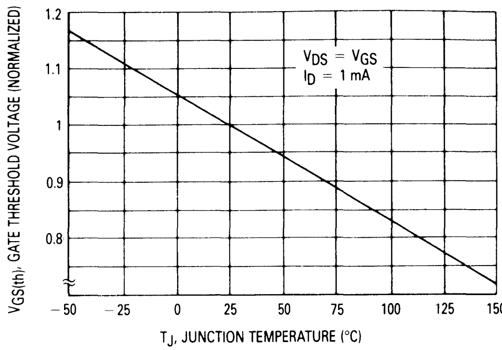


Figure 2. Gate-Threshold Voltage Variation With Temperature

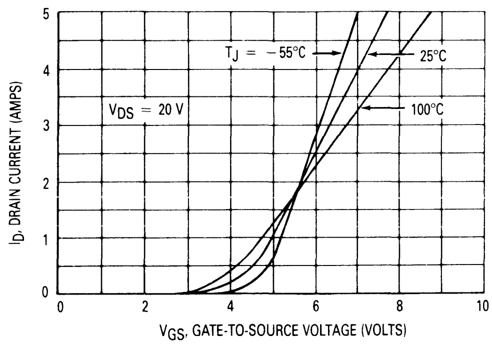


Figure 3. Transfer Characteristics

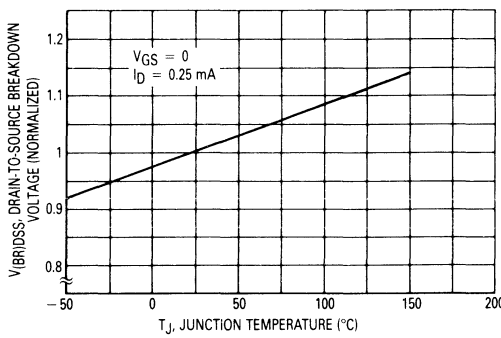


Figure 4. Breakdown Voltage Variation With Temperature

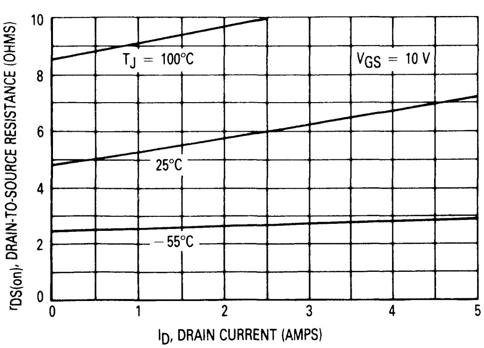


Figure 5. On-Resistance versus Drain Current

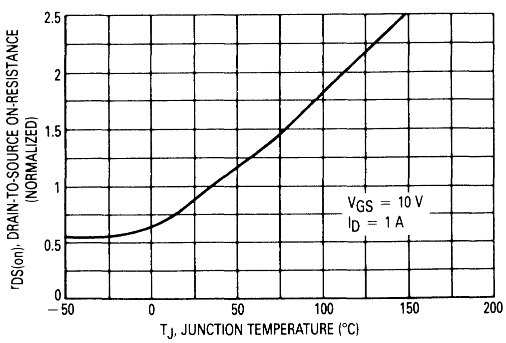


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

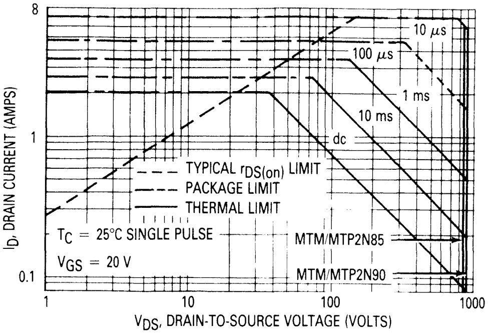


Figure 7. Maximum Rated Forward Biased Safe Operating Area

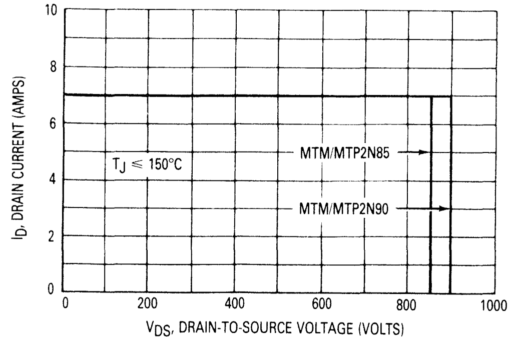


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

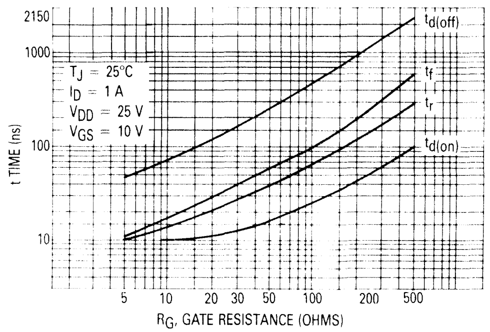


Figure 9. Resistive Switching Time Variation versus Gate Resistance

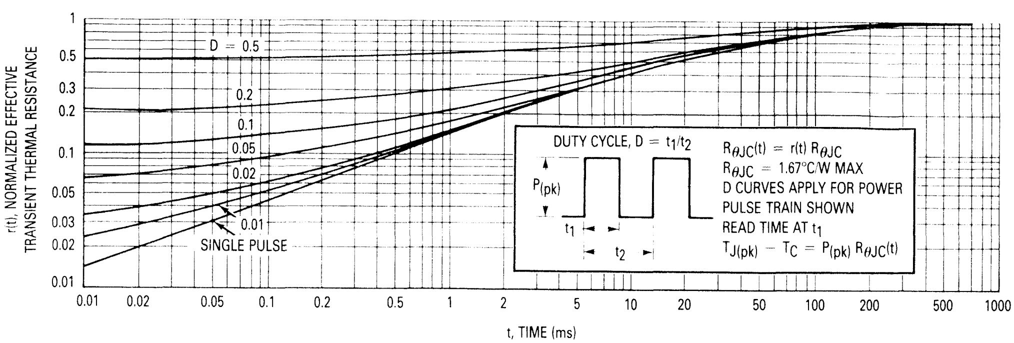


Figure 10. Thermal Response

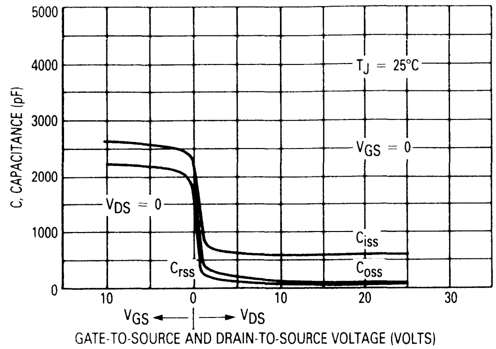


Figure 11. Capacitance Variation

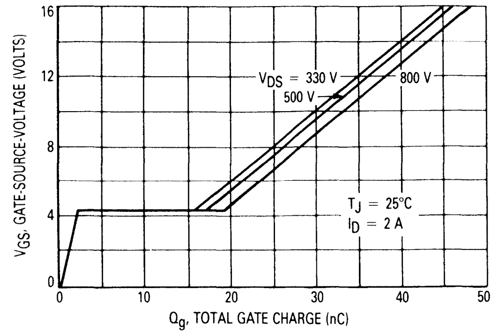


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

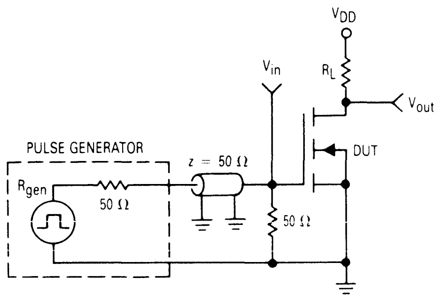


Figure 13. Switching Test Circuit

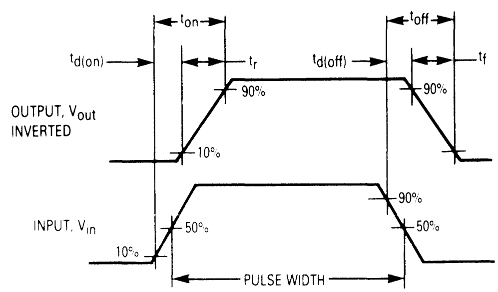
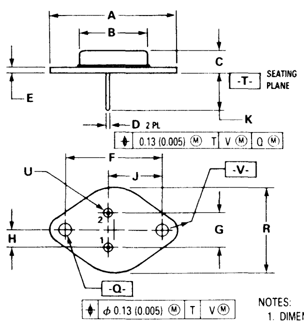


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

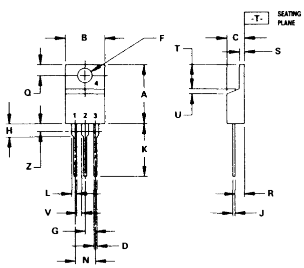


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM2P45 MTM2P50 MTP2P45 MTP2P50

Designer's Data Sheet

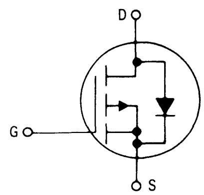
Power Field Effect Transistor

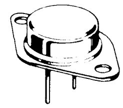
P-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 6 OHMS
450 and 500 VOLTS

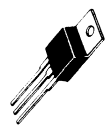
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM2P45
MTM2P50
CASE 1-06
TO-204AA



MTP2P45
MTP2P50
CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MTM2P45 / MTP2P45	MTM2P50 / MTP2P50	Unit
Drain-Sourve Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current Continuous Pulsed	I_D I_{DM}	2 8		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient TO-204 TO-220	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 30 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM2P45/MTP2P45 MTM2P50/MTP2P50	$V_{(BR)DSS}$	 450 500	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued ($T_C = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*				
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1$ mA)	$V_{GS(th)}$	2	4.5	Vdc
$T_J = 100°C$		1.5	4	
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 1$ Adc)	$r_{DS(on)}$	—	6	Ohms
Drain-Source On-Voltage ($V_{GS} = 10$ V) ($I_D = 1$ Adc)	$V_{DS(on)}$	—	6	Vdc
($I_D = 1$ Adc, $T_J = 100°C$)		—	12	
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 1$ A)	g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance ($V_{DS} = 25$ V, $V_{GS} = 0$, f = 1 MHz) See Figure 11	C_{iss}	—	100	pF
Output Capacitance	C_{oss}	—	200	
Reverse Transfer Capacitance	C_{rss}	—	80	
SWITCHING CHARACTERISTICS* ($T_J = 100°C$)				
Turn-On Delay Time ($V_{DS} = 125$ V, $I_D = 0.5$ Rated I_D, $R_{gen} = 50$ ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time	t_r	—	100	
Turn-Off Delay Time	$t_{d(off)}$	—	150	
Fall Time	t_f	—	50	
Total Gate Charge ($V_{DS} = 0.8$ Rated V_{DSS}, $I_D =$ Rated I_D, $V_{GS} = 10$ V) See Figure 12	Q_g	20 (Typ)	25	nC
Gate-Source Charge	Q_{gs}	10 (Typ)	—	
Gate-Drain Charge	Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage ($I_S =$ Rated I_D, $V_{GS} = 0$)	V_{SD}	1.8 (Typ)	2.5	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	120 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance (Measured from contact screw on tab to center of die)	L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

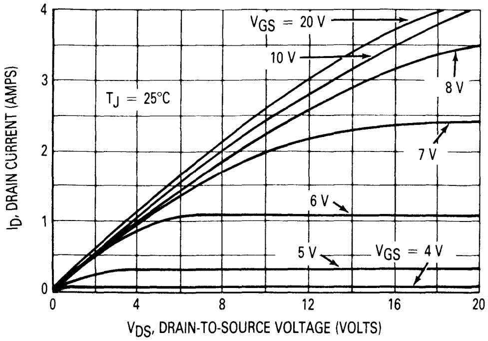


Figure 1. On-Region Characteristics

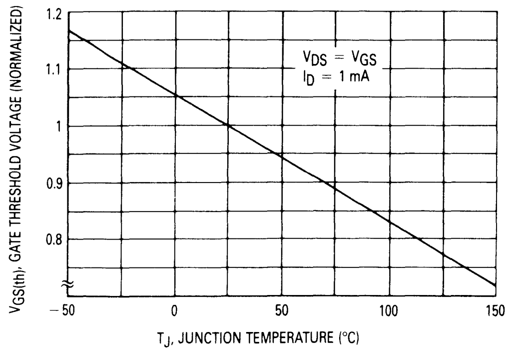


Figure 2. Gate-Threshold Voltage Variation With Temperature

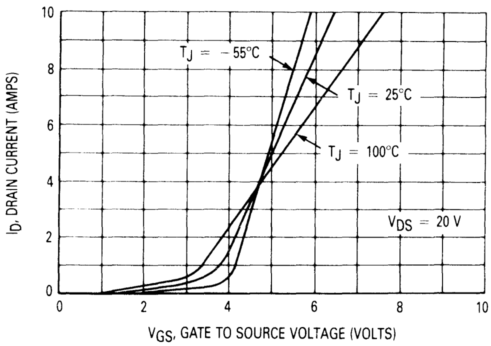


Figure 3. Transfer Characteristics

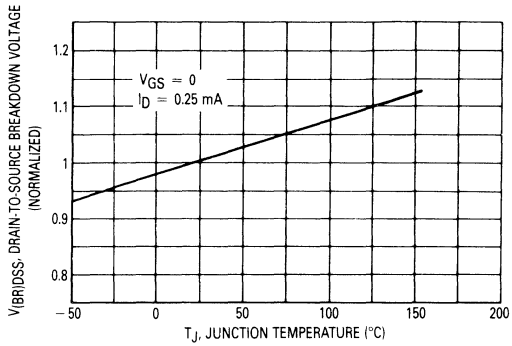


Figure 4. Breakdown Voltage Variation With Temperature

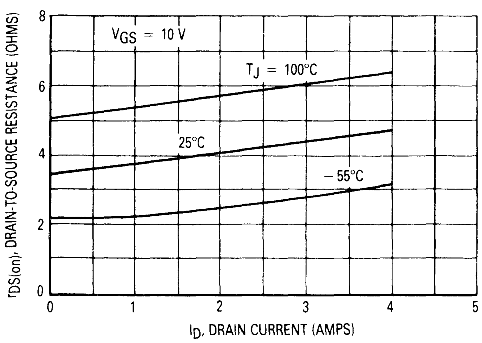


Figure 5. On-Resistance versus Drain Current

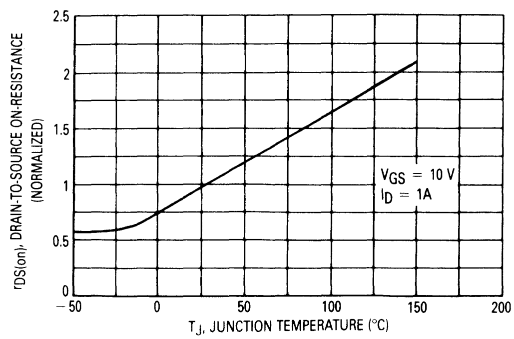


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

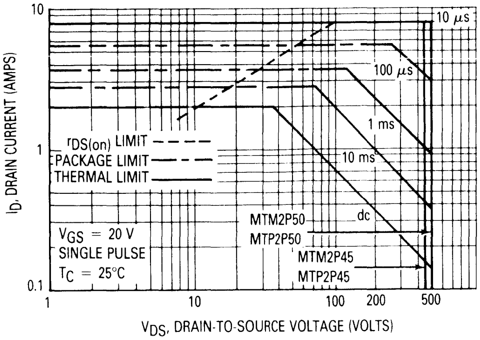


Figure 7. Maximum Rated Forward Biased Safe Operating Area

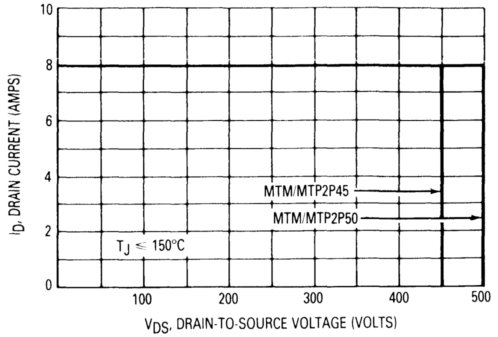


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

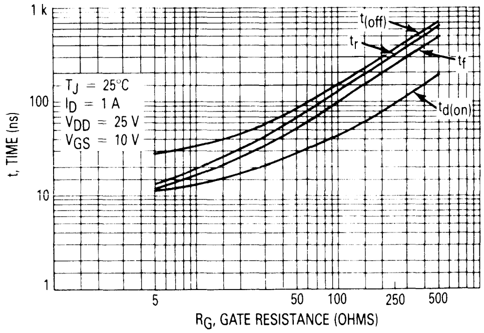


Figure 9. Resistive Switching Time Variation versus Gate Resistance

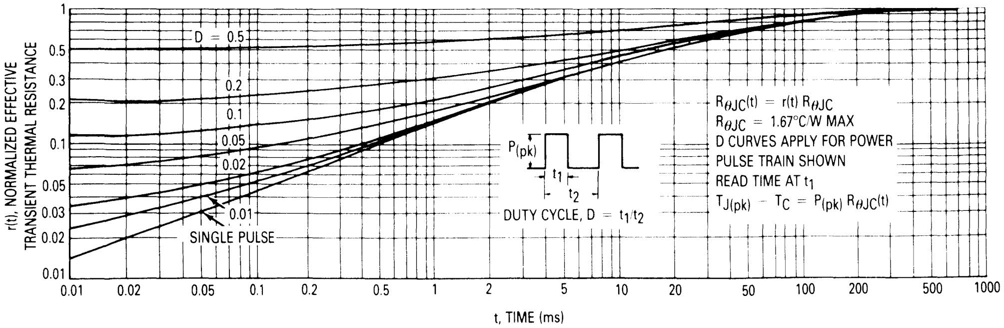


Figure 10. Thermal Response

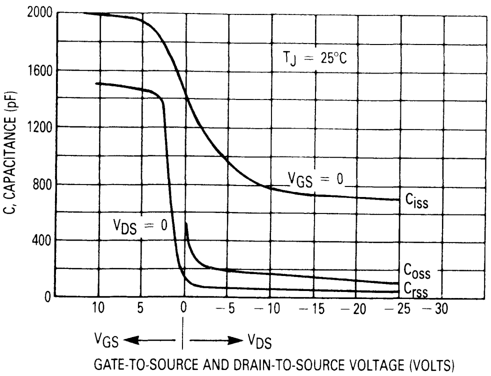


Figure 11. Capacitance Variation

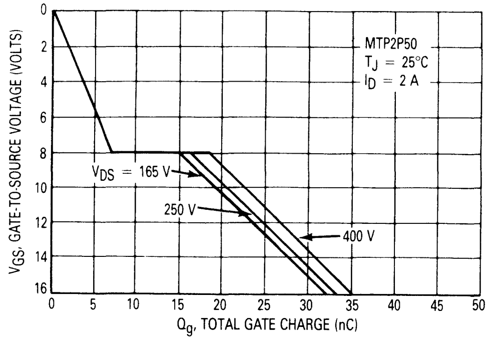


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

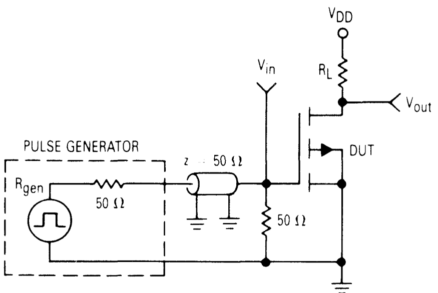


Figure 13. Switching Test Circuit

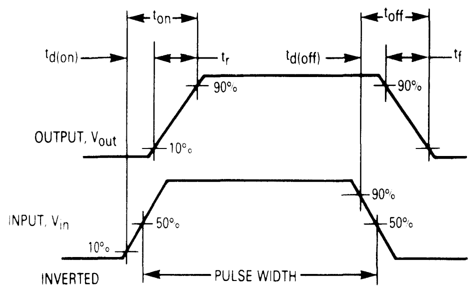
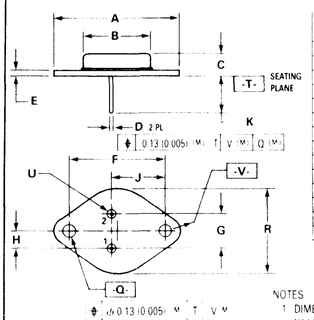


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA



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A	—	39.37	—	1.550
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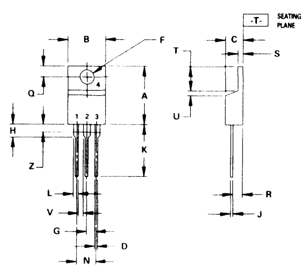
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 221A-04
TO-220AB



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J	0.36	0.55	0.014	0.022
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L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15		0.045	
Z	—	2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTM3N60
MTP3N55
MTP3N60

Designer's Data Sheet

Power Field Effect Transistor

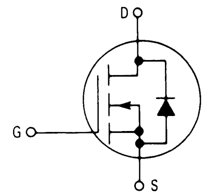
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS

TMOS POWER FETs
3 AMPERES
$r_{DS(on)}$ = 2.5 OHMS
550 and 600 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



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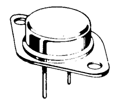
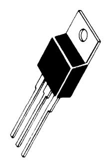


MTM3N60
CASE 1-06
TO-204AA



MTP3N55
MTP3N60
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP3N55	MTM3N60 / MTP3N60	Unit
Drain-Source Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 3 10		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating		Symbol	Value	Unit
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP3N55 MTM/MTP3N60	$V_{(BR)DSS}$	550 600	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	2.5	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc) (I_D = 1.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	9 7.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	180	
Fall Time		t_f	—	80	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	16 (Typ)	18	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	165 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

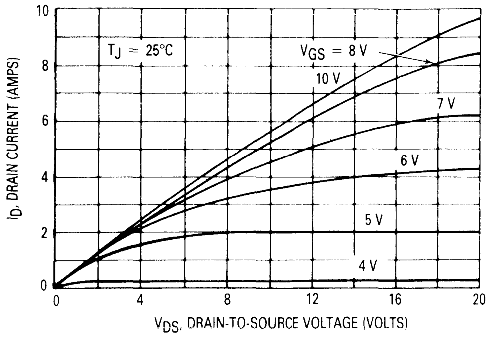


Figure 1. On-Region Characteristics

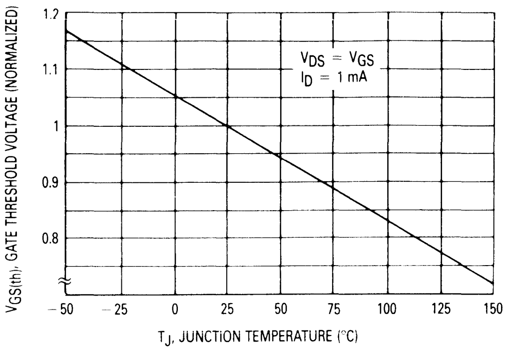


Figure 2. Gate-Threshold Voltage Variation With Temperature

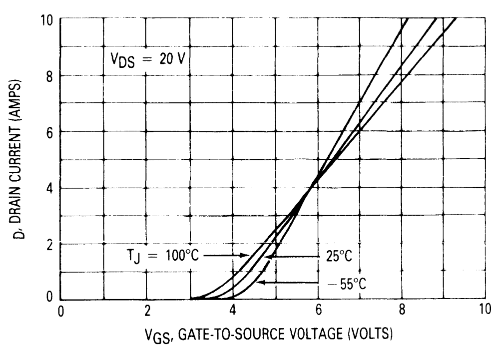


Figure 3. Transfer Characteristics

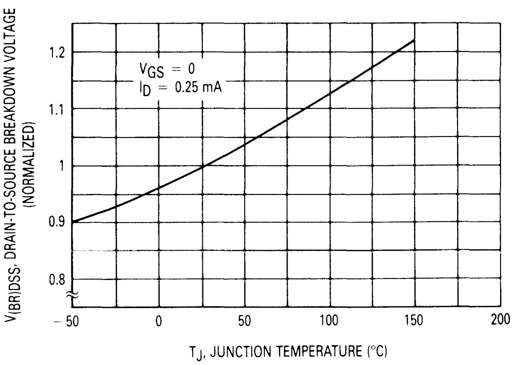


Figure 4. Breakdown Voltage Variation With Temperature

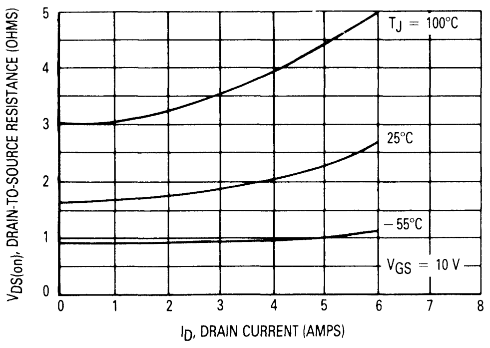


Figure 5. On-Resistance versus Drain Current

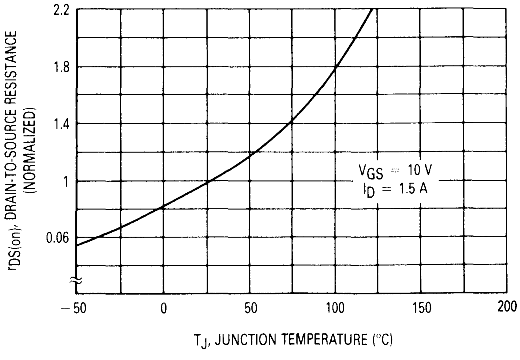


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

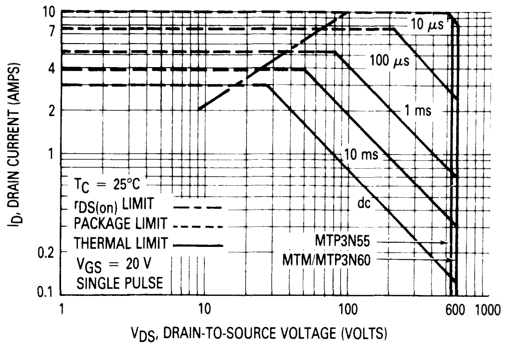


Figure 7. Maximum Rated Forward Biased Safe Operating Area

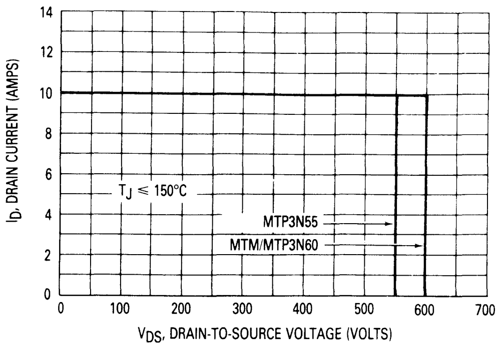


Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

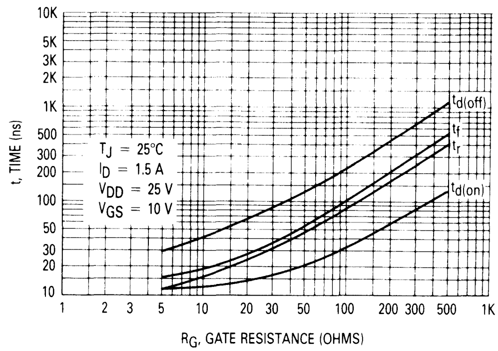


Figure 9. Resistive Switching Time Variation versus Gate Resistance

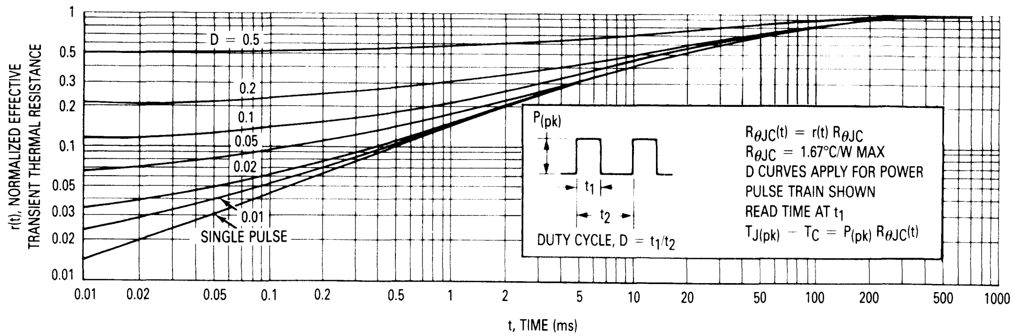


Figure 10. Thermal Response

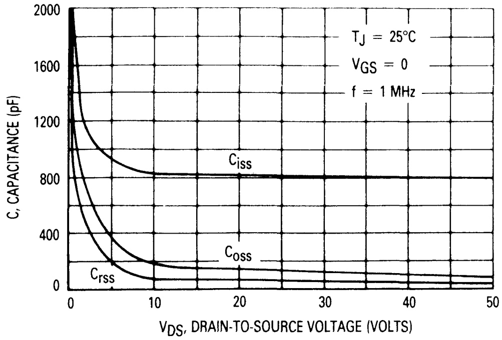


Figure 11. Capacitance Variation

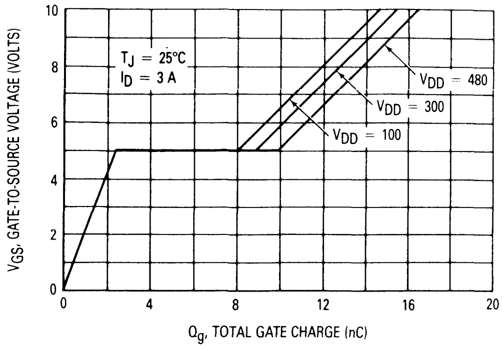


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

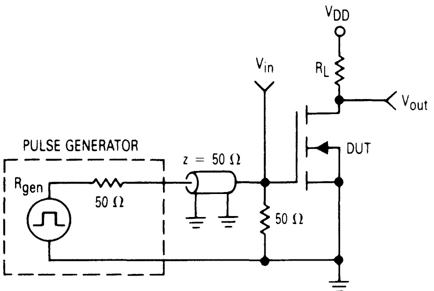


Figure 13. Switching Test Circuit

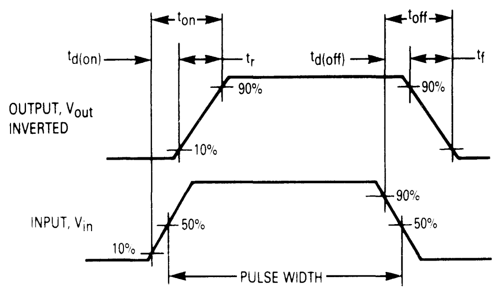
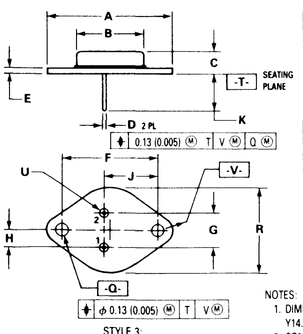


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

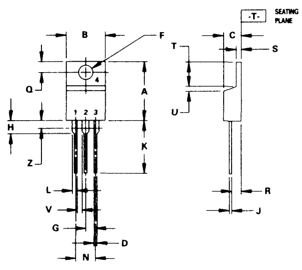


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTM3N75
MTM3N80
MTP3N75
MTP3N80

Designer's Data Sheet

Power Field Effect Transistor

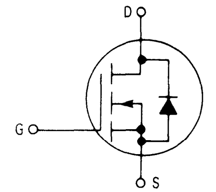
N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, high voltage power supplies and grid drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS

TMOS POWER FETs
3 AMPERES
$r_{DS(on)}$ = 7 OHMS
750 and 800 VOLTS

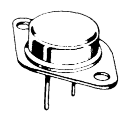


MAXIMUM RATINGS

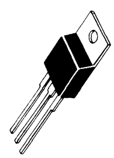
Rating	Symbol	MTM3N75 / MTP3N75	MTM3N80 / MTP3N80	Unit
Drain-Source Voltage	V_{DSS}	750	800	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	750	800	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3 8		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds		T_L	275	°C



MTM3N75
MTM3N80
CASE 1-06
TO-204AA



MTP3N75
MTP3N80
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP3N75		$V_{(BR)DSS}$	750	—	Vdc
MTM/MTP3N80			800	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	7	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc)		$V_{DS(on)}$	—	21	Vdc
(I_D = 1.5 Adc, T_J = 100°C)			—	21	
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	35 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1 (Typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	420 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

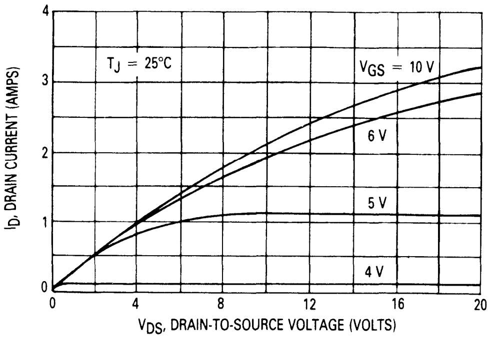


Figure 1. On-Region Characteristics

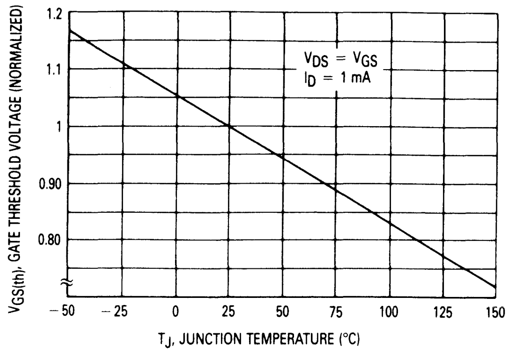


Figure 2. Gate-Threshold Voltage Variation With Temperature

3

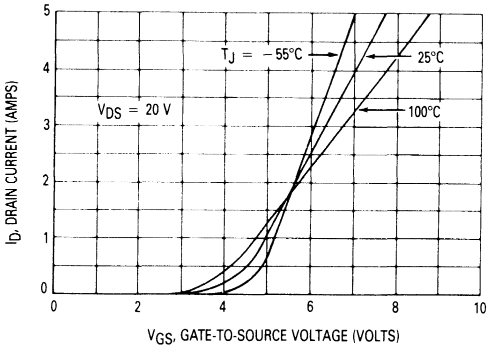


Figure 3. Transfer Characteristics

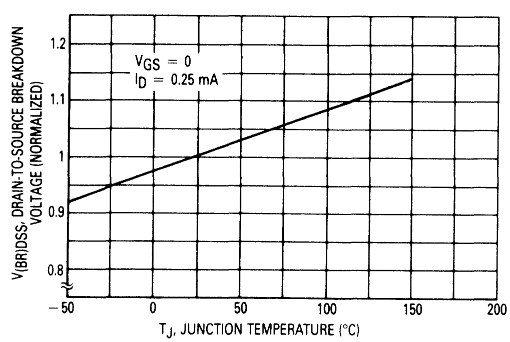


Figure 4. Breakdown Voltage Variation With Temperature

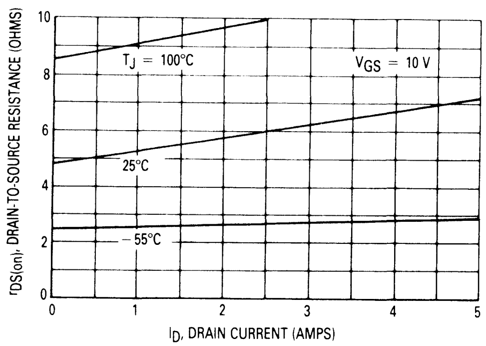


Figure 5. On-Resistance versus Drain Current

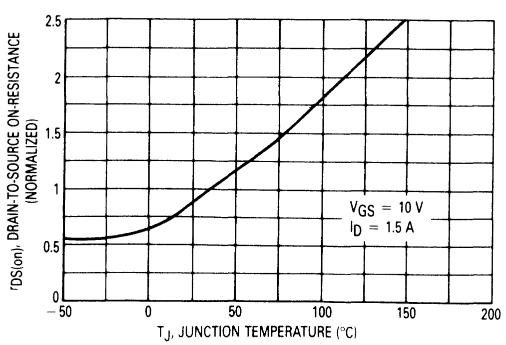


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

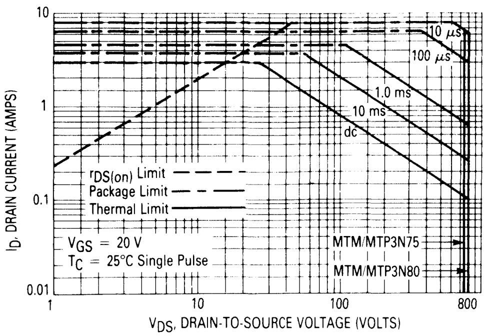


Figure 7. Maximum Rated Forward Biased Safe Operating Area

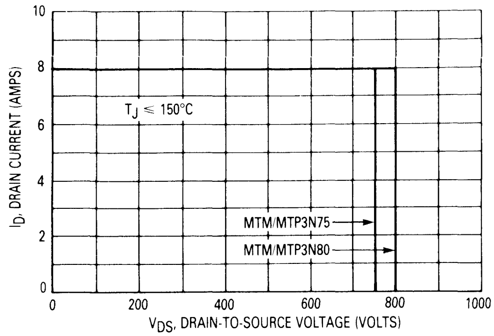


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

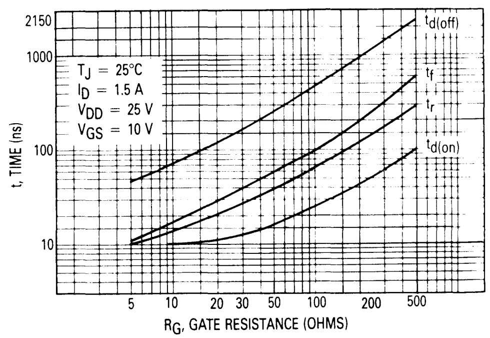


Figure 9. Resistive Switching Time Variation versus Gate Resistance

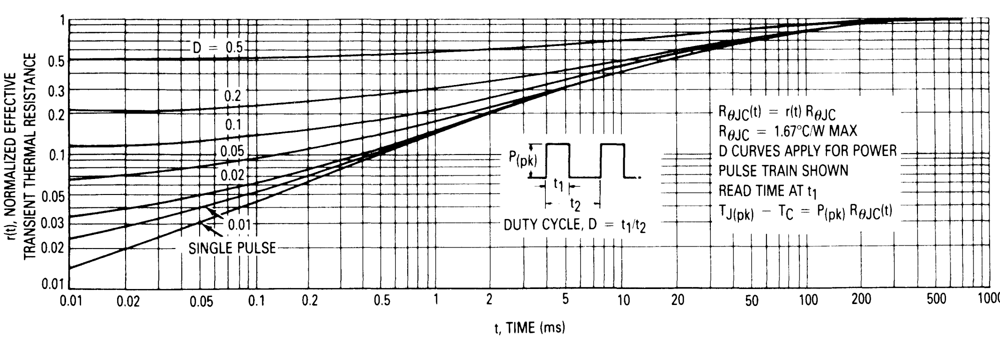


Figure 10. Thermal Response

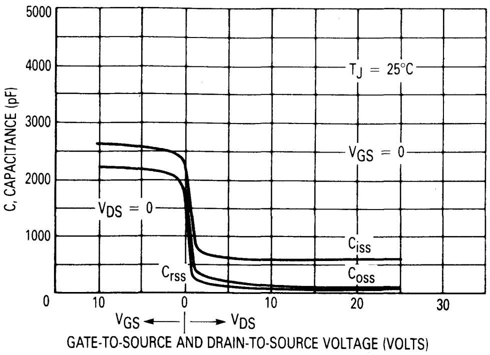


Figure 11. Capacitance Variation

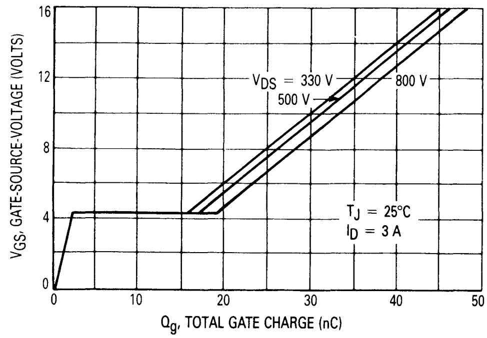


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

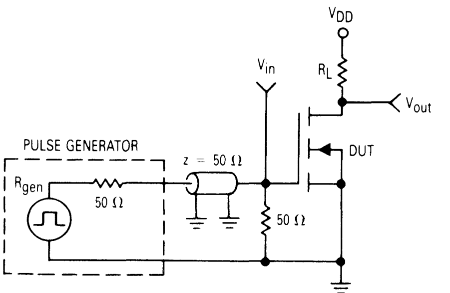


Figure 13. Switching Test Circuit

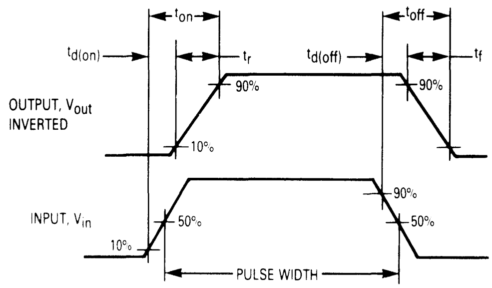
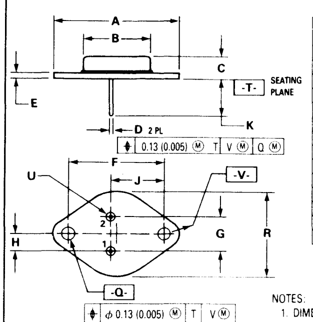


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

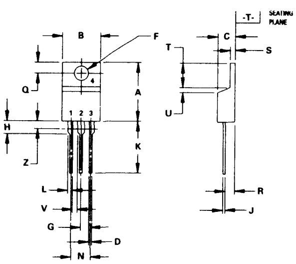


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 1-06
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

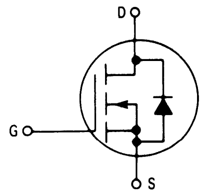
MTM3N95
MTM3N100
MTM4N85
MTM4N90

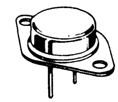
Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
3 and 4 AMPERES
$r_{DS(on)}$ = 4 OHMS
850, 900, 950
and 1000 VOLTS





CASE 1-06
TO-204AA

MAXIMUM RATINGS

Rating	Symbol	MTM 4N85	MTM 4N90	MTM 3N95	MTM 3N100	Unit
Drain-Source Voltage	V_{DSS}	850	900	950	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	850	900	950	1000	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40				Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 4 18		 3 16		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C
THERMAL CHARACTERISTICS						
Thermal Resistance Junction to Case	$R_{\theta JC}$	1				°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275				°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM4N85 MTM4N90 MTM3N95 MTM3N100	$V_{(BR)DSS}$	850 900 950 1000	— — — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.25 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc) (V_{GS} = 10 Vdc, I_D = 2 Adc)	MTM3N95/3N100 MTM4N85/4N90	$r_{DS(on)}$	— —	4 4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc) (I_D = 1.5 Adc, T_J = 100°C) (I_D = 4 Adc) (I_D = 2 Adc, T_C = 100°C)	MTM3N95/3N100 MTM4N85/4N90	$V_{DS(on)}$	— — — —	12 10 16 14	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A) (V_{DS} = 10 V, I_D = 2 A)	MTM3N95/3N100 MTM4N85/4N90	g_{fs}	2 2	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1500	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	60	

SWITCHING CHARACTERISTICS (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figs. 8 and 9.	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	40	
Turn-Off Delay Time		$t_{d(off)}$	—	250	
Fall Time		t_f	—	75	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 Vdc) See Figs. 6 and 10.	Q_g	55 (typ)	85	nC
Gate-Source Charge		Q_{gs}	30 (typ)	—	
Gate-Drain Charge		Q_{gd}	25 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figs. 15 and 16.	V_{SD}	1.1 (typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	200 (typ)	—	ns
Reverse Recovery Time		t_{rr}	1000 (typ)	—	ns

3

TYPICAL CHARACTERISTICS

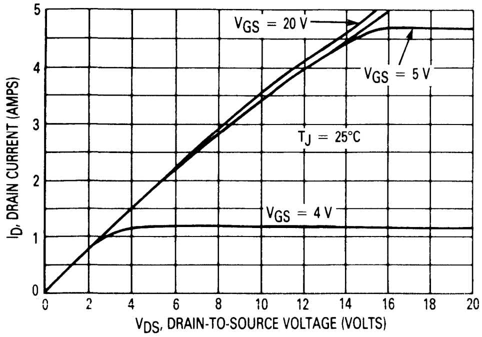


Figure 1. On-Region Characteristics

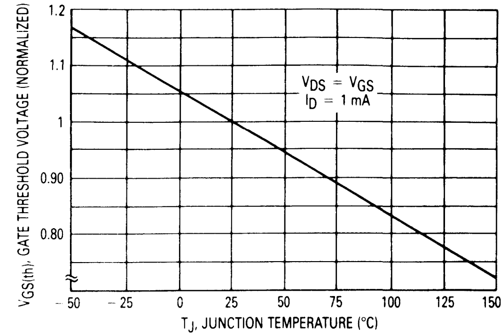


Figure 2. Gate-Threshold Voltage Variation with Temperature

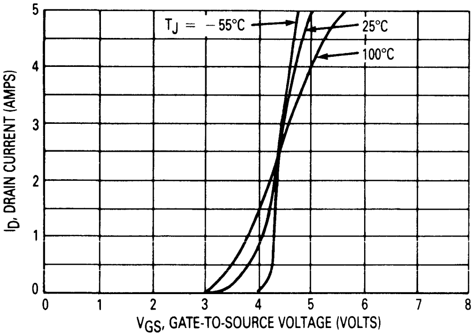


Figure 3. Transfer Characteristics

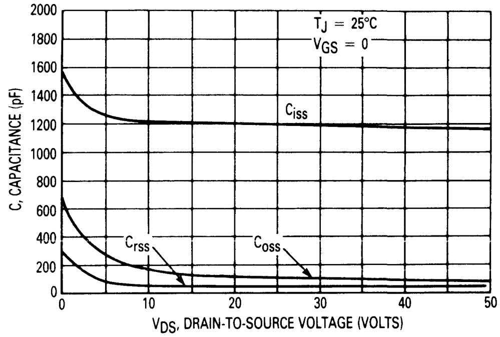


Figure 4. Capacitance Variation

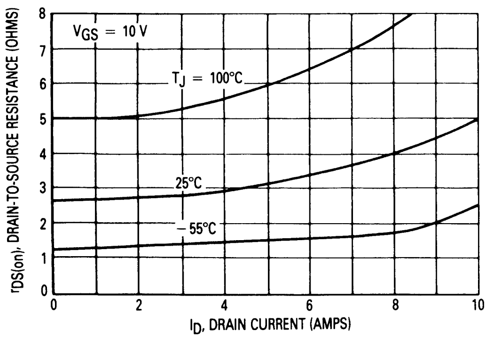


Figure 5. On-Resistance versus Drain Current

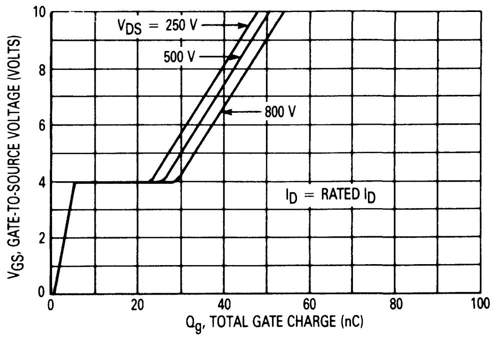


Figure 6. Gate Charge Variation

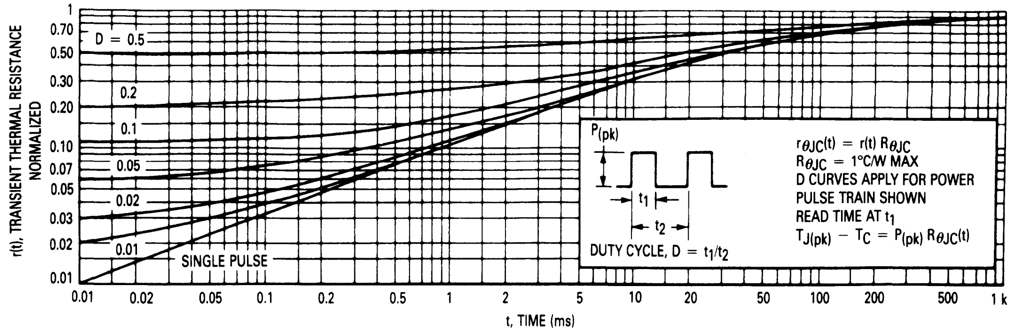


Figure 7. Thermal Response

RESISTIVE SWITCHING

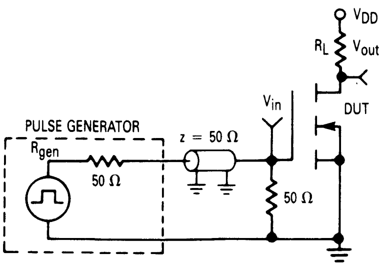


Figure 8. Switching Test Circuit

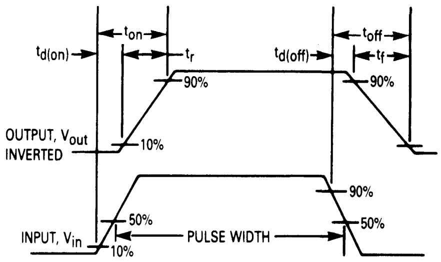
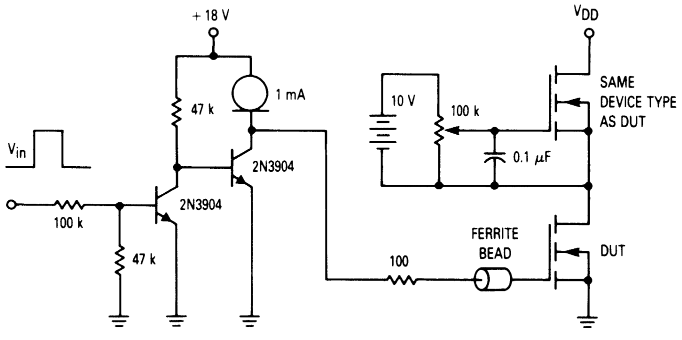


Figure 9. Switching Waveforms



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

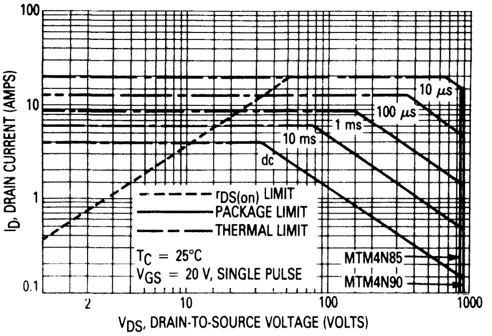


Figure 11. Maximum Rated Forward Biased Safe Operating Area

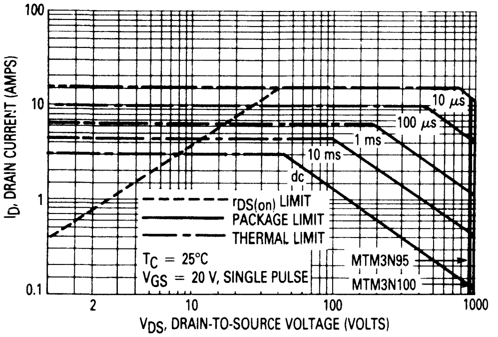


Figure 12. Maximum Rated Forward Biased Safe Operating Area

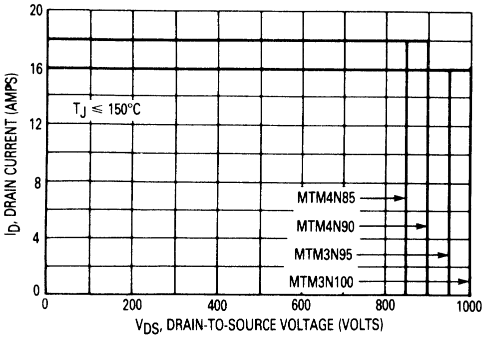


Figure 13. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

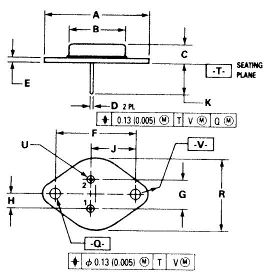
$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 11 and 12
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 7

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE EMITTER

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

CASE 1-06
TO-204AA

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM3P25
MTP3P25

Designer's Data Sheet

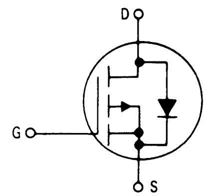
Power Field Effect Transistors

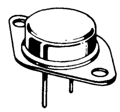
P-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

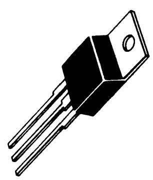
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$, and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
3 AMPERES
$r_{DS(on)}$ = 4 OHMS
250 VOLTS





MTM3P25
CASE 1-04
TO-204AA



MTP3P25
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM3P25	MTP3P25	Unit
Drain-Source Voltage	V_{DSS}	250		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250		Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous Pulsed	I_D I_{DM}	3 10		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient TO-204 TO-220	$R_{\theta JA}$	30 62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

(continued)

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage	$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)		2	4.5	
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)	$r_{DS(on)}$	—	4	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 3 Adc)		—	12	
(I_D = 1.5 Adc, T_J = 100°C)		—	10	
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A)	g_{FS}	1	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	750	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	30	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 12 and 13	$t_{d(on)}$	—	30	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	60	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	10 (Typ)	25	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	4 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	150 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-204)

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	

INTERNAL PACKAGE INDUCTANCE (TO-220)

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

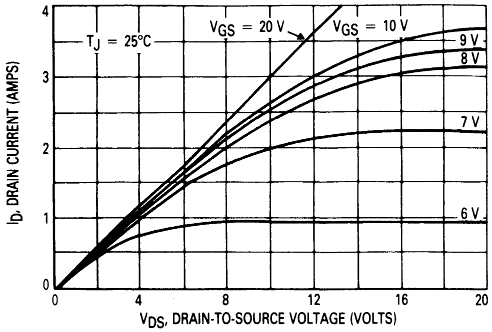


Figure 1. On-Region Characteristics

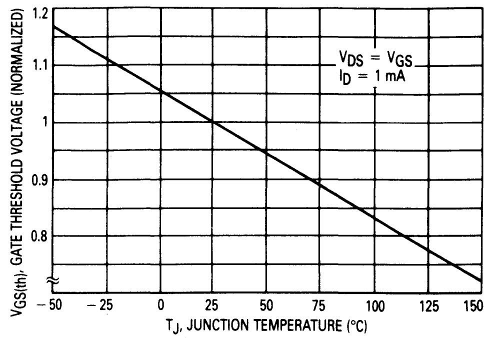


Figure 2. Gate-Threshold Voltage Variation with Temperature

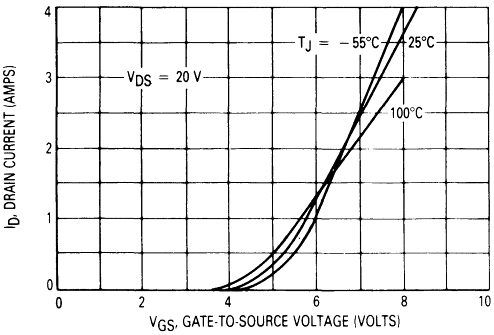


Figure 3. Transfer Characteristics

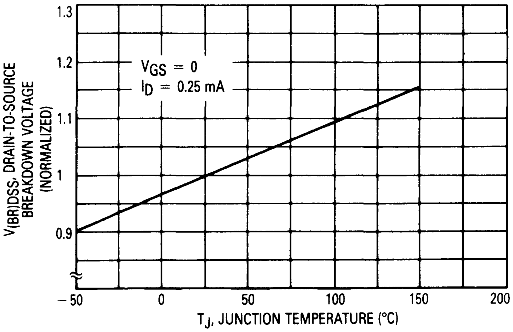


Figure 4. Breakdown Voltage Variation with Temperature

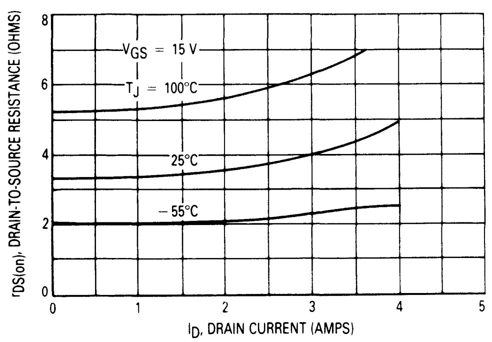


Figure 5. On-Resistance versus Drain Current

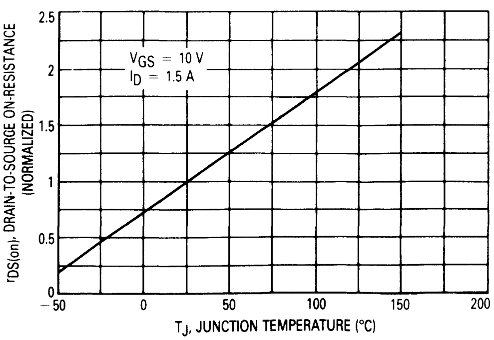


Figure 6. On-Resistance Variation with Temperature

SAFE OPERATING AREA INFORMATION

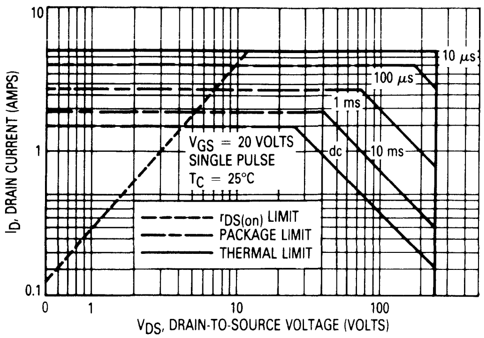


Figure 7. Maximum Rated Forward Bias Safe Operating Area

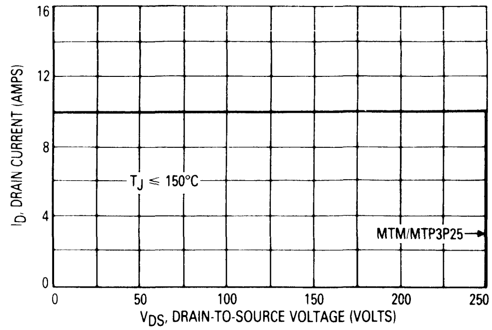


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

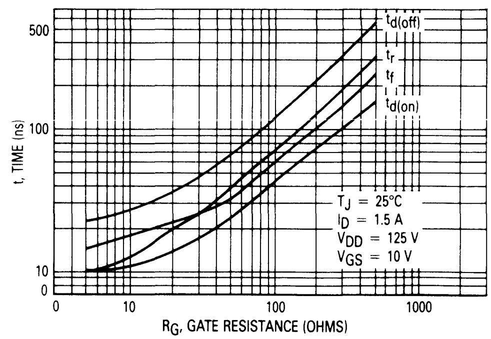


Figure 9. Resistive Switching Time Variation

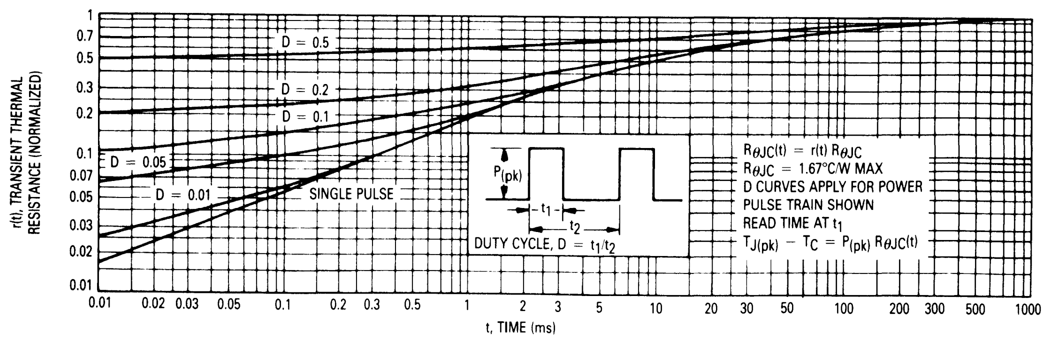


Figure 10. Thermal Response

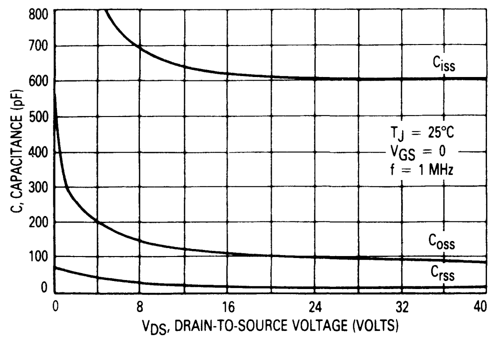


Figure 11. Capacitance Variation

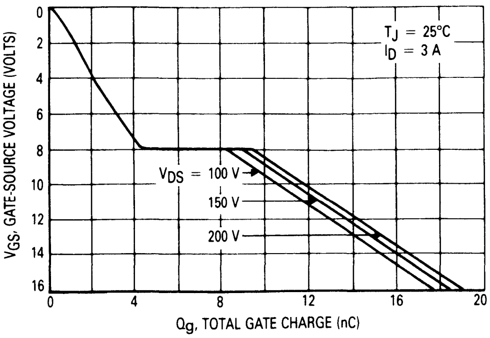


Figure 12. Gate Charge Variation

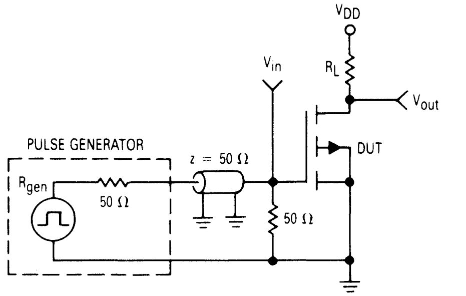


Figure 13. Switching Test Circuit

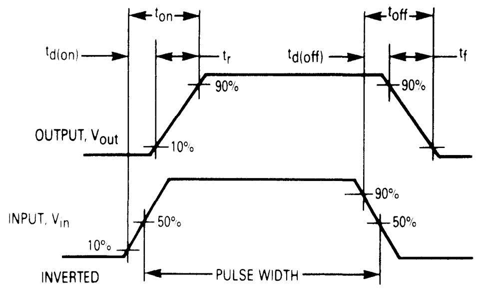
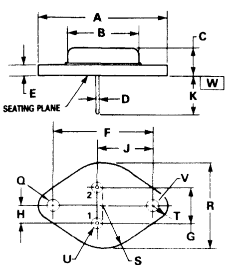


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

MTM3P25
CASE 1-04
TO-204AA

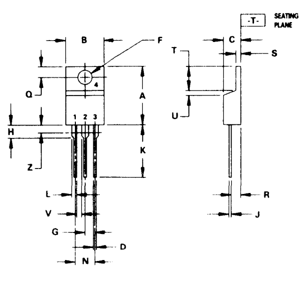


PIN 1. GATE
2. SOURCE
CASE DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTP3P25
CASE 221A-04
TO-220AB



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MTM4N45
MTM4N50
MTP4N45
MTP4N50

Designer's Data Sheet

Power Field Effect Transistor

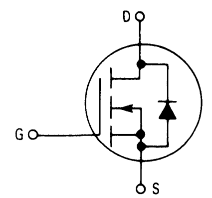
N-Channel Enhancement-Mode Silicon Gate TMOS

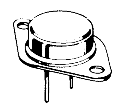
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

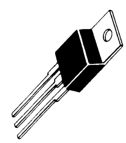
TMOS™

TMOS POWER FETs
4 AMPERES
$r_{DS(on)}$ = 1.5 OHMS
450 and 500 VOLTS





MTM4N45
MTM4N50
CASE 1-06
TO-204AA



MTP4N45
MTP4N50
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM4N45 / MTP4N45	MTM4N50 / MTP4N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 4 10		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP4N45 / MTM/MTP4N50	$V_{(BR)DSS}$	450 / 500	— / —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) / (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— / —	0.2 / 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) / T_J = 100°C	$V_{GS(th)}$	2 / 1.5	4.5 / 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)	$r_{DS(on)}$	—	1.5	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4 Adc) / (I_D = 2 Adc, T_J = 100°C)	$V_{DS(on)}$	— / —	7.5 / 6	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)	g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance	C_{oss}	—	300	
Reverse Transfer Capacitance	C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time	t_r	—	100	
Turn-Off Delay Time	$t_{d(off)}$	—	200	
Fall Time	t_f	—	100	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	27 (Typ)	32	nC
Gate-Source Charge	Q_{gs}	17 (Typ)	—	
Gate-Drain Charge	Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	210 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) / (Measured from the drain lead 0.25″ from package to center of die)	L_d	3.5 (Typ) / 4.5 (Typ)	— / —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

3

TYPICAL ELECTRICAL CHARACTERISTICS

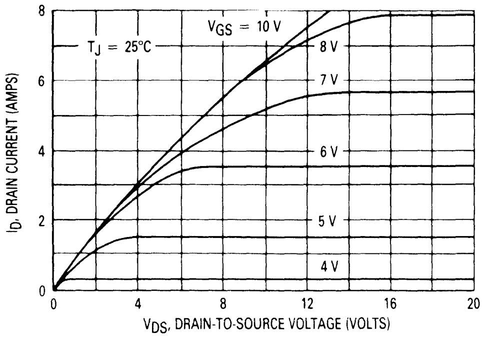


Figure 1. On-Region Characteristics

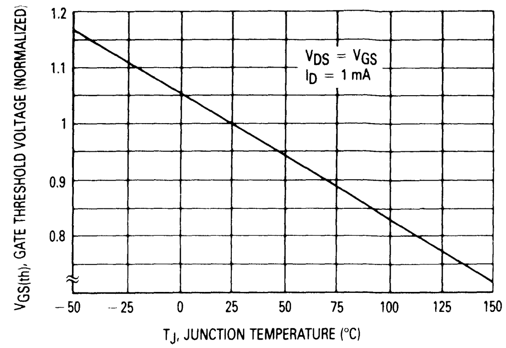


Figure 2. Gate-Threshold Voltage Variation With Temperature

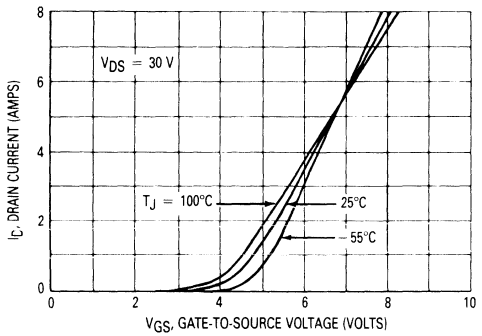


Figure 3. Transfer Characteristics

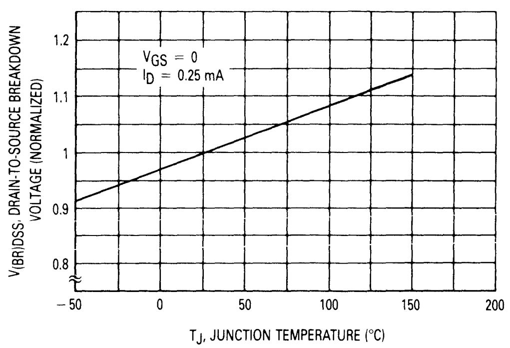


Figure 4. Breakdown Voltage Variation With Temperature

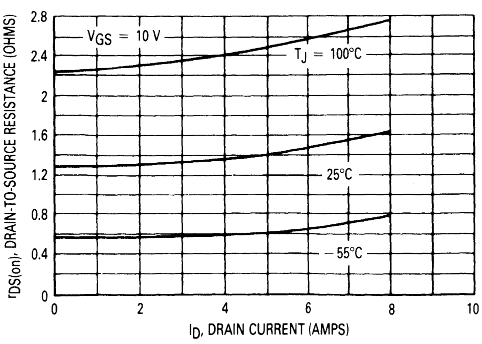


Figure 5. On-Resistance versus Drain Current

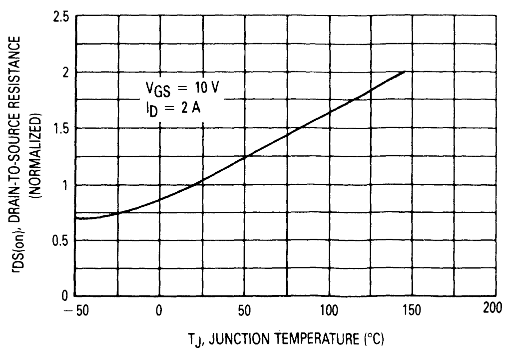


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

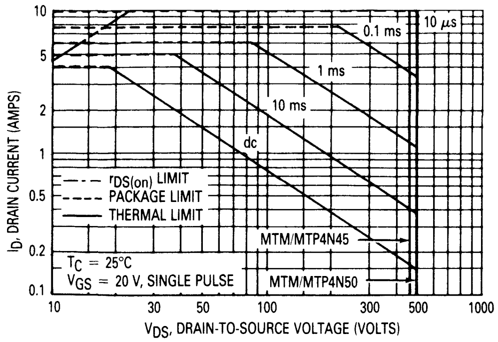


Figure 7. Maximum Rated Forward Biased Safe Operating Area

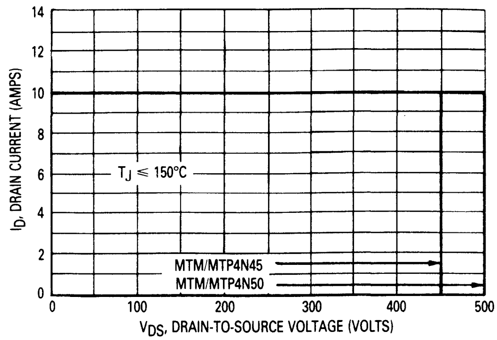


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

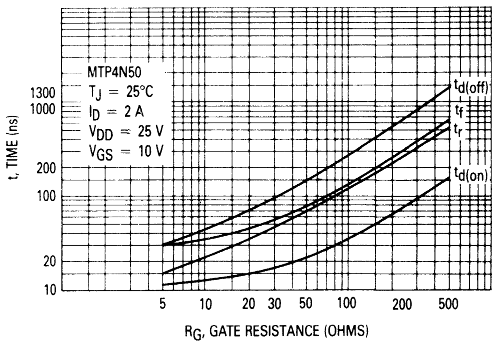


Figure 9. Resistive Switching Time Variation versus Gate Resistance

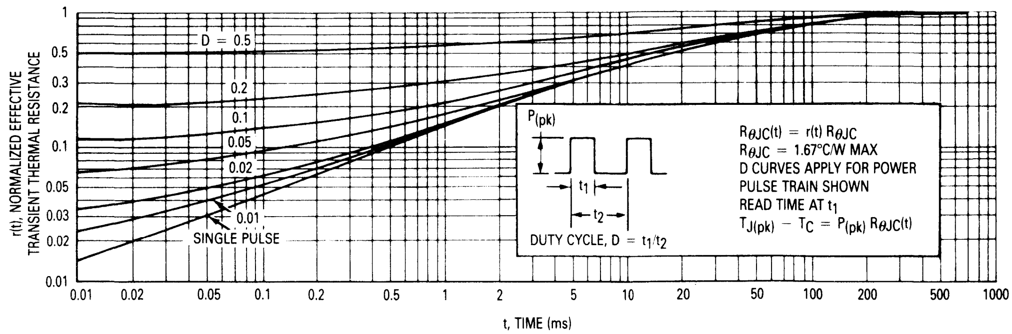


Figure 10. Thermal Response

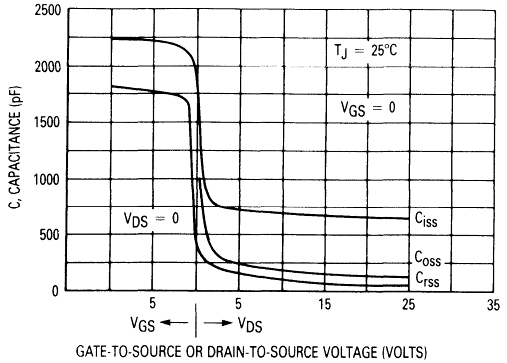


Figure 11. Capacitance Variation

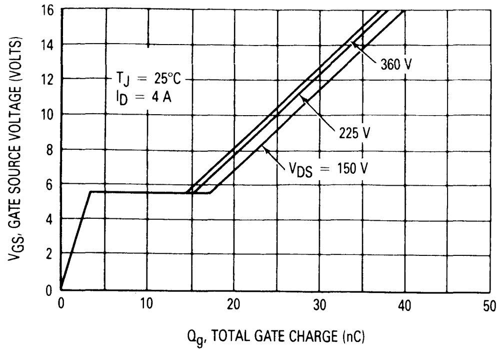


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

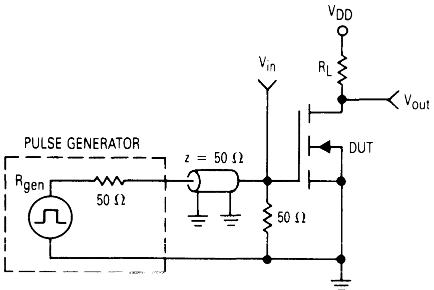


Figure 13. Switching Test Circuit

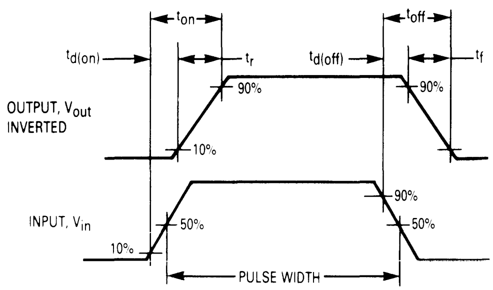
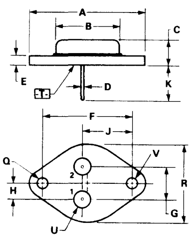


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

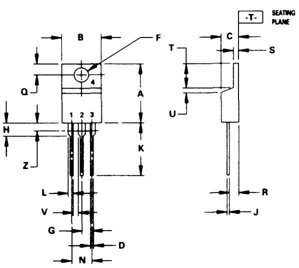


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
| ⌖ | 0.13 (0.005) Ⓜ | T | V Ⓜ |
FOR LEADS:
| ⌖ | 0.13 (0.005) Ⓜ | T | V Ⓜ | Q Ⓜ |
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 221A-04
TO-220AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTM5N35
MTM5N40
MTP5N35
MTP5N40

Designer's Data Sheet

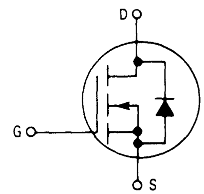
Power Field Effect Transistor

N-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 1 OHM
350 and 400 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

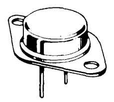


MAXIMUM RATINGS

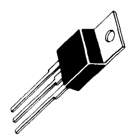
Rating	Symbol	MTM5N35 / MTP5N35	MTM5N40 / MTP5N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 5 12		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient — TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



MTM5N35
MTM5N40
CASE 1-06
TO-204AA



MTP5N35
MTP5N40
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP5N35 MTM/MTP5N40		$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	1	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	6.2 5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	27 (Typ)	32	nC
Gate-Source Charge		Q_{gs}	17 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	210 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

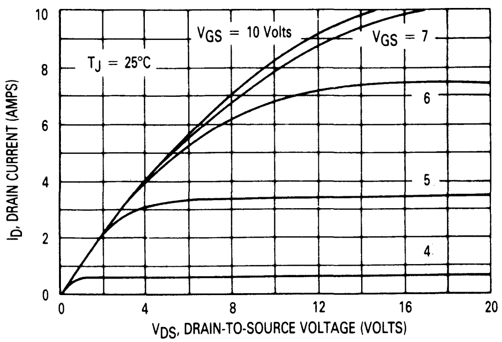

Figure 1. On-Region Characteristics

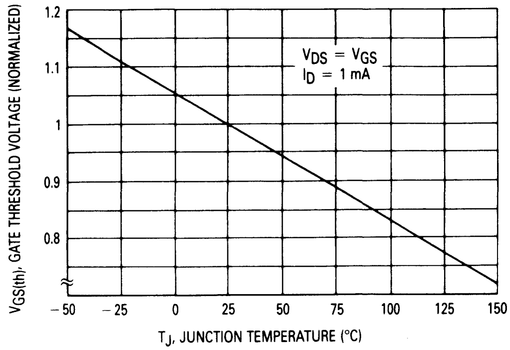

Figure 2. Gate-Threshold Voltage Variation With Temperature

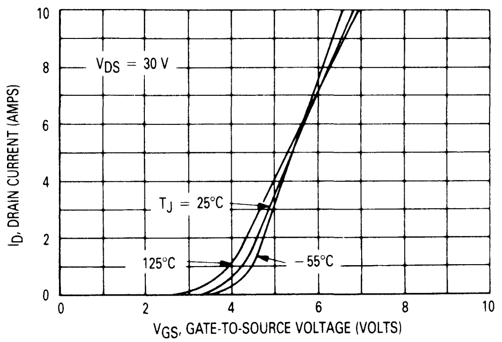

Figure 3. Transfer Characteristics

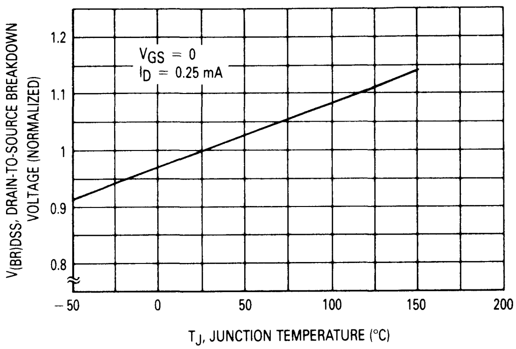

Figure 4. Breakdown Voltage Variation With Temperature

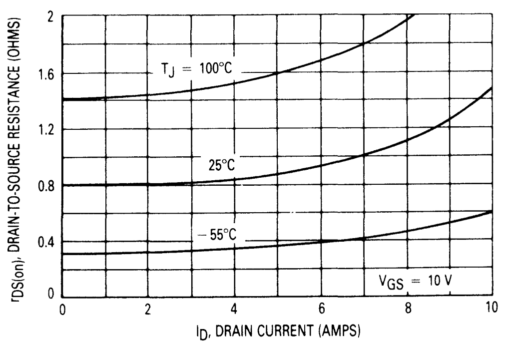

Figure 5. On-Resistance versus Drain Current

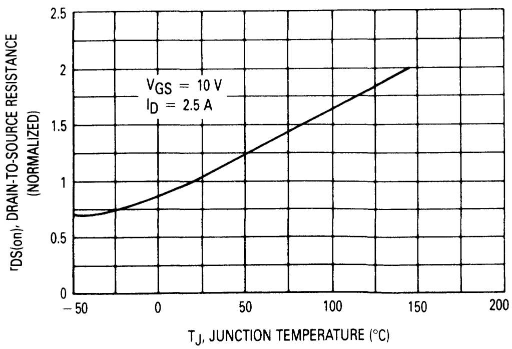

Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

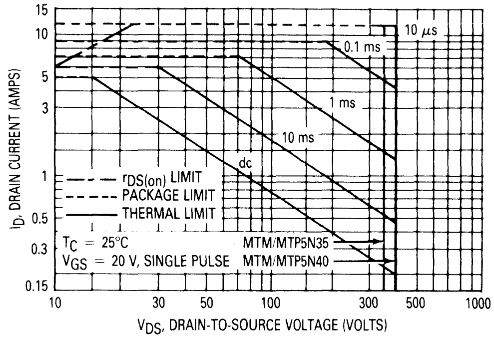


Figure 7. Maximum Rated Forward Biased Safe Operating Area

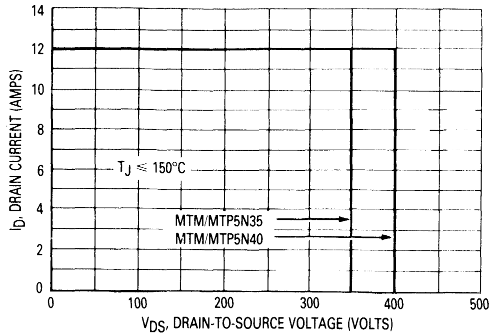


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

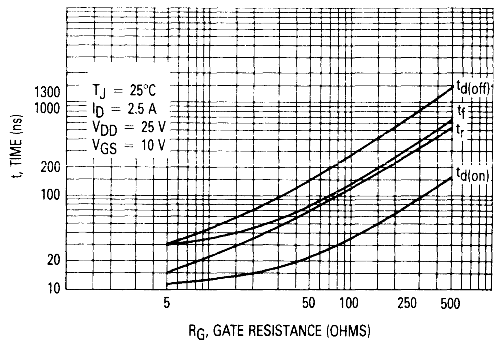


Figure 9. Resistive Switching Time Variation versus Gate Resistance

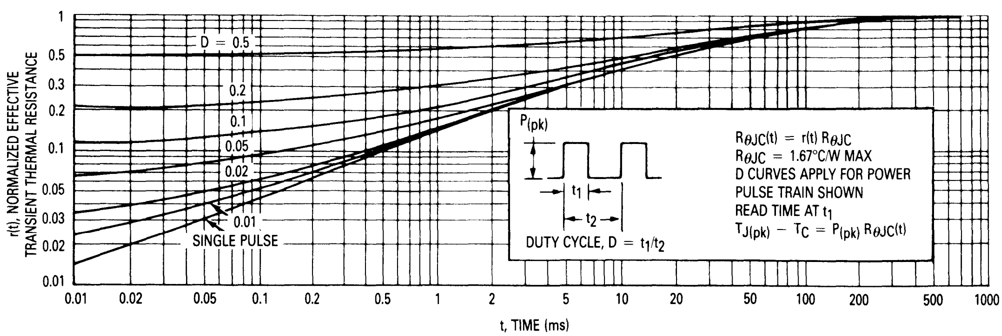


Figure 10. Thermal Response

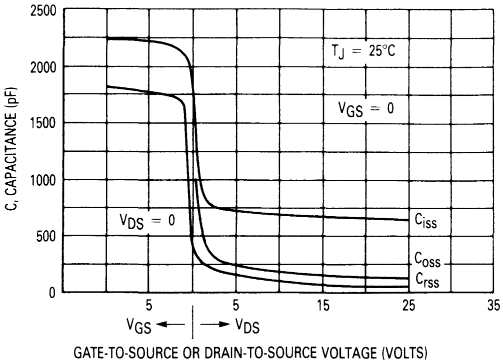


Figure 11. Capacitance Variation

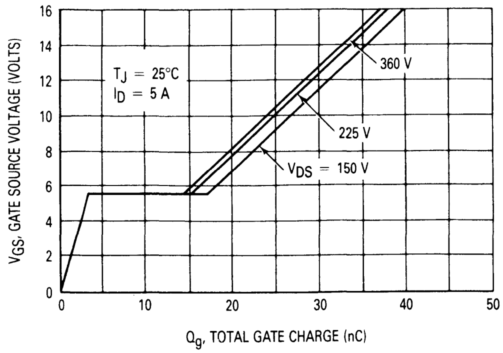


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

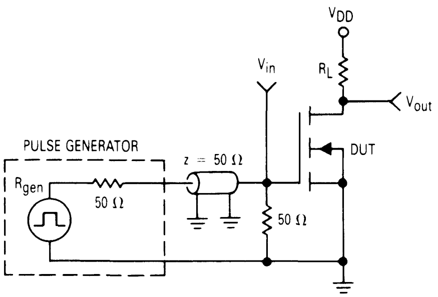


Figure 13. Switching Test Circuit

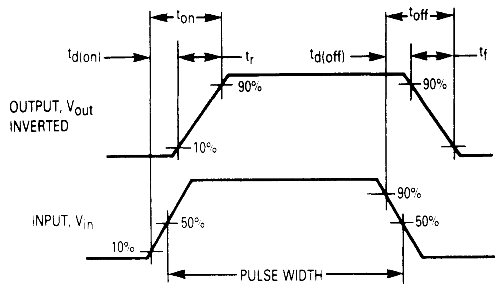
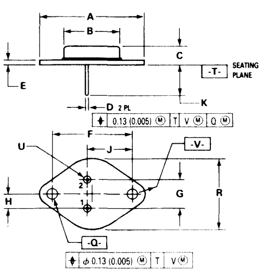


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-06
TO-204AA

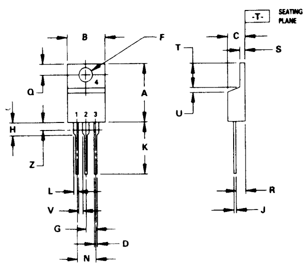


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTM5P18
MTM5P20
MTP5P18
MTP5P20

Designer's Data Sheet

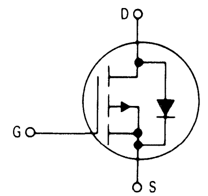
Power Field Effect Transistor

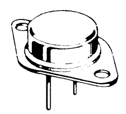
P-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 1 OHM
180 and 200 VOLTS

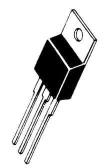
These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM5P18
MTM5P20
CASE 1-04
TO-204AA



MTP5P18
MTP5P20
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 5P18	5P20	Unit
Drain-Source Voltage	V_{DSS}	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	180	200	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current				Adc
Continuous	I_D	5		
Pulsed	I_{DM}	20		
Total Power Dissipation @ T_C = 25°C	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM/MTP5P18 MTM/MTP5P20	$V_{(BR)DSS}$	180 200	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	1	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	5 4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	250	
Reverse Transfer Capacitance		C_{rss}	—	75	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 11 and 12	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	60	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2 (Typ)	4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	(Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

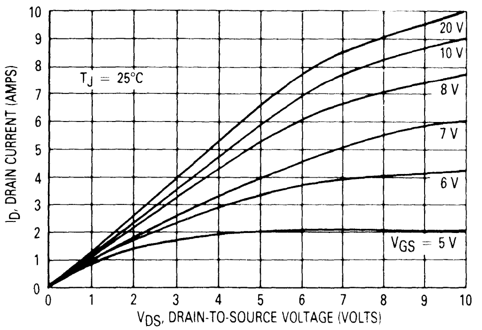


Figure 1. On-Region Characteristics

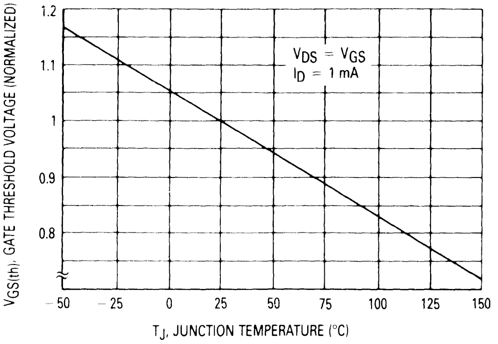


Figure 2. Gate-Threshold Voltage Variation With Temperature

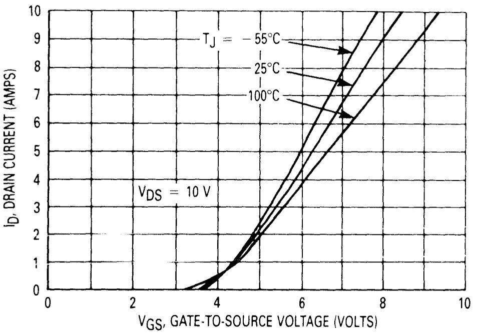


Figure 3. Transfer Characteristics

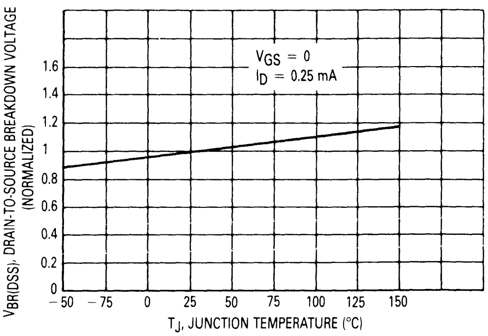


Figure 4. Normalized Breakdown Voltage versus Temperature

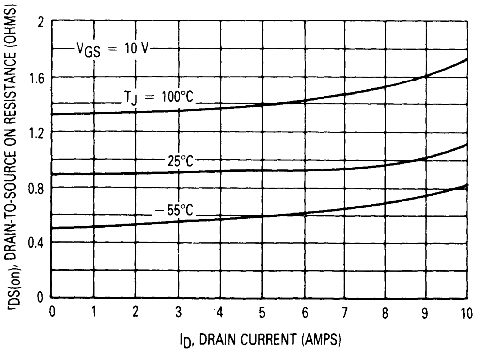


Figure 5. On-Resistance versus Drain Current

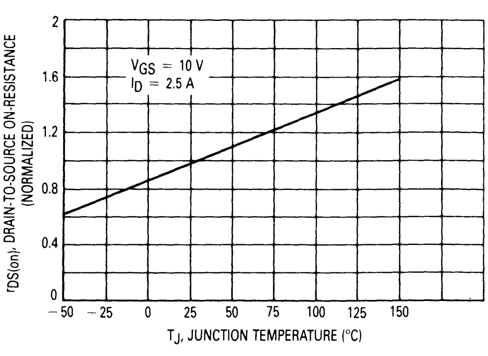


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

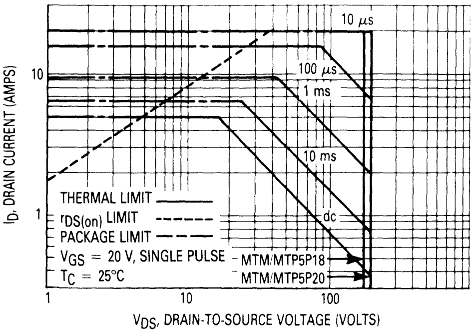


Figure 7. Maximum Rated Forward Biased Safe Operating Area

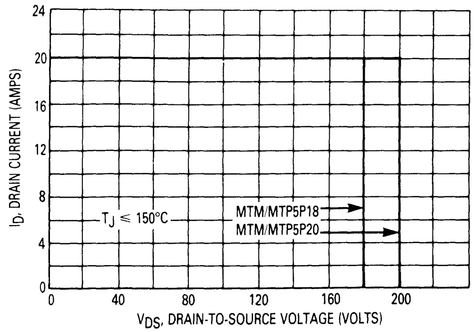


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 7 is based on a case temperature (T_C) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 6.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 9.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 7 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

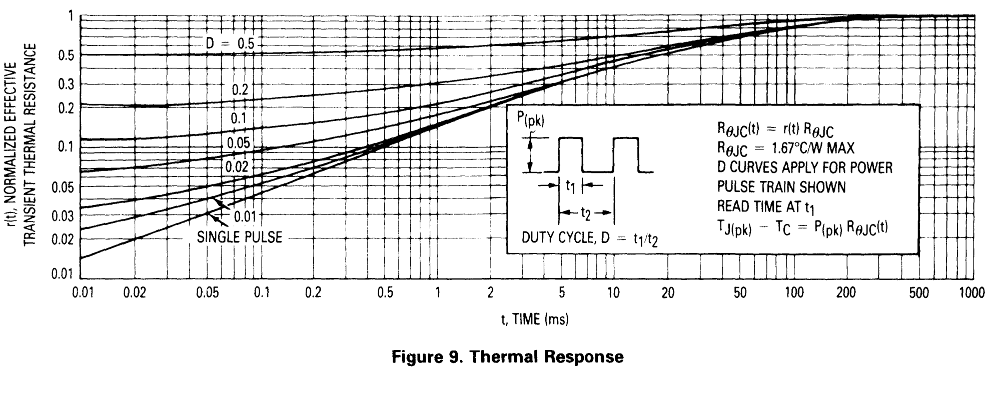


Figure 9. Thermal Response

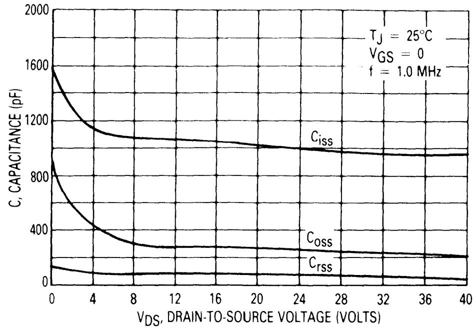


Figure 10. Capacitance Variation

3

RESISTIVE SWITCHING

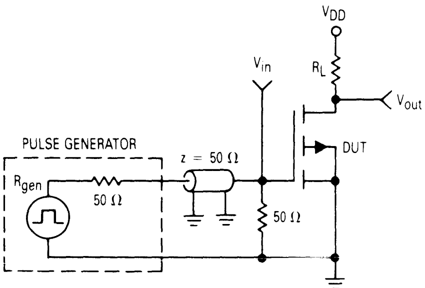


Figure 11. Switching Test Circuit

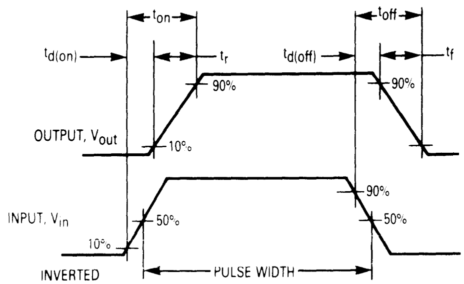
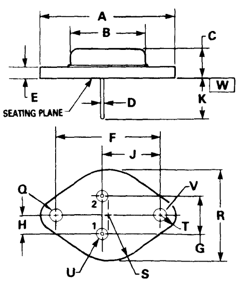


Figure 12. Switching Waveforms

OUTLINE DIMENSIONS

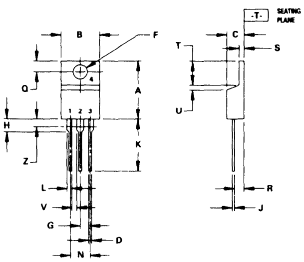


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
| ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
| ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM5P25
MTP5P25

Advance Information

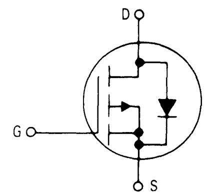
Power Field Effect Transistors

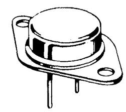
P-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and motor drives.

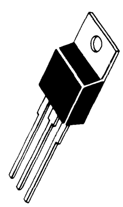
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$, and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 3 OHMS
250 VOLTS





MTM5P25
CASE 1-04
TO-204AA



MTP5P25
CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MTM5P25	MTP5P25	Unit
Drain-Source Voltage	V_{DSS}	250		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250		Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	5 15		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	MTM5P25	MTP5P25	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67		°C/W
Junction to Ambient	$R_{\theta JA}$	30	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

This document contains information on a new product. Specifications and information herein are subject to change without notice.

(continued)

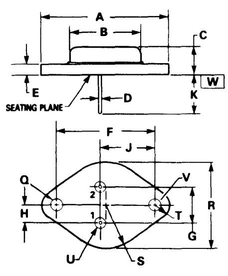
3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc)		$V_{DS(on)}$	—	16	Vdc
(I_D = 2.5 Adc, T_J = 100°C)			—	15	
Forward Transconductance (V_{DS} = 10 V, I_D = 2.5 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 14	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	250	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 11, 12 and 13	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	70	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 10	Q_g	15 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	3 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	180 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
| ⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
| ⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
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F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
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R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
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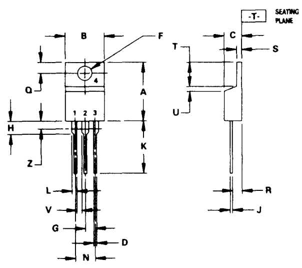

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
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Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

TYPICAL ELECTRICAL CHARACTERISTICS

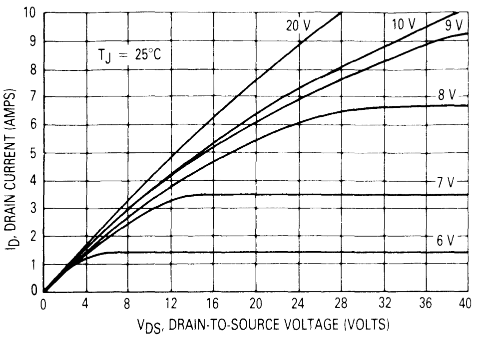

Figure 1. On-Region Characteristics

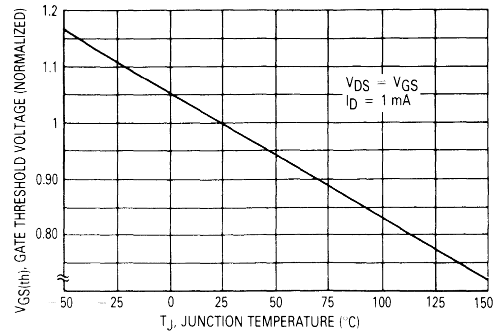

Figure 2. Gate-Threshold Voltage Variation With Temperature

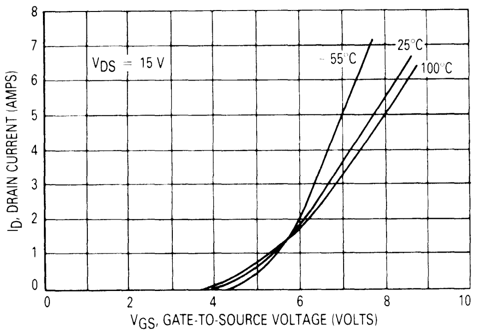

Figure 3. Transfer Characteristics

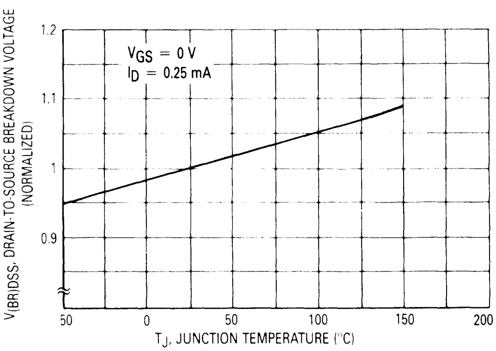

Figure 4. Drain-To-Source Breakdown Voltage Variation With Temperature

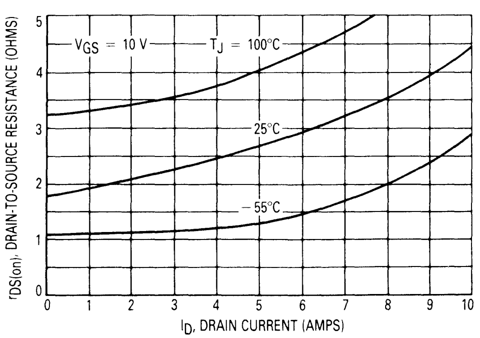

Figure 5. On-Resistance versus Drain Current

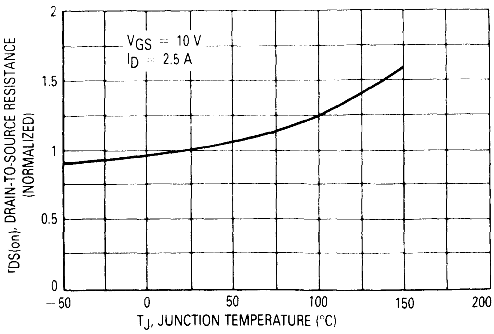

Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

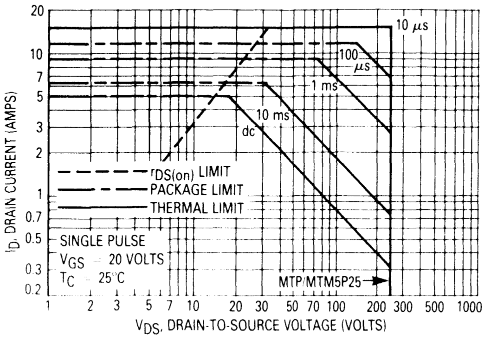

Figure 7. Maximum Rated Forward Bias Safe Operating Area

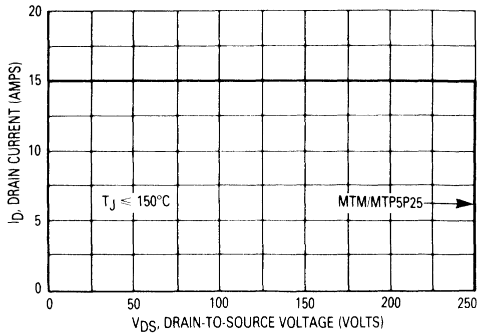

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

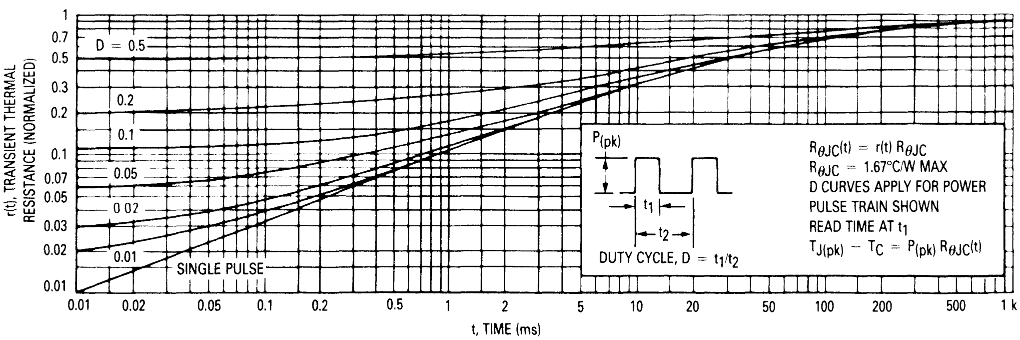

Figure 9. Thermal Response

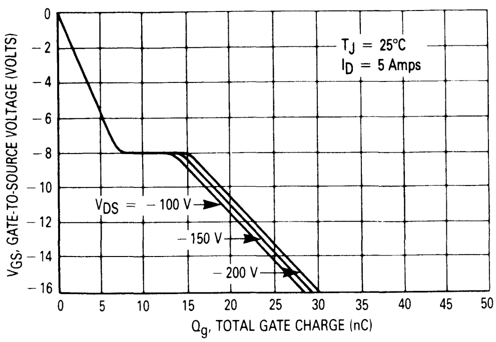

Figure 10. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

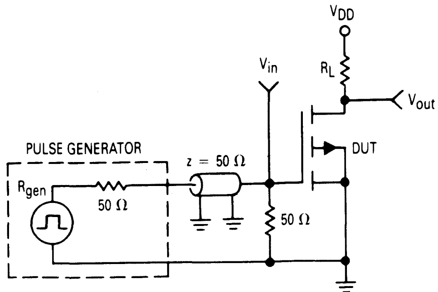

Figure 11. Switching Test Circuit

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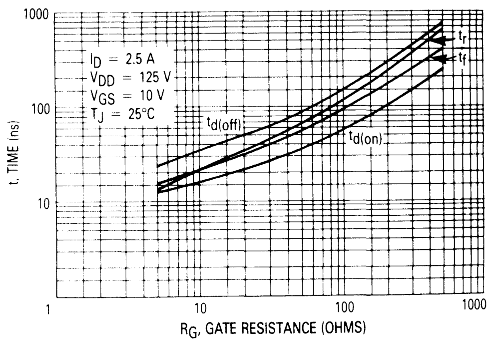


Figure 12. Resistive Switching versus Gate Resistance

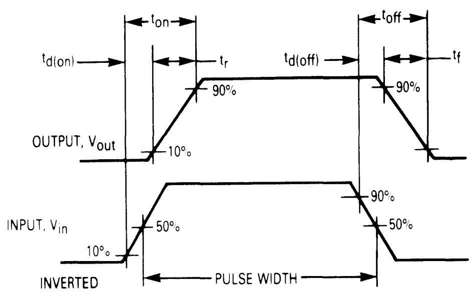


Figure 13. Switching Waveforms

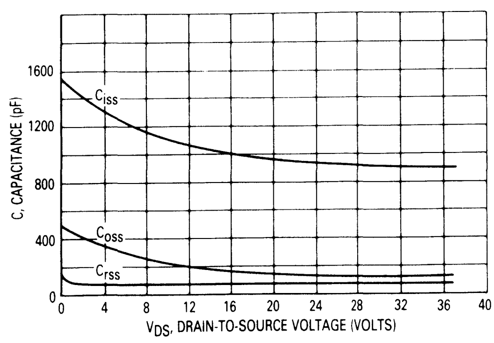


Figure 14. Capacitance Variation

MTM8N20
MTP8N20

Designer's Data Sheet

Power Field Effect Transistor

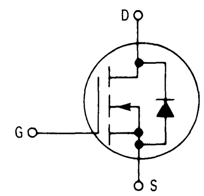
N-Channel Enhancement-Mode Silicon Gate TMOS

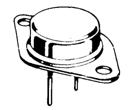
TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

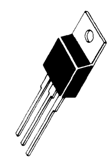
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.4 OHM
200 VOLTS





MTM8N20
CASE 1-04
TO-204AA



MTP8N20
CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP8N20		$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4 3.6	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	3	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V)	Q_g	15 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

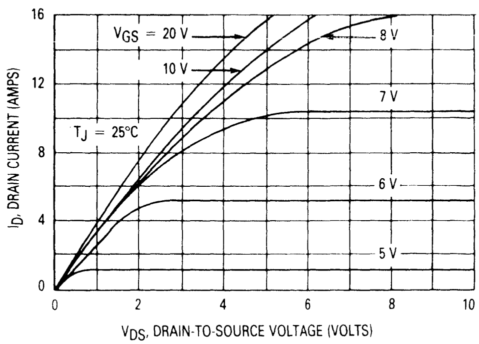


Figure 1. On-Region Characteristics

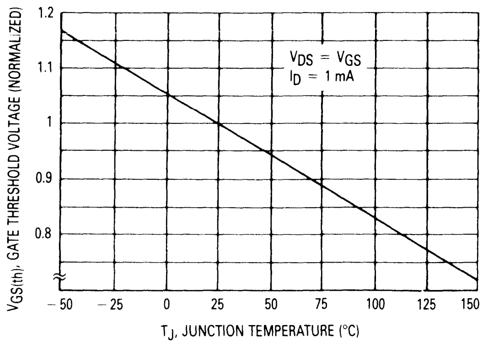


Figure 2. Gate-Threshold Voltage Variation With Temperature

3

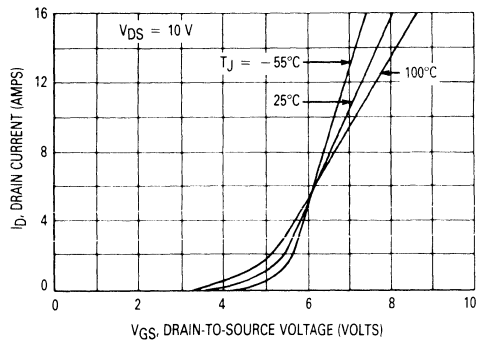


Figure 3. Transfer Characteristics

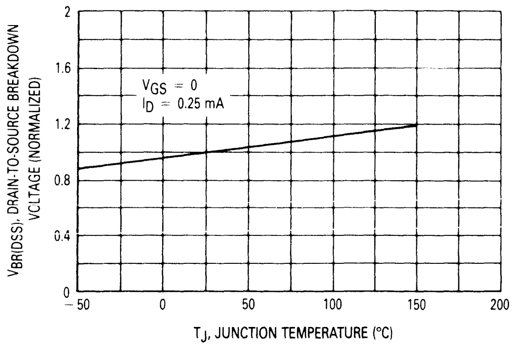


Figure 4. Breakdown Voltage Variation With Temperature

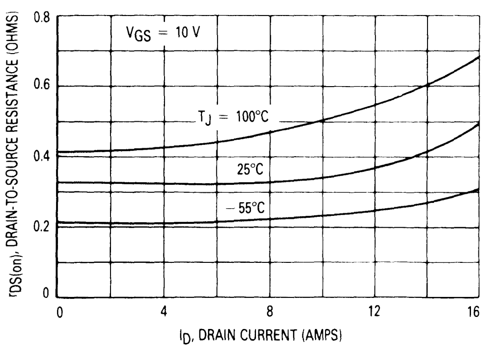


Figure 5. On-Resistance versus Drain Current

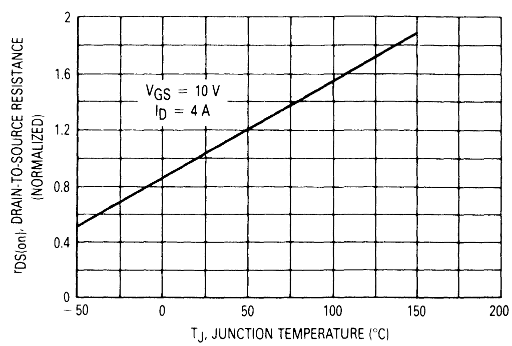


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

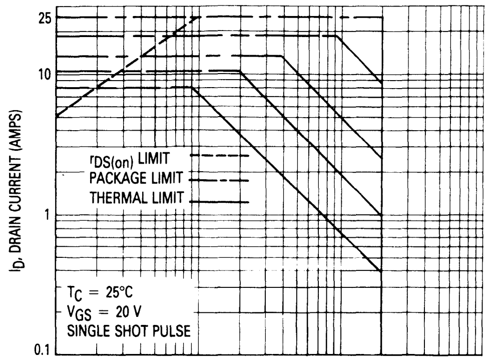


Figure 7. Maximum Rated Forward Biased Safe Operating Area

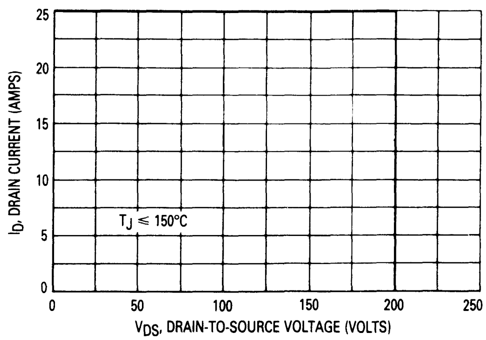


Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

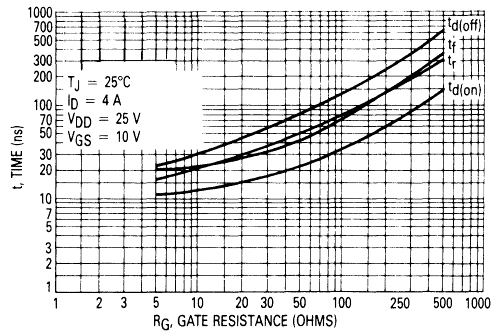


Figure 9. Resistive Switching Time versus Gate Resistance

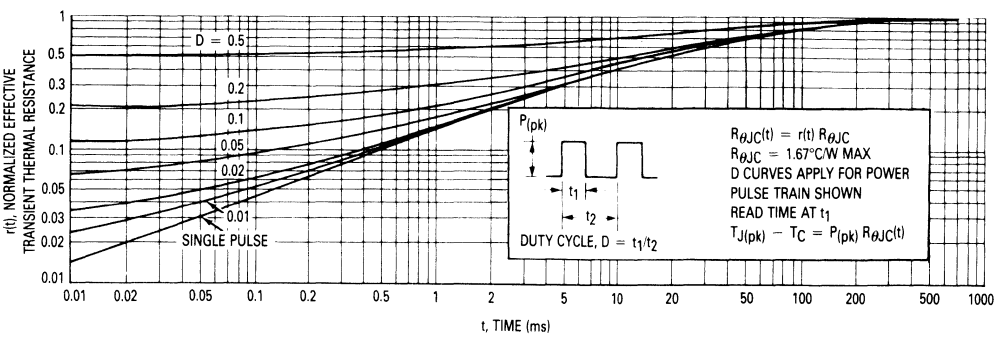


Figure 10. Thermal Response

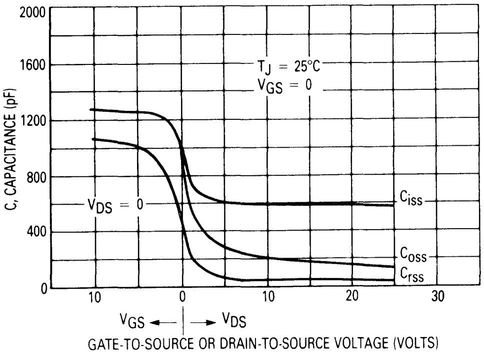


Figure 11. Capacitance Variation

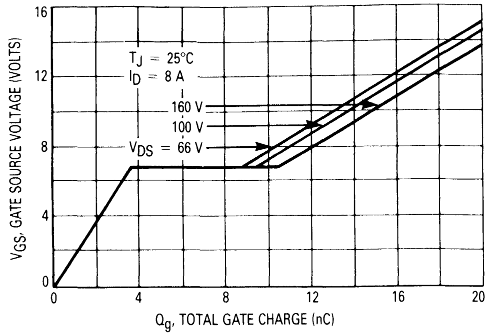


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

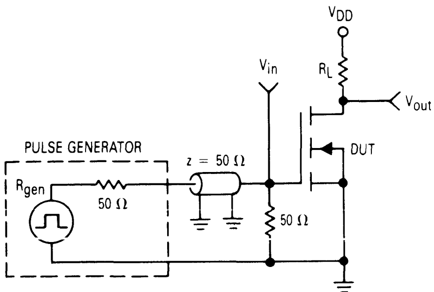


Figure 13. Switching Test Circuit

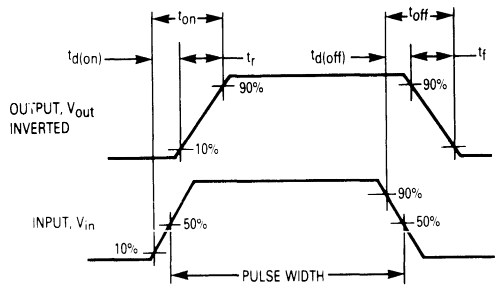
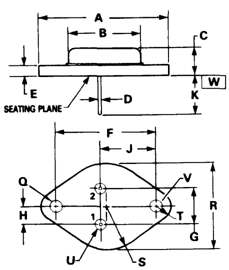


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

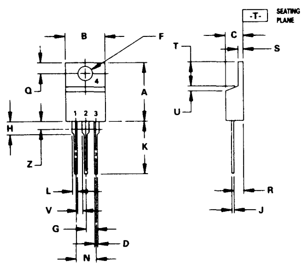


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   | ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
   | ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MTM8P08
MTM8P10
MTP8P08
MTP8P10

Designer's Data Sheet

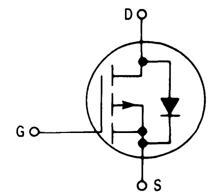
Power Field Effect Transistor

P-Channel Enhancement-Mode
Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.4 OHM
80 and 100 VOLTS



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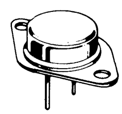
MAXIMUM RATINGS

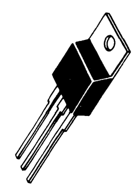
Rating	Symbol	MTM or MTP 8P08	MTM or MTP 8P10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 25		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic		Symbol	Value	Unit
Thermal Resistance Junction to Case		$R_{\theta JC}$	1.67	°C/W
Junction to Ambient	TO-204	$R_{\theta JA}$	30	
	TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds		T_L	275	°C



MTM8P08
MTM8P10
CASE 1-04
TO-204AA



MTP8P08
MTP8P10
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM/MTP8P08 MTM/MTP8P10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.8 3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	180	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	80	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V)	Q_g	33 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	16 (Typ)	—	
Gate-Drain Charge		Q_{gd}	17 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	3 (Typ)	6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

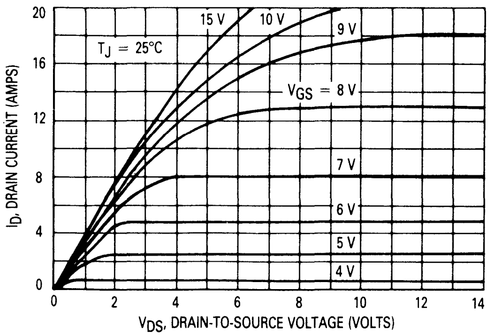


Figure 1. On-Region Characteristics

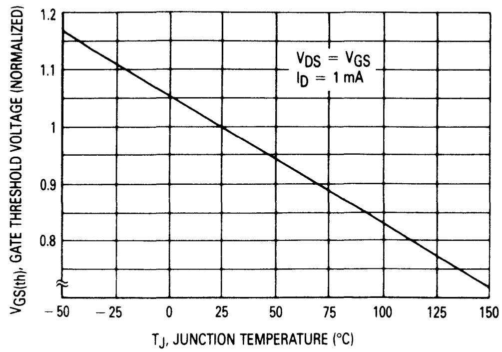


Figure 2. Gate-Threshold Voltage Variation With Temperature

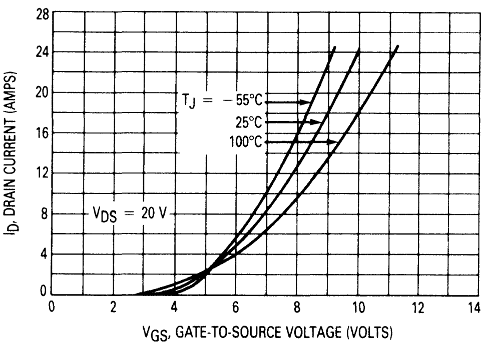


Figure 3. Transfer Characteristics

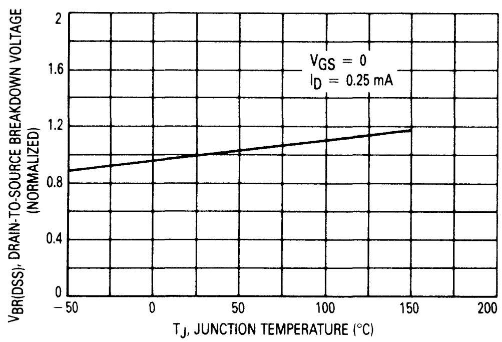


Figure 4. Normalized Breakdown Voltage versus Temperature

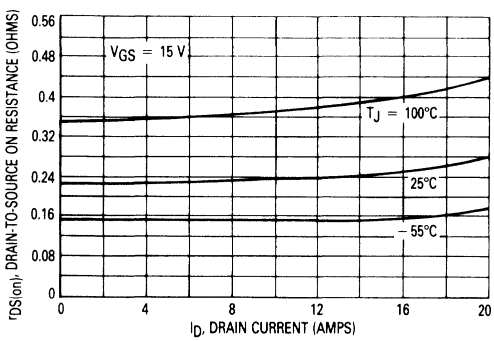


Figure 5. On-Resistance versus Drain Current

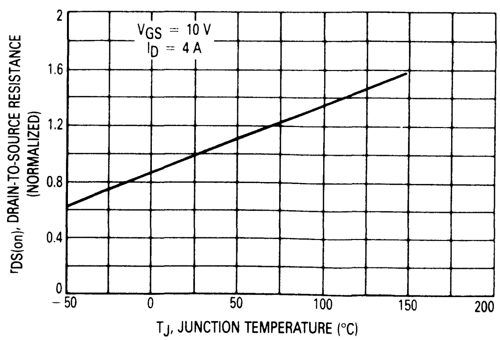


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

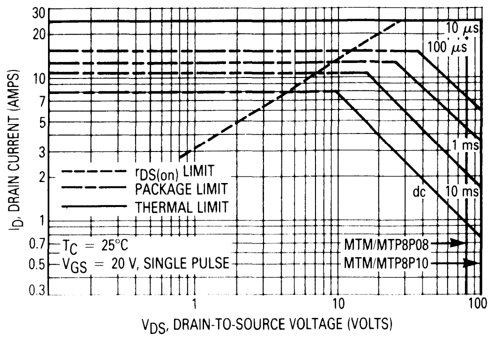

Figure 7. Maximum Rated Forward Biased Safe Operating Area

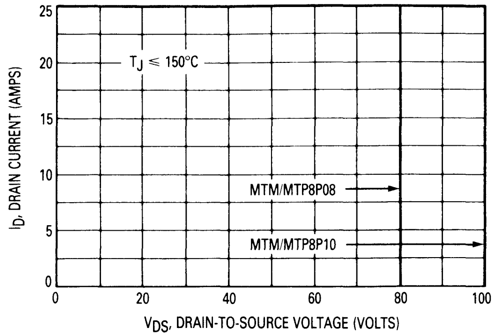

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

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The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

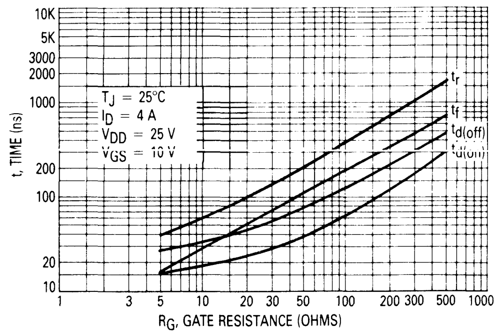


Figure 9. Resistive Switching Time Variation versus Gate Resistance

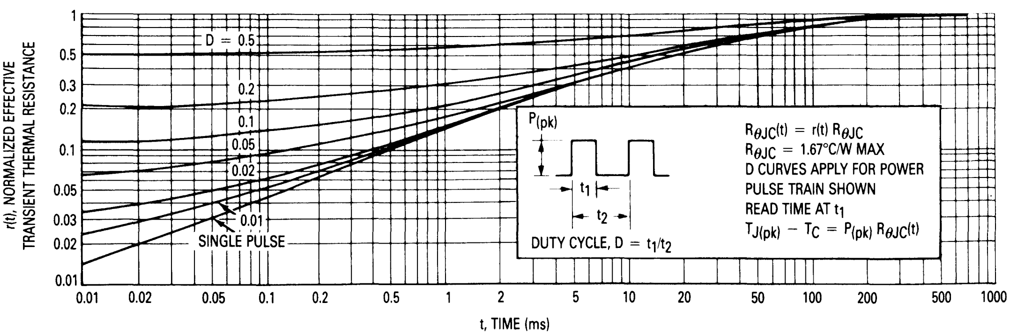


Figure 10. Thermal Response

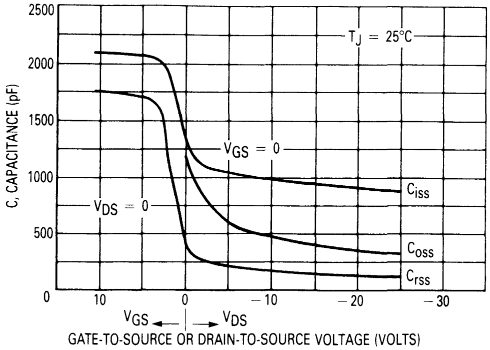


Figure 11. Capacitance Variation

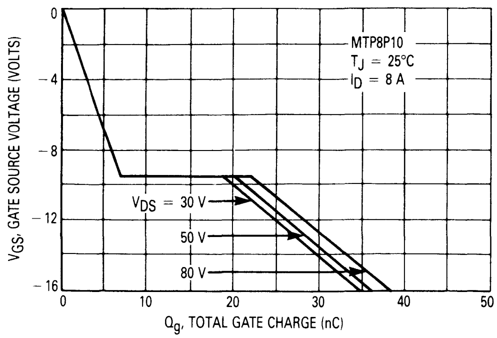


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

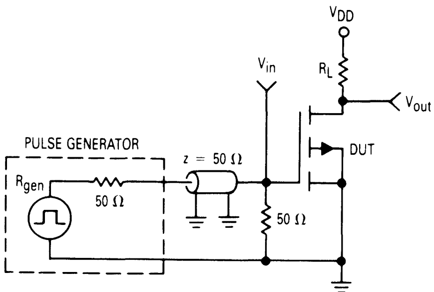


Figure 13. Switching Test Circuit

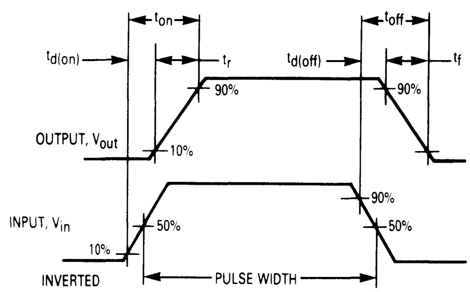
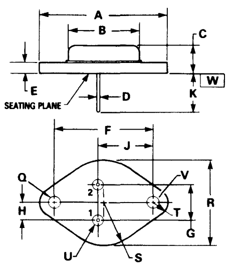


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

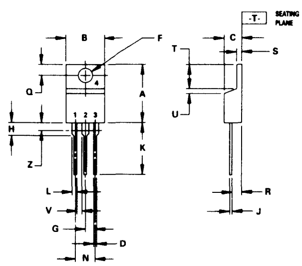


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MTM8P25
MTP8P25

Advance Information

Power Field Effect Transistors

P-Channel Enhancement-Mode Silicon Gate TMOS

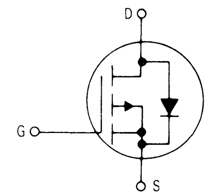
TMOS

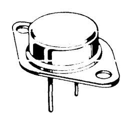
TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 2 OHMS
250 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and motor drives.

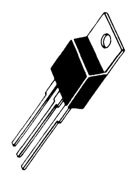
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designers Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$, and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

3





MTM8P25
CASE 1-04
TO-204AA



MTP8P25
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM8P25	MTP8P25	Unit
Drain-Source Voltage	V_{DSS}	250		Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250		Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 24		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	MTM8P25	MTP8P25	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67		°C/W
Junction to Ambient	$R_{\theta JA}$	30	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275		°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Characteristic	Symbol	Min	Max	Unit
Gate Threshold Voltage	$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)		2	4.5	
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	$r_{DS(on)}$	—	2	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 8 Adc)		—	18	
(I_D = 4 Adc, T_J = 100°C)		—	16	
Forward Transconductance (V_{DS} = 10 V, I_D = 4 A)	g_{FS}	3	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 14	C_{iss}	—	2200	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	300	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

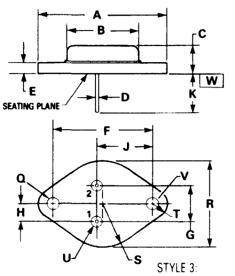
Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 11, 12 and 13	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	160	
Fall Time		t_f	—	90	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 10	Q_g	20 (Typ)	40	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	3 (Typ)	5	Vdc
Forward Turn-On Time		t_{on}	200 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

OUTLINE DIMENSIONS



NOTES:
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   ⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
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   ⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
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C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
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J	16.89 BSC		0.665 BSC	
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Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
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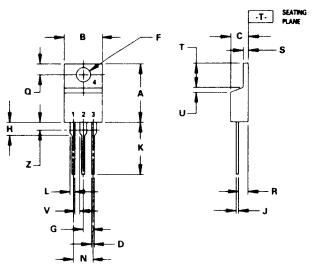
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
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D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
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L	1.15	1.39	0.045	0.055
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R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
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2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

CASE 221A-04
TO-220AB

TYPICAL ELECTRICAL CHARACTERISTICS

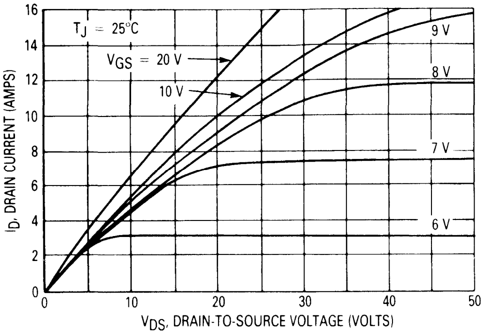


Figure 1. On-Region Characteristics

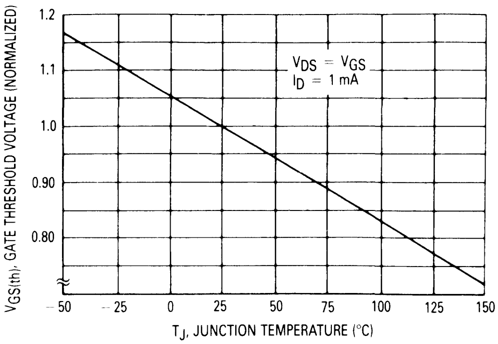


Figure 2. Gate-Threshold Voltage Variation With Temperature

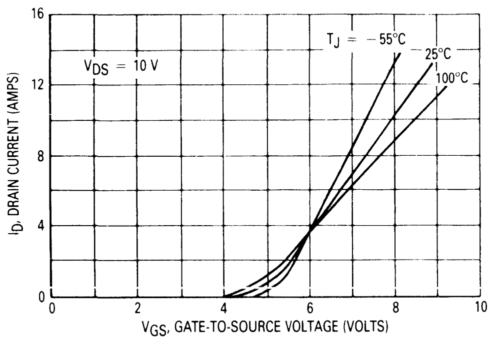


Figure 3. Transfer Characteristics

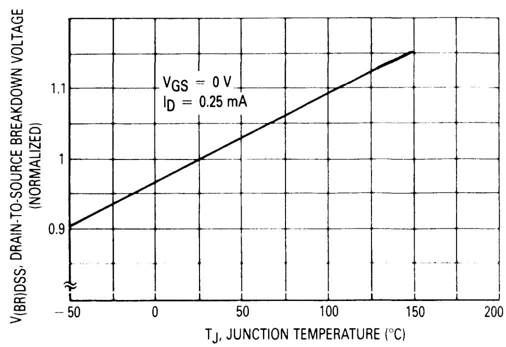


Figure 4. Normalized Breakdown Voltage versus Temperature

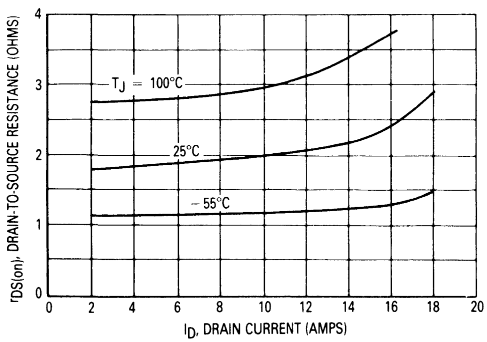


Figure 5. On-Resistance versus Drain Current

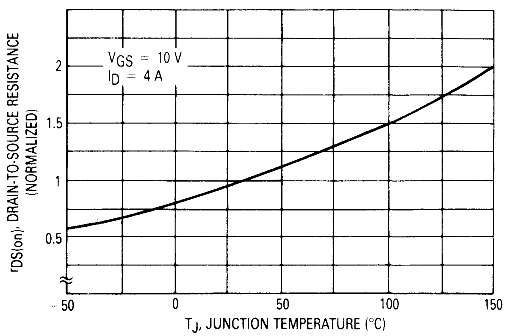


Figure 6. Normalized On-Resistance versus Temperature

SAFE OPERATING AREA INFORMATION

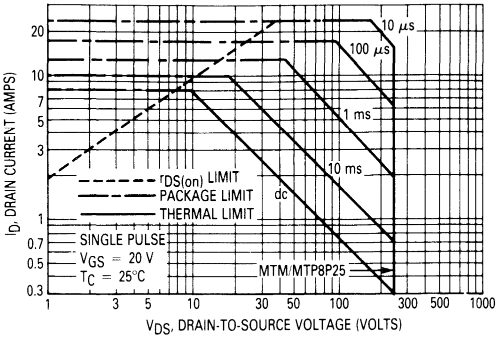


Figure 7. Maximum Rated Forward Bias Safe Operating Area

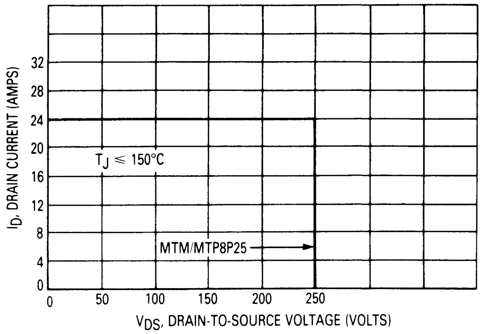


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

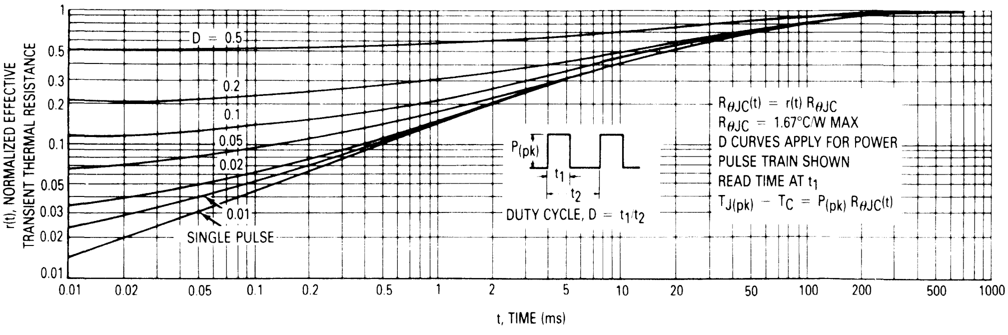


Figure 9. Thermal Response

RESISTIVE SWITCHING

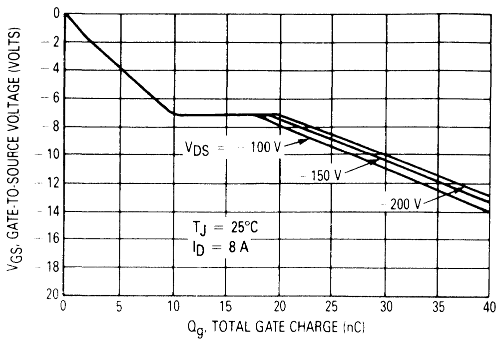


Figure 10. Gate Charge versus Gate-To-Source Voltage

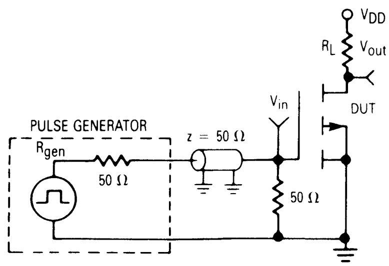


Figure 11. Switching Test Circuit

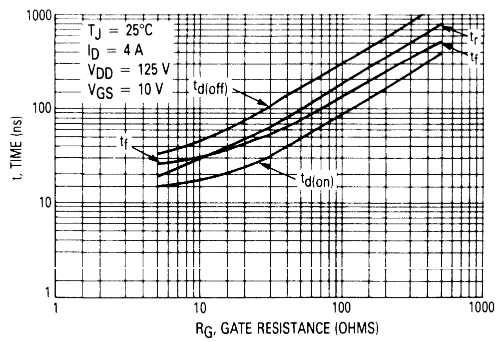


Figure 12. Resistive Switching versus Gate Resistance

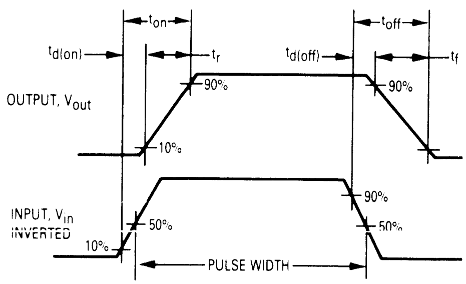


Figure 13. Switching Waveforms

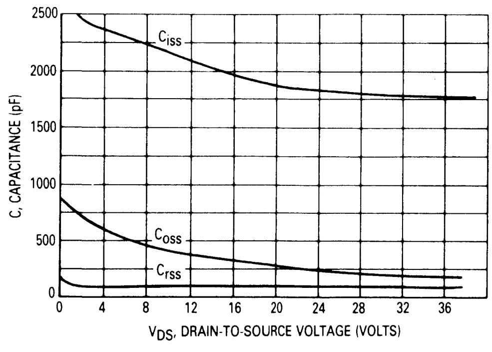


Figure 14. Capacitance Variation

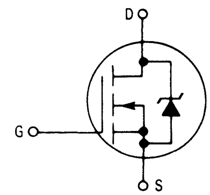
3

MTM10N06E
MTP10N06E

Designer's Data Sheet

TMOS IV
Power Field Effect Transistors
N-Channel Enhancement-Mode Silicon Gate

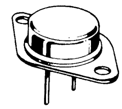
TMOS POWER FETs
10 AMPERES
$r_{DS(on)}$ = 0.20 OHM
60 VOLTS



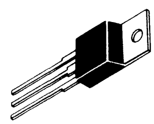
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS™



MTM10N06E
CASE 1-04
TO-204AA



MTP10N06E
CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	MTM10N06E MTP10N06E	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 28	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient MTM10N06E MTP10N06E	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 30 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM/MTP10N06E	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.2	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc)		$V_{DS(on)}$	—	2.2	Vdc
(I_D = 5 Adc, T_J = 100°C)			—	1.5	
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)		g_{FS}	3.8	—	mhos
DRAIN-TO-SOURCE AVALANCHE STRESS CAPABILITY					
Unclamped Inductive Switching Energy See Figures 14 and 15 (I_D = 28 A, V_{DD} = 10 V, T_C = 25°C, Single Pulse, Non-repetitive)		W_{DSR}	—	35	mJ
(I_D = 10 A, V_{DD} = 10 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)			—	55	
(I_D = 4 A, V_{DD} = 10 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)			—	22	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 14 and 15	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	15 (Typ)	26	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 0.5 Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	70 (Typ)	90	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured frrom the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

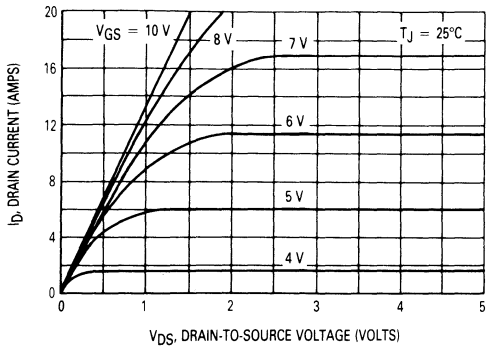


Figure 1. On-Region Characteristics

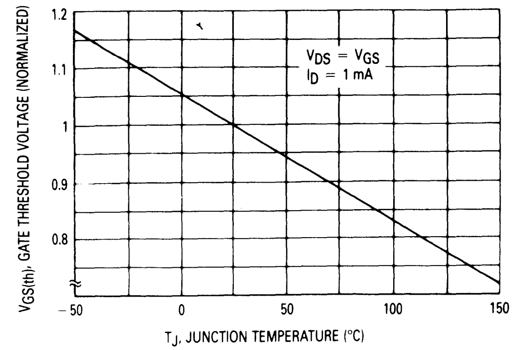


Figure 2. Gate-Threshold Voltage Variation With Temperature

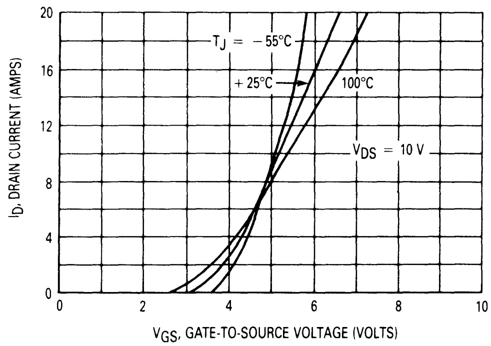


Figure 3. Transfer Characteristics

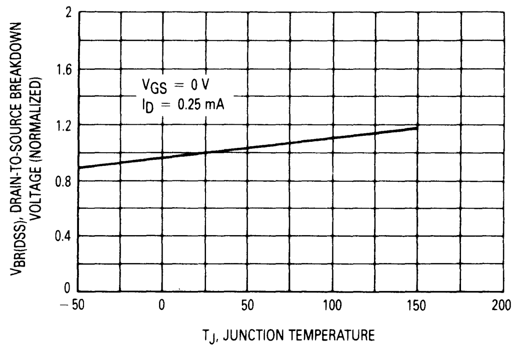


Figure 4. Breakdown Voltage Variation With Temperature

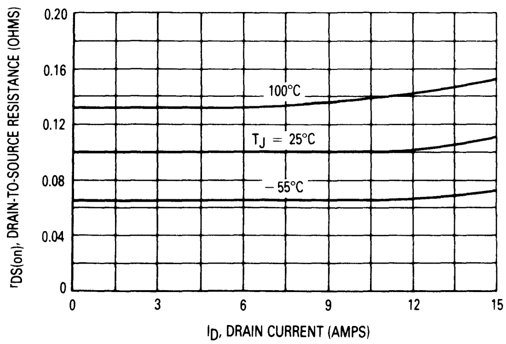


Figure 5. On-Resistance versus Drain Current

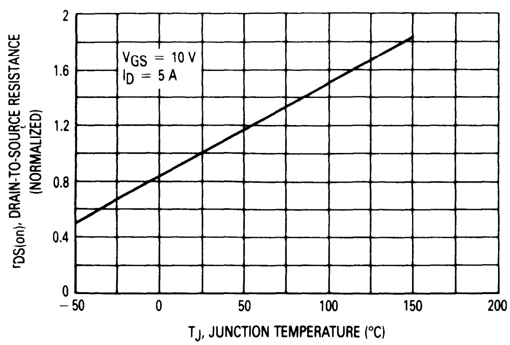


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

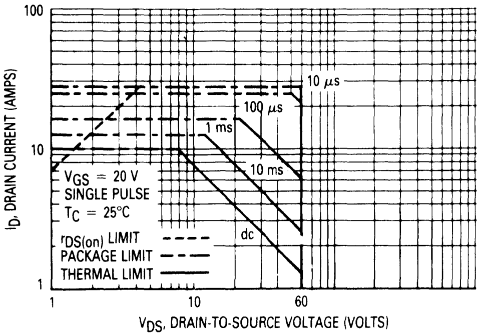


Figure 7. Maximum Rated Forward Biased Safe Operating Area

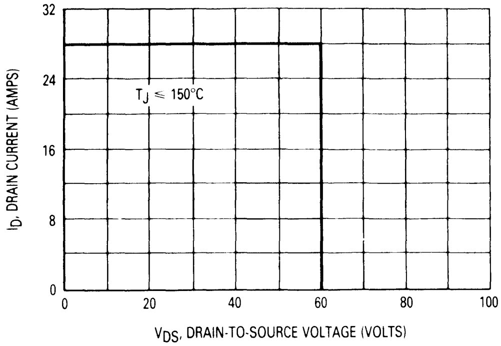


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

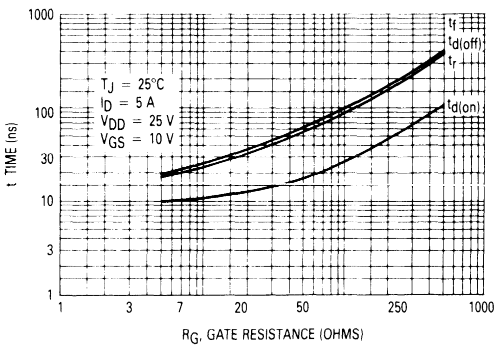


Figure 9. Resistive Switching Time Variation versus Gate Resistance

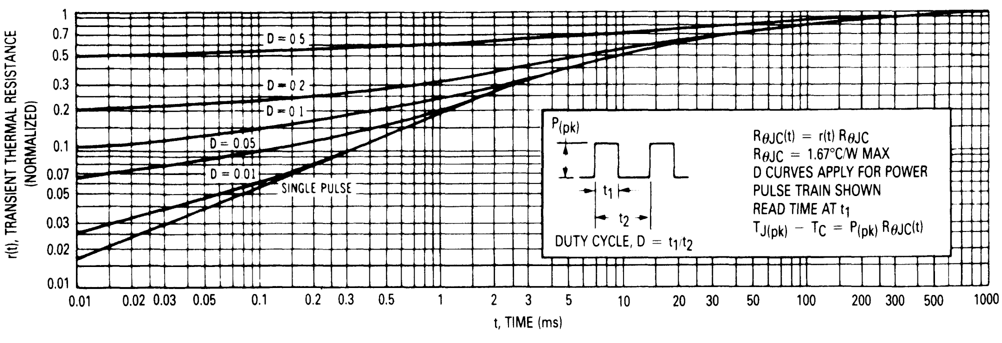


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

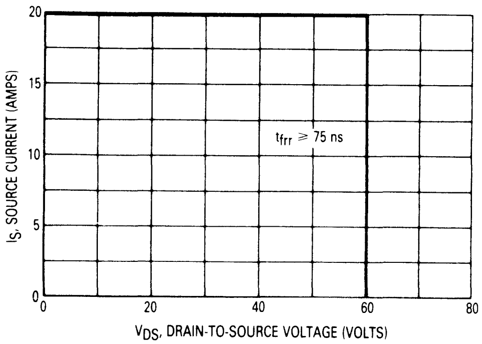


Figure 12. Commutating Safe Operating Area (CSOA)

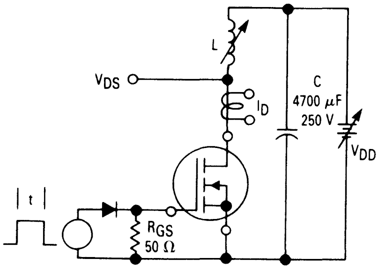


Figure 14. Unclamped Inductive Switching Test Circuit

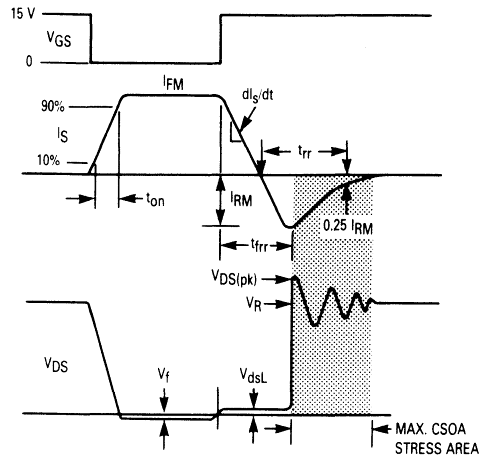


Figure 11. Commutating Waveforms

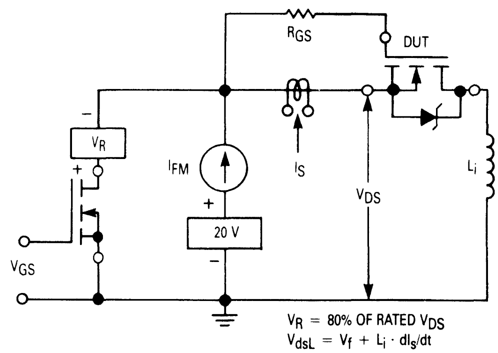
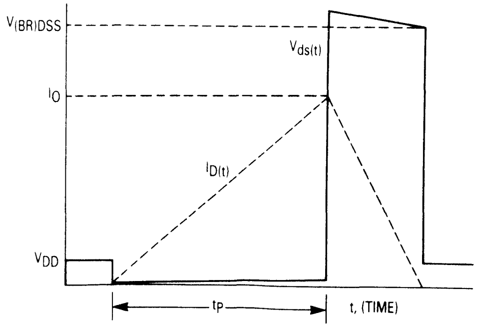


Figure 13. Commutating Safe Operating Area Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

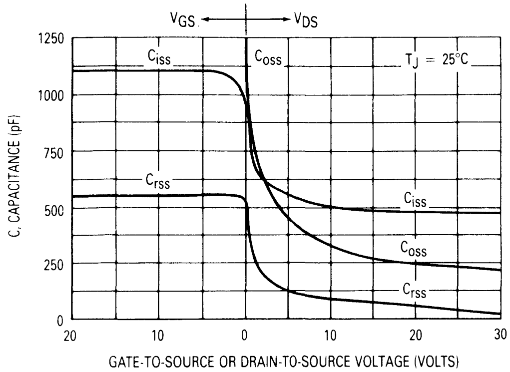


Figure 16. Capacitance Variation

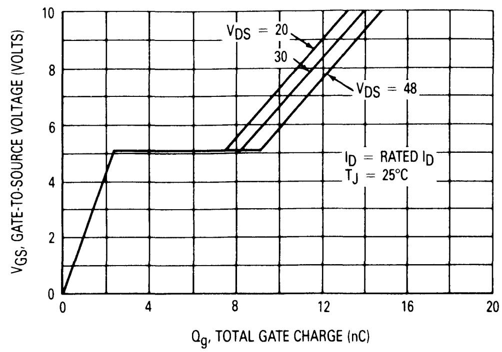


Figure 17. Gate Charge versus Gate-to-Source Voltage

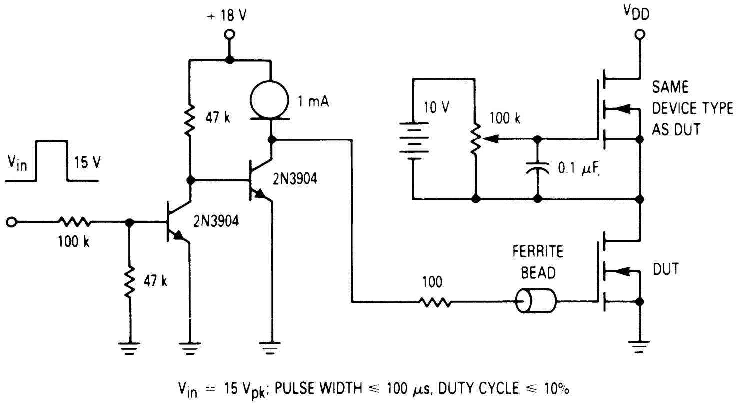
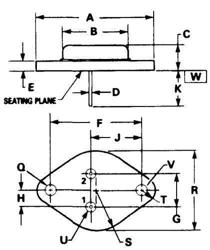


Figure 18. Gate Charge Test Circuit

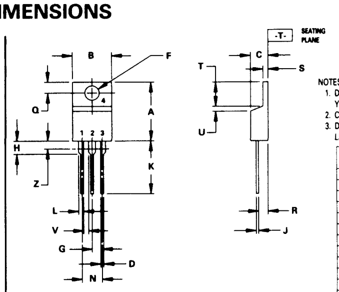
OUTLINE DIMENSIONS



NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

CASE 1-04
MTM10N06E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
MTP10N06E

MTM10N12L
MTM10N15L
MTP10N12L
MTP10N15L

Designer's Data Sheet

Power Field Effect Transistors

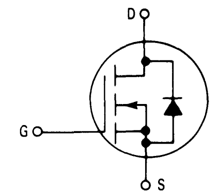
N-Channel Enhancement-Mode Silicon Gate TMOS

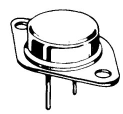
TMOS POWER FETs
LOGIC LEVEL
10 AMPERES
$r_{DS(on)}$ = 0.3 OHM
120 and 150 VOLTS

3

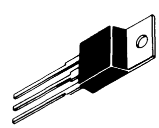
These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM10N12L
MTM10N15L
CASE 1-06
TO-204AA



MTP10N12L
MTP10N15L
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM10N12L MTP10N12L	MTM10N15L MTP10N15L	Unit
Drain-Source Voltage	V_{DSS}	120	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	120	150	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±15 ±20		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 28		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient MTM10N12/15L MTP10N12/15L	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 30 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA) MTM/MTP10N12L MTM/MTP10N15L	$V_{(BR)DSS}$	 120 150	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 10 Adc) (I_D = 5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 4 3.5	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	1200	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	2800	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	60	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	2400	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{oss}	—	250	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 7.5 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	135	
Turn-Off Delay Time		$t_{d(off)}$	—	135	
Fall Time		t_f	—	135	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 15 A, V_{GS} = 5 Vdc) See Figures 6 and 10.	Q_g	14 (typ)	20	nC
Gate-Source Charge		Q_{gs}	7 (typ)	—	
Gate-Drain Charge		Q_{gd}	7 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.6 (typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	150 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

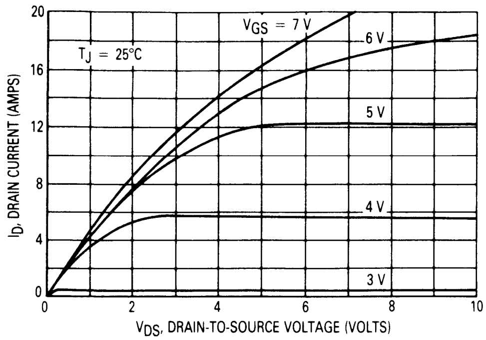


Figure 1. On-Region Characteristics

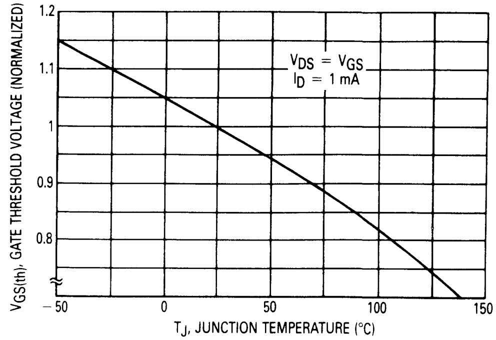


Figure 2. Gate-Threshold Voltage Variation With Temperature

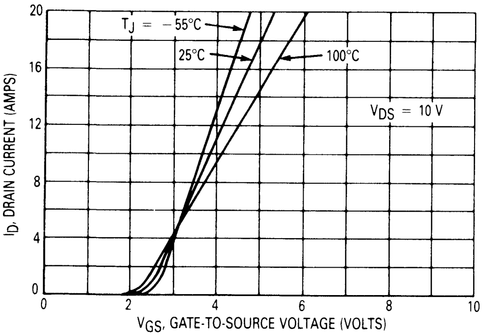


Figure 3. Transfer Characteristics

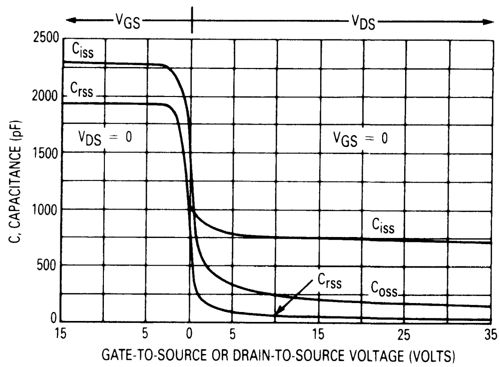


Figure 4. Capacitance Variation With Voltage

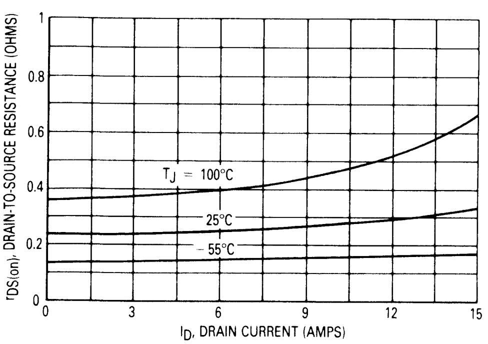


Figure 5. On-Resistance Variation With Drain Current

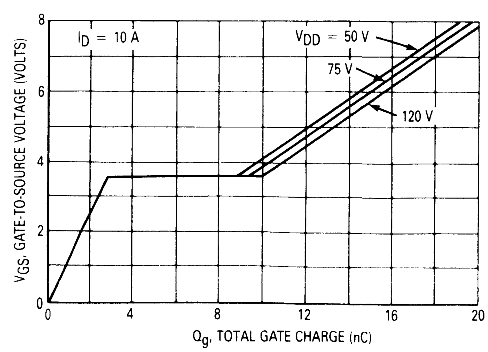


Figure 6. Gate Charge versus Gate-To-Source Voltage

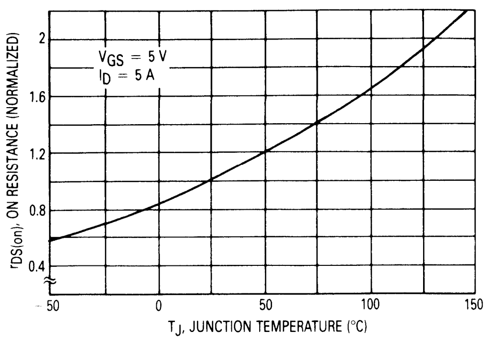


Figure 7. On-Resistance Variation With Temperature

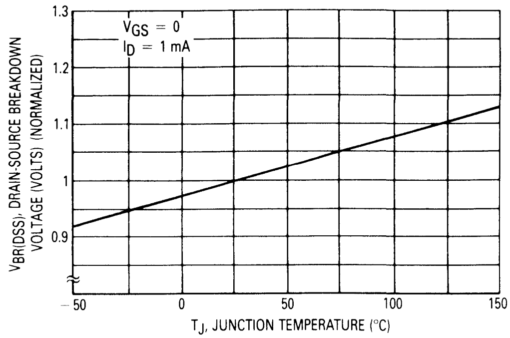


Figure 8. Breakdown Voltage Variation With Temperature

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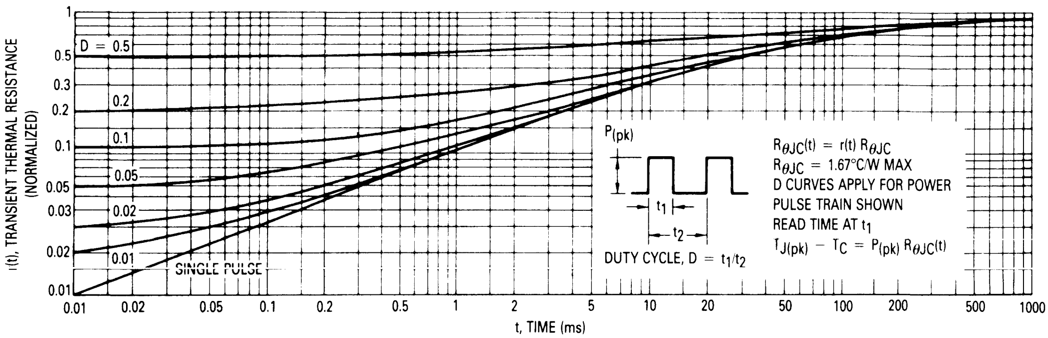
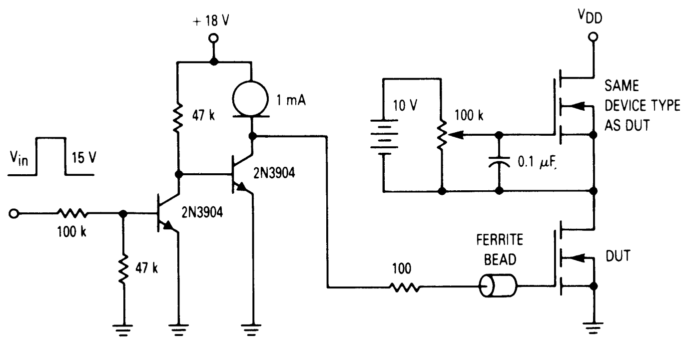


Figure 9. Thermal Response



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge Test Circuit

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

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The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

3

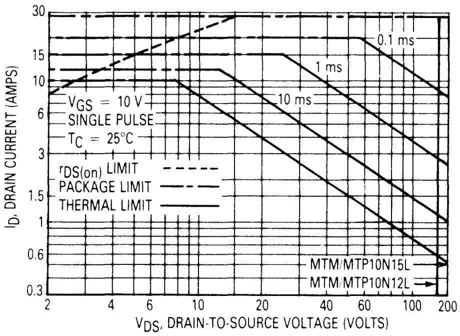


Figure 11. Maximum Rated Forward Biased Safe Operating Area

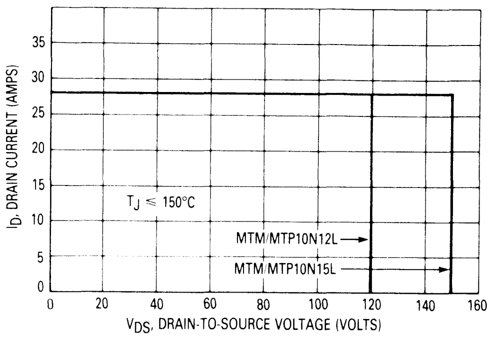
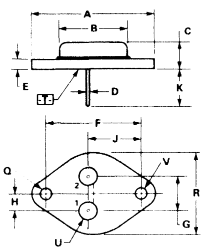


Figure 12. Maximum Rated Switching Safe Operating Area

OUTLINE DIMENSIONS

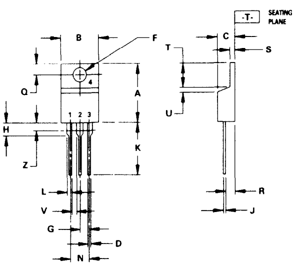


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ 0.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS:
⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-06
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5.
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MTM10N25
MTP10N25

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

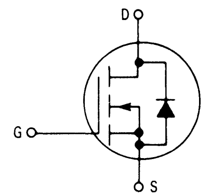
TMOS

TMOS POWER FETs
10 AMPERES
$r_{DS(on)}$ = 0.45 OHM
250 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

3

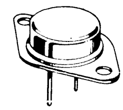


MAXIMUM RATINGS

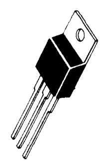
Rating	Symbol	MTM or MTP 10N25	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 30	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Junction to Ambient TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTM10N25
CASE 1-04
TO-204AA



MTP10N25
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.45	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc) (I_D = 5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 5.6 4.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)		g_{FS}	3.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1500	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	37 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	21 (Typ)	—	
Gate-Drain Charge		Q_{gd}	16 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.6 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

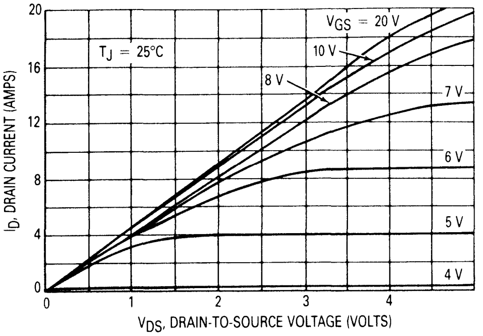


Figure 1. On-Region Characteristics

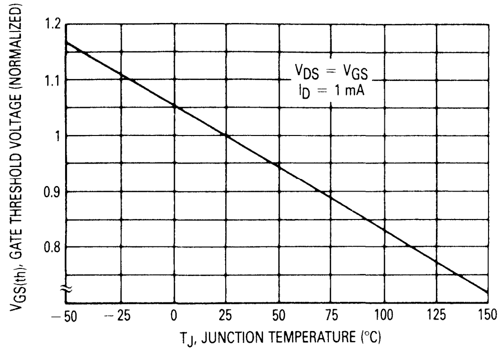


Figure 2. Gate-Threshold Voltage Variation With Temperature

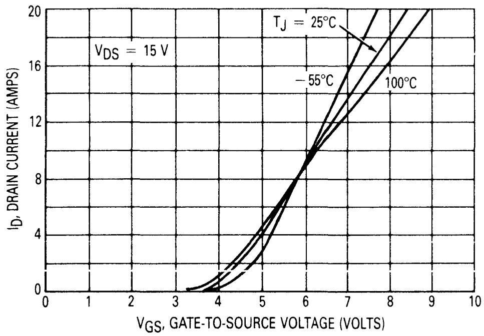


Figure 3. Transfer Characteristics

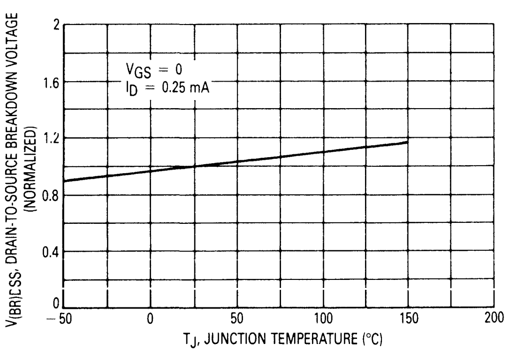


Figure 4. Breakdown Voltage Variation With Temperature

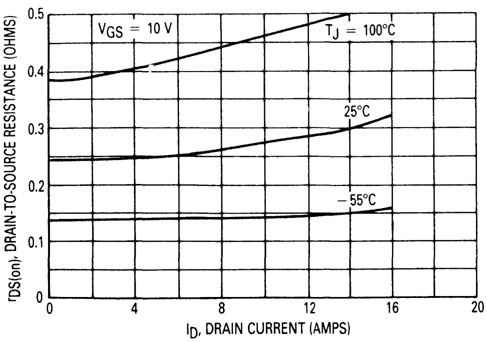


Figure 5. On-Resistance versus Drain Current

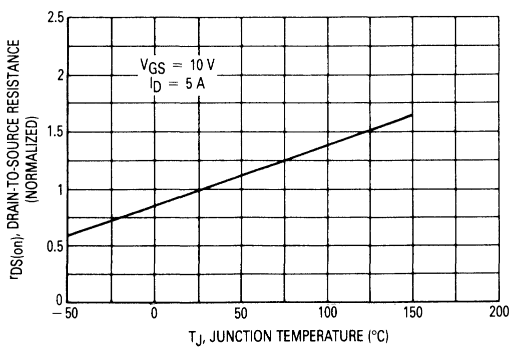


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

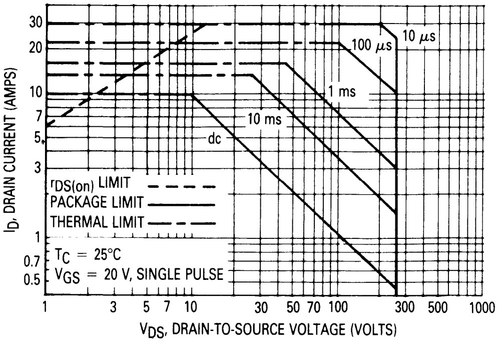


Figure 7. Maximum Rated Forward Biased Safe Operating Area

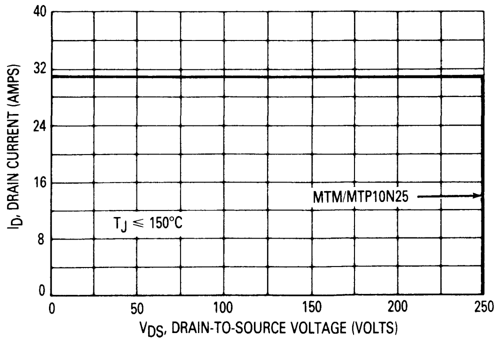


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

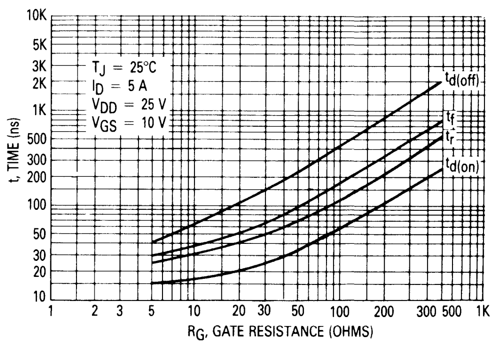


Figure 9. Resistive Switching Time versus Gate Resistance

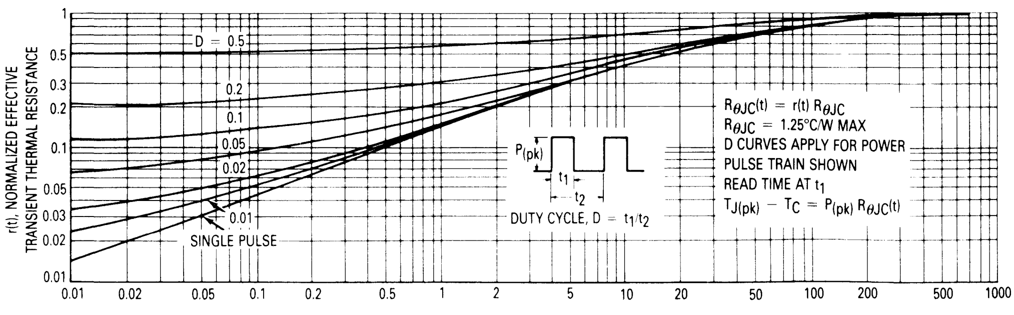


Figure 10. Thermal Response

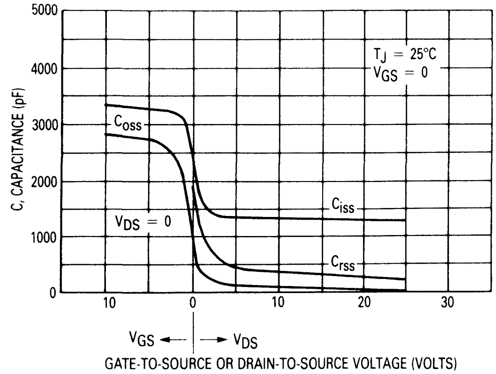


Figure 11. Capacitance Variation

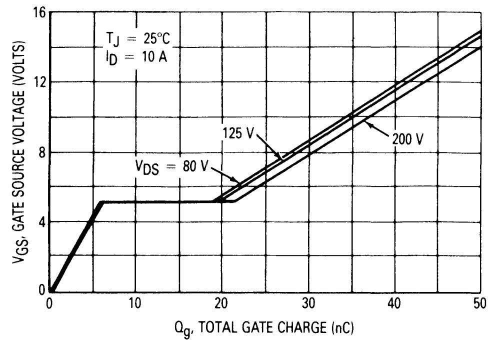


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

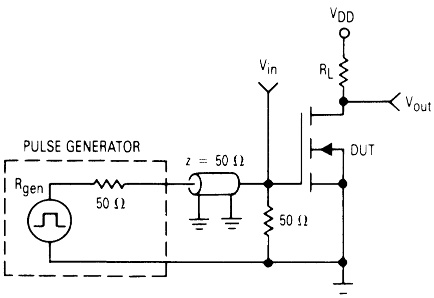


Figure 13. Switching Test Circuit

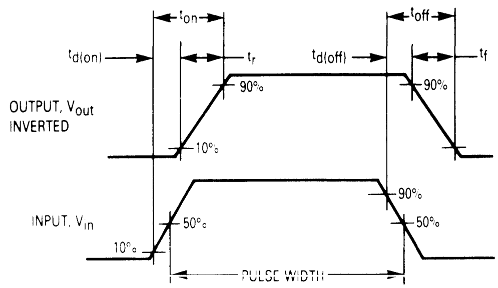
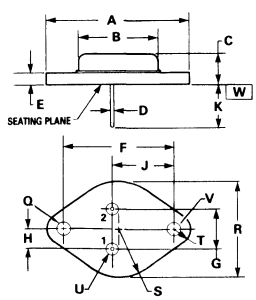


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

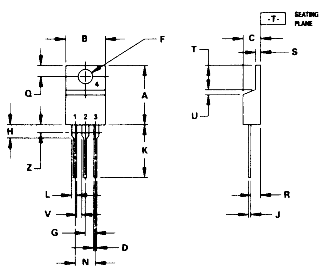


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM12N05
MTP12N05
MTP12N06

Designer's Data Sheet

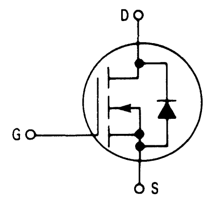
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
12 AMPERES
$r_{DS(on)}$ = 0.2 OHM
50 and 60 VOLTS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

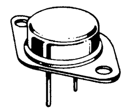


MAXIMUM RATINGS

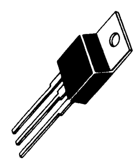
Rating	Symbol	MTM12N05	MTP12N05 MTP12N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 12 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.67	°C/W
Junction to Ambient TO-204 TO-220	$R_{\theta JA}$	30 62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTM12N05
CASE 1-04
TO-204AA



MTP12N05
MTP12N06
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP12N05 MTP12N06	$V_{(BR)DSS}$	 50 60	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)	$r_{DS(on)}$	—	0.2	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 3 2.8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)	g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	400	pF
Output Capacitance	C_{oss}	—	300	
Reverse Transfer Capacitance	C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time	t_r	—	160	
Turn-Off Delay Time	$t_{d(off)}$	—	80	
Fall Time	t_f		110	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	13 (Typ)	26	nC
Gate-Source Charge	Q_{gs}	6 (Typ)	—	
Gate-Drain Charge	Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8 (Typ)	3.2	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)				
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)	L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)	L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)				
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

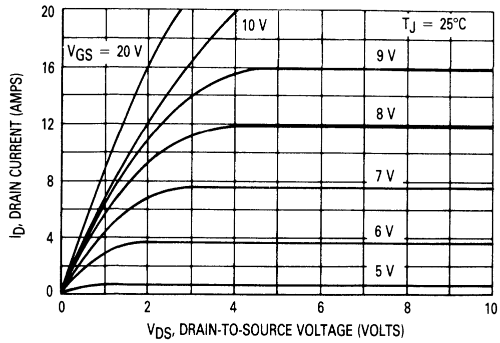


Figure 1. On-Region Characteristics

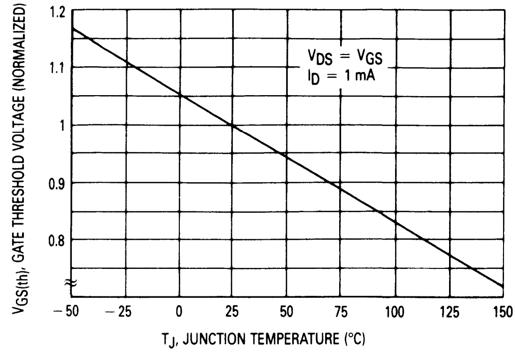


Figure 2. Gate-Threshold Voltage Variation With Temperature

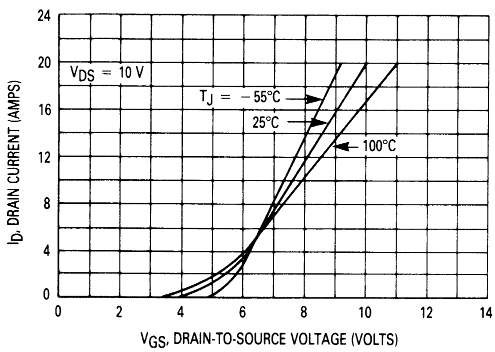


Figure 3. Transfer Characteristics

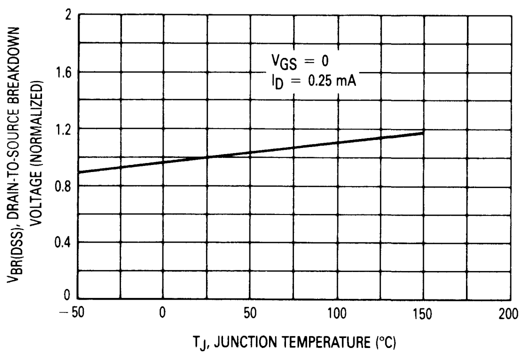


Figure 4. Breakdown Voltage Variation With Temperature

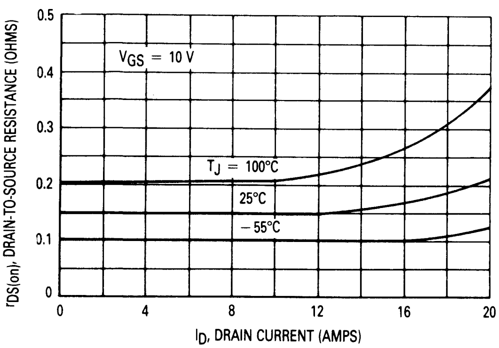


Figure 5. On-Resistance versus Drain Current

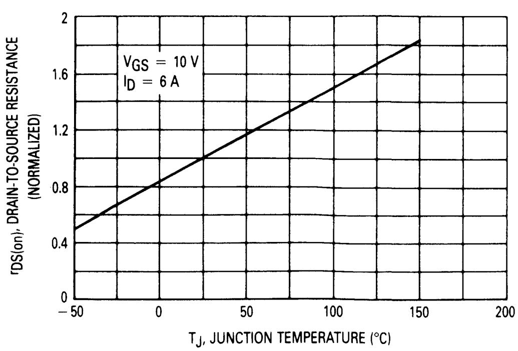


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

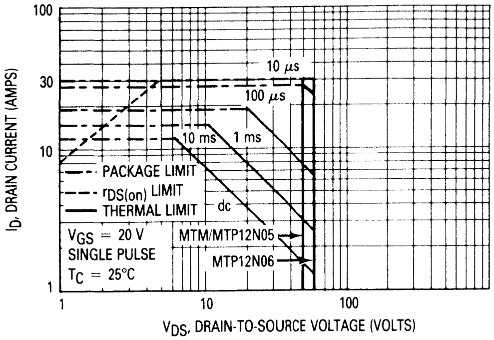


Figure 7. Maximum Rated Forward Biased Safe Operating Area

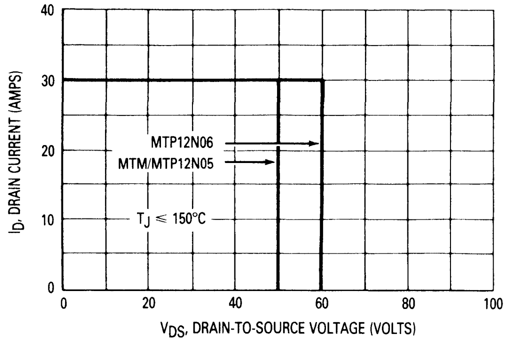


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

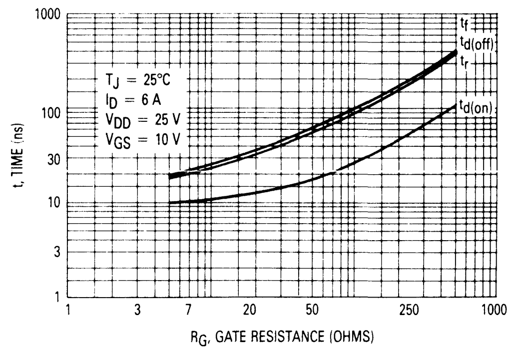


Figure 9. Resistive Switching Time Variation versus Gate Resistance

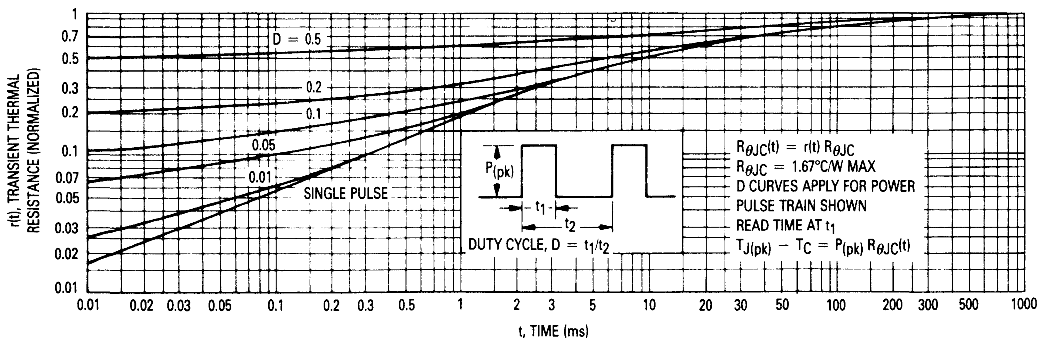


Figure 10. Thermal Response

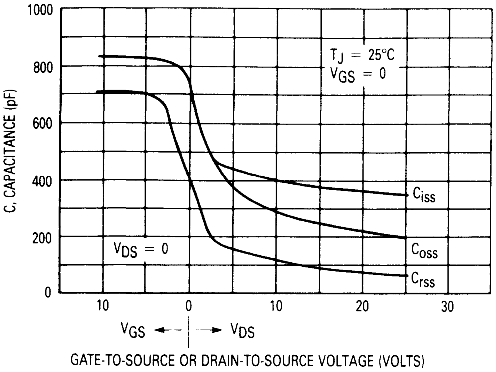


Figure 11. Capacitance Variation

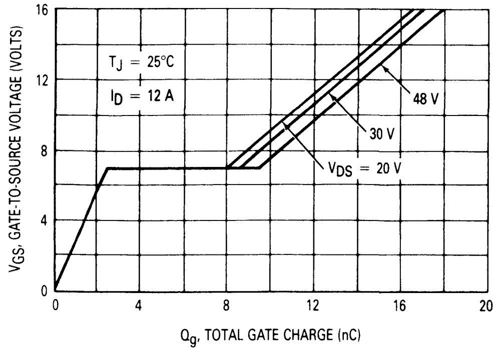


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

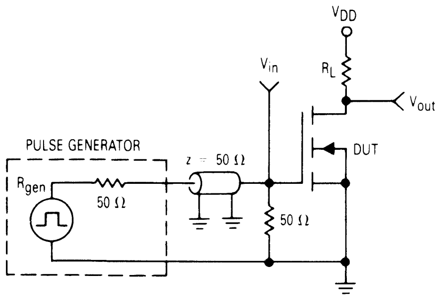


Figure 13. Switching Test Circuit

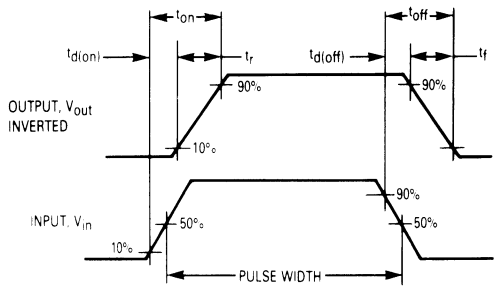
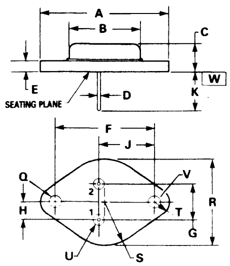


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 1-04
TO-204AA



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	--	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

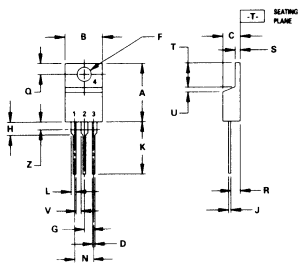
NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:

⌖	ϕ 0.25 (0.010) Ⓜ	W	V Ⓜ

3. POSITIONAL TOLERANCE FOR LEADS:

⌖	ϕ 0.30 (0.012) Ⓜ	W	V Ⓜ	Q Ⓜ

CASE 221A-04
TO-220AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM12N10
MTP12N08
MTP12N10

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

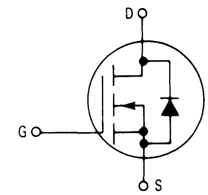
TMOS

TMOS POWER FETs
12 AMPERES
$r_{DS(on)}$ = 0.18 OHM
80 and 100 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

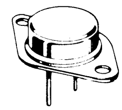
3

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



MAXIMUM RATINGS

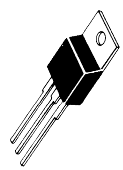
Rating	Symbol	MTM12N10	MTP12N08 MTP12N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C



MTM12N10
CASE 1-04
TO-204AA

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.67	°C/W
Junction to Ambient TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTP12N08
MTP12N10
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP12N08		$V_{(BR)DSS}$	80	—	Vdc
MTM/MTP12N10			100	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc)		$V_{DS(on)}$	—	2.6	Vdc
(I_D = 6 Adc, T_J = 100°C)			—	2.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)		g_{FS}	3	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	17 (Typ)	36	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	9 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.2 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

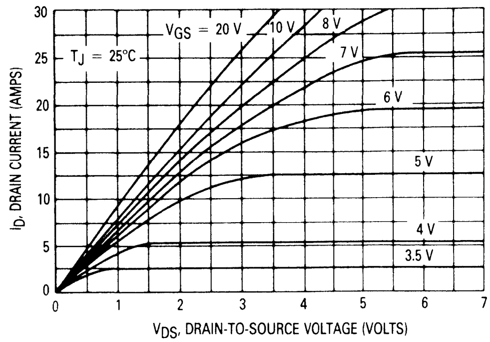


Figure 1. On-Region Characteristics

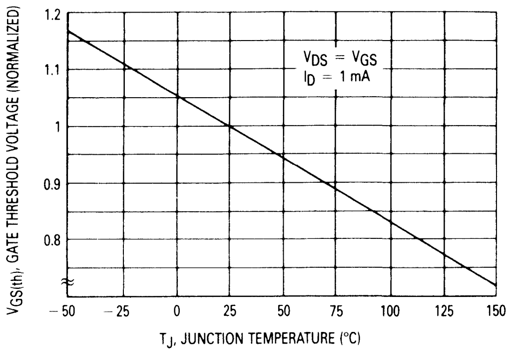
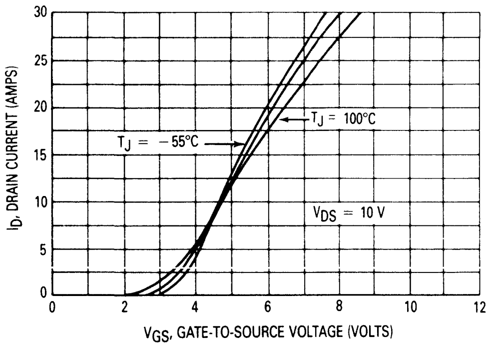


Figure 2. Gate-Threshold Voltage Variation With Temperature



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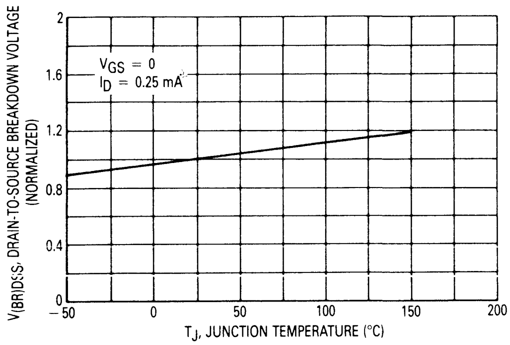

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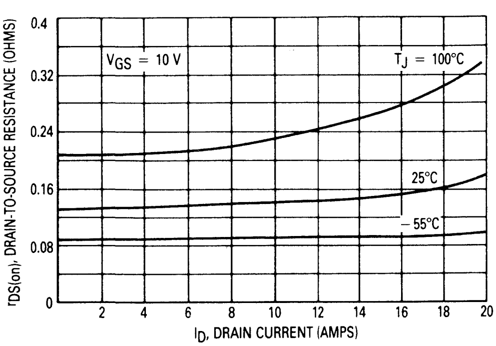

Figure 5. On-Resistance versus Drain Current

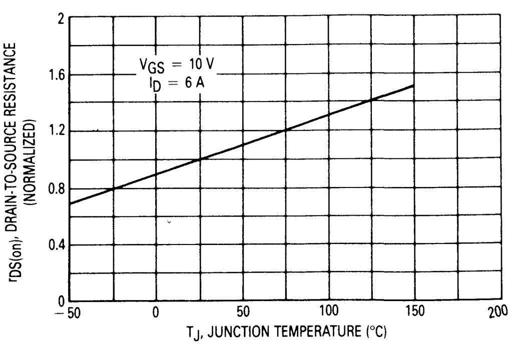

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

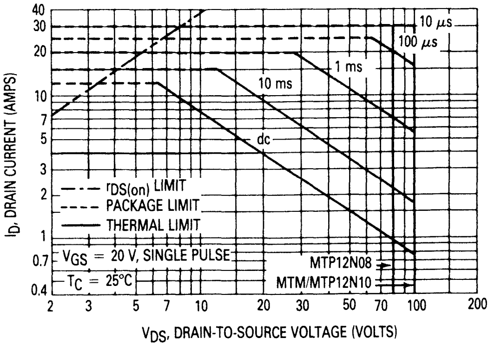

Figure 7. Maximum Rated Forward Biased Safe Operating Area

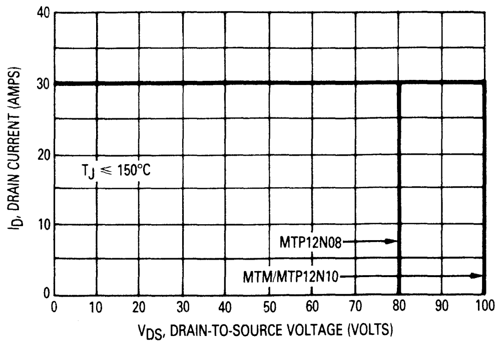

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

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The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

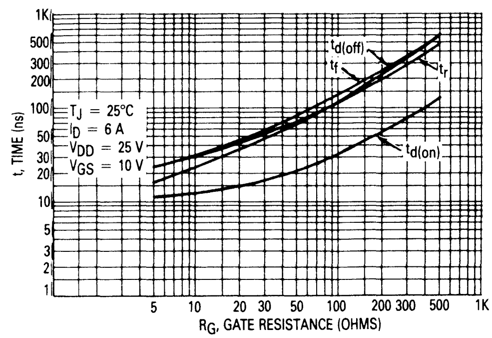


Figure 9. Resistive Switching Time versus Gate Resistance

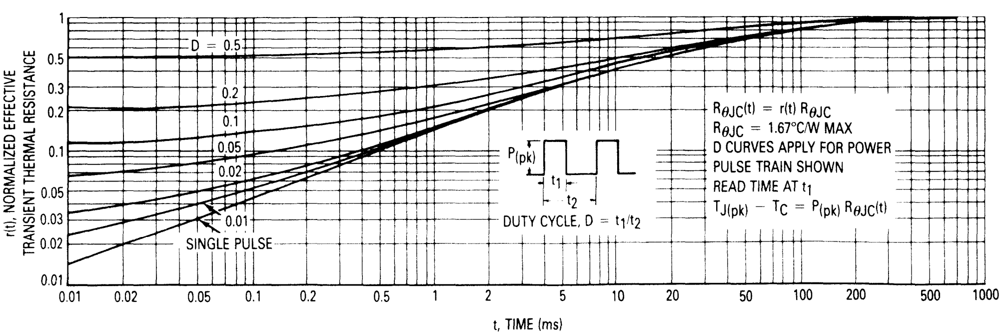


Figure 10. Thermal Response

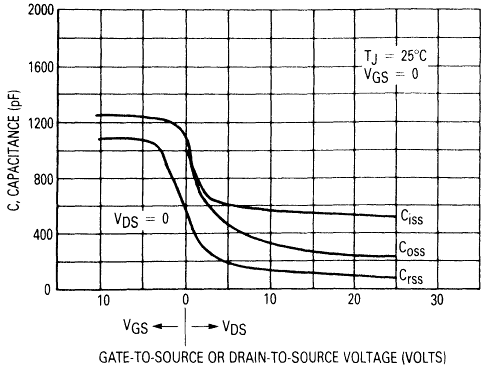


Figure 11. Capacitance Variation

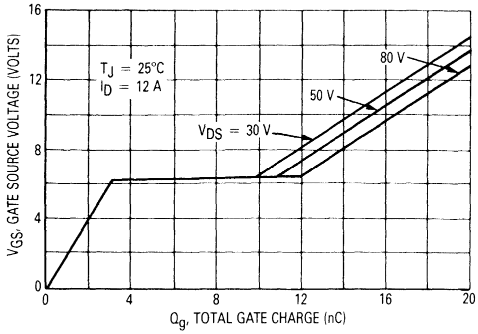


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

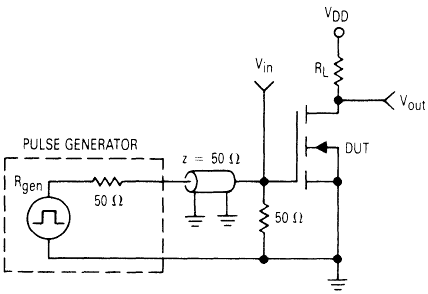


Figure 13. Switching Test Circuit

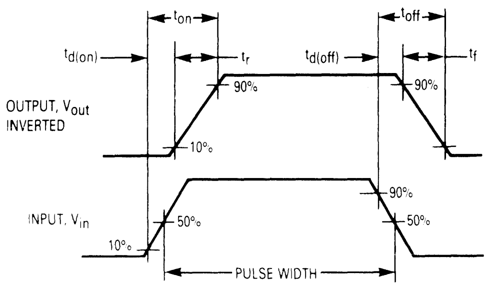
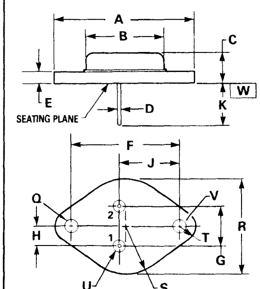


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
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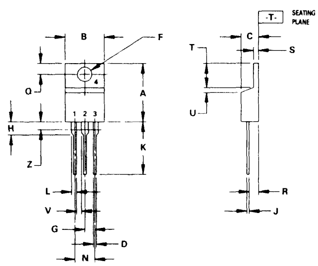
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⊕ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⊕ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

CASE 221A-04
TO-220AB

MTM12P05
MTM12P06
MTM12P08
MTM12P10
MTP12P05
MTP12P06
MTP12P08
MTP12P10

Designer's Data Sheet

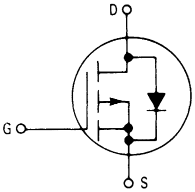
Power Field Effect Transistor

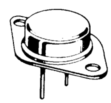
P-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

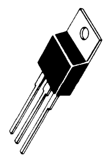
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
12 AMPERES
$r_{DS(on)}$ = 0.3 OHM
50, 60, 80 and 100 VOLTS





MTM12P05
MTM12P06
MTM12P08
MTM12P10
CASE 1-04
TO-204AA



MTP12P05
MTP12P06
MTP12P08
MTP12P10
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM OR MTP				Unit
		12P05	12P06	12P08	12P10	
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40				Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 12 28				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient — TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM/MTP12P05 MTM/MTP12P06 MTM/MTP12P08 MTM/MTP12P10	$V_{(BR)DSS}$	50 60 80 100	— — — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.2 3.8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	920	pF
Output Capacitance		C_{oss}	—	575	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	33 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	16 (Typ)	—	
Gate-Drain Charge		Q_{gd}	17 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	4 (Typ)	5.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

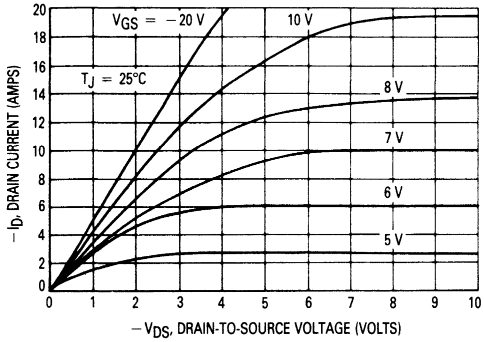


Figure 1. On-Region Characteristics

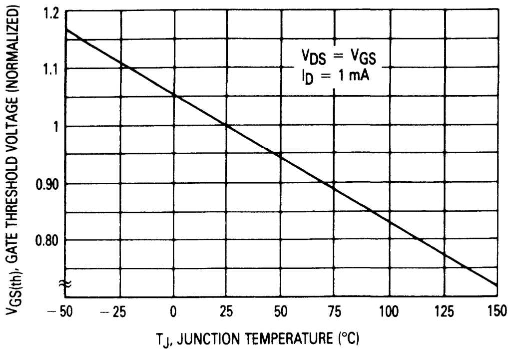


Figure 2. Gate-Threshold Voltage Variation With Temperature

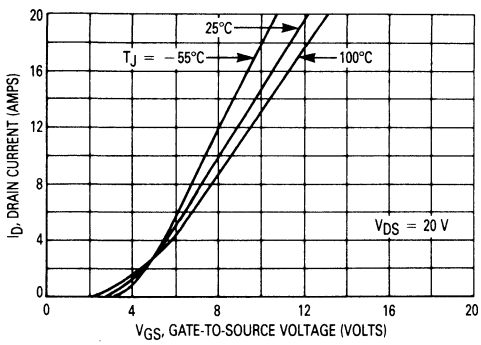


Figure 3. Transfer Characteristics

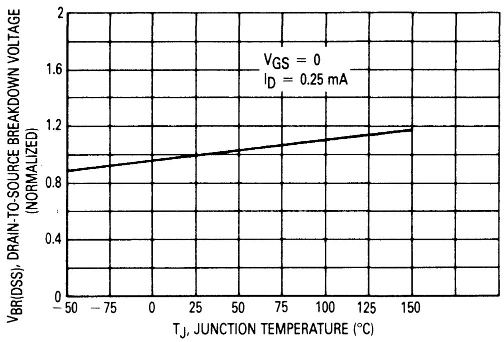


Figure 4. Normalized Breakdown Voltage versus Temperature

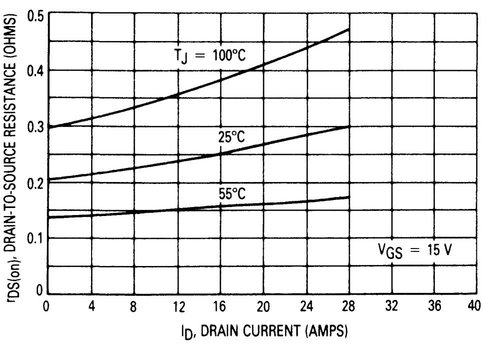


Figure 5. On-Resistance versus Drain Current

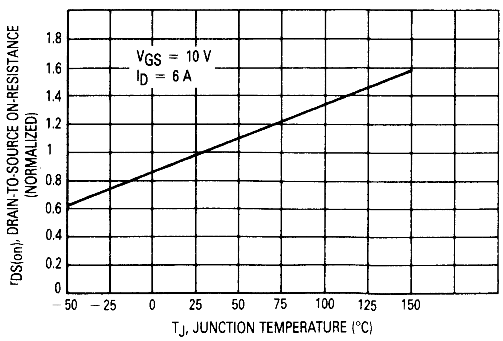


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

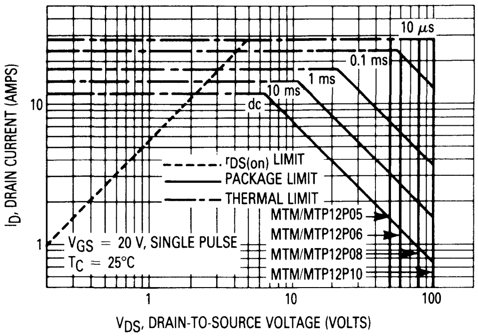


Figure 7. Maximum Rated Forward Biased Safe Operating Area

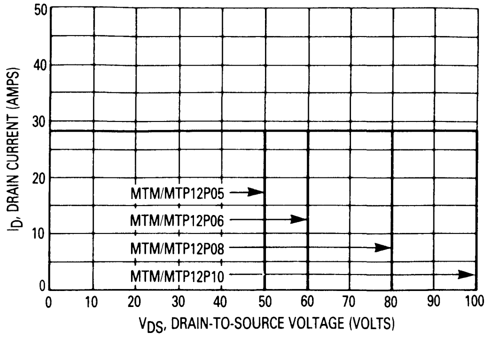


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

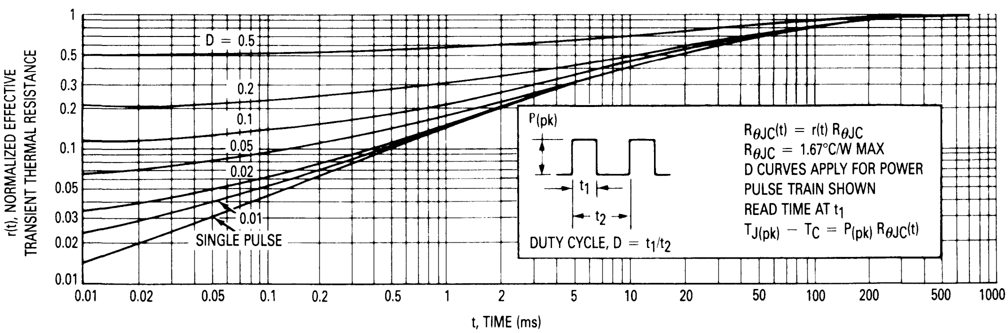


Figure 9. Thermal Response

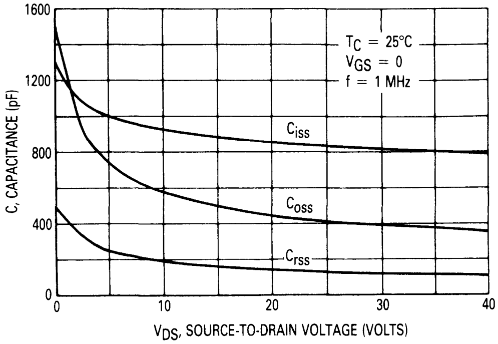


Figure 10. Capacitance Variation

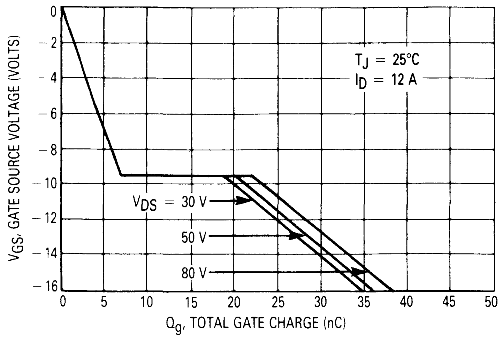


Figure 11. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

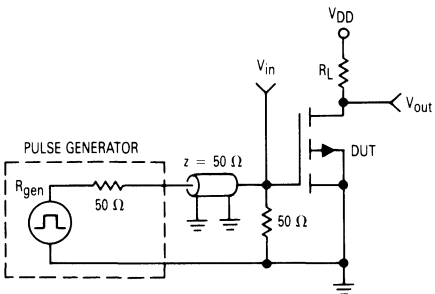


Figure 12. Switching Test Circuit

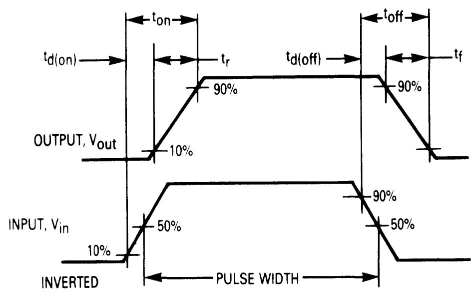
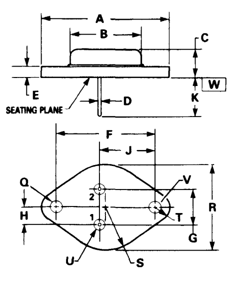


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

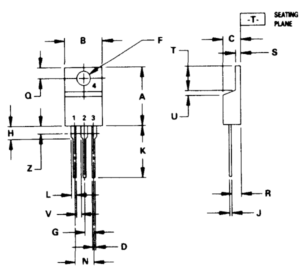


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | φ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | φ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM15N05L MTM15N06L MTP15N05L MTP15N06L

Designer's Data Sheet

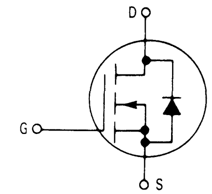
Power Field Effect Transistors

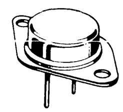
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
LOGIC LEVEL
15 AMPERES
$r_{DS(on)}$ = 0.15 OHM
50 and 60 VOLTS

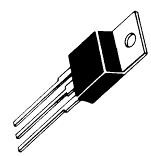
These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM15N05L
MTM15N06L
CASE 1-04
TO-204AA



MTP15N05L
MTP15N06L
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM15N05L MTP15N05L	MTM15N06L MTP15N06L	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±15 ±20		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 40		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.67	°C/W
Junction to Ambient MTM15N05L/06L MTP15N05L/06L	$R_{\theta JA}$	30 62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1 mA) MTM/MTP15N05L MTM/MTP15N06L	$V_{(BR)DSS}$	 50 60	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	2	Vdc
(T_J = 100°C)			0.75	1.5	
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 15 Adc)		$V_{DS(on)}$	—	3	Vdc
(I_D = 7.5 Adc, T_J = 100°C)			—	1.5	
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	900	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 4		—	2800	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	200	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 4		—	2400	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 4	C_{oss}	—	450	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 7.5 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	260	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 15 A, V_{GS} = 5 Vdc) See Figures 6 and 10.	Q_g	14 (typ)	22	nC
Gate-Source Charge		Q_{gs}	7 (typ)	—	
Gate-Drain Charge		Q_{gd}	7 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 14 and 15.	V_{SD}	1.8 (typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and center of the die.)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad.)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

3

TYPICAL CHARACTERISTICS

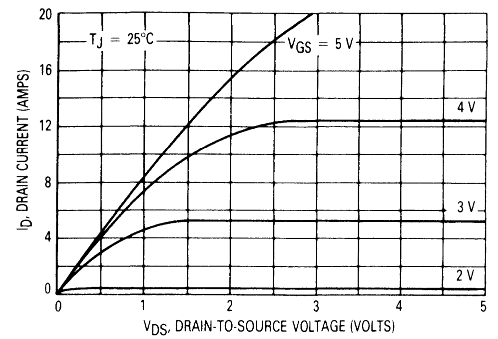


Figure 1. On-Region Characteristics

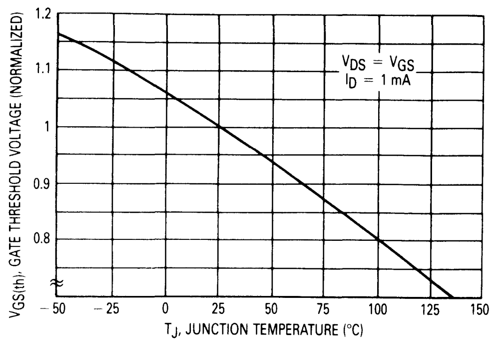


Figure 2. Gate-Threshold Voltage Variation With Temperature

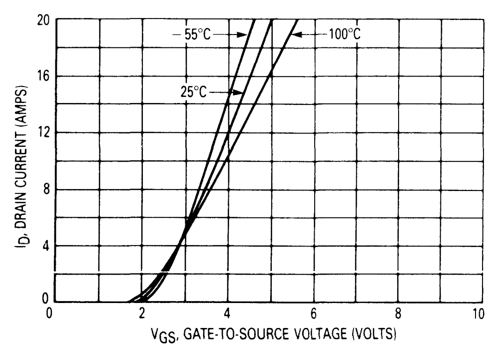


Figure 3. Transfer Characteristics

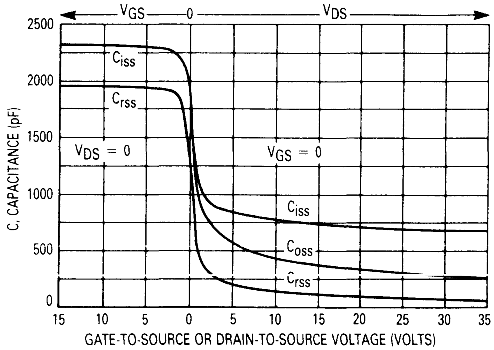


Figure 4. Capacitance Variation

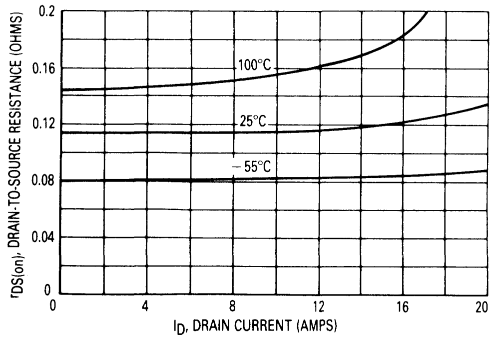


Figure 5. On-Resistance versus Drain Current

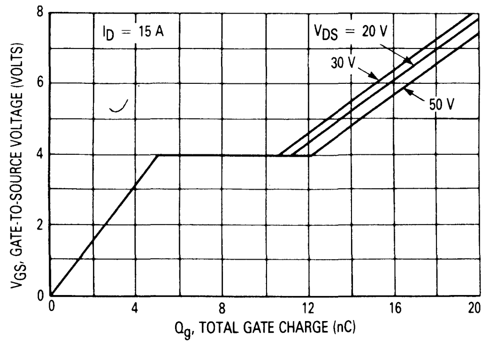


Figure 6. Gate Charge Variation

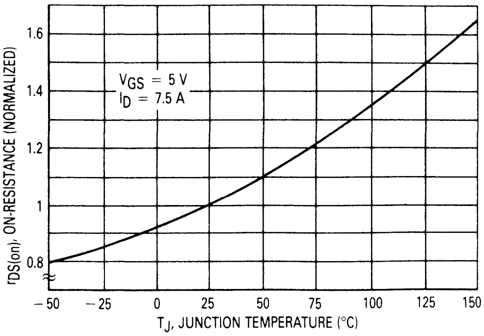


Figure 7. On-Resistance Variation with Temperature

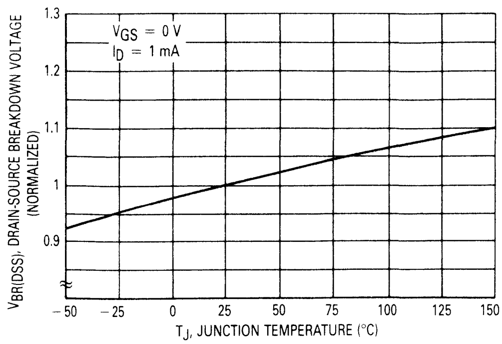


Figure 8. Drain-Source Breakdown Voltage Variation with Temperature

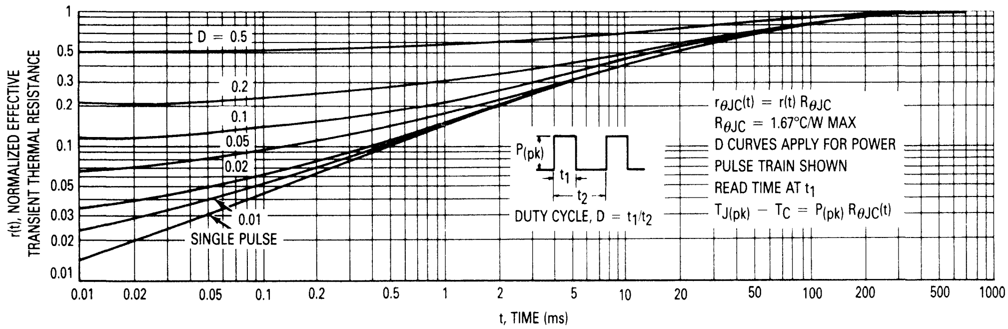
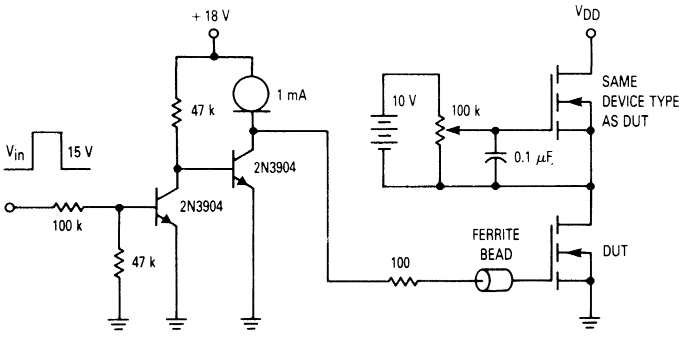


Figure 9. Thermal Response



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

3

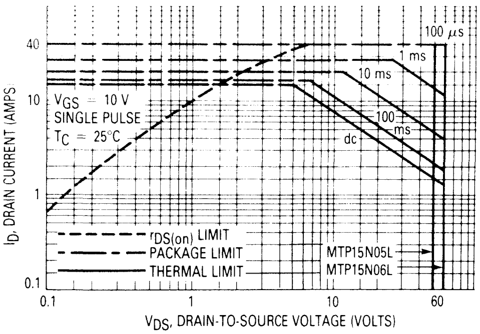


Figure 11. Maximum Rated Forward Biased Safe Operating Area

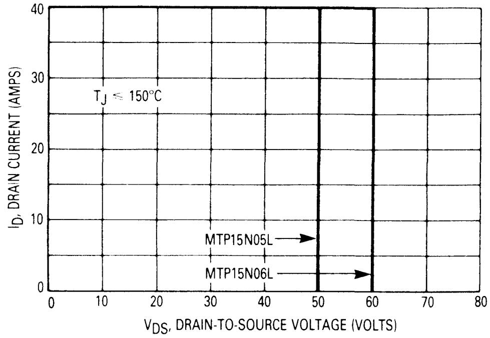
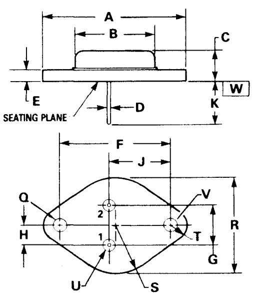


Figure 12. Maximum Rated Switching Safe Operating Area

OUTLINE DIMENSIONS

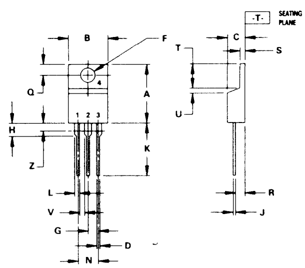


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM15N06E
MTP15N06E

Designer's Data Sheet

TMOS IV

Power Field Effect Transistors

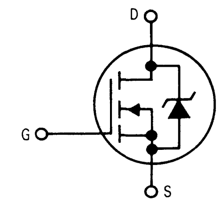
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER FETs
15 AMPERES
$r_{DS(on)}$ = 0.15 OHM
60 VOLTS

3

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

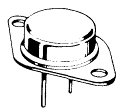


MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

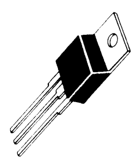
Rating	Symbol	MTM15N06E MTP15N06E	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 40	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient MTM15N06E MTP15N06E	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 30 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



MTM15N06E
CASE 1-04
TO-204AA



MTP15N06E
CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2.6 1.3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	4	—	mhos
DRAIN-TO-SOURCE AVALANCHE STRESS CAPABILITY					
Unclamped Inductive Switching Energy See Figures 14 and 15 (I_D = 40 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 18 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 6 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		W_{DSR}	 — — —	 35 55 22	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 14 and 15	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	15 (Typ)	35	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	9 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 0.5 Rated I_D V_{GS} = 0)	V_{SD}	1.2 (Typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	70 (Typ)	90	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured frrom the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

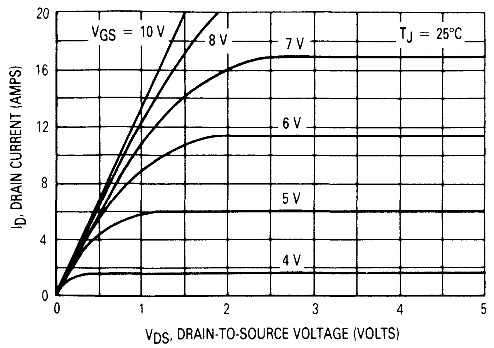


Figure 1. On-Region Characteristics

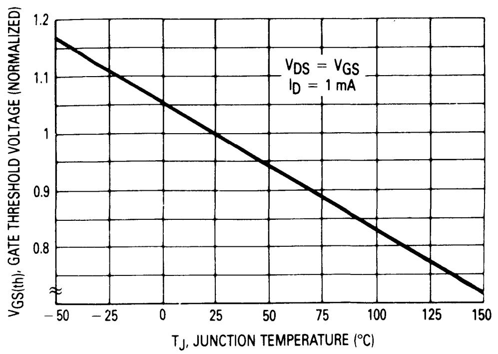


Figure 2. Gate-Threshold Voltage Variation With Temperature

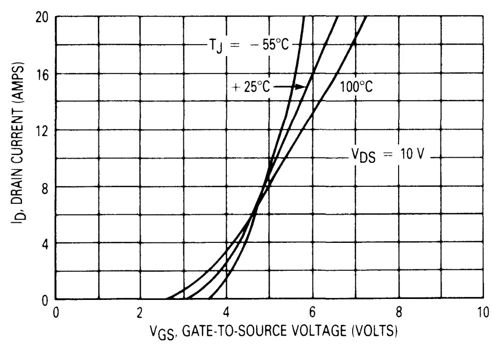


Figure 3. Transfer Characteristics

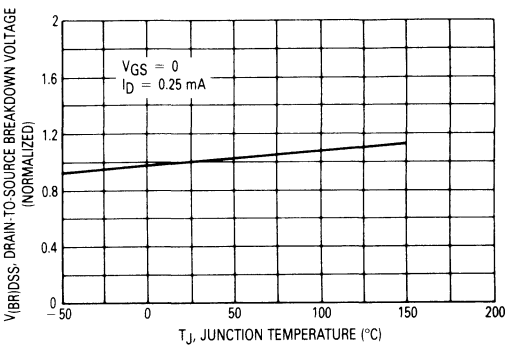


Figure 4. Breakdown Voltage Variation With Temperature

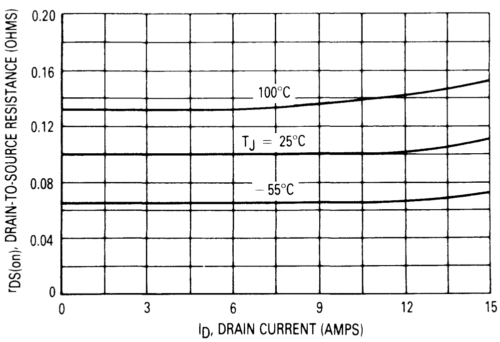


Figure 5. On-Resistance versus Drain Current

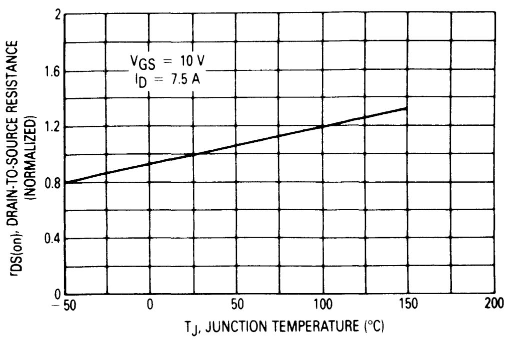


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

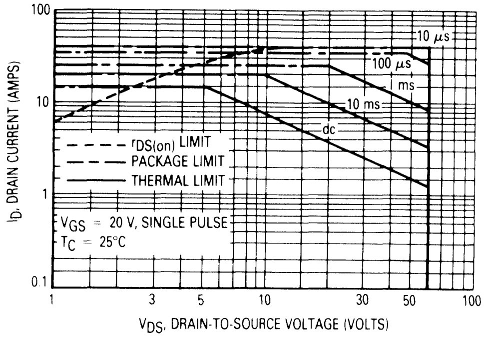


Figure 7. Maximum Rated Forward Biased Safe Operating Area

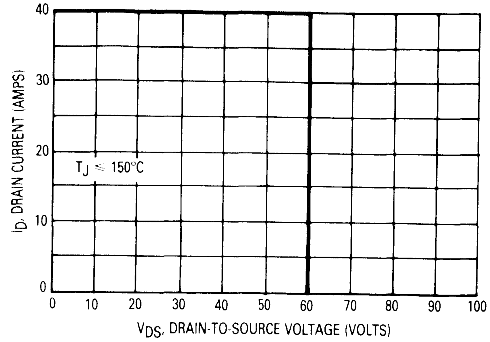


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

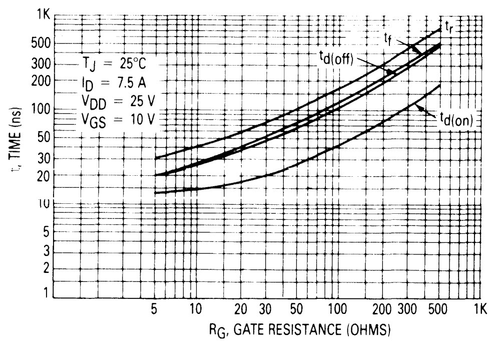


Figure 9. Resistive Switching Time versus Gate Resistance

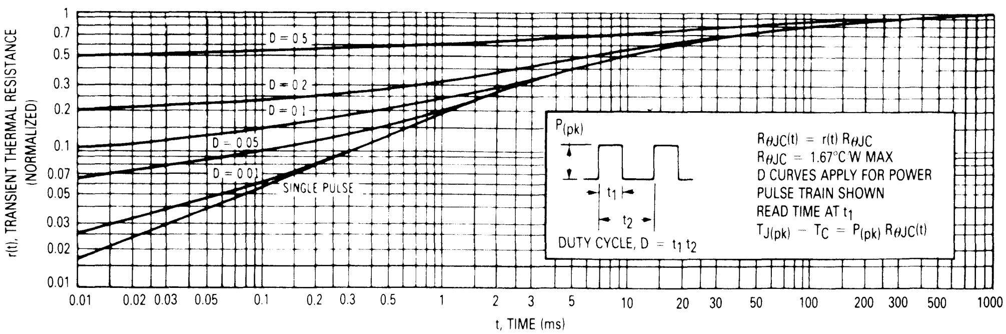


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

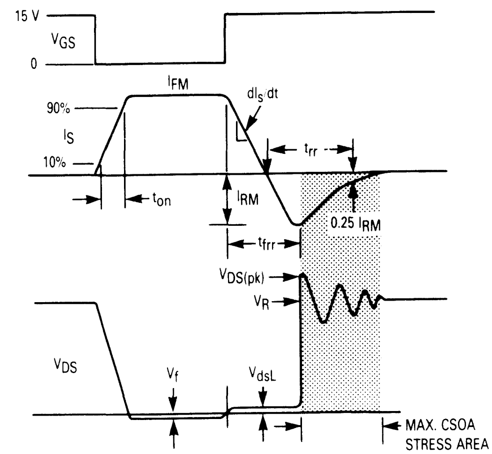


Figure 11. Commutating Waveforms

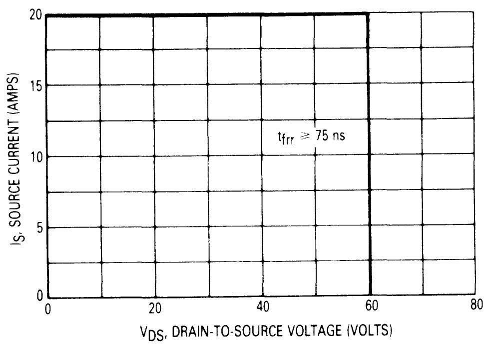


Figure 12. Commutating Safe Operating Area (CSOA)

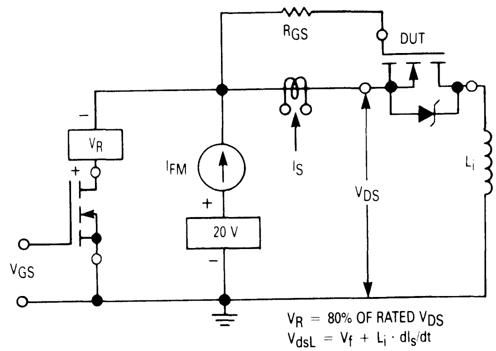


Figure 13. Commutating Safe Operating Area Test Circuit

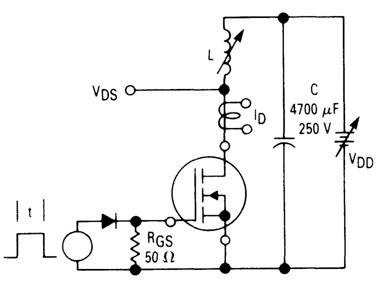
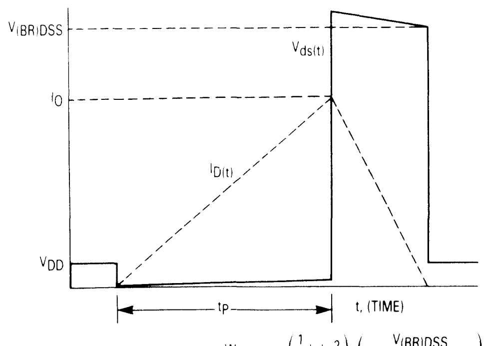


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

3

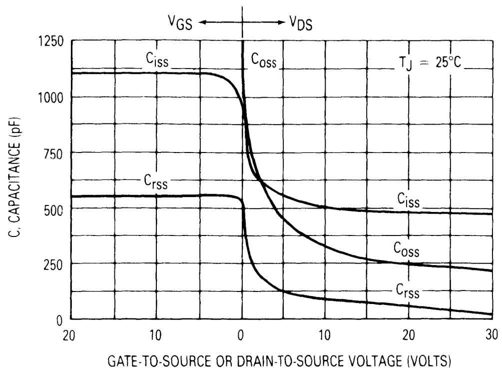


Figure 16. Capacitance Variation

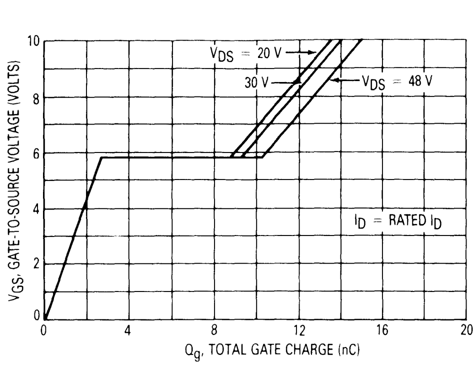
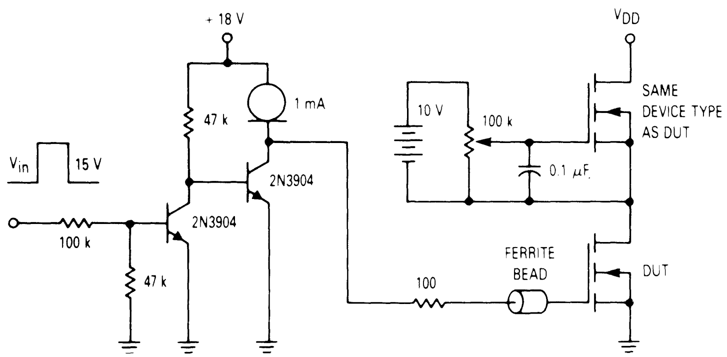


Figure 17. Gate Charge versus Gate-to-Source Voltage

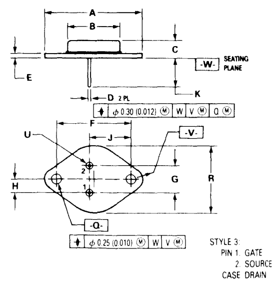
3



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

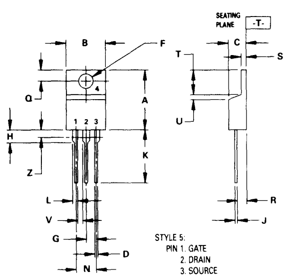
OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.84	4.19	0.151	0.165

CASE 1-04
MTM15N06E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
MTP15N06E

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM15N35
MTM15N40

Designer's Data Sheet

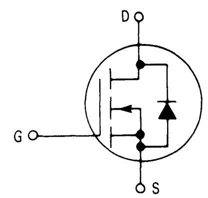
Power Field Effect Transistor

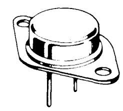
N-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
15 AMPERES
$r_{DS(on)}$ = 0.3 OHM
350 and 400 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 197A-02
TO-204AE

MAXIMUM RATINGS

Rating	Symbol	MTM 15N35	MTM 15N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 70		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.5 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM15N35 MTM15N40	$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	— —	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	6	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	450	
Fall Time		t_f	—	180	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	110 (Typ)	160	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.3 (Typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

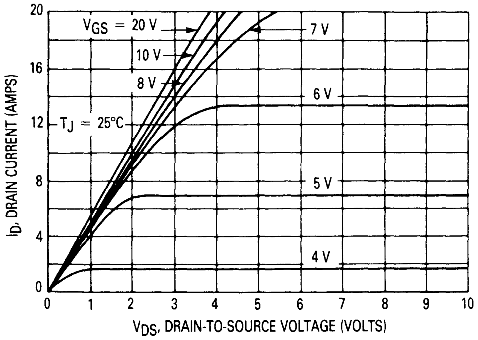


Figure 1. On-Region Characteristics

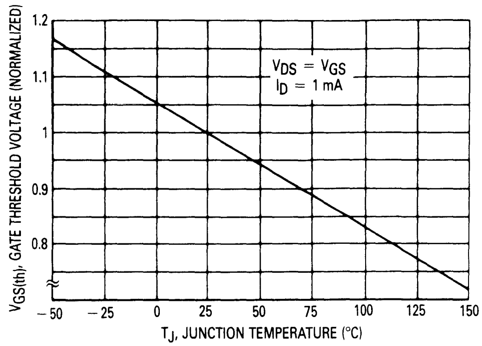


Figure 2. Gate-Threshold Voltage Variation With Temperature

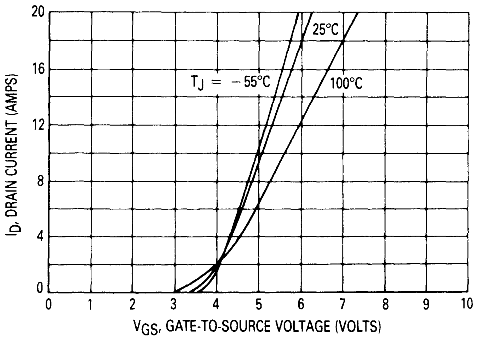


Figure 3. Transfer Characteristics

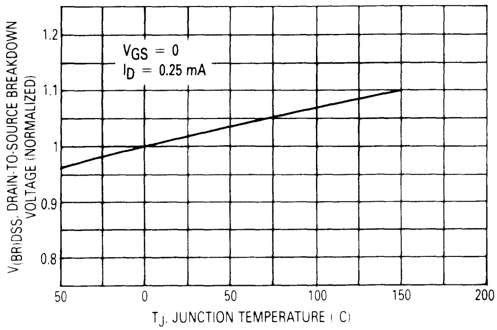


Figure 4. Breakdown Voltage Variation With Temperature

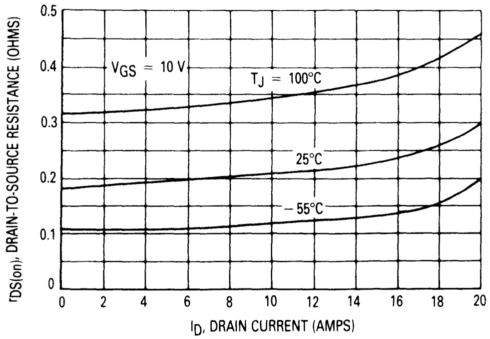


Figure 5. On-Resistance versus Drain Current

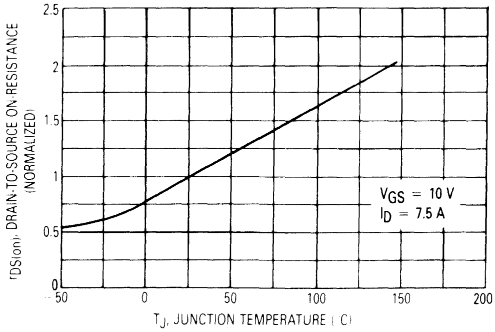


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

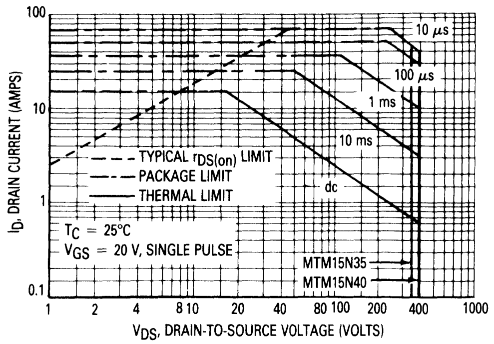


Figure 7. Maximum Rated Forward Biased Safe Operating Area

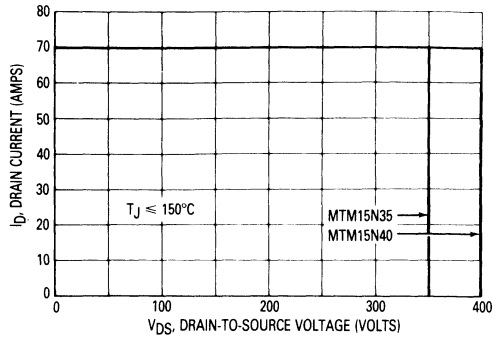


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

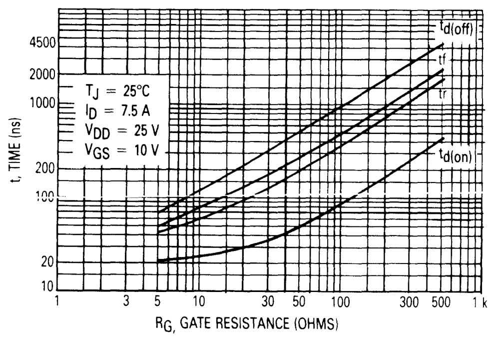


Figure 9. Resistive Switching Time Variation With Gate Resistance

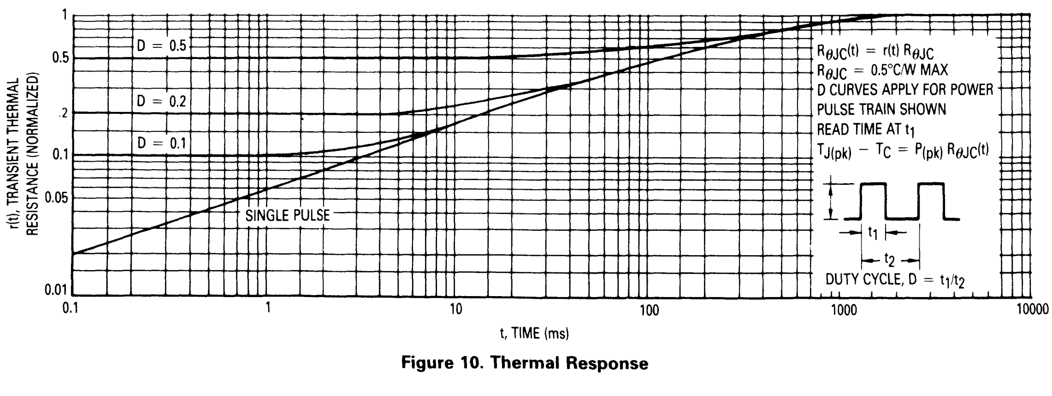


Figure 10. Thermal Response

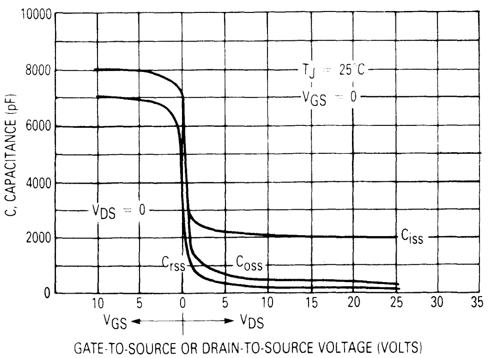


Figure 11. Capacitance Variation

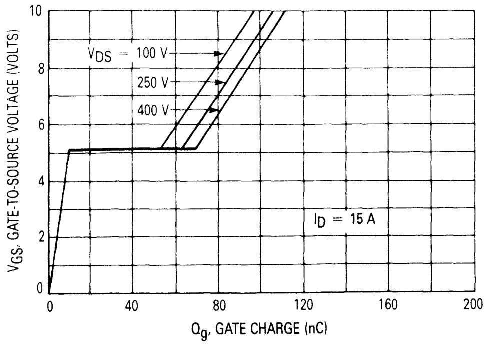


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

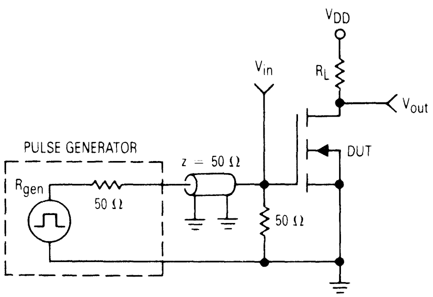


Figure 13. Switching Test Circuit

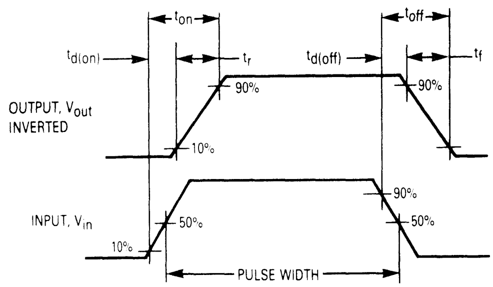
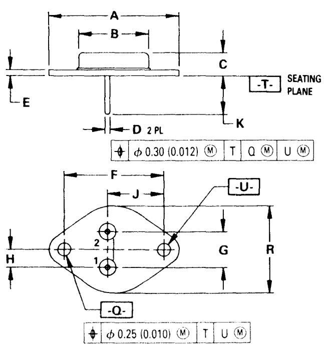


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 197A-02
TO-204AE

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

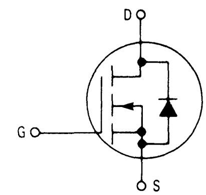
N-Channel Enhancement-Mode Silicon Gate TMOS

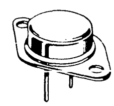
MTM15N45
MTM15N50

TMOS POWER FETs
15 AMPERES
$r_{DS(on)}$ = 0.4 OHM
450 and 500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 197A-02
TO-204AE

3

MAXIMUM RATINGS

Rating	Symbol	MTM 15N45	MTM 15N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 65		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.5 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM15N45		$V_{(BR)DSS}$	450	—	Vdc
MTM15N50			500	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	0.2	mAdc
(V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	1	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7.5 Adc)		$V_{DS(on)}$	—	6	Vdc
(I_D = 15 Adc, T_J = 100°C)			—	5.8	
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	450	
Fall Time		t_f	—	180	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	110 (Typ)	160	nC
Gate-Source Charge		Q_{gs}	50 (Typ)	—	
Gate-Drain Charge		Q_{gd}	60 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	1200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

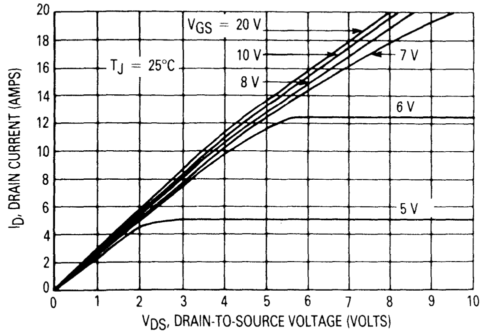


Figure 1. On-Region Characteristics

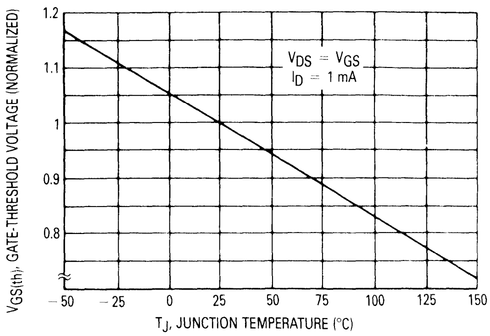


Figure 2. Gate-Threshold Voltage Variation With Temperature

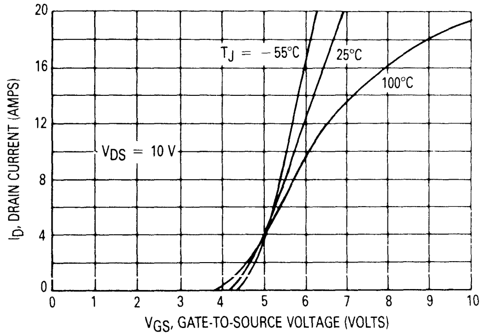


Figure 3. Transfer Characteristics

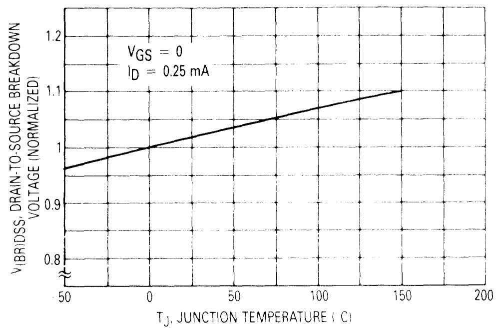


Figure 4. Breakdown Voltage Variation With Temperature

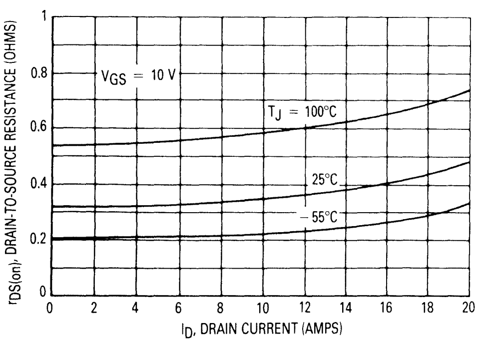


Figure 5. On-Resistance versus Drain Current

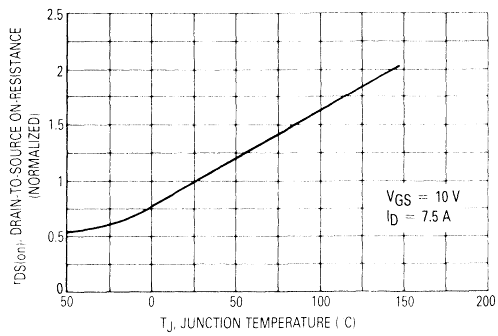


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

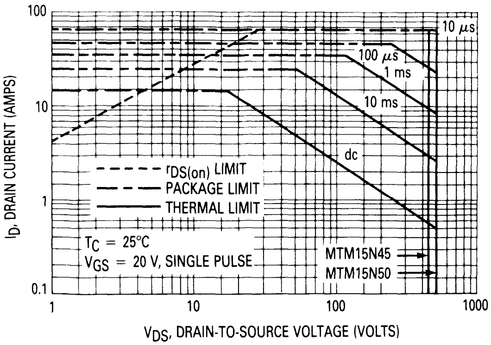


Figure 7. Maximum Rated Forward Biased Safe Operating Area

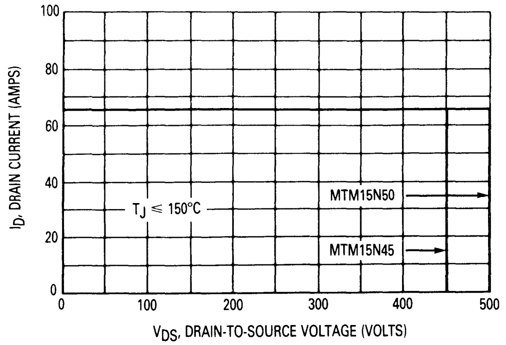


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

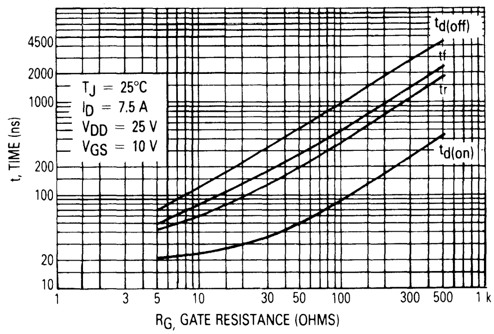


Figure 9. Resistive Switching Time Variation versus Gate Resistance

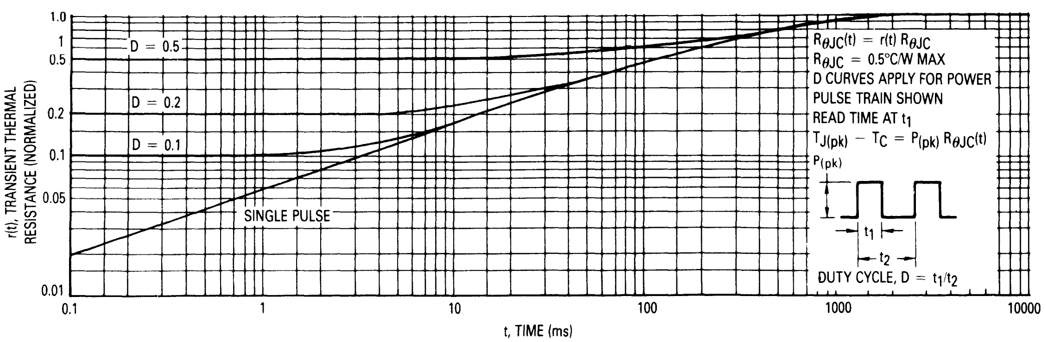


Figure 10. Thermal Response

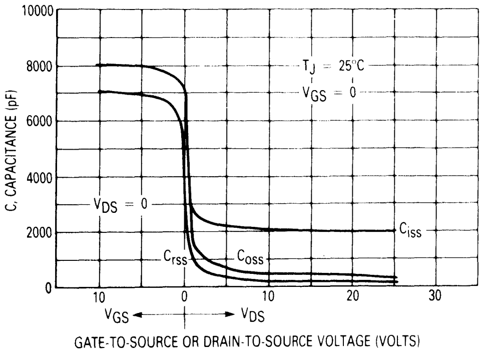


Figure 11. Capacitance Variation

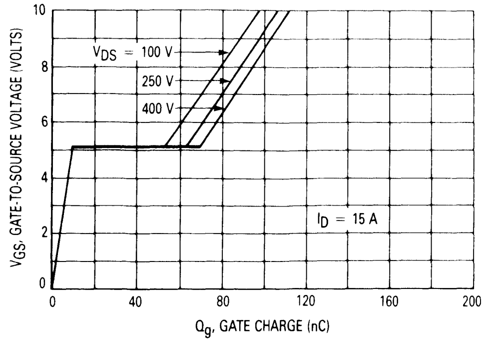


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

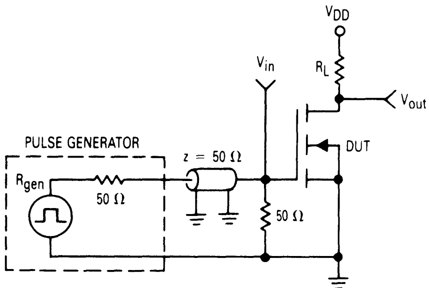


Figure 13. Switching Test Circuit

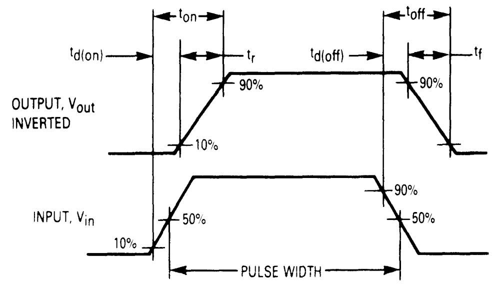
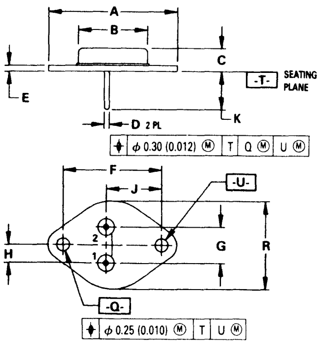


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

CASE 197A-02
TO-204AE

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM20N10 MTP20N08 MTP20N10

Designer's Data Sheet

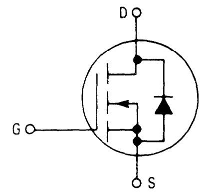
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

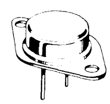
TMOS POWER FETs
20 AMPERES
$r_{DS(on)}$ = 0.15 OHM
80 and 100 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

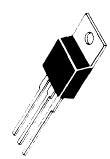
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



3



MTM20N10
CASE 1-04
TO-204AA



MTP20N08
MTP20N10
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM20N10	MTP20N08 MTP20N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \le 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	20 60		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.25	°C/W
Junction to Ambient TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP20N08 MTM/MTP20N10		$V_{(BR)DSS}$	 80 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 3.6 3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 10 A)		g_{FS}	6	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	28 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	15 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.8 (Typ)	3.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

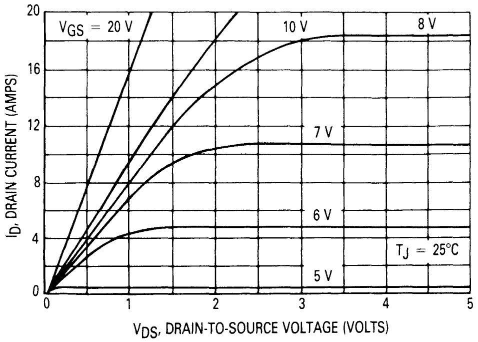


Figure 1. On-Region Characteristics

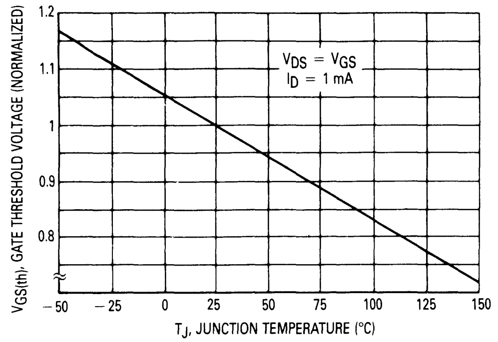


Figure 2. Gate-Threshold Voltage Variation With Temperature

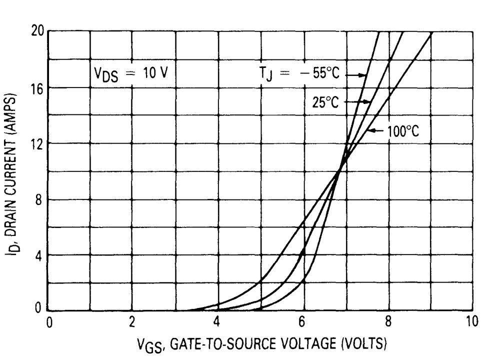


Figure 3. Transfer Characteristics

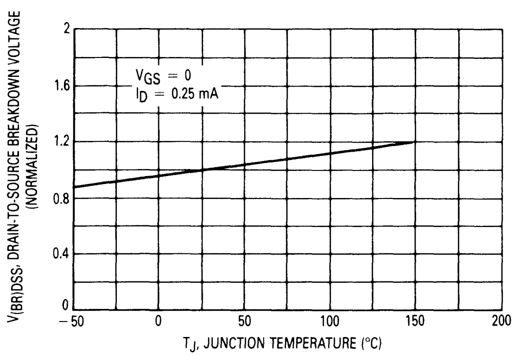


Figure 4. Breakdown Voltage Variation With Temperature

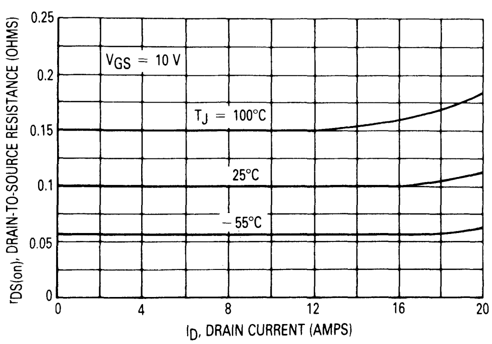


Figure 5. On-Resistance versus Drain Current

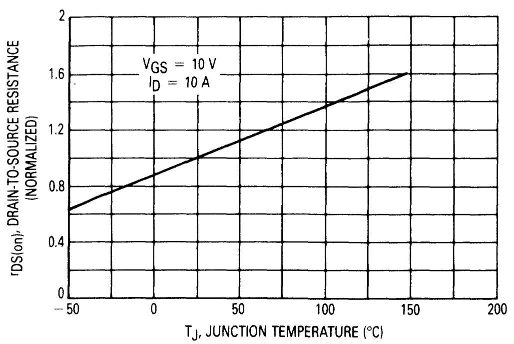


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

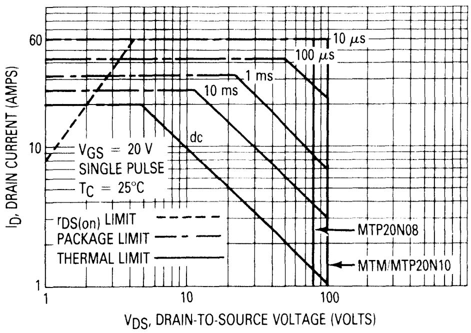


Figure 7. Maximum Rated Forward Biased Safe Operating Area

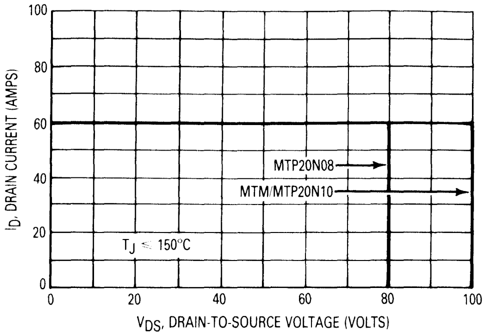


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

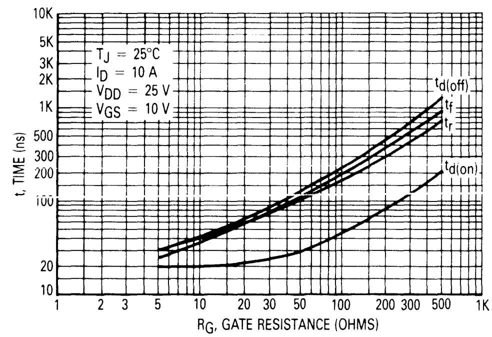


Figure 9. Resistive Switching Time versus Gate Resistance

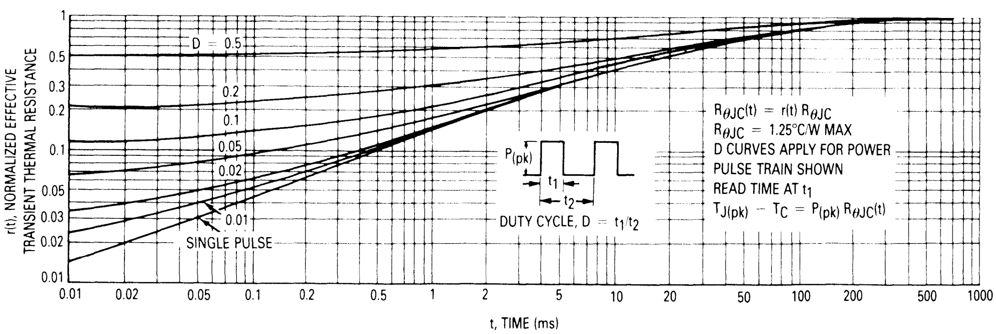


Figure 10. Thermal Response

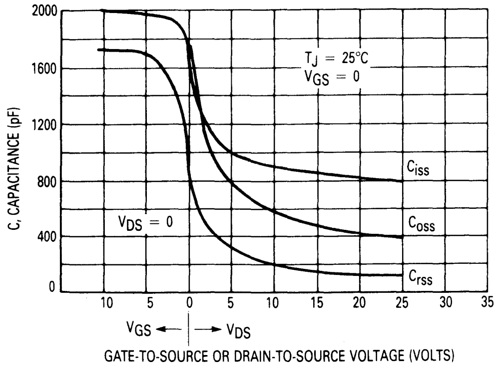


Figure 11. Capacitance Variation

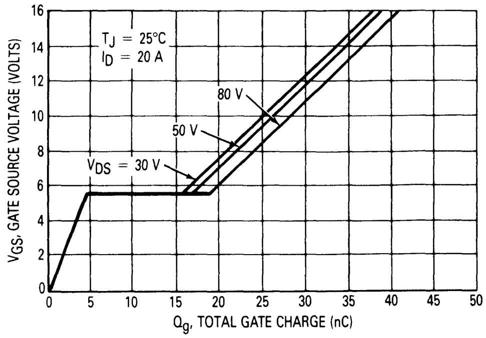


Figure 12. Gate Charge versus Gate-To-Source Voltage

3

RESISTIVE SWITCHING

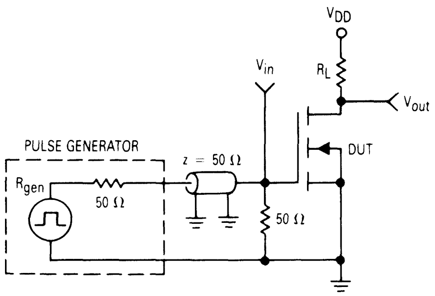


Figure 13. Switching Test Circuit

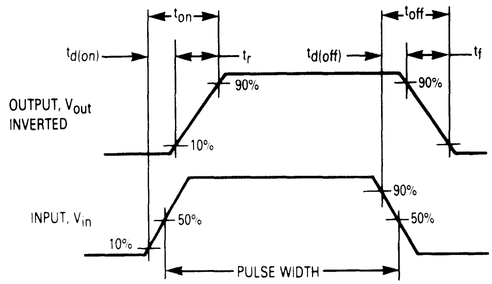
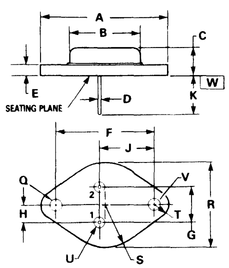


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

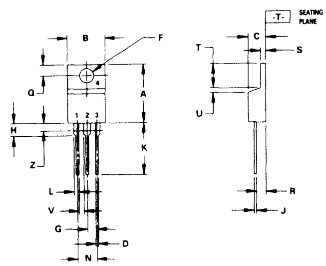


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS
2. POSITIONAL TOLERANCE FOR HOLE Q:
   | ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ |
3. POSITIONAL TOLERANCE FOR LEADS:
   | ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ |

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

3

MTM25N05
MTM25N06
MTP25N05
MTP25N06

Designer's Data Sheet

Power Field Effect Transistor

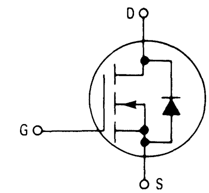
N-Channel Enhancement-Mode Silicon Gate TMOS

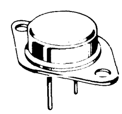
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

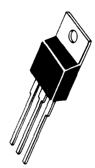
TMOS™

TMOS POWER FETs
25 AMPERES
$r_{DS(on)}$ = 0.08 OHM
50 and 60 VOLTS





MTM25N05
MTM25N06
CASE 1-04
TO-204AA



MTP25N05
MTP25N06
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 25N05	MTM or MTP 25N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 80		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Junction to Ambient — TO-204	$R_{\theta JA}$	30	
TO-220		62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTM/MTP25N05	$V_{(BR)DSS}$	50	—	Vdc
	MTM/MTP25N06		60	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$r_{DS(on)}$	—	0.08	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 25 Adc)		$V_{DS(on)}$	—	2.4	Vdc
(I_D = 12.5 Adc, T_J = 100°C)			—	2	
Forward Transconductance (V_{DS} = 15 V, I_D = 12.5 A)		g_{FS}	6	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	300	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	60 (Typ)	150	nC
Gate-Source Charge		Q_{gs}	32 (Typ)	—	
Gate-Drain Charge		Q_{gd}	28 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

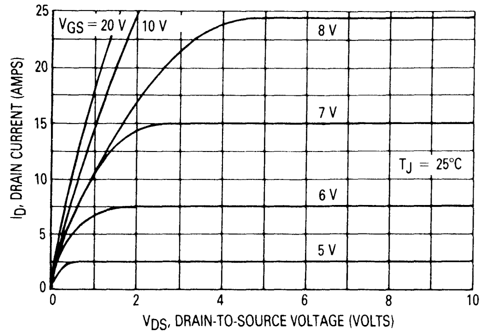


Figure 1. On-Region Characteristics

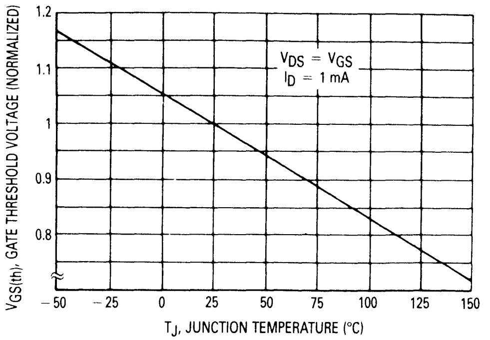


Figure 2. Gate-Threshold Voltage Variation With Temperature

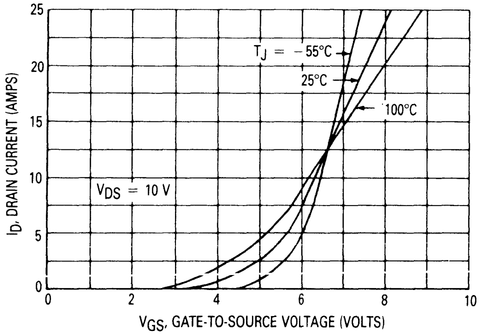


Figure 3. Transfer Characteristics

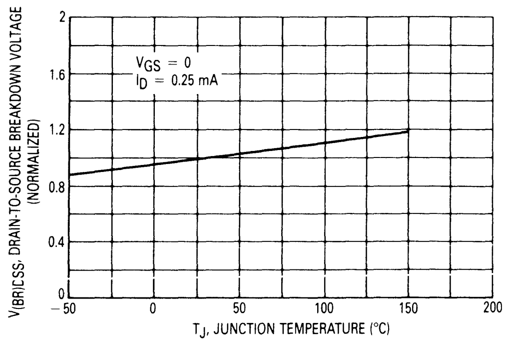


Figure 4. Breakdown Voltage Variation With Temperature

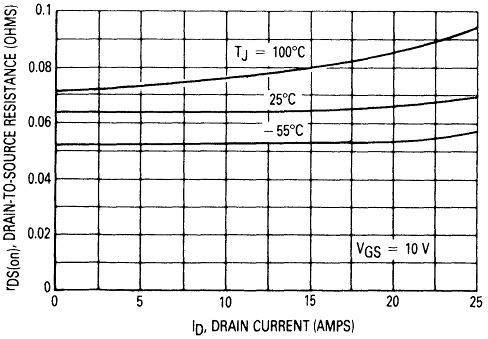


Figure 5. On-Resistance versus Drain Current

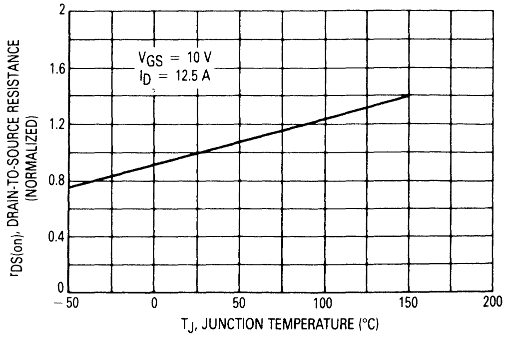


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

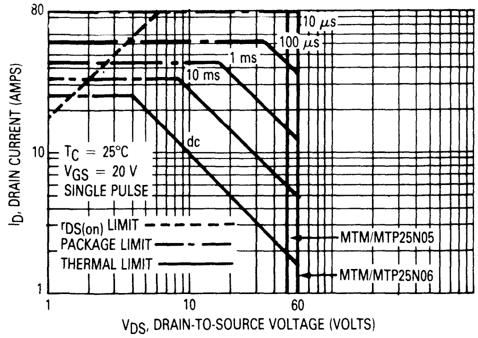


Figure 7. Maximum Rated Forward Biased Safe Operating Area

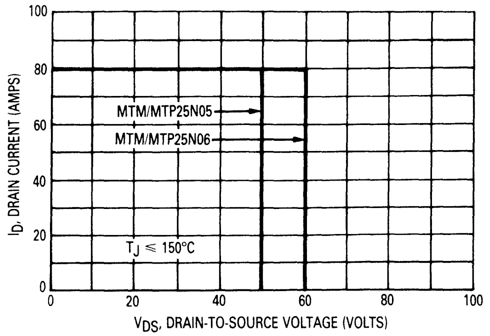


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

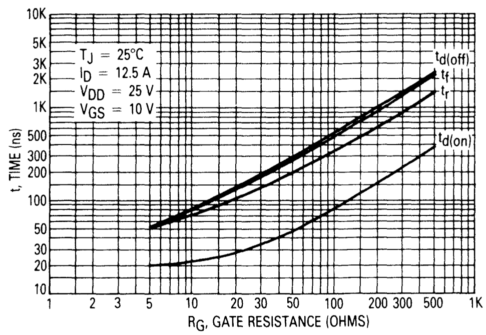


Figure 9. Resistive Switching Time versus Gate Resistance

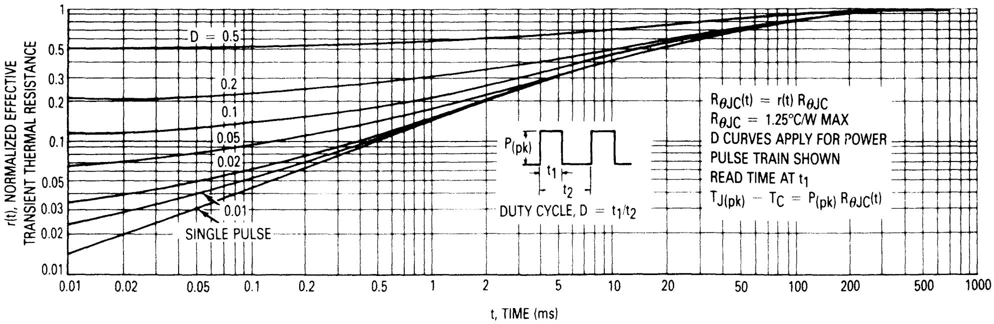


Figure 10. Thermal Response

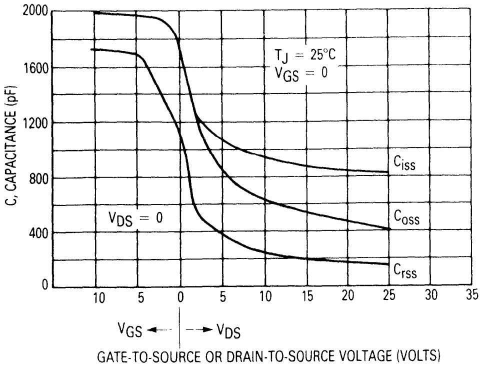


Figure 11. Capacitance Variation

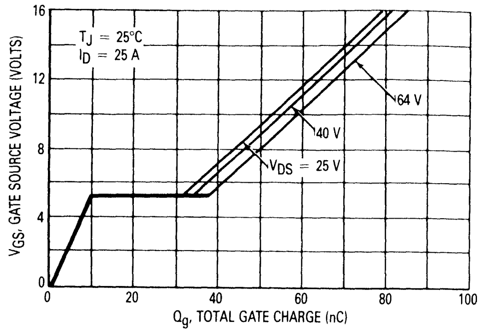


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

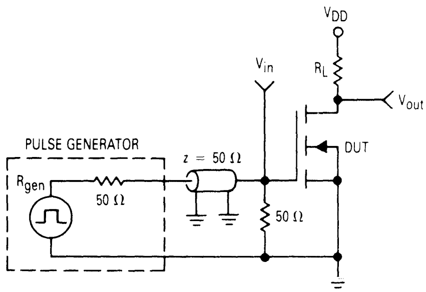


Figure 13. Switching Test Circuit

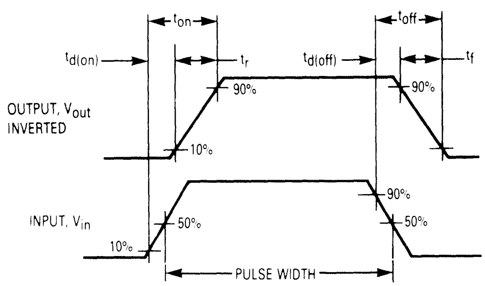
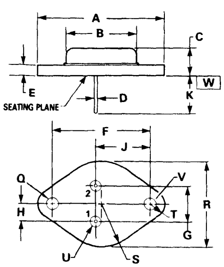


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

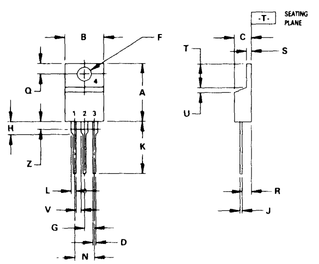


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.151	0.165

NOTES:
1. DIAMETER V AND SURFACE W ARE DATUMS.
2. POSITIONAL TOLERANCE FOR HOLE Q:
   ⌖ | ϕ 0.25 (0.010) Ⓜ | W | V Ⓜ
3. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | ϕ 0.30 (0.012) Ⓜ | W | V Ⓜ | Q Ⓜ

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MTM25N05L
MTM25N06L
MTP25N05L
MTP25N06L

Designer's Data Sheet

Power Field Effect Transistors

N-Channel Enhancement-Mode Silicon Gate TMOS

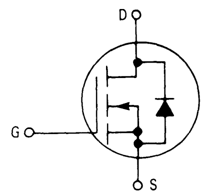
TMOS

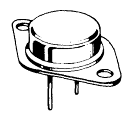
TMOS POWER FETs
LOGIC LEVEL
25 AMPERES
$r_{DS(on)}$ = 0.1 OHM
50 and 60 VOLTS

3

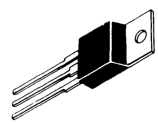
These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





MTM25N05L
MTM25N06L
CASE 1-04
TO-204AA



MTP25N05L
MTP25N06L
CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM25N05L MTP25N05L	MTM25N06L MTP25N06L	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±15 ±20		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 80		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.25	°C/W
— Junction to Ambient TO-204 TO-220	$R_{\theta JA}$	30 62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM/MTP25N05L MTM/MTP25N06L	$V_{(BR)DSS}$	 50 60	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 50	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	2	Vdc
(T_J = 100°C)			0.75	1.5	
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 12.5 Adc)		$r_{DS(on)}$	—	0.1	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 25 Adc)		$V_{DS(on)}$	—	2.7	Vdc
(I_D = 12.5 Adc, T_J = 100°C)			—	2	
Forward Transconductance (V_{DS} = 15 V, I_D = 12.5 A)		g_{FS}	9	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	1400	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	4800	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	250	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	4000	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	750	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 12.5 A, V_{GS} = 5 V, R_{gen} = 50 ohms) See Figures 8 and 9	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	300	
Fall Time		t_f	—	350	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 25 A, V_{GS} = 5 Vdc) See Figures 6 and 10	Q_g	24 (Typ)	36	nC
Gate-Source Charge		Q_{gs}	13 (Typ)	—	
Gate-Drain Charge		Q_{gd}	11 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figures 14 and 15	V_{SD}	2.5 (typ)	—	Vdc
Forward Turn-On Time		t_{on}	50 (typ)	—	ns
Reverse Recovery Time		t_{rr}	300 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

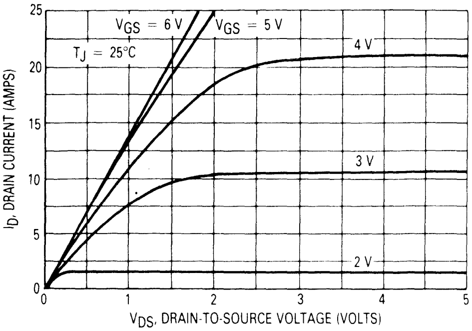


Figure 1. On-Region Characteristics

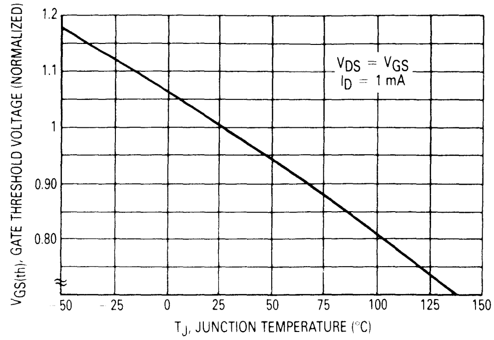


Figure 2. Gate-Threshold Voltage Variation With Temperature

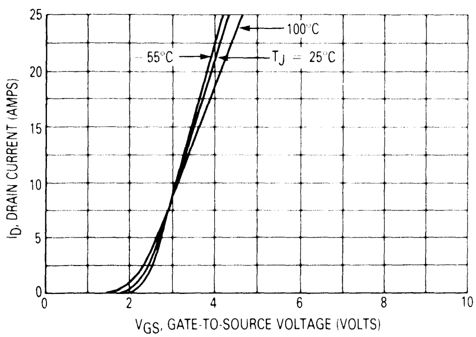


Figure 3. Transfer Characteristics

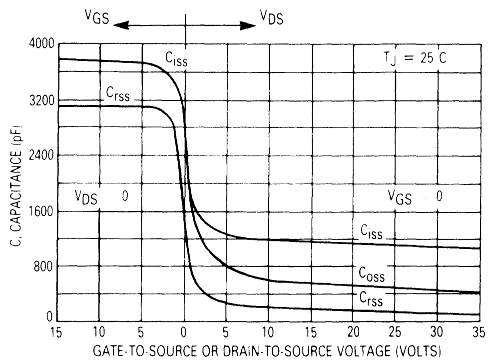


Figure 4. Capacitance Variation

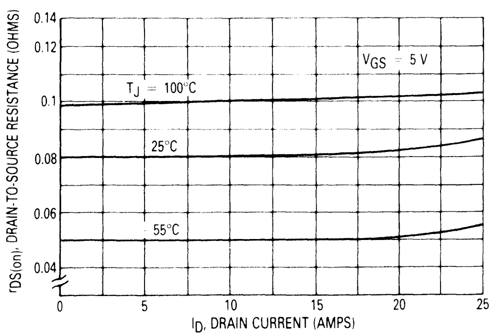


Figure 5. On-Resistance versus Drain Current

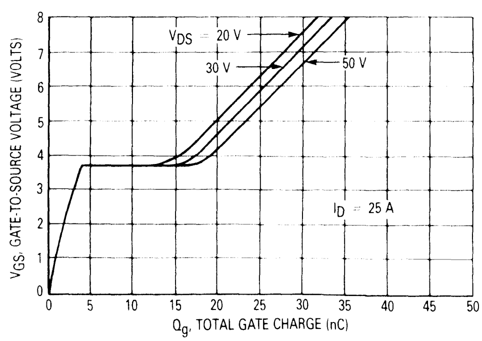


Figure 6. Gate Charge Variation

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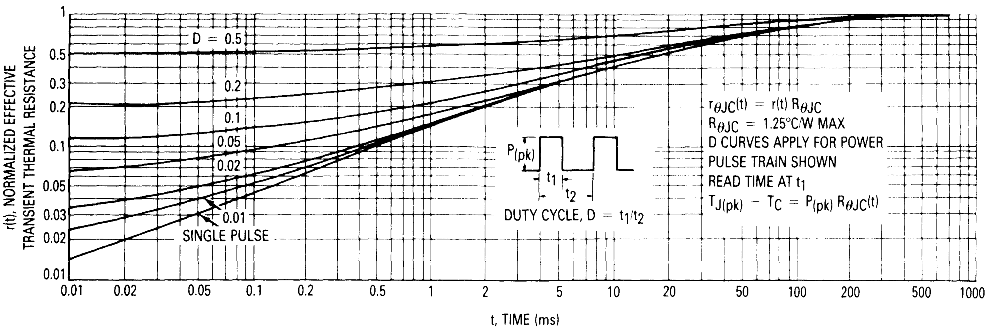


Figure 7. Thermal Response

RESISTIVE SWITCHING

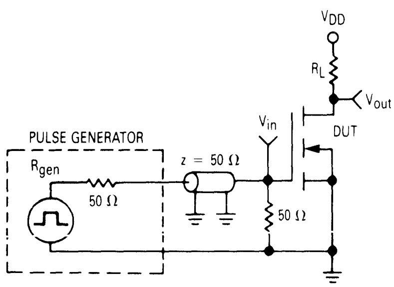


Figure 8. Switching Test Circuit

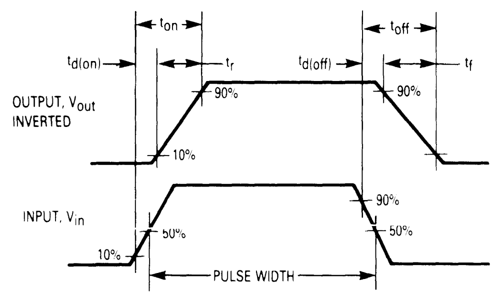
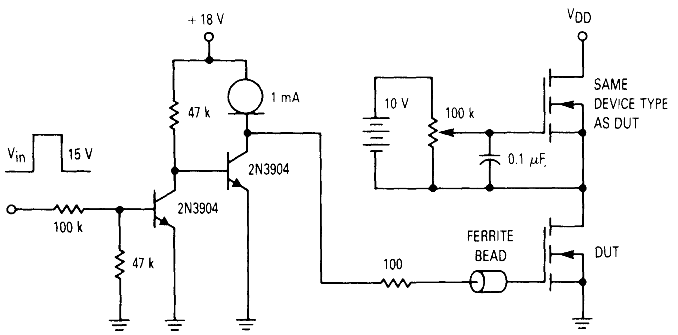


Figure 9. Switching Waveforms



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

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The switching safe operating area (SOA) of Figure 12 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 12 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

3

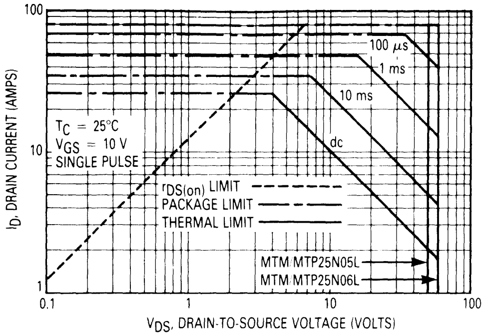


Figure 11. Maximum Rated Forward Biased Safe Operating Area

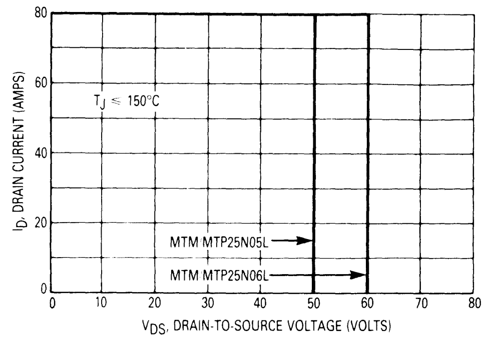
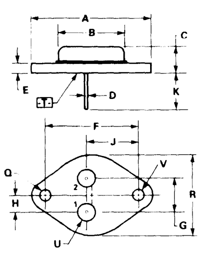


Figure 12. Maximum Rated Switching Safe Operating Area

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
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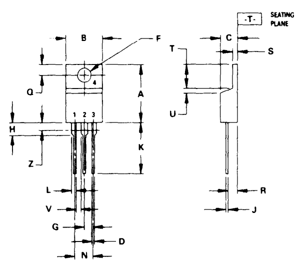
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.151	0.165
R	—	26.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.81	4.19	0.151	0.165

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN

NOTES:
1. DIMENSIONS Q AND V ARE DATUMS.
2. -T- IS SEATING PLANE AND DATUM.
3. POSITIONAL TOLERANCE FOR MOUNTING HOLE Q:
⌖ 0.13 (0.005) Ⓜ T V Ⓜ
FOR LEADS:
⌖ 0.13 (0.005) Ⓜ T V Ⓜ Q Ⓜ
4. DIMENSIONS AND TOLERANCES PER ANSI Y14.5, 1973.

CASE 1-04
TO-204AA



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

Designer's Data Sheet

Power Field Effect Transistor

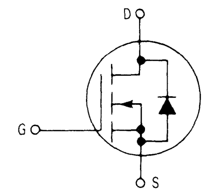
N-Channel Enhancement-Mode Silicon Gate TMOS

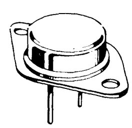
MTM40N20

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FET
40 AMPERES
$r_{DS(on)}$ = 0.08 OHM
200 VOLTS





CASE 197A-02
TO-204AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	40 200	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.5 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM40N20	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc)		$r_{DS(on)}$	—	0.08	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 40 Adc) (I_D = 20 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 3.8 3.2	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 20 A)		g_{FS}	10	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	5500	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	400	
Fall Time		t_f	—	250	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	85 (Typ)	95	nC
Gate-Source Charge		Q_{gs}	45 (Typ)	—	
Gate-Drain Charge		Q_{gd}	40 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.0 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

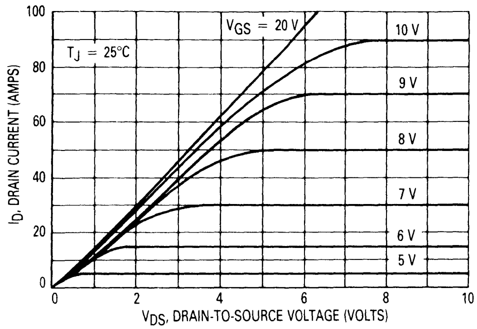

Figure 1. On-Region Characteristics

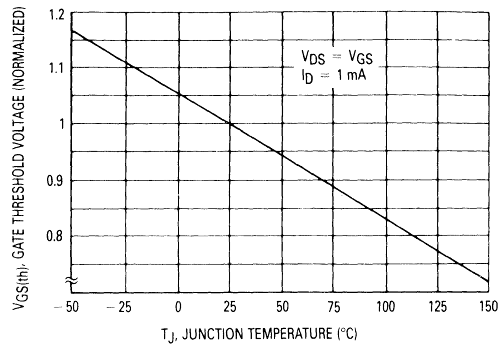

Figure 2. Gate-Threshold Voltage Variation With Temperature

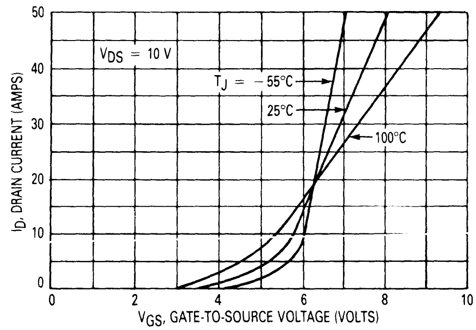

Figure 3. Transfer Characteristics

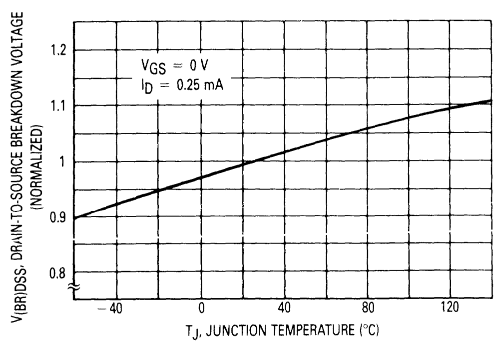

Figure 4. Breakdown Voltage Variation With Temperature

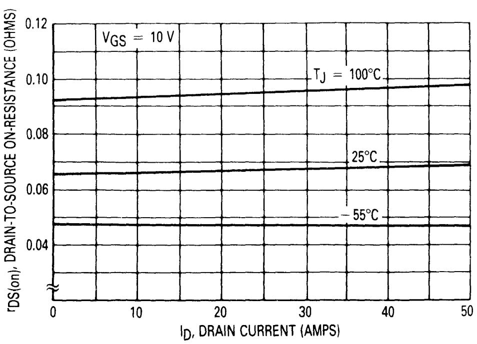

Figure 5. On-Resistance versus Drain Current

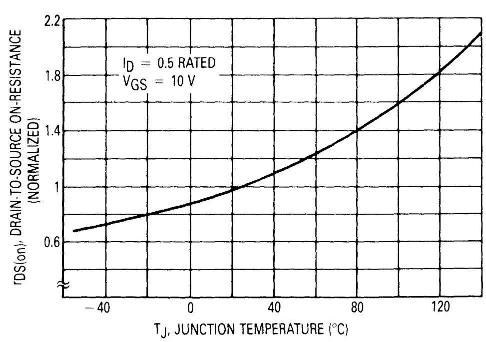

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

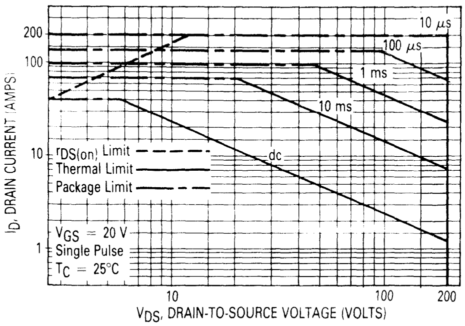

Figure 7. Maximum Rated Forward Biased Safe Operating Area

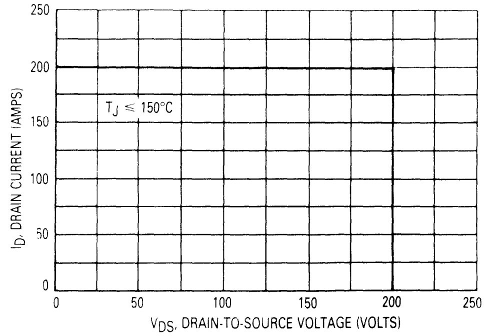

Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

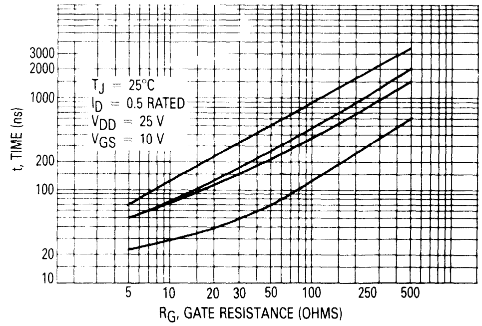


Figure 9. Resistive Switching Time Variation versus Gate Resistance

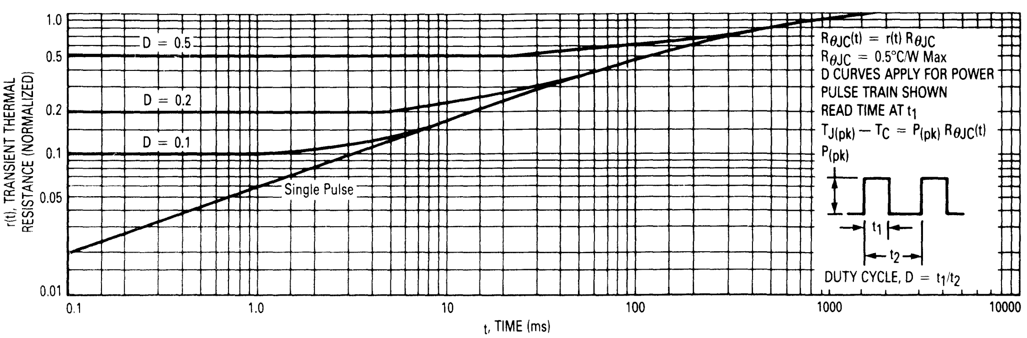


Figure 10. Thermal Response

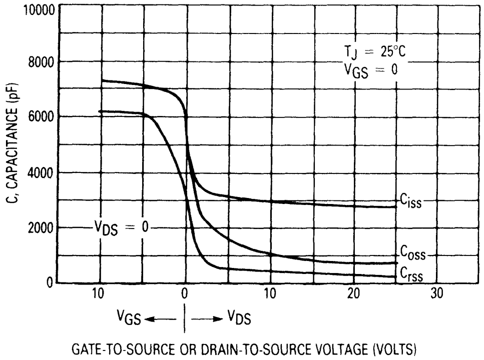


Figure 11. Capacitance Variation

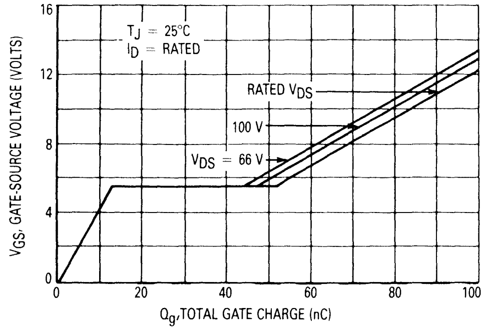


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

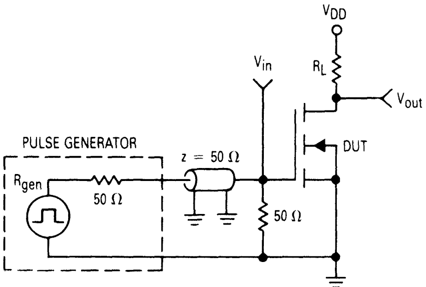


Figure 13. Switching Test Circuit

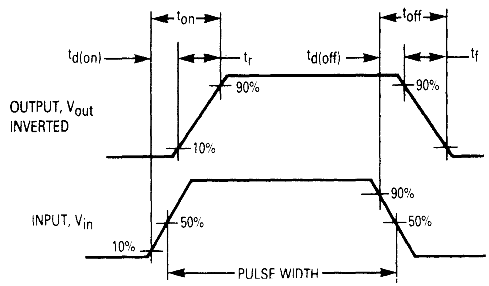
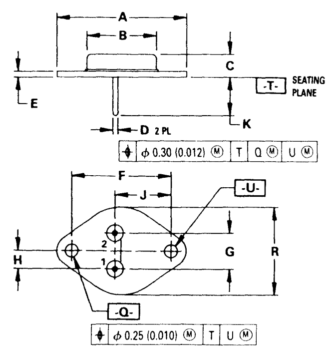


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 197A-02
TO-204AE

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM45N05E
MTP45N05E

Designer's Data Sheet

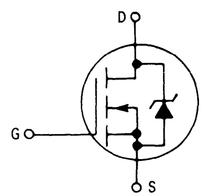
TMOS IV
Power Field Effect Transistors
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER FETs
45 AMPERES
$r_{DS(on)}$ = 0.035 OHM
50 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to BUZ11

TMOS



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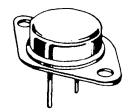
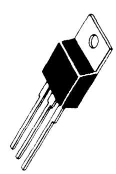


MTM45N05E
CASE 197A-02
TO-204AE



MTP45N05E
CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	45 145	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient MTM45N05E MTP45N05E	 $R_{\theta JC}$ $R_{\theta JA}$	 1.0 30 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25$ mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, $V_{GS} = 0$)			—	10	
(V_{DS} = Rated V_{DSS}, $V_{GS} = 0$, $T_J = 125°C$)			—	100	
Gate-Body Leakage Current, Forward ($V_{GSF} = 20$ Vdc, $V_{DS} = 0$)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20$ Vdc, $V_{DS} = 0$)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage		$V_{GS(th)}$			Vdc
($V_{DS} = V_{GS}$, $I_D = 250\ \mu$A)			2.0	4	
$T_J = 100°C$			1.5	3.5	
Static Drain-Source On-Resistance ($V_{GS} = 10$ Vdc, $I_D = 29$ Adc)		$r_{DS(on)}$	—	0.035	Ohm
Drain-Source On-Voltage ($V_{GS} = 10$ V)		$V_{DS(on)}$			Vdc
($I_D = 45$ Adc)			—	1.5	
($I_D = 22.5$ Adc, $T_J = 100°C$)			—	0.9	
Forward Transconductance ($V_{DS} = 15$ V, $I_D = 29$ A)		g_{FS}	17	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Inductive Switching Energy See Figures 14 and 15		W_{DSR}			mJ
($I_D = 145$ A, $V_{DD} = 25$ V, $T_C = 25°C$, Single Pulse, Non-repetitive)			—	50	
($I_D = 45$ A, $V_{DD} = 25$ V, $T_C = 25°C$, P.W. $\leq 45\ \mu s$, Duty Cycle $\leq 1\%$)			—	110	
($I_D = 18$ A, $V_{DD} = 25$ V, $T_C = 100°C$, P.W. $\leq 45\ \mu s$, Duty Cycle $\leq 1\%$)			—	40	
DYNAMIC CHARACTERISTICS					
Input Capacitance	($V_{DS} = 25$ V, $V_{GS} = 0$, f = 1 MHz) See Figure 16	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* ($T_J = 100°C$)					
Turn-On Delay Time	($V_{DD} = 25$ V, $I_D = 29$ A $R_{gen} = 4.7$ ohms) See Figure 9	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	70	
Fall Time		t_f	—	25	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, $V_{GS} = 10$ V) See Figures 17 and 18	Q_g	55 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	30 (Typ)	—	
Gate-Drain Charge		Q_{gd}	25 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	($I_S = 46$ A $V_{GS} = 0$ $di_S/dt = 100\ A/\mu s$)	V_{SD}	1.8 (Typ)	2.2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq 300\ \mu s$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

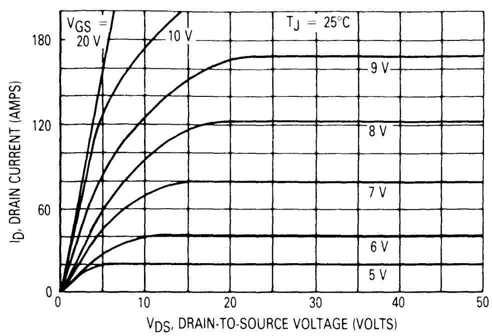


Figure 1. On-Region Characteristics

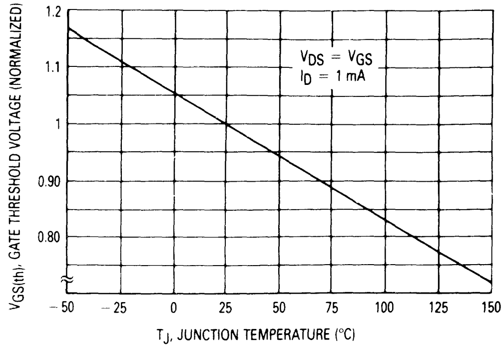


Figure 2. Gate-Threshold Voltage Variation With Temperature

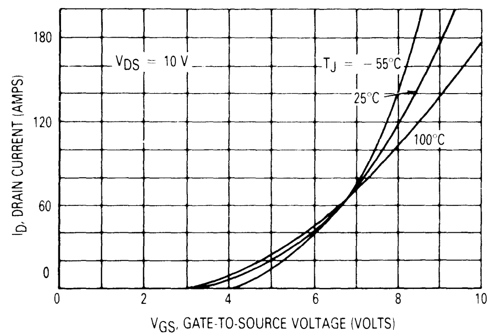


Figure 3. Transfer Characteristics

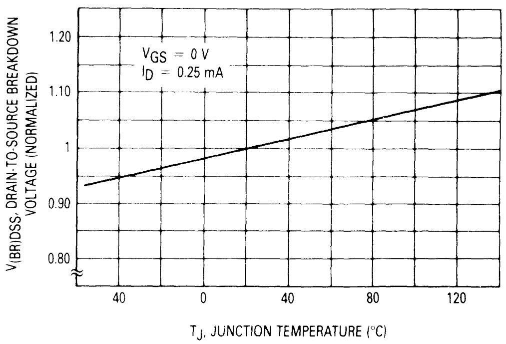


Figure 4. Breakdown Voltage Variation With Temperature

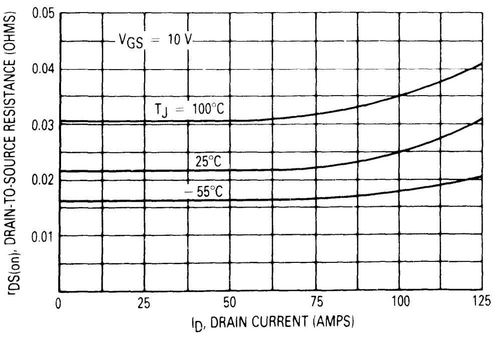


Figure 5. On-Resistance versus Drain Current

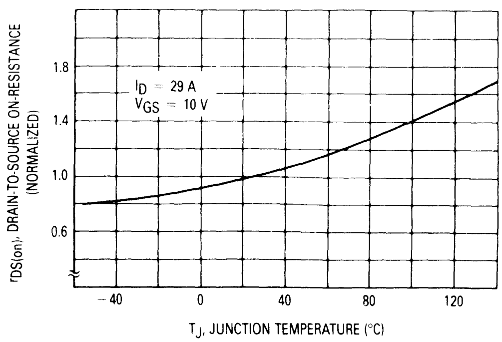


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

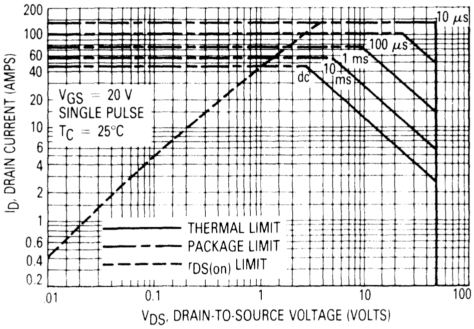


Figure 7. Maximum Rated Forward Bias Safe Operating Area

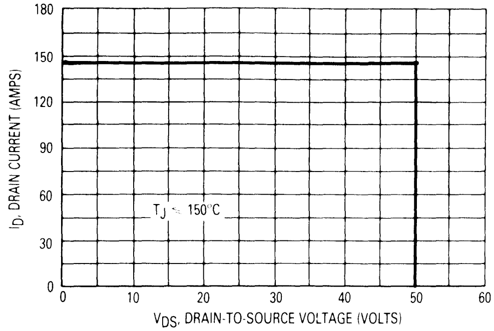


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

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The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

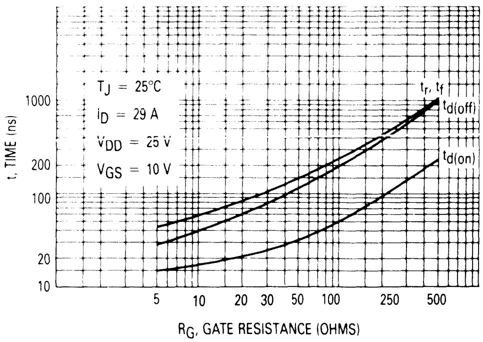


Figure 9. Resistive Switching Time Variation versus Gate Resistance

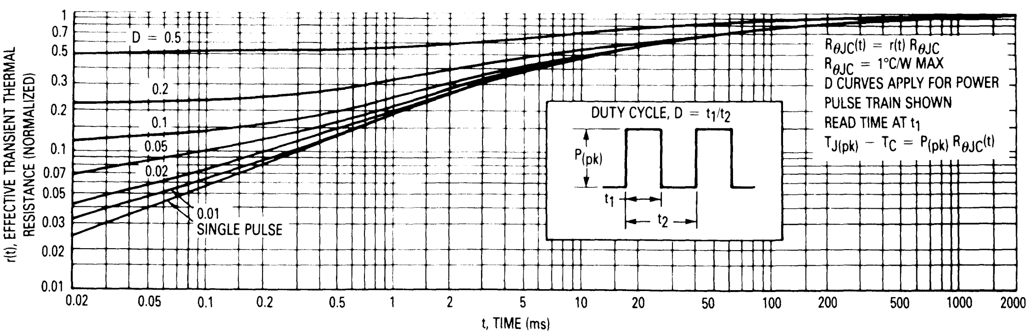


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

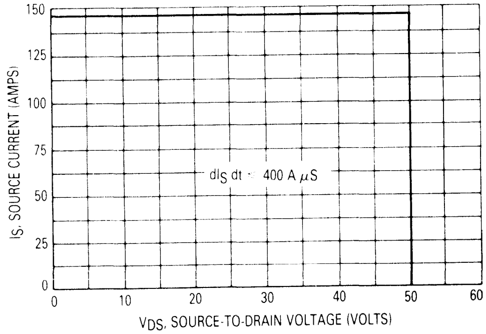


Figure 12. Commutating Safe Operating Area (CSOA)

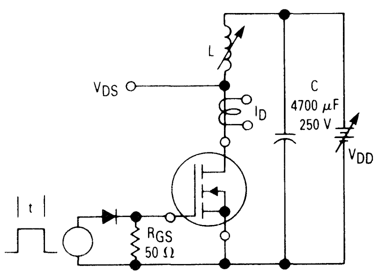


Figure 14. Unclamped Inductive Switching Test Circuit

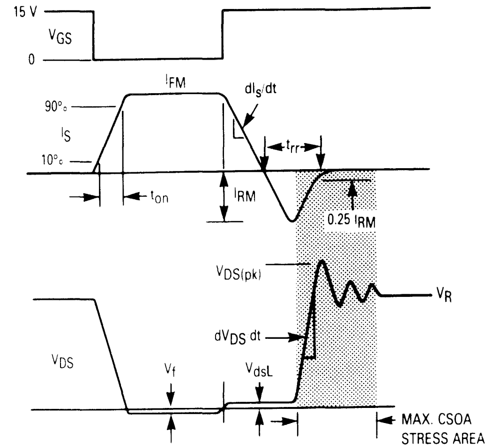


Figure 11. Commutating Waveforms

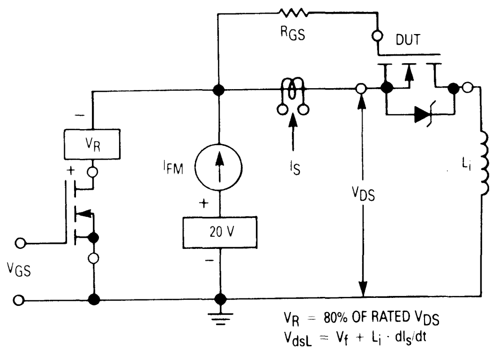
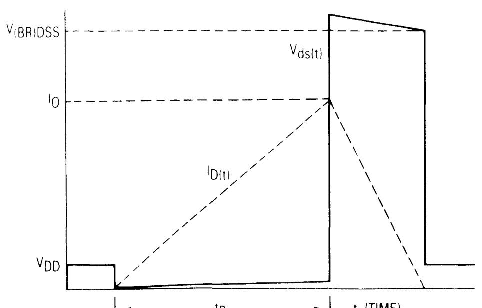


Figure 13. Commutating Safe Operating Area Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

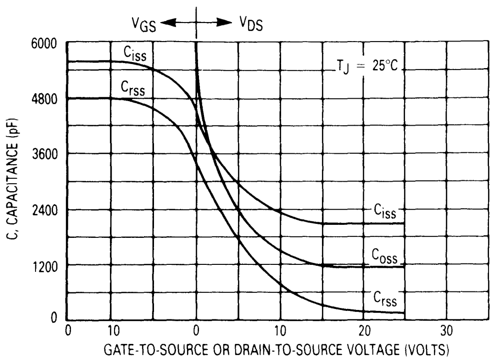


Figure 16. Capacitance Variation

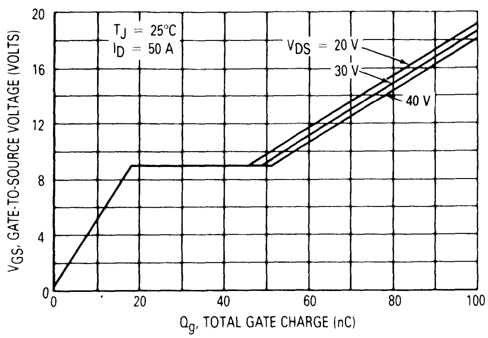
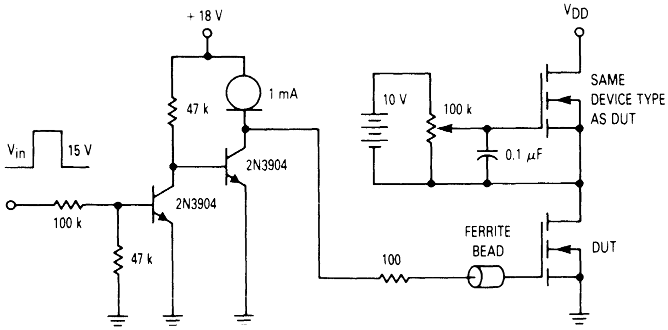


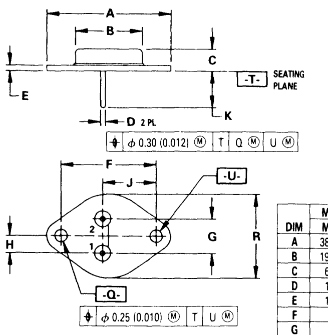
Figure 17. Gate Charge versus Gate-to-Source Voltage



$V_{in} = 15\ V_{pk}$; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

CASE 197A-02
MTM45N05E

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

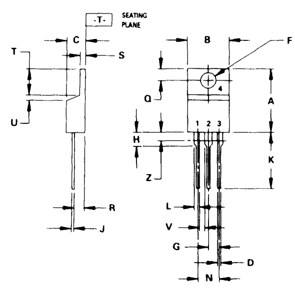
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 221A-04
MTP45N05E

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED



MTM45N15

Designer's Data Sheet

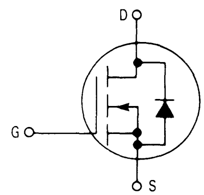
Power Field Effect Transistor

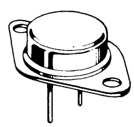
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
45 AMPERES
$r_{DS(on)}$ = 0.06 OHM
150 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 197A-02
TO-204AE

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	45 225	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.5 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTM45N15	$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 22.5 Adc)		$r_{DS(on)}$	—	0.06	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 45 Adc) (I_D = 22.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 3.24 2.7	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 22.5 A)		g_{FS}	10	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	5500	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	300	
Turn-Off Delay Time		$t_{d(off)}$	—	400	
Fall Time		t_f	—	250	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	85 (Typ)	95	nC
Gate-Source Charge		Q_{gs}	45 (Typ)	—	
Gate-Drain Charge		Q_{gd}	40 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

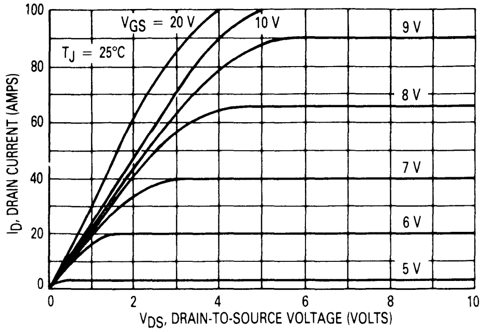


Figure 1. On-Region Characteristics

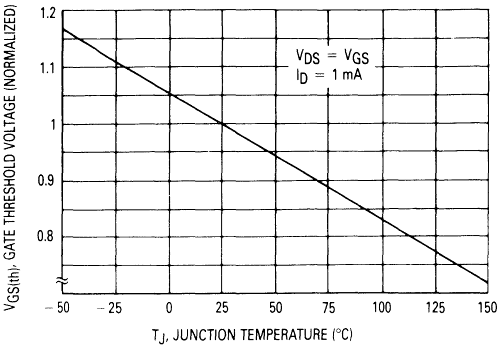


Figure 2. Gate-Threshold Voltage Variation With Temperature

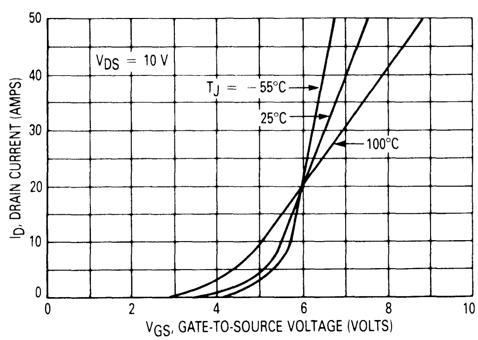


Figure 3. Transfer Characteristics

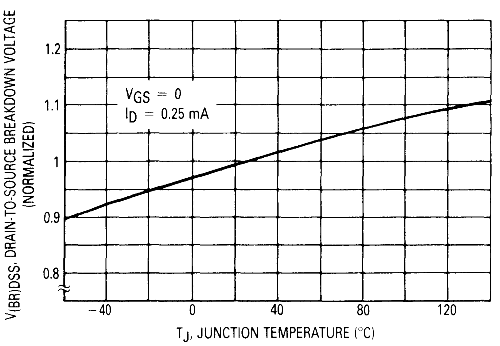


Figure 4. Breakdown Voltage Variation With Temperature

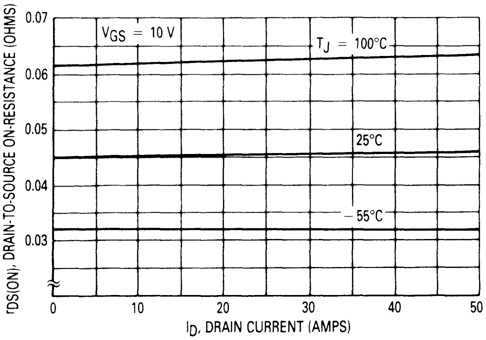


Figure 5. On-Resistance versus Drain Current

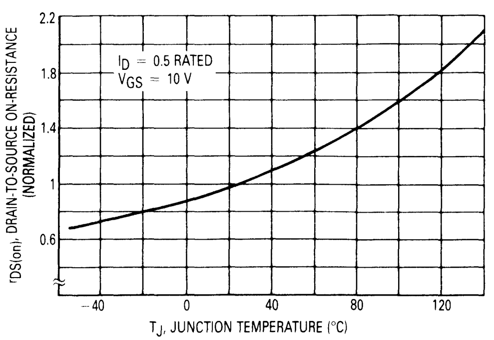


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

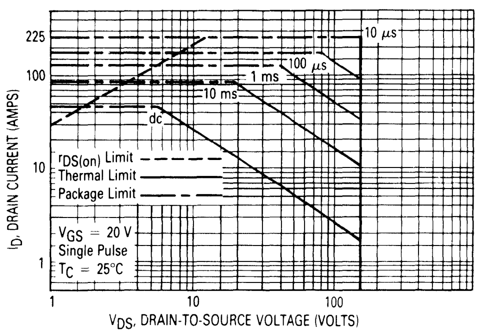
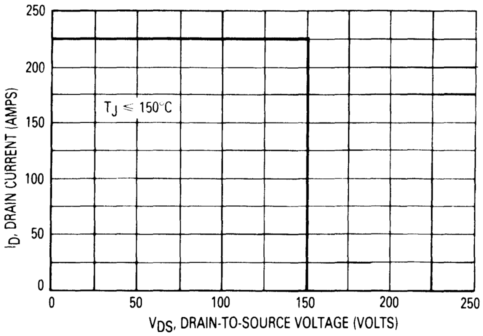


Figure 7. Maximum Rated Forward Biased Safe Operating Area



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FORWARD BIASED SAFE OPERATING AREA

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The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

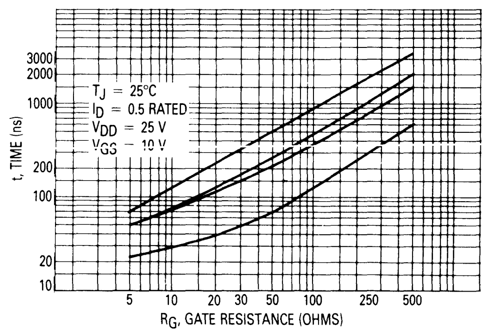


Figure 9. Resistive Switching Time Variation versus Gate Resistance

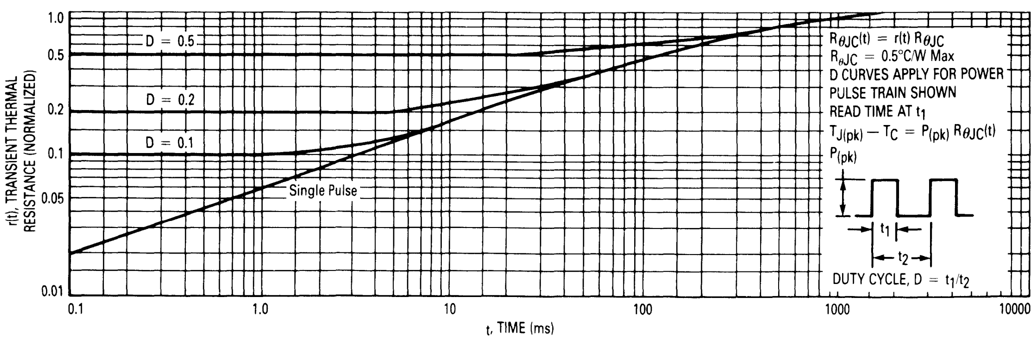


Figure 10. Thermal Response

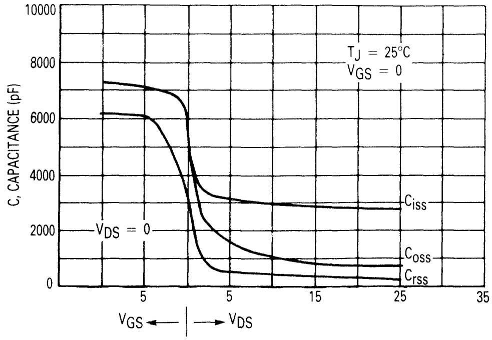


Figure 11. Capacitance Variation

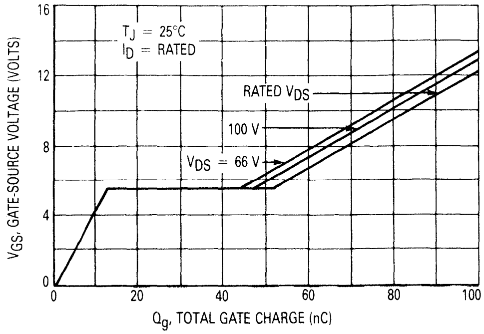


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

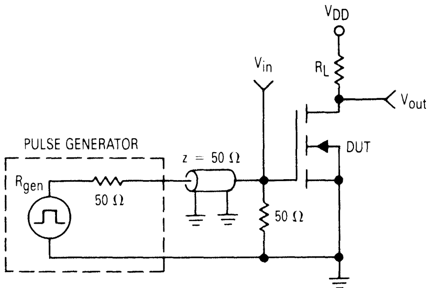


Figure 13. Switching Test Circuit

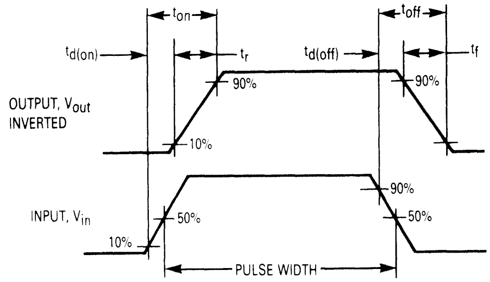
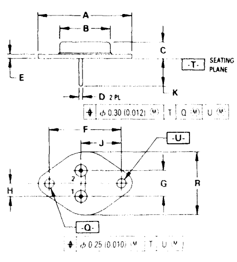


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
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K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 197A-02
TO-204AE

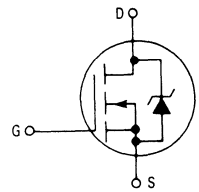
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM50N05E
MTP50N05E

Designer's Data Sheet

TMOS IV
Power Field Effect Transistors
N-Channel Enhancement-Mode Silicon Gate

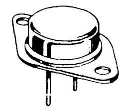
TMOS POWER FETs
50 AMPERES
$r_{DS(on)}$ = 0.028 OHM
50 VOLTS



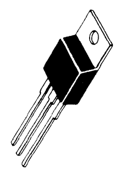
This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- DC Equivalent to IRFZ40

TMOS



MTM50N05E
CASE 197A-02
TO-204AE



MTP50N05E
CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	50 160	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient MTM50N05E MTP50N05E	 $R_{\theta JC}$ $R_{\theta JA}$	 1 30 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 80	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4 3.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 25 Adc)		$r_{DS(on)}$	—	0.028	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 50 Adc) (I_D = 25 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 1.4 1.3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 25 A)		g_{FS}	17	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Inductive Switching Energy See Figures 14 and 15 (I_D = 160 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 50 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 35 μs, Duty Cycle ≤ 1%) (I_D = 20 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 35 μs, Duty Cycle ≤ 1%)		W_{DSR}	 — — —	 55 100 35	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1200	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 4.7 ohms) See Figure 9	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	70	
Fall Time		t_f	—	25	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	55 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	30 (Typ)	—	
Gate-Drain Charge		Q_{gd}	25 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_{SD} = 51 A, V_{GS} = 0, dI_S/dt = 100 A/μs)	V_{SD}	1.9 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	(Typ)	250	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured frrom the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

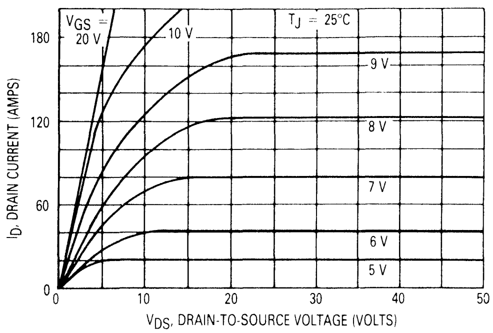


Figure 1. On-Region Characteristics

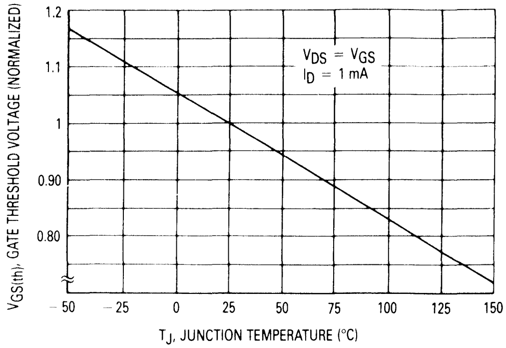


Figure 2. Gate-Threshold Voltage Variation With Temperature

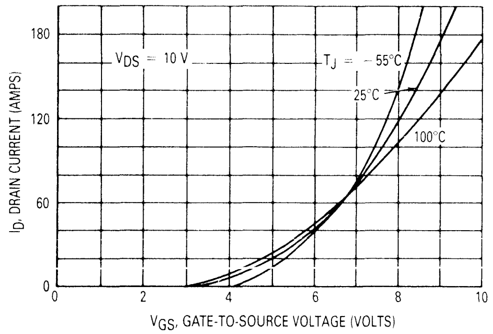


Figure 3. Transfer Characteristics

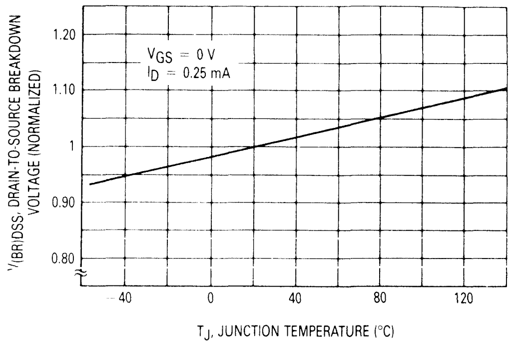


Figure 4. Breakdown Voltage Variation With Temperature

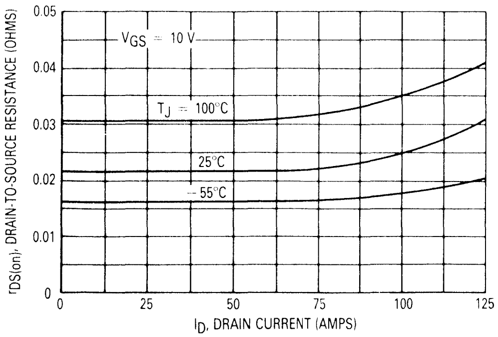


Figure 5. On-Resistance versus Drain Current

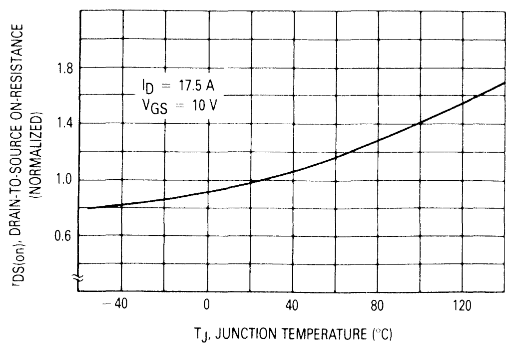


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

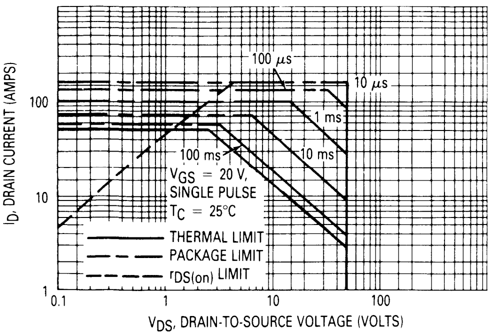


Figure 7. Maximum Rated Forward Biased Safe Operating Area

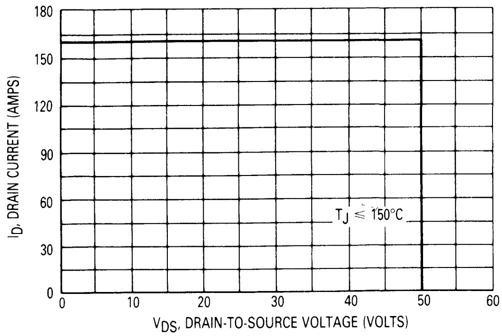


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

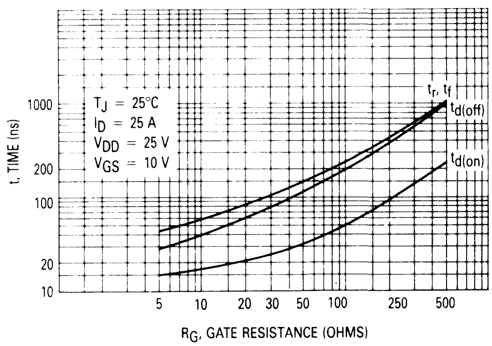


Figure 9. Resistive Switching Time Variation versus Gate Resistance

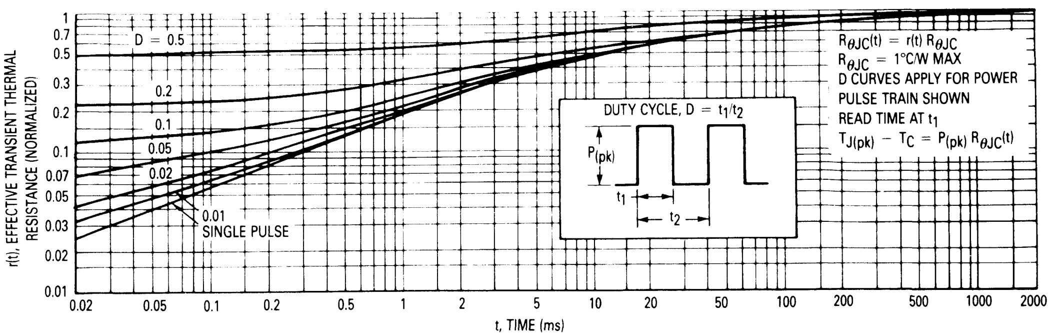


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

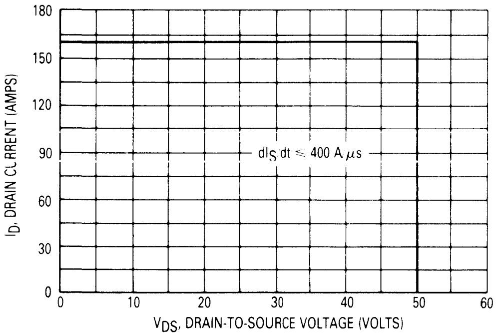


Figure 12. Commutating Safe Operating Area (CSOA)

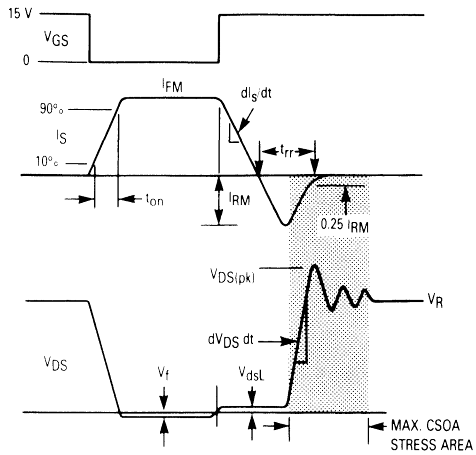


Figure 11. Commutating Waveforms

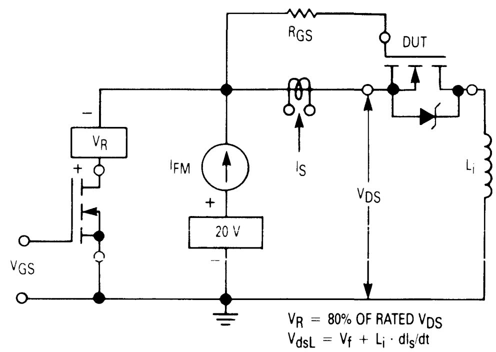


Figure 13. Commutating Safe Operating Area Test Circuit

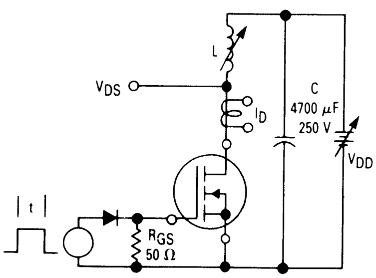
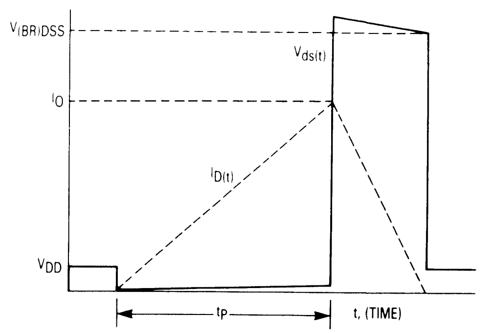


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

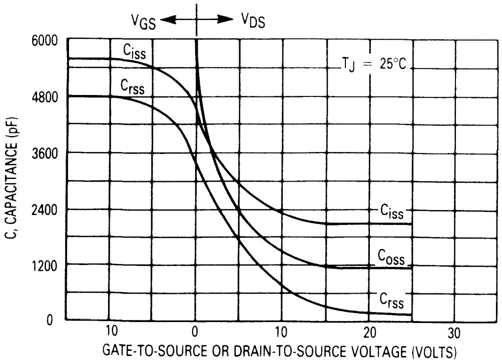


Figure 16. Capacitance Variation

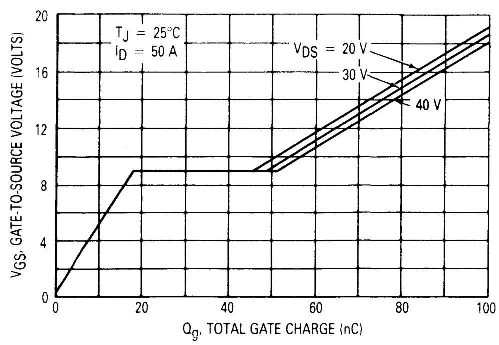
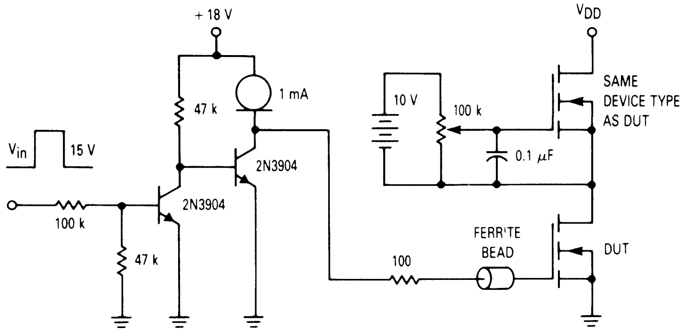


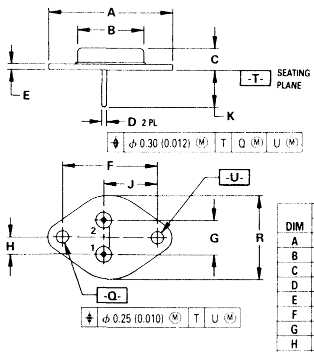
Figure 17. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH

CASE 197A-02
MTM50N05E

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

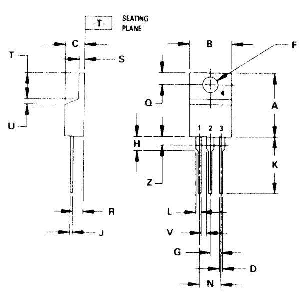
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 221A-04
MTP50N05E

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH
3 DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	–	0.045	–
Z	–	2.04	–	0.080



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTM55N08
MTM55N10
MTM60N05
MTM60N06

Designer's Data Sheet

55 and 60 AMPERE

N-CHANNEL TMOS POWER FETs

$r_{DS(on)}$ = 0.04 OHM
80 and 100 VOLTS

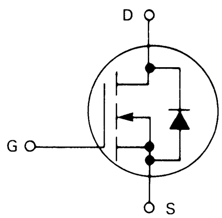
$r_{DS(on)}$ = 0.028 OHM
50 and 60 VOLTS

N-CHANNEL ENHANCEMENT-MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

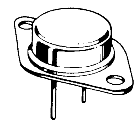
These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

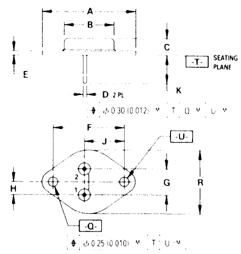
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS



MTM55N08
MTM55N10
MTM60N05
MTM60N06





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	38.36	39.37	1.510	1.550
B	19.31	21.08	0.760	0.830
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	25.15	26.67	0.990	1.050
U	3.84	4.19	0.151	0.165

CASE 197A-02
TO-204AE

MAXIMUM RATINGS

Rating	Symbol	MTM 60N05	MTM 60N06	MTM 55N08	MTM 55N10	Unit
Drain-Source Voltage	V_{DSS}	50	60	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	80	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40				 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 60 300		 55 275		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	250 2				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic			Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM60N05		$V_{BR(DSS)}$	50	—	Vdc
	MTM60N06			60	—	
	MTM55N08			80	—	
	MTM55N10			100	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DS}, V_{GS} = 0)			I_{DSS}	—	10	μAdc
T_C = 125°C				—	100	
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)			I_{GSS}	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA), V_{DS} = V_{GS}			$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C				1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 30 Adc)	MTM60N05/MTM60N06		$r_{DS(on)}$	—	0.028	Ohm
(V_{GS} = 10 Vdc, I_D = 27.5 Adc)	MTM55N08/MTM55N10			—	0.04	
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 60 Adc)	MTM60N05/MTM60N06		$V_{DS(on)}$	—	1.98	Vdc
(I_D = 30 Adc, T_J = 100°C)	MTM60N05/MTM60N06			—	1.68	
(I_D = 55 Adc)	MTM55N08/MTM55N10			—	2.6	
(I_D = 27.5 Adc, T_C = 100°C)	MTM55N08/MTM55N10			—	2.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 30 A)	MTM60N05/MTM60N06		g_{FS}	10	—	mhos
(V_{DS} = 15 V, I_D = 27.5 A)	MTM55N08/MTM55N10			10	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance		(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 8	C_{iss}	—	5000	pF
Output Capacitance			C_{oss}	—	2500	
Reverse Transfer Capacitance			C_{rss}	—	1000	
SWITCHING CHARACTERISTICS* (T_J = 100°C)						
Turn-On Delay Time		(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figure 16	$t_{d(on)}$	—	70	ns
Rise Time			t_r	—	350	
Turn-Off Delay Time			$t_{d(off)}$	—	350	
Fall Time			t_f	—	400	
Total Gate Charge		V_{DS} – 0.8 Rated, I_D = Rated, V_{GS} = 10 V See Figure 15	Q_g	105 (Typ)	120	nC
			Q_{gs}	74 (Typ)	—	
			Q_{gd}	31 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage		I_S = Rated I_D V_{GS} = 0	V_{SD}	3.5	4	Vdc
Forward Turn-On Time			t_{on}	Limited by stray inductance.		
Reverse Recovery Time			t_{rr}	200	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)			L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin 0.25″ from the package to the source bond pad)			L_s	12.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

3

TYPICAL CHARACTERISTICS

MTM60N05, MTM60N06

FIGURE 1 — ON-REGION CHARACTERISTICS

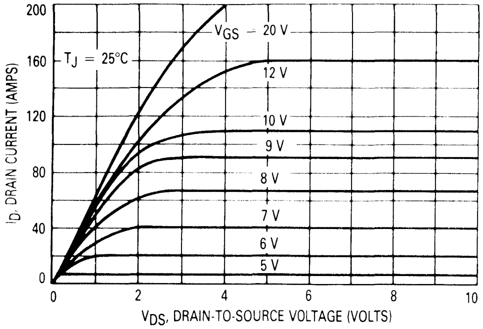


FIGURE 3 — TRANSFER CHARACTERISTICS

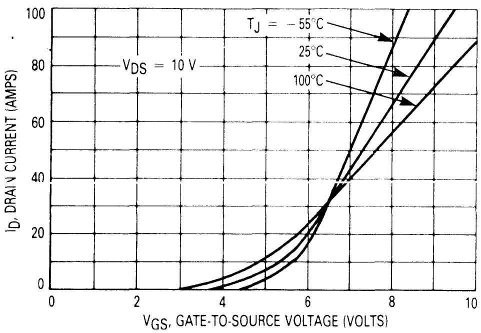
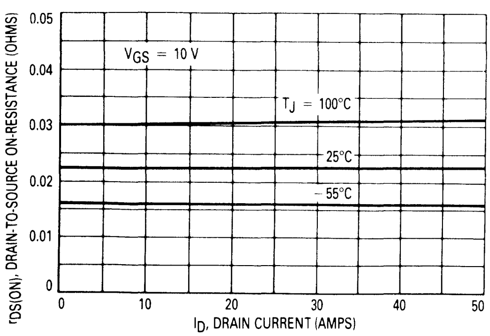


FIGURE 5 — ON-RESISTANCE versus DRAIN CURRENT



MTM55N08, MTM55N10

FIGURE 2 — ON-REGION CHARACTERISTICS

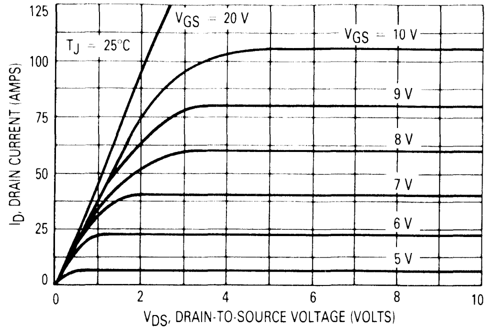


FIGURE 4 — TRANSFER CHARACTERISTICS

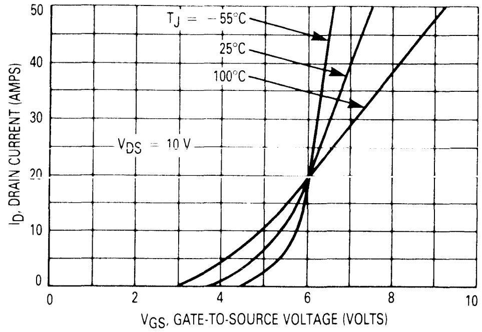
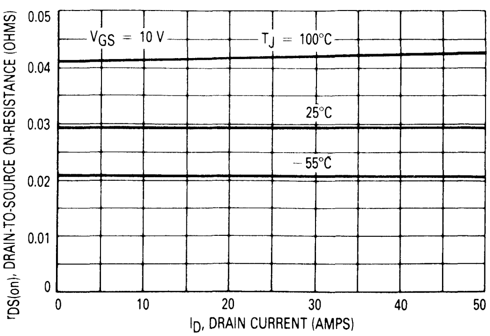


FIGURE 6 — ON-RESISTANCE versus DRAIN CURRENT



TYPICAL CHARACTERISTICS

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

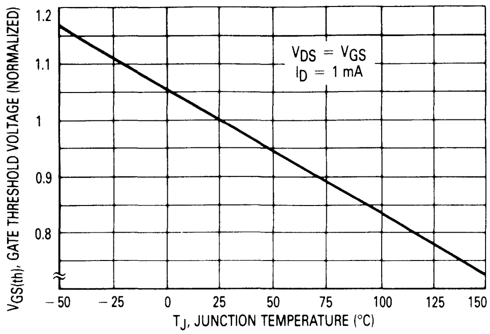


FIGURE 8 — CAPACITANCE VARIATION

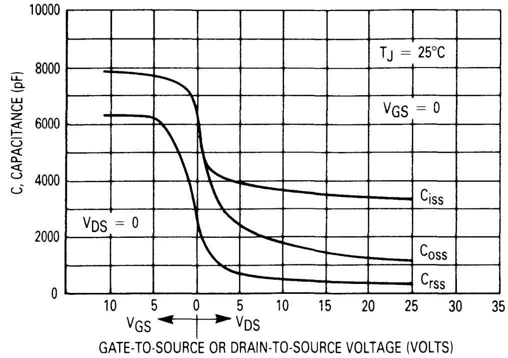


FIGURE 9 — BREAKDOWN VOLTAGE VARIATION WITH TEMPERATURE

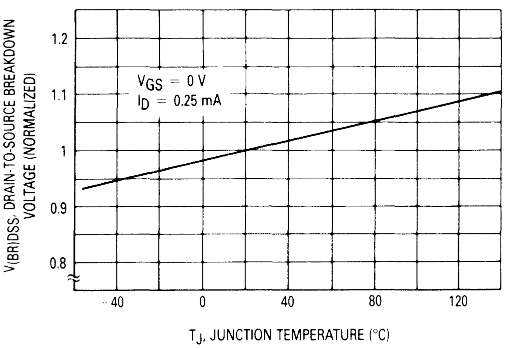


FIGURE 10 — ON-RESISTANCE VARIATION WITH TEMPERATURE

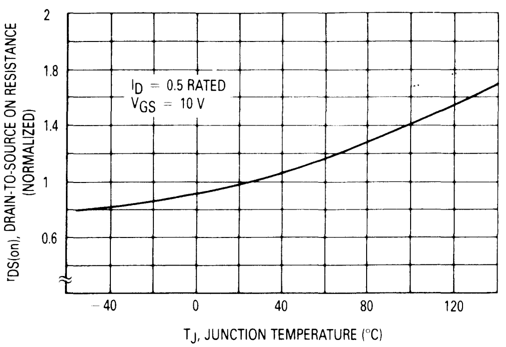
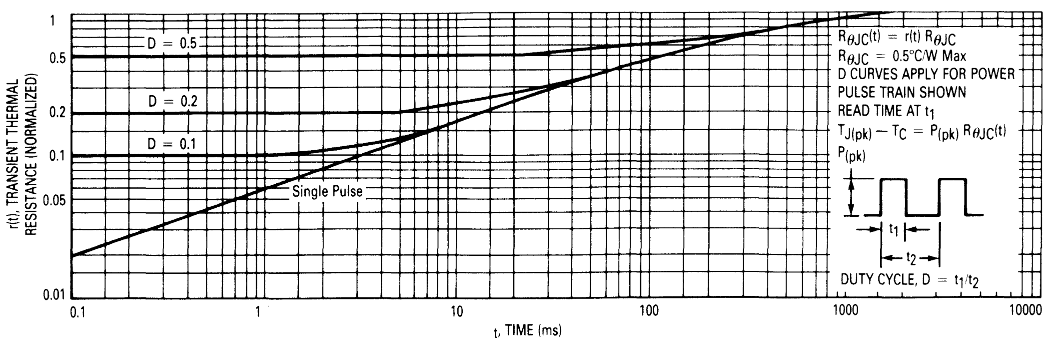


FIGURE 11 — THERMAL RESPONSE



SAFE OPERATING AREA INFORMATION

FIGURE 12 — MTM60N05, MTM60N06

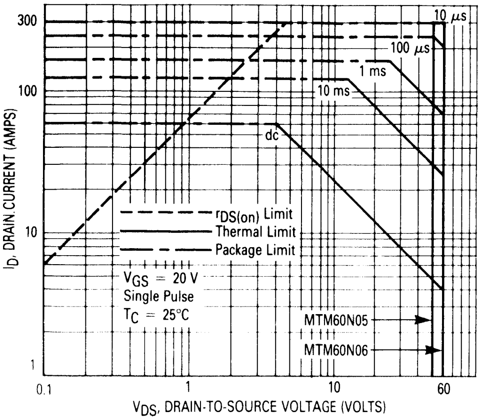
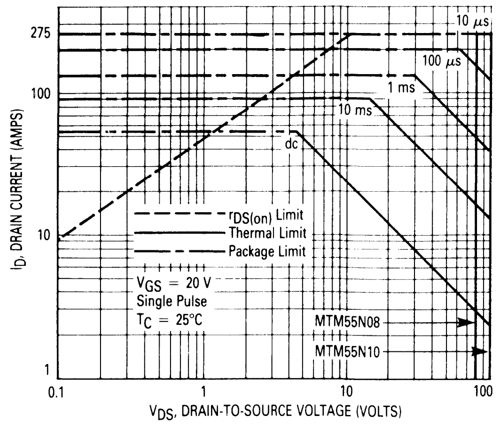


FIGURE 13 — MTM55N08, MTM55N10



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 14 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA

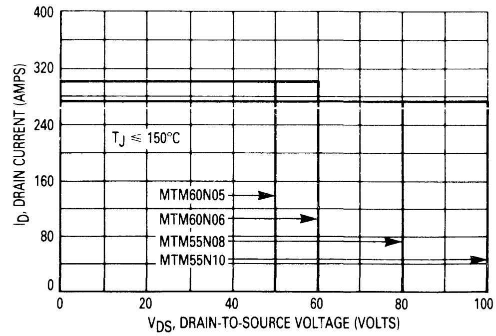


FIGURE 15 — STORED CHARGE versus GATE-TO-SOURCE VOLTAGE

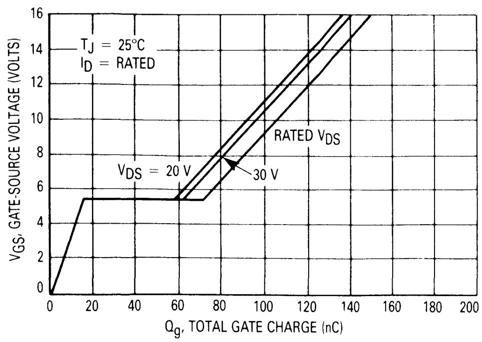
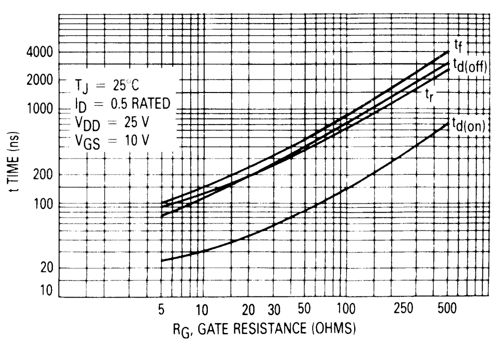


FIGURE 16 — RESISTIVE SWITCHING TIME VARIATION WITH GATE RESISTANCE



MTP1N45
MTP1N50

Designer's Data Sheet

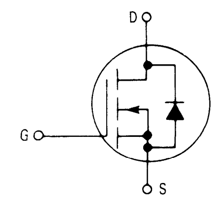
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
1 AMPERE
$r_{DS(on)}$ = 8 OHMS
450 and 500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



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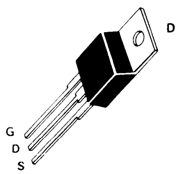


CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 1N45	MTP 1N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	1 4		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP1N45 MTP1N50	$V_{(BR)DSS}$	 450 500	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS*				
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$r_{DS(on)}$	—	8	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1 Adc) (I_D = 0.5 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 9.5 8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 0.5 A)	g_{FS}	0.5	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	200	pF
Output Capacitance		C_{oss}	—	30	
Reverse Transfer Capacitance		C_{rss}	—	10	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	35	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	9 (Typ)	11	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	2 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8 (Typ)	2.2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	150 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

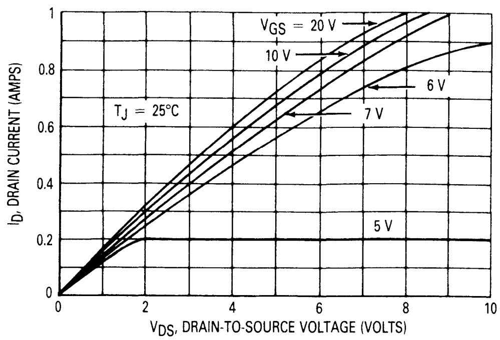


Figure 1. On-Region Characteristics

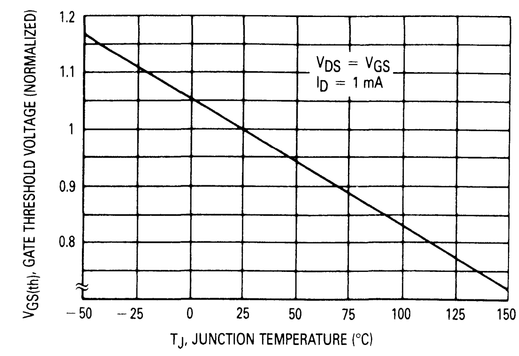


Figure 2. Gate-Threshold Voltage Variation With Temperature

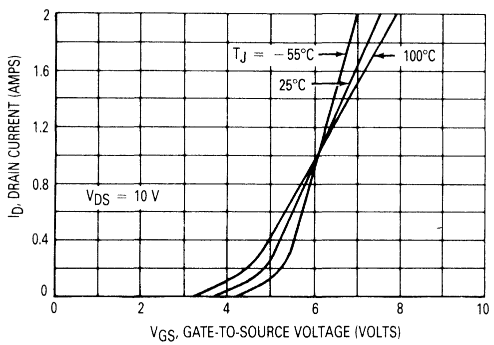


Figure 3. Transfer Characteristics

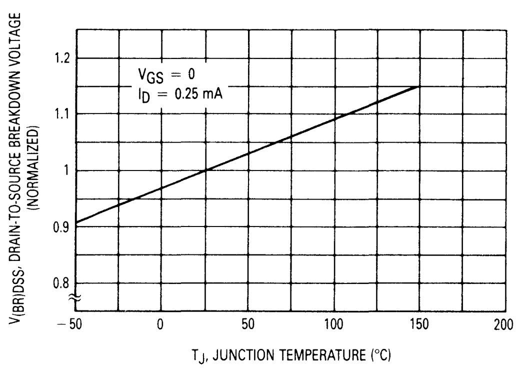


Figure 4. Breakdown Voltage Variation With Temperature

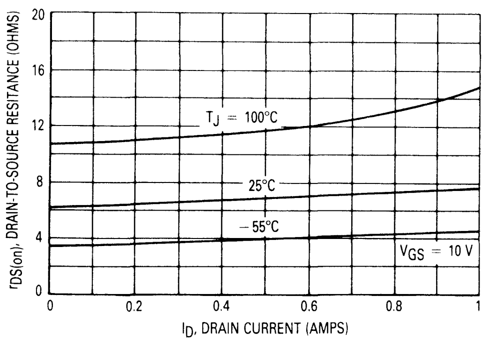


Figure 5. On-Resistance versus Drain Current

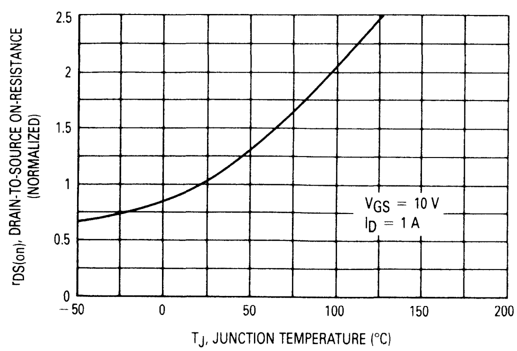


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

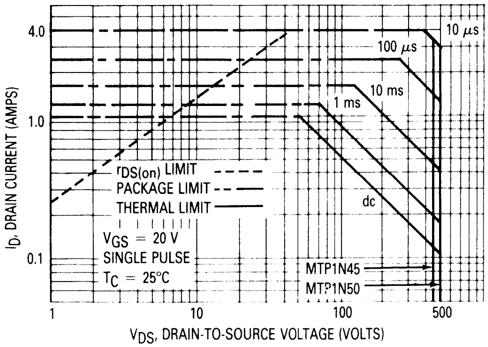


Figure 7. Maximum Rated Forward Biased Safe Operating Area

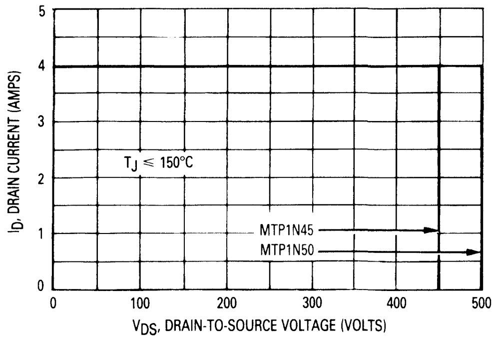


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

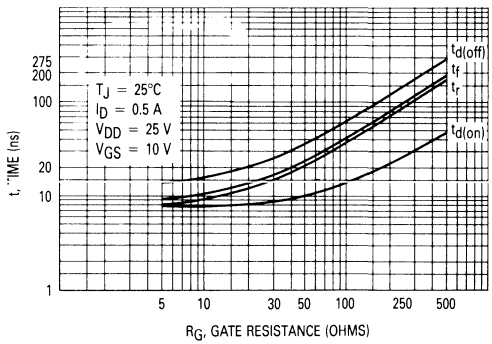


Figure 9. Resistive Switching Time Variation versus Gate Resistance

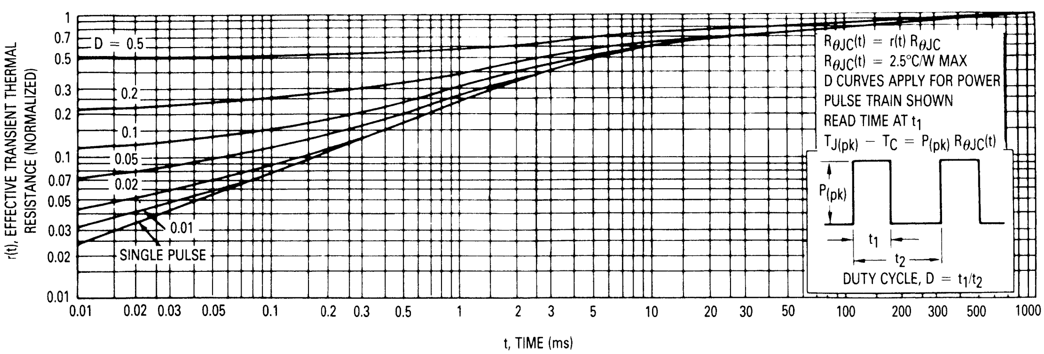


Figure 10. Thermal Response

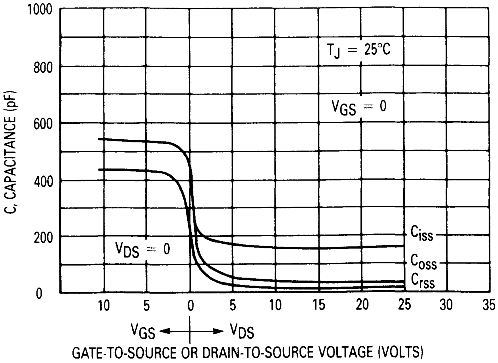


Figure 11. Capacitance Variation

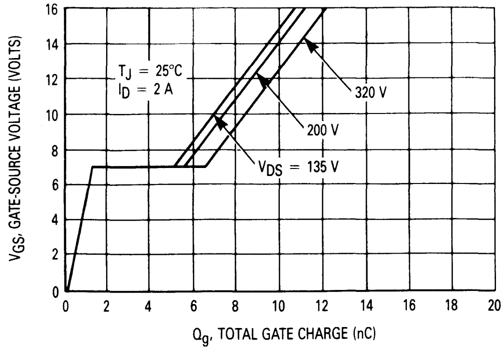


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

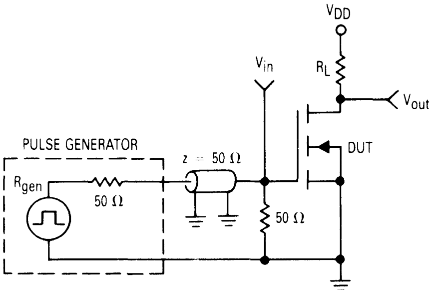


Figure 13. Switching Test Circuit

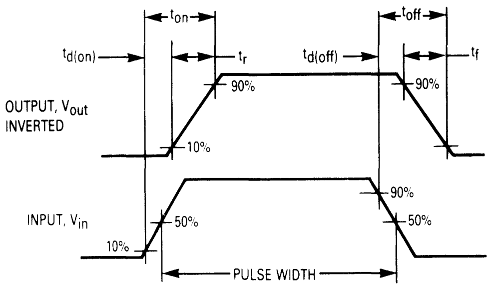
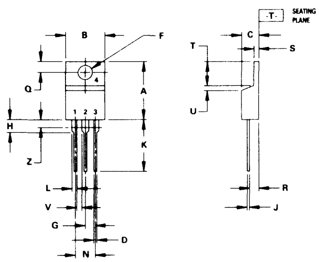


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP1N55
MTP1N60

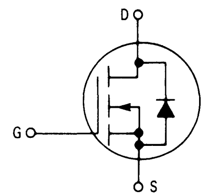
Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

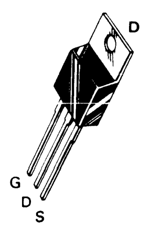
TMOS POWER FETs
1 AMPERE
$r_{DS(on)}$ = 12 OHMS
550 and 600 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

3





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 1N55	MTP 1N60	Unit
Drain-Source Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	1 3		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP1N55 MTP1N60	$V_{(BR)DSS}$	550 600	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$r_{DS(on)}$	—	12	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 0.5 Adc) (I_D = 0.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 6 12	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 0.5 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	200	pF
Output Capacitance		C_{oss}	—	30	
Reverse Transfer Capacitance		C_{rss}	—	10	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	35	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	8 (Typ)	10	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	4 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1 (Typ)	1.2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

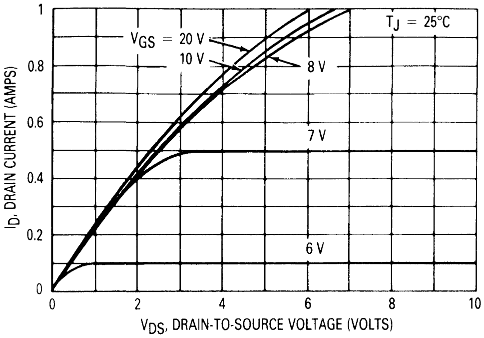


Figure 1. On-Region Characteristics

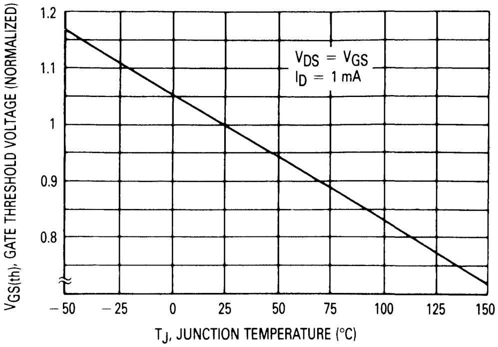


Figure 2. Gate-Threshold Voltage Variation With Temperature

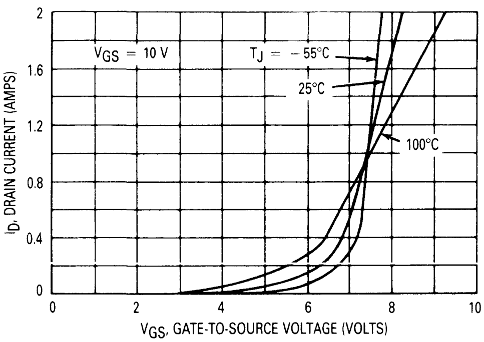


Figure 3. Transfer Characteristics

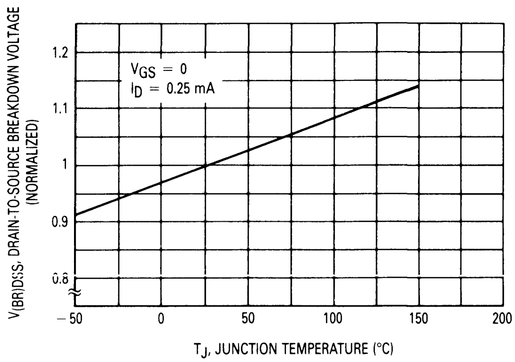


Figure 4. Breakdown Voltage Variation With Temperature

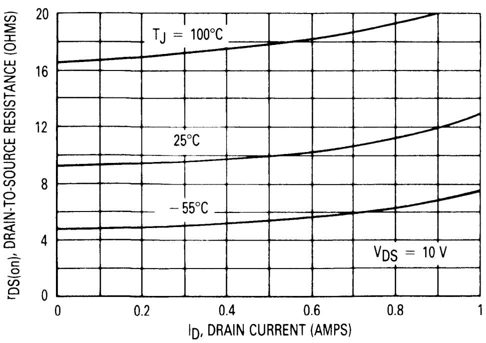


Figure 5. On-Resistance versus Drain Current

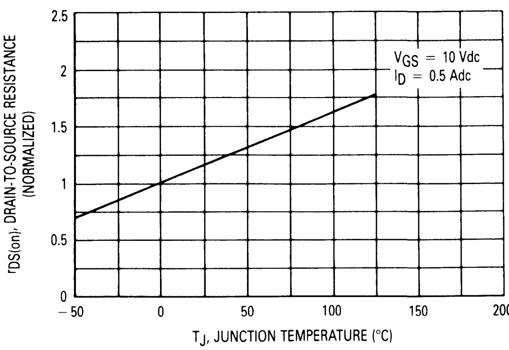


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

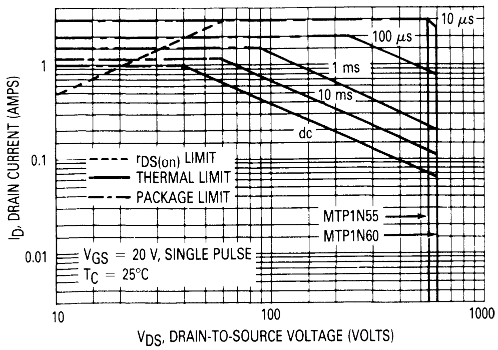


Figure 7. Maximum Rated Forward Biased Safe Operating Area

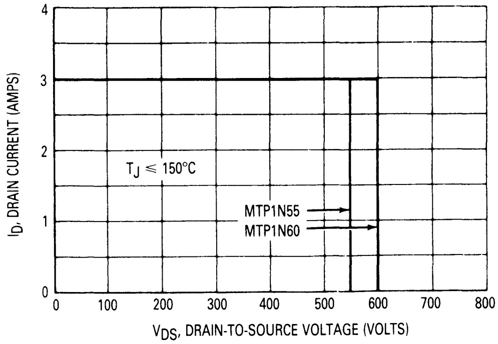


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

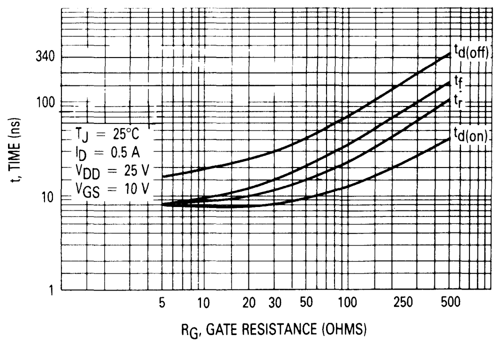


Figure 9. Resistive Switching Time Variation versus Gate Resistance

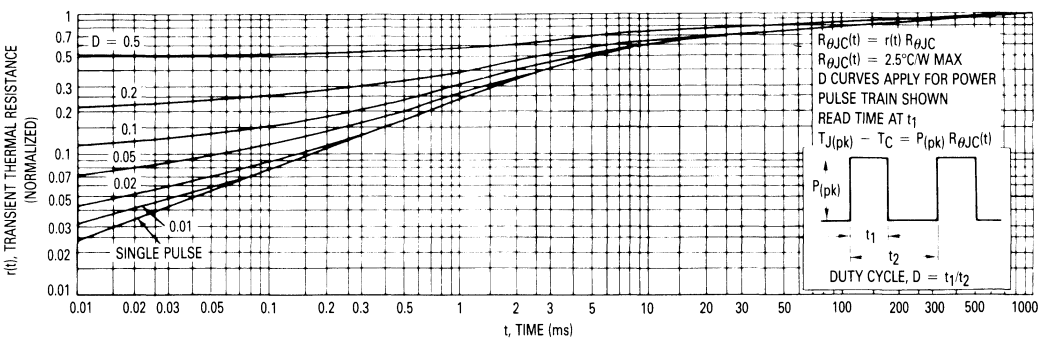


Figure 10. Thermal Response

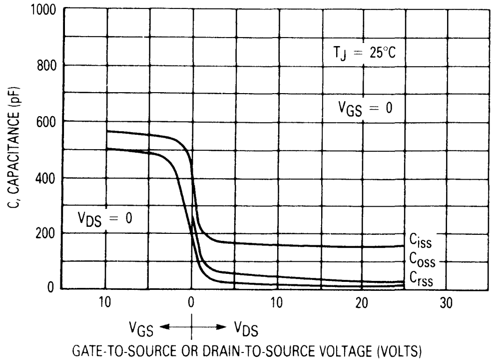


Figure 11. Capacitance Variation

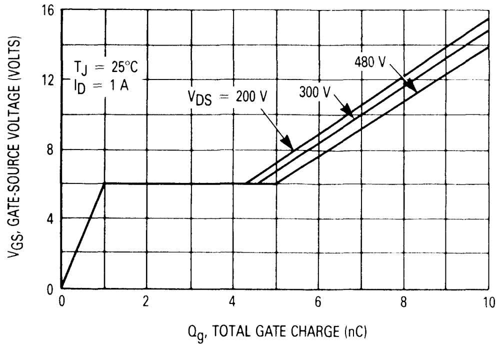


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

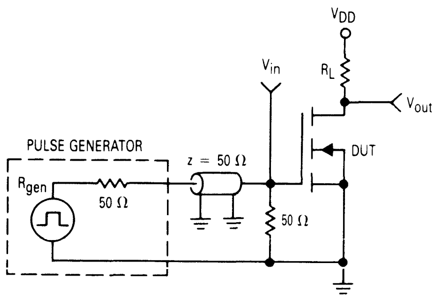


Figure 13. Switching Test Circuit

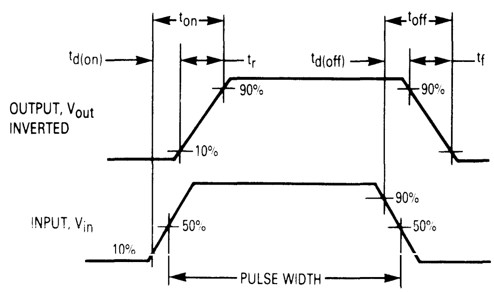
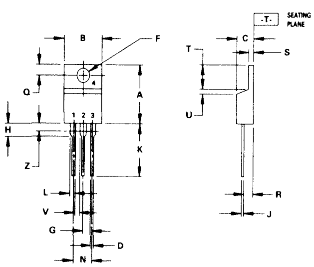


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

Designer's Data Sheet

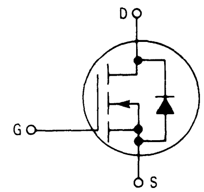
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

MTP2N20

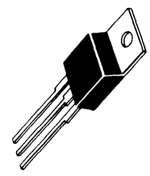
TMOS

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 1.8 OHMS
200 VOLTS



This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	1.8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.4 3.6	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	250	pF
Output Capacitance		C_{oss}	—	100	
Reverse Transfer Capacitance		C_{rss}	—	50	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	30	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	15	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	3.5 (Typ)	10	nC
Gate-Source Charge		Q_{gs}	2 (Typ)	—	
Gate-Drain Charge		Q_{gd}	1.5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	60 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

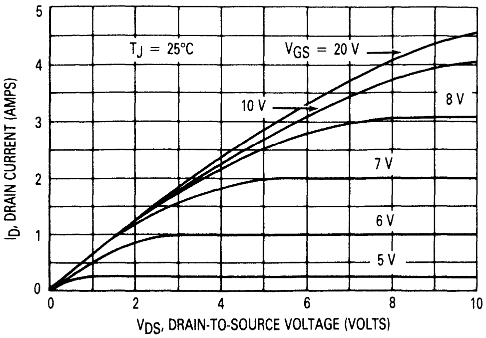


Figure 1. On-Region Characteristics

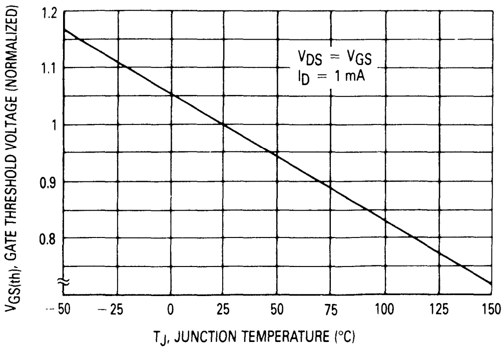


Figure 2. Gate-Threshold Voltage Variation With Temperature

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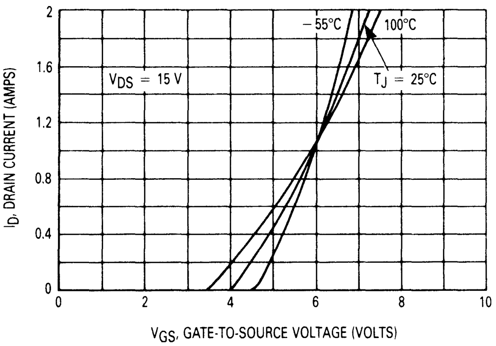

Figure 3. Transfer Characteristics

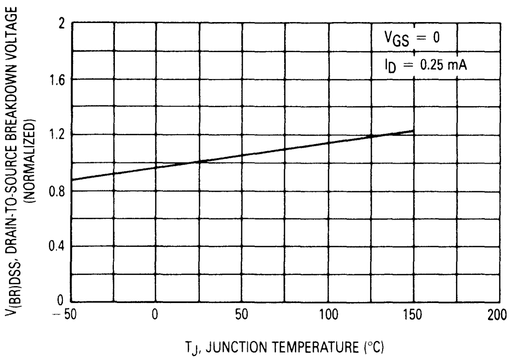

Figure 4. Breakdown Voltage Variation With Temperature

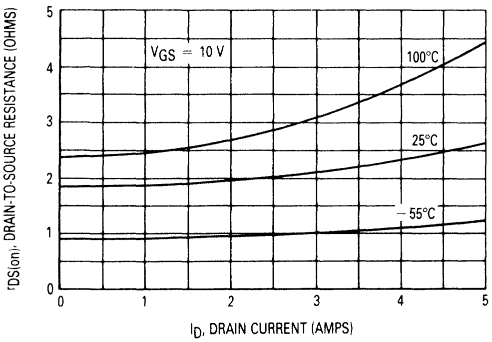

Figure 5. On-Resistance versus Drain Current

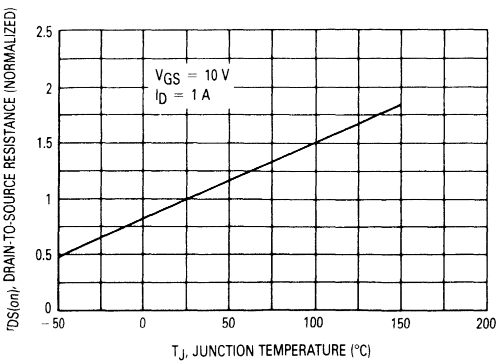

Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

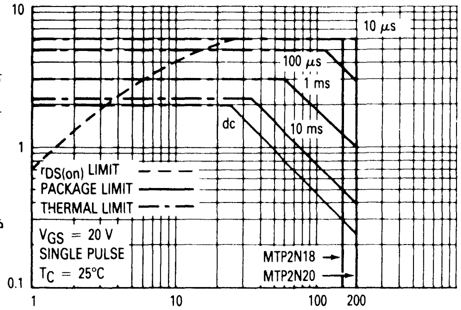

Figure 7. Maximum Rated Forward Biased Safe Operating Area

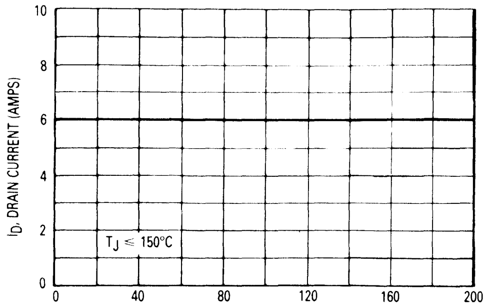

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

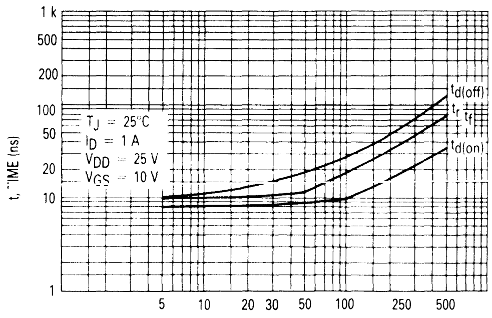

Figure 9. Resistive Switching Time Variation versus Gate Resistance

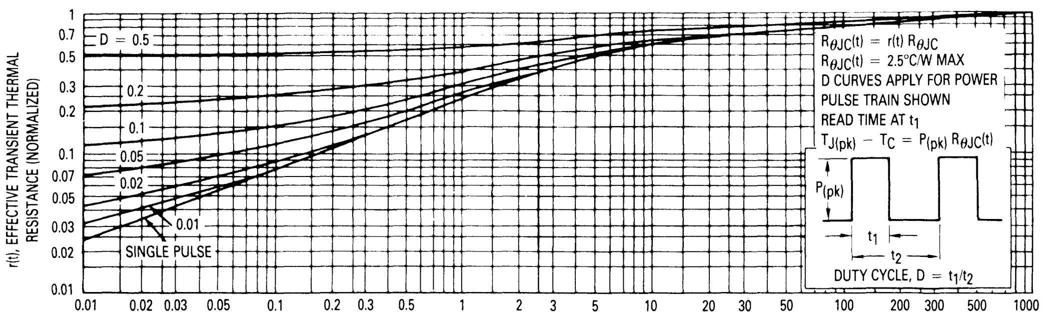

Figure 10. Thermal Response

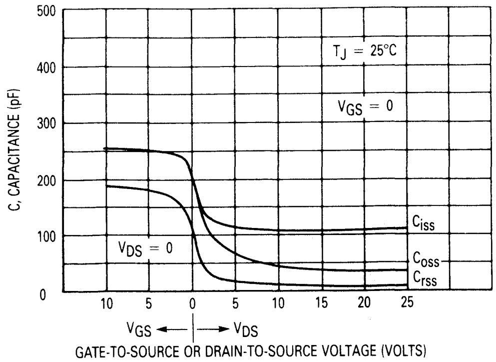

Figure 11. Capacitance Variation

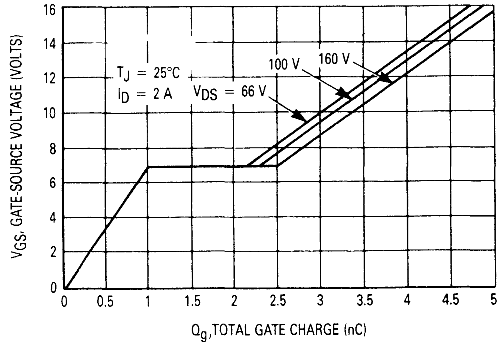

Figure 12. Gate Charge versus Gate-to-Source Voltage

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RESISTIVE SWITCHING

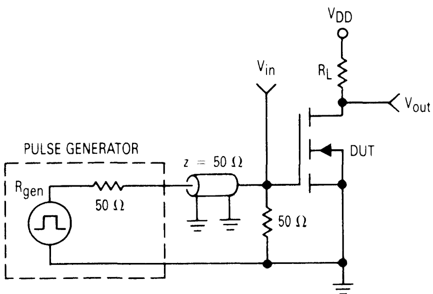


Figure 13. Switching Test Circuit

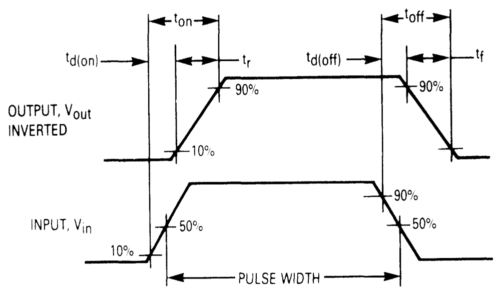
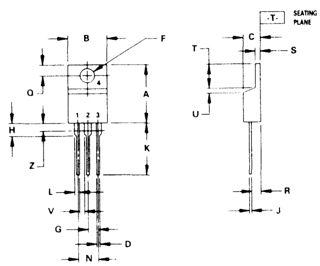


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

Designer's Data Sheet

Power Field Effect Transistor

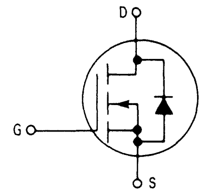
N-Channel Enhancement-Mode Silicon Gate TMOS

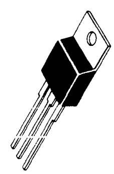
MTP2N25

**TMOS POWER FET
2 AMPERES
$r_{DS(on)}$ = 2.8 OHMS
250 VOLTS**

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





**CASE 221A-04
TO-220AB**

MAXIMUM RATINGS

Rating	Symbol	MTP2N25	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	250	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	2.8	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 5.6 4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.8	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	65	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	20	
Turn-Off Delay Time		$t_{d(off)}$	—	35	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	6.5 (Typ)	9	nC
Gate-Source Charge		Q_{gs}	3.5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	3 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	2 (Typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	190 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

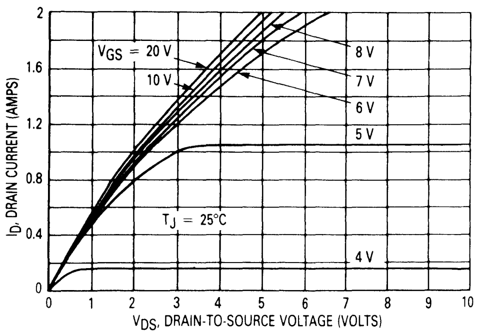


Figure 1. On-Region Characteristics

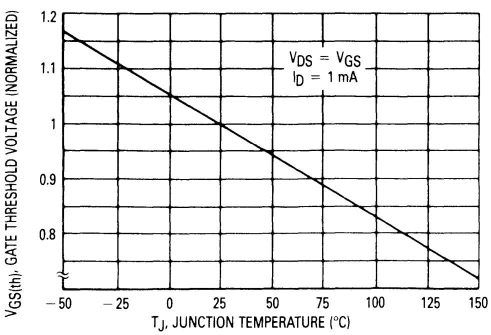


Figure 2. Gate-Threshold Voltage Variation With Temperature

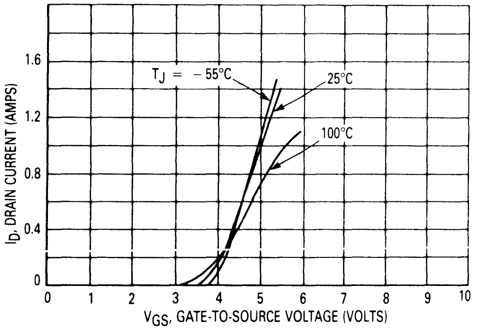


Figure 3. Transfer Characteristics

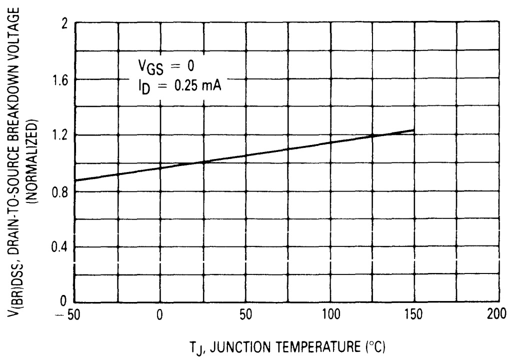


Figure 4. Breakdown Voltage Variation With Temperature

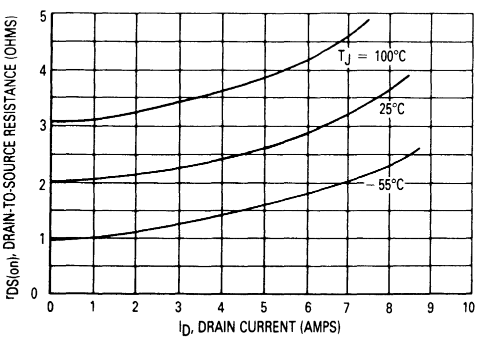


Figure 5. On-Resistance versus Drain Current

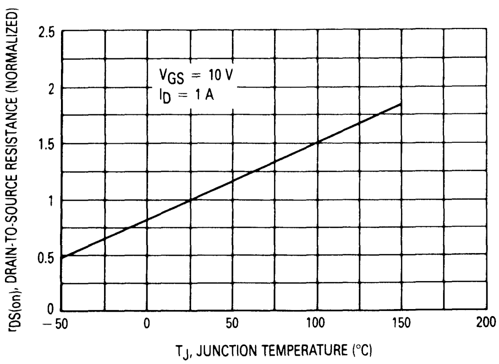


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

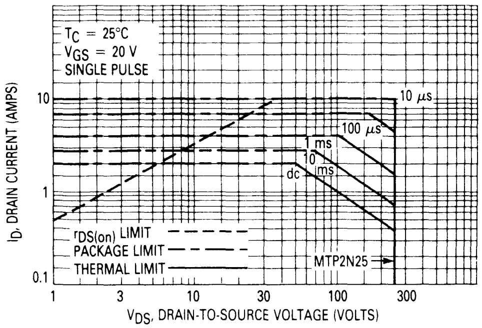


Figure 7. Maximum Rated Forward Biased Safe Operating Area

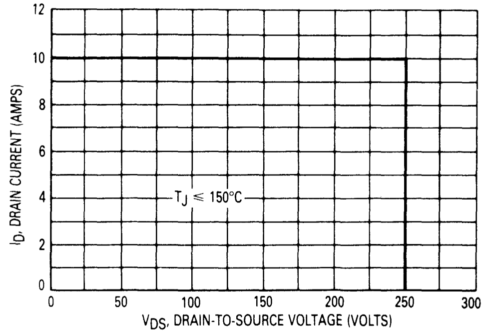


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

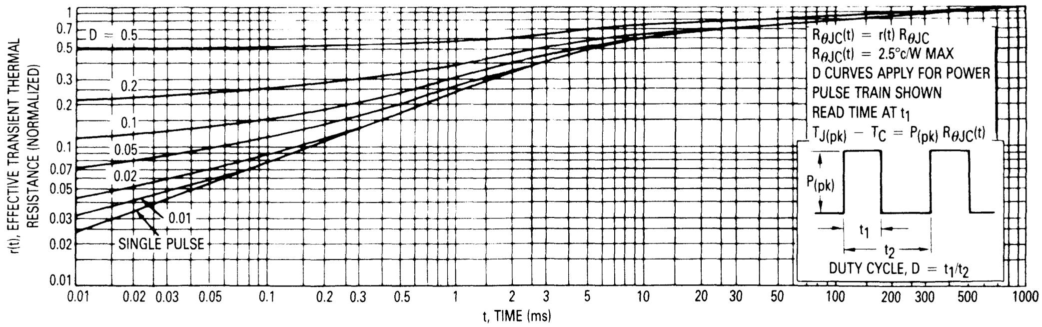


Figure 9. Thermal Response

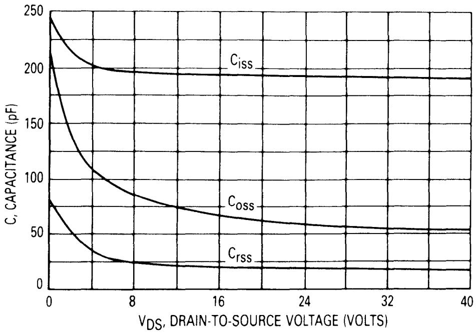


Figure 10. Capacitance Variation

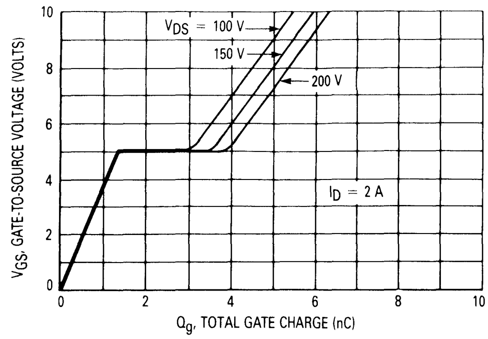


Figure 11. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

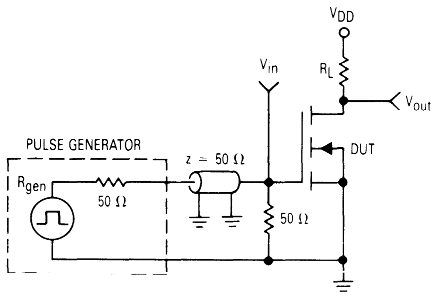


Figure 12. Switching Test Circuit

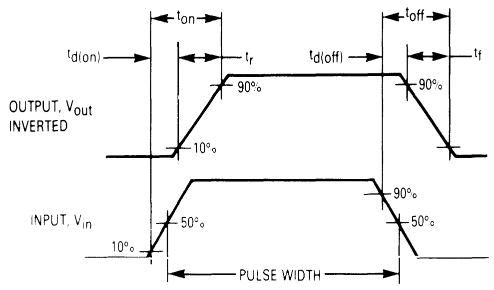
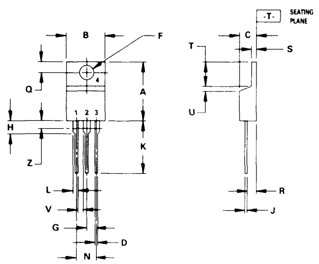


Figure 13. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5.
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

MTP2N35
MTP2N40

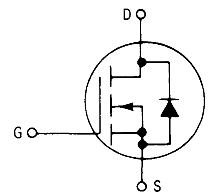
TMOS

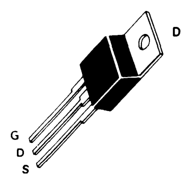
TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 5 OHMS
350 and 400 VOLTS

3

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 2N35	MTP 2N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP2N35 MTP2N40	$V_{(BR)DSS}$	 350 400	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	5	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 2 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 13 10	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1 A)		g_{FS}	0.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	200	pF
Output Capacitance		C_{oss}	—	30	
Reverse Transfer Capacitance		C_{rss}	—	10	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	15	
Turn-Off Delay Time		$t_{d(off)}$	—	35	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	9 (Typ)	11	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	2 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.8 (Typ)	2.2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	150 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

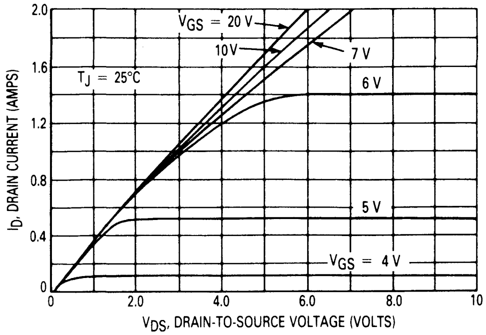


Figure 1. On-Region Characteristics

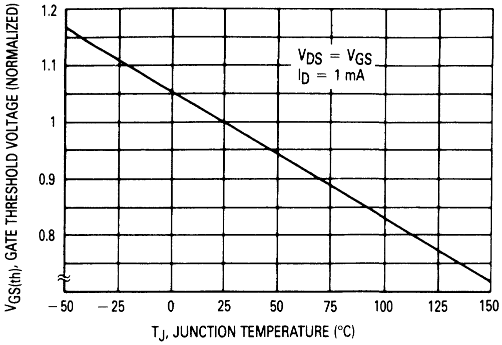


Figure 2. Gate-Threshold Voltage Variation With Temperature

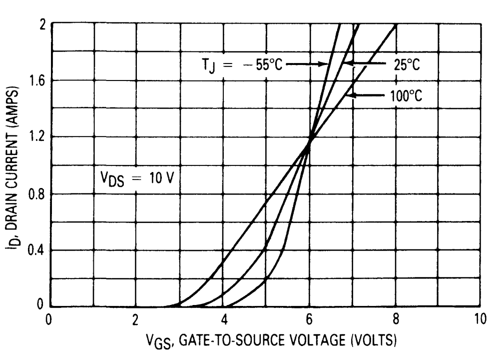


Figure 3. Transfer Characteristics

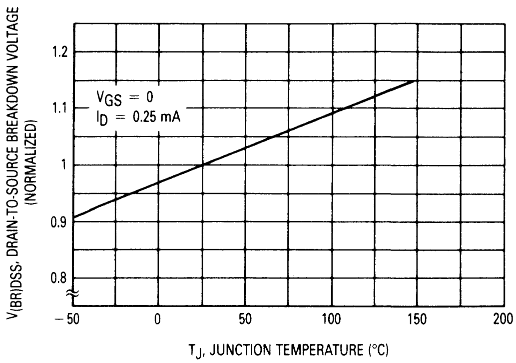


Figure 4. Breakdown Voltage Variation With Temperature

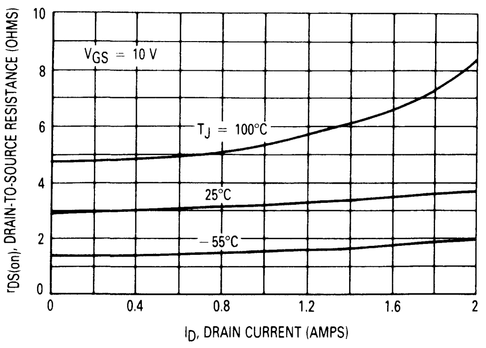


Figure 5. On-Resistance versus Drain Current

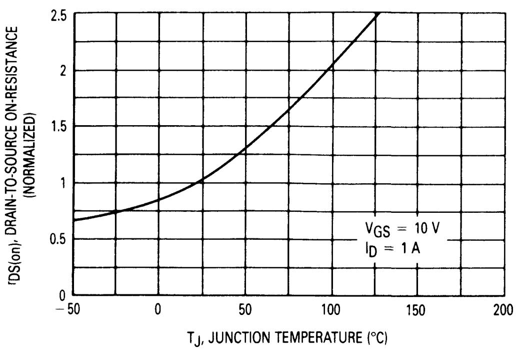


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

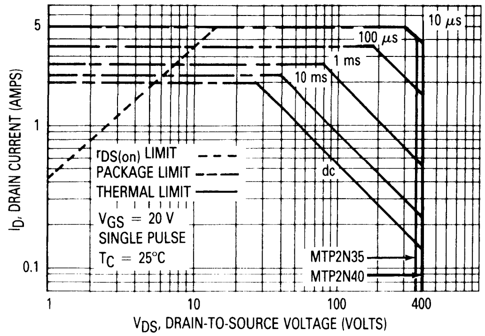


Figure 7. Maximum Rated Forward Biased Safe Operating Area

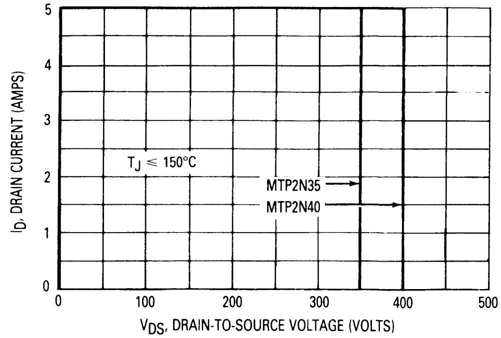


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

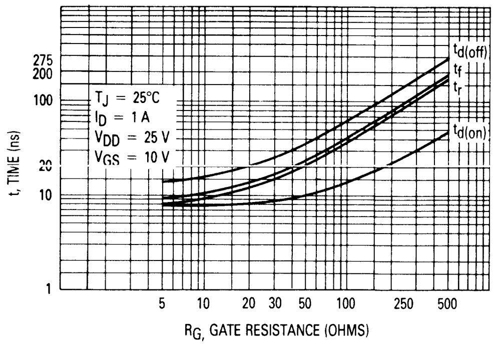


Figure 9. Resistive Switching Time Variation versus Gate Resistance

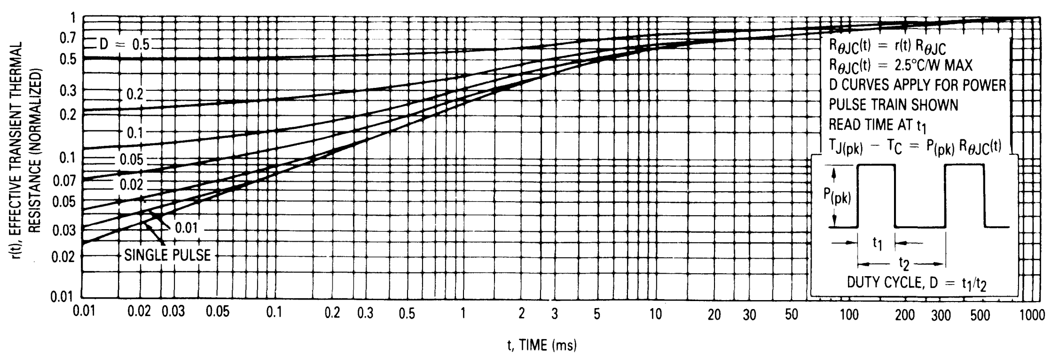


Figure 10. Thermal Response

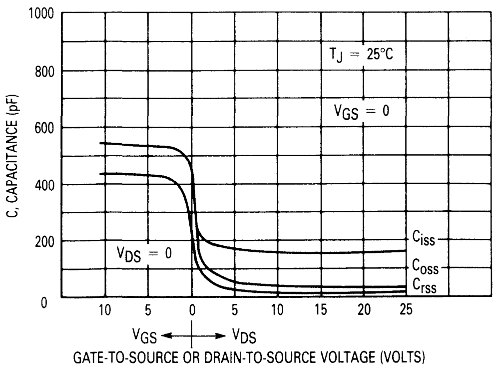


Figure 11. Capacitance Variation

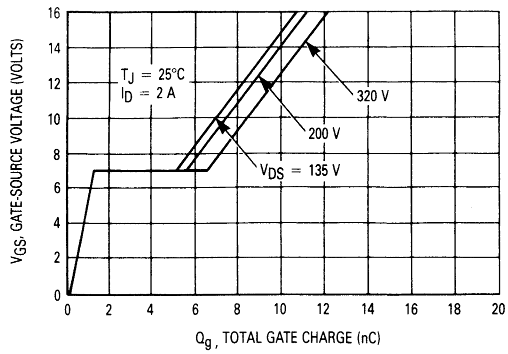


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

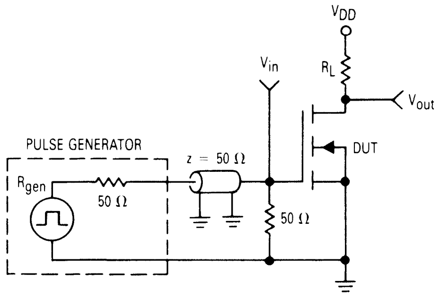


Figure 13. Switching Test Circuit

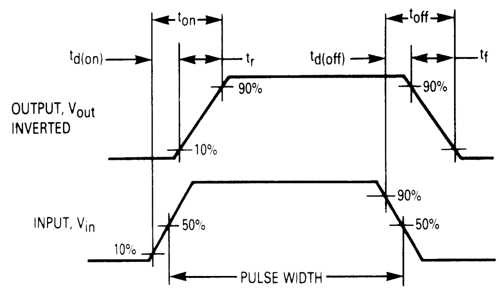
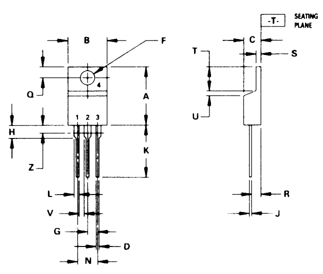


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5.
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES.
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet

Power Field Effect Transistor

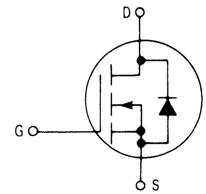
N-Channel Enhancement-Mode Silicon Gate TMOS

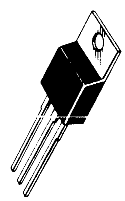
MTP2N55
MTP2N60

TMOS POWER FETs
2 AMPERES
$r_{DS(on)}$ = 6 OHMS
550 and 600 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low drive requirements $V_{GS(th)}$ = 4.5 V(max)





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP2N55	MTP2N60	Unit
Drain-Sourve Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40		 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	2 9		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient TO-220	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP2N55 MTP2N60	$V_{(BR)DSS}$	 550 600	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1 Adc)		$r_{DS(on)}$	—	6	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 1 Adc) (I_D = 1 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 6 10	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	40	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	30	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	16 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	9 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

3

TYPICAL ELECTRICAL CHARACTERISTICS

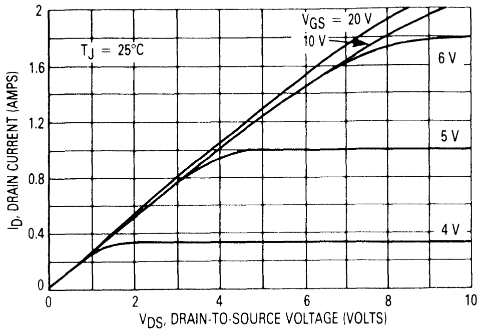


Figure 1. On-Region Characteristics

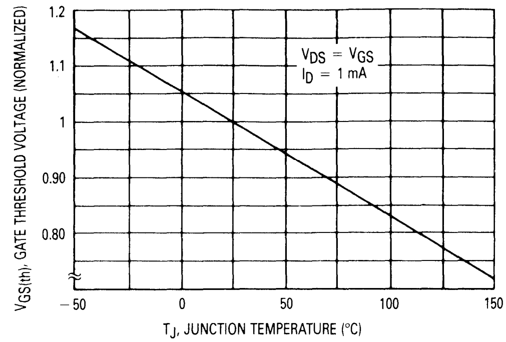


Figure 2. Gate-Threshold Voltage Variation With Temperature

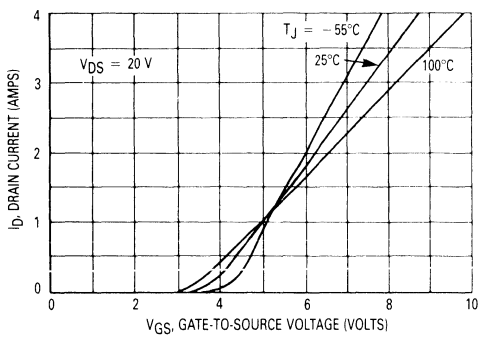


Figure 3. Transfer Characteristics

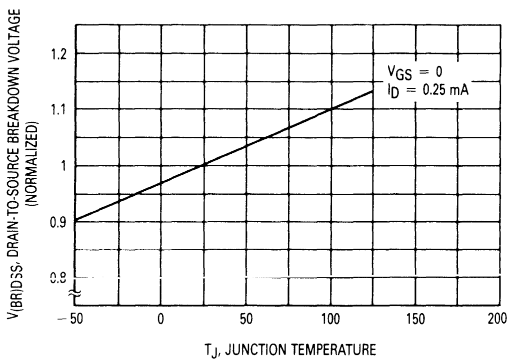


Figure 4. Breakdown Voltage Variation With Temperature

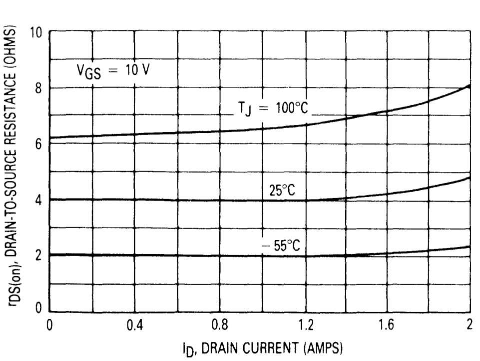


Figure 5. On-Resistance versus Drain Current

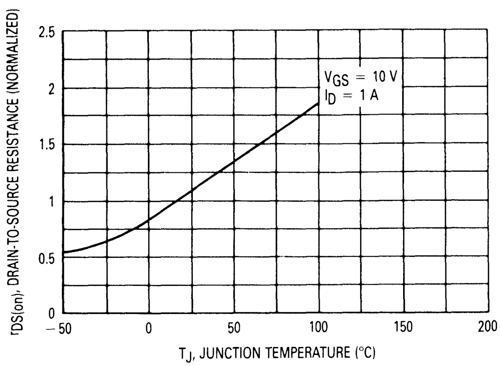


Figure 6. On-Resistance Variation With Temperature

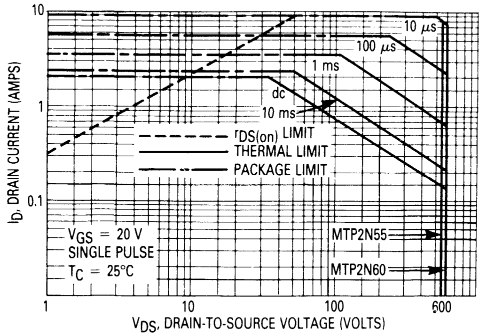


Figure 7. Maximum Rated Forward Biased Safe Operating Area

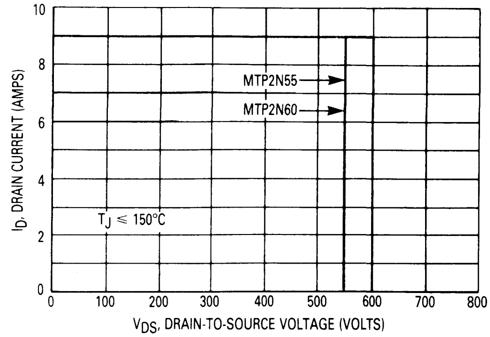


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

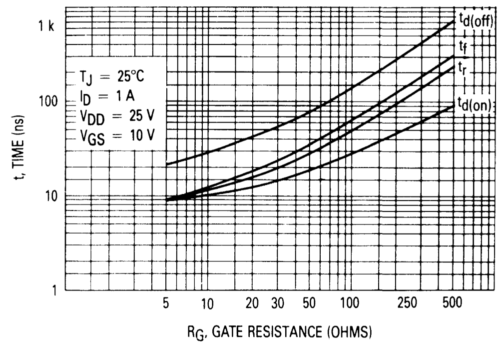


Figure 9. Resistive Switching Time Variation versus Gate Resistance

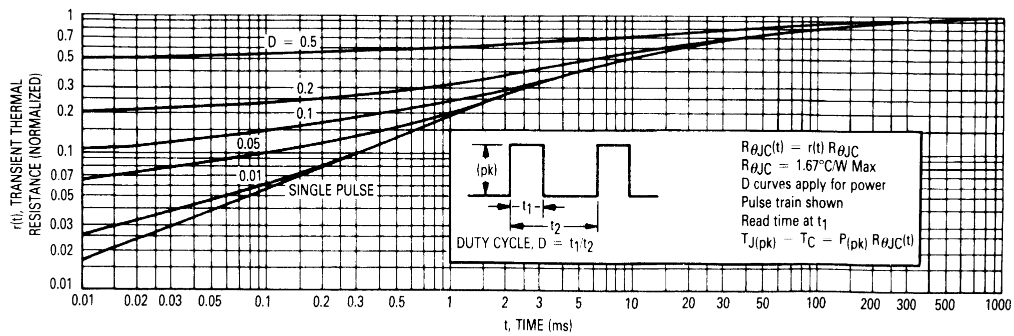


Figure 10. Thermal Response

3

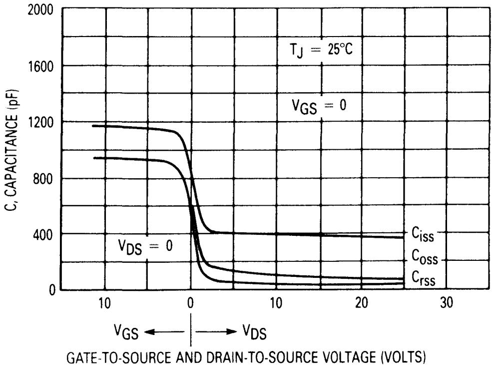


Figure 11. Capacitance Variation

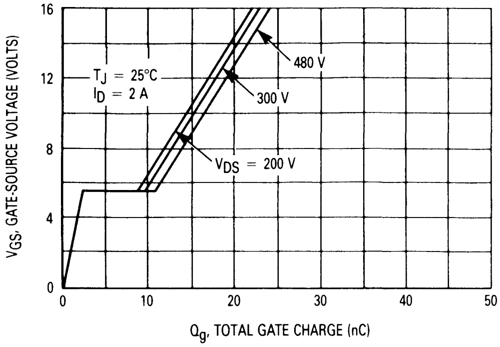


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

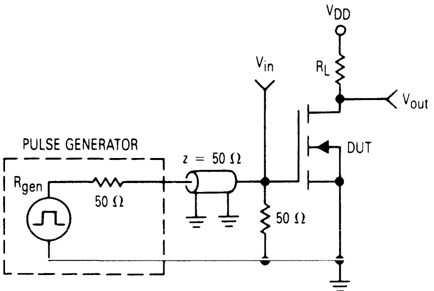


Figure 13. Switching Test Circuit

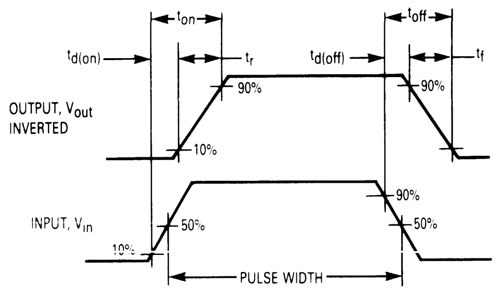
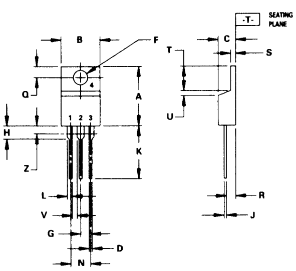


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTP3N08L
MTP3N10L

Designer's Data Sheet

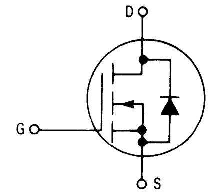
Power Field Effect Transistor

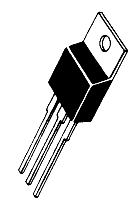
N-Channel Enhancement-Mode
Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)} = 2$ Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
LOGIC LEVEL
3 AMPERES
$r_{DS(on)} = 0.8$ OHM
80 and 100 VOLTS





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MTP3N08L	MTP3N10L	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage ($R_{GS} = 1\ M\Omega$)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±15 ±20		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3 14		Adc
Total Power Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	25 0.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS ($T_C = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 250\ \mu A$)	 MTP3N08L MTP3N10L	$V_{(BR)DSS}$	 80 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, $V_{GS} = 0$) (V_{DS} = Rated V_{DSS}, $V_{GS} = 0$, $T_J = 125°C$)		I_{DSS}	 — —	 1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	2	Vdc
(T_J = 100°C)			0.75	1.5	
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	0.8	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 3 Adc)		$V_{DS(on)}$	—	2.6	Vdc
(I_D = 2 Adc, T_J = 100°C)			—	2.4	
Forward Transconductance (V_{DS} = 10 V, I_D = 2 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	225	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	600	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	40	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	360	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{oss}	—	100	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 2 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	40	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 3 A, V_{GS} = 5 Vdc) See Figures 11 and 12.	Q_g	5 (typ)	8	nC
Gate-Source Charge		Q_{gs}	2 (typ)	—	
Gate-Drain Charge		Q_{gd}	3 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = 3 A, V_{GS} = 0) See Figures 14 and 15.	V_{SD}	1.5 (typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	(typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

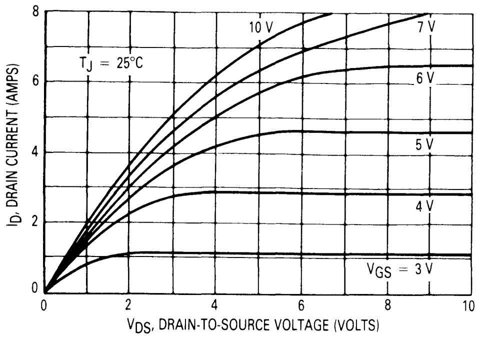


Figure 1. On-Region Characteristics

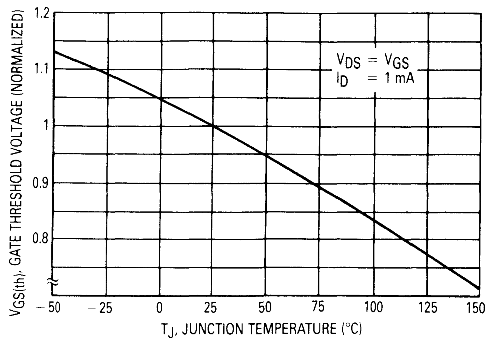


Figure 2. Gate-Threshold Variation With Temperature

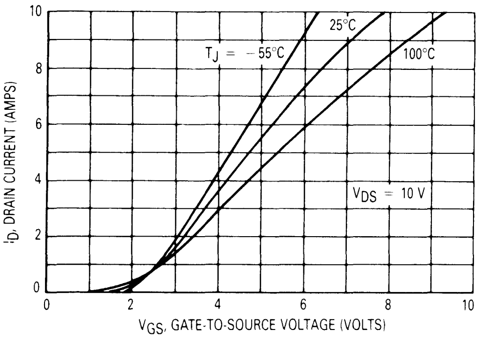


Figure 3. Transfer Characteristics

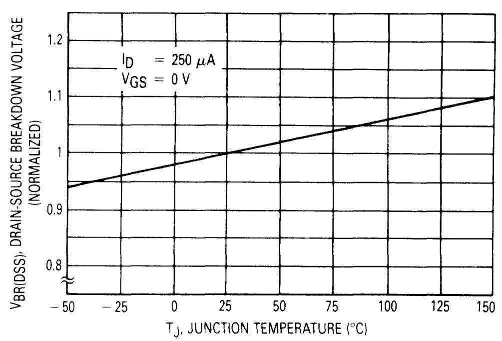


Figure 4. Breakdown Voltage Variation With Temperature

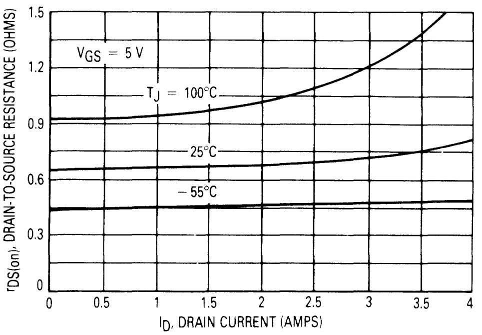


Figure 5. On-Resistance versus Drain Current

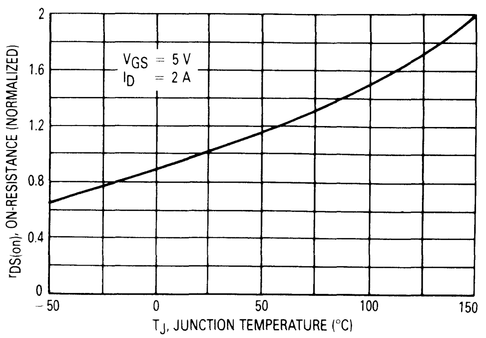


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

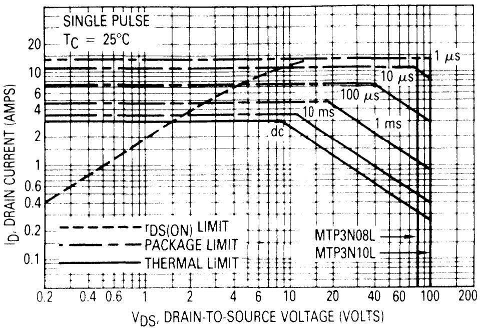


Figure 7. Maximum Rated Forward Biased Safe Operating Area

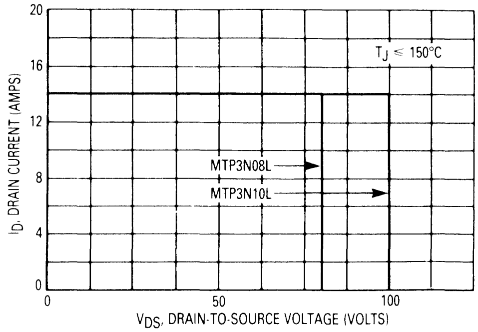


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

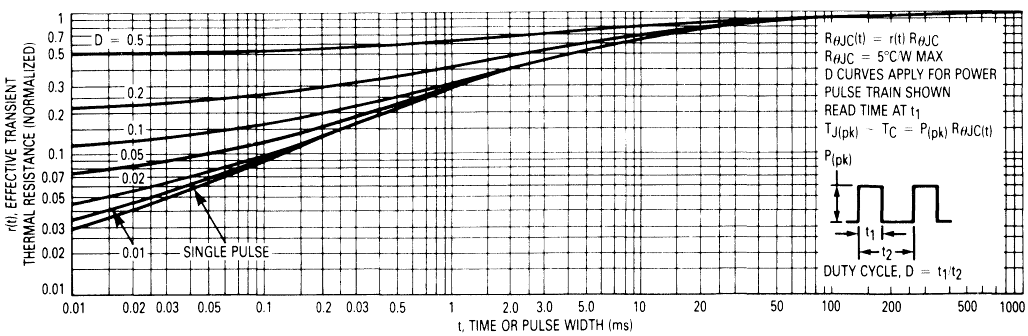


Figure 9. Thermal Response

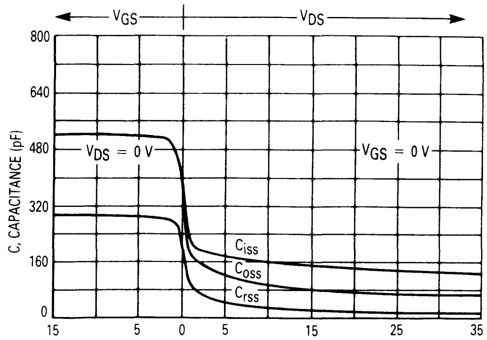


Figure 10. Capacitance Variation

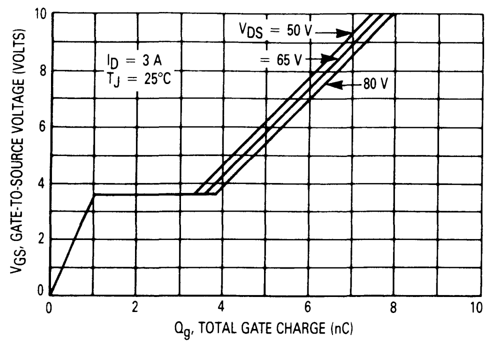
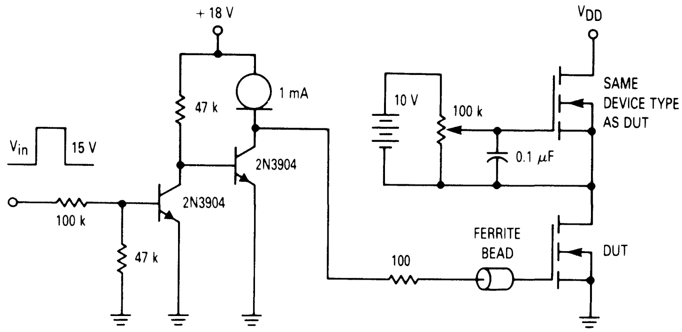


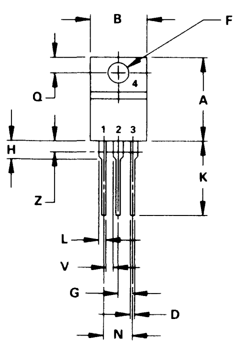
Figure 11. Gate Charge versus Gate-to-Source Voltage

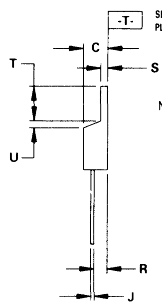


V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 12. Gate Charge Test Circuit

OUTLINE DIMENSIONS





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP3N40

Designer's Data Sheet

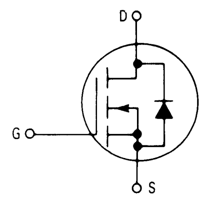
Power Field Effect Transistor

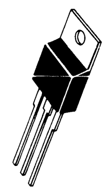
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
3 AMPERES
$r_{DS(on)}$ = 3.3 OHMS
400 VOLTS

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement $V_{G(th)}$ = 4.5 Volts (max)





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3 8	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient TO-204	$R_{\theta JA}$	30	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	400	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	3.3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc) (I_D = 1.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	12 10	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	100	
Reverse Transfer Capacitance		C_{rss}	—	50	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 125 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	60	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	16 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1 (Typ)	1.4	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	

3

TYPICAL ELECTRICAL CHARACTERISTICS

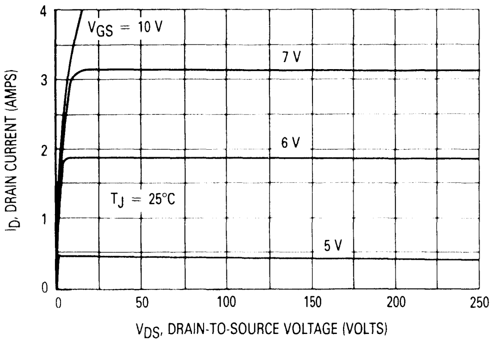


Figure 1. On-Region Characteristics

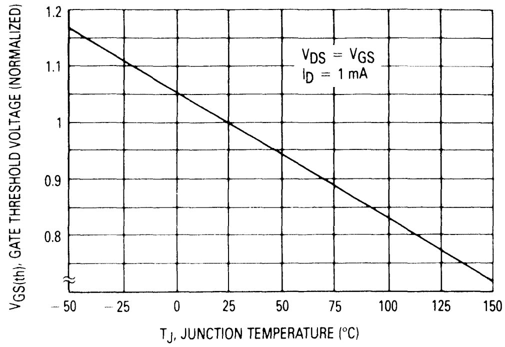


Figure 2. Gate-Threshold Voltage Variation With Temperature

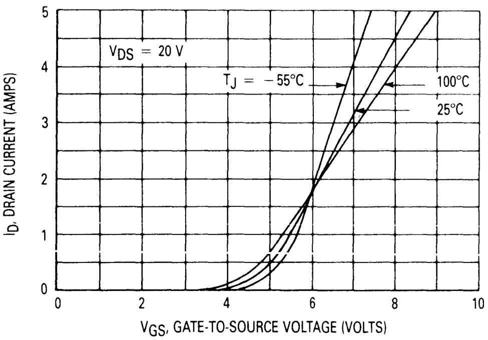


Figure 3. Transfer Characteristics

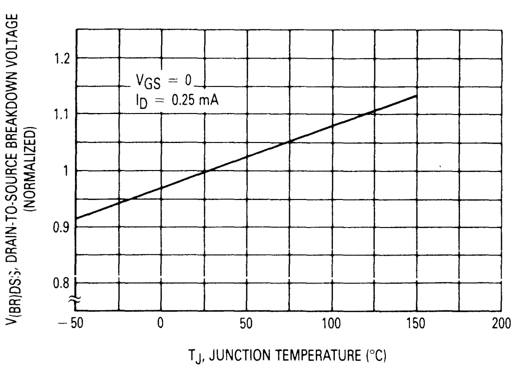


Figure 4. Breakdown Voltage Variation With Temperature

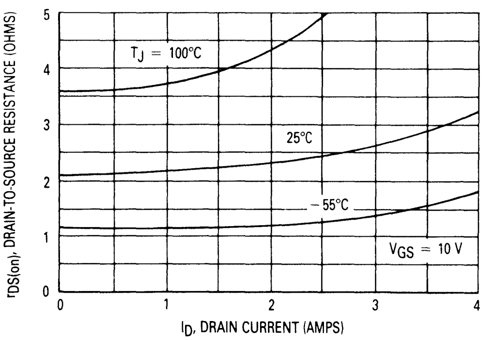


Figure 5. On-Resistance versus Drain Current

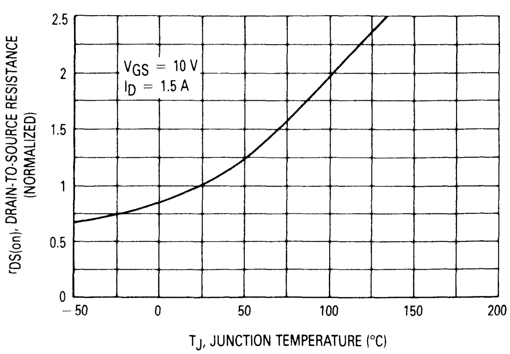


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

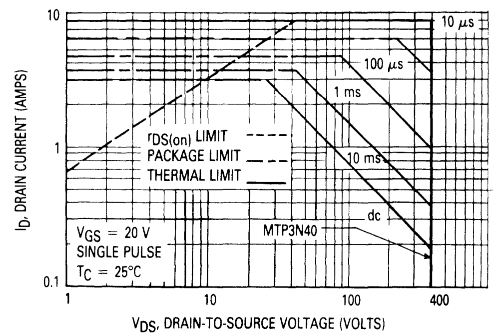


Figure 7. Maximum Rated Forward Biased Safe Operating Area

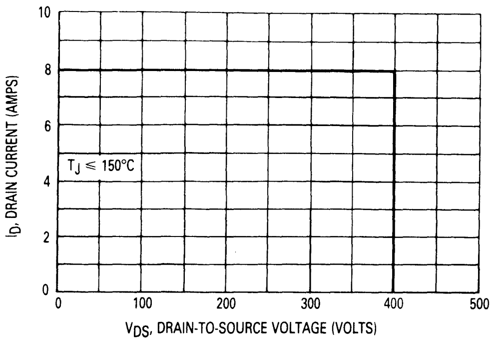


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

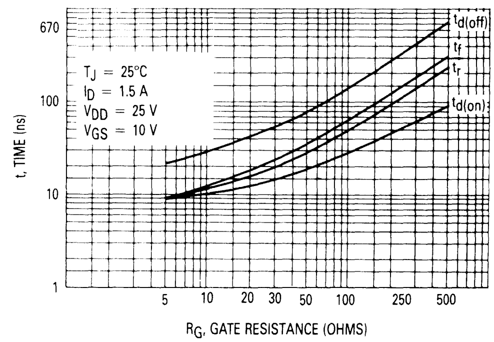


Figure 9. Resistive Switching Time Variation versus Gate Resistance

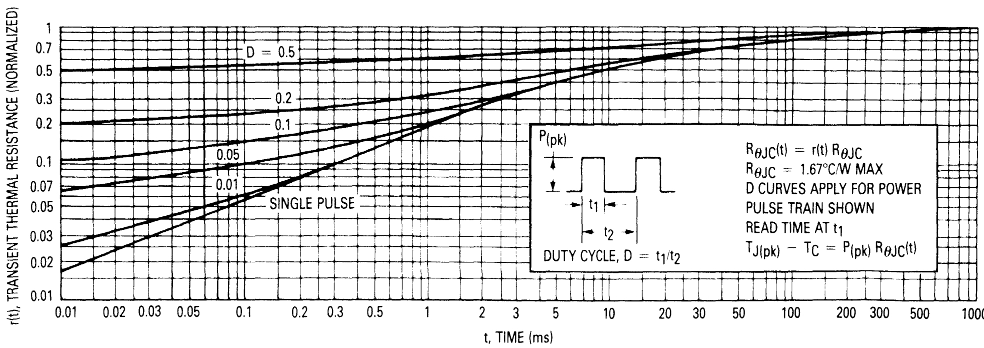


Figure 10. Thermal Response

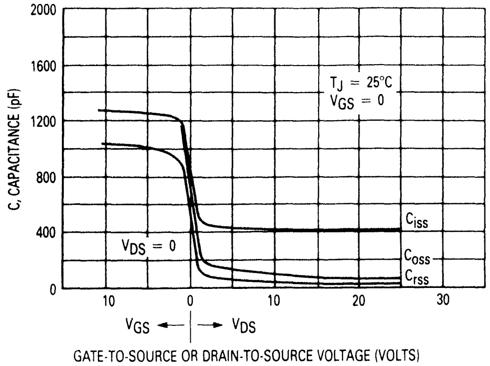


Figure 11. Capacitance Variation

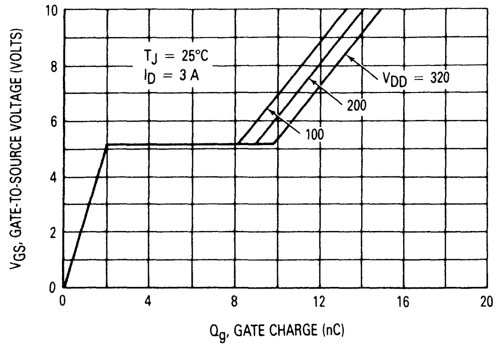


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

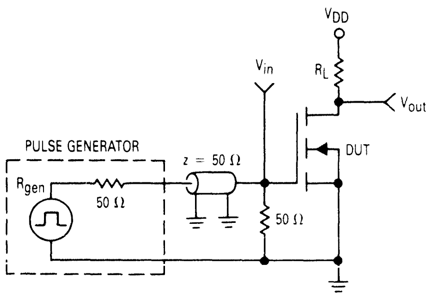


Figure 13. Switching Test Circuit

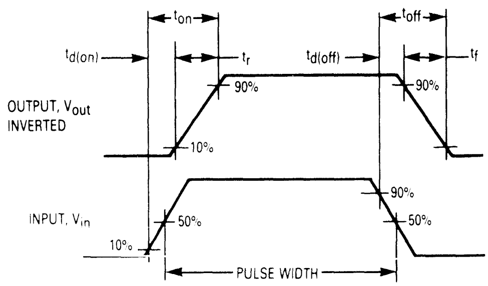
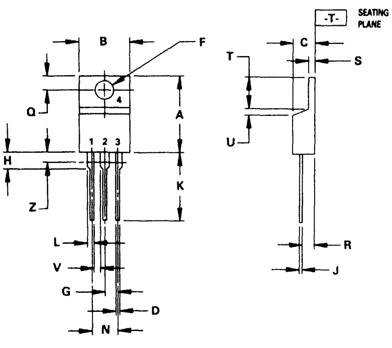


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



CASE 221A-04
TO-220AB

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MTP3N45
MTP3N50

Designer's Data Sheet

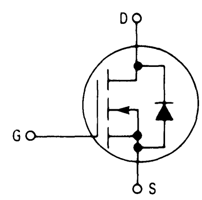
Power Field Effect Transistor

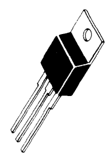
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
3 AMPERES
$r_{DS(on)}$ = 3 OHMS
450 and 500 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MTP3N45	MTP3N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current				Adc
Continuous	I_D	3		
Pulsed	I_{DM}	10		
Total Power Dissipation @ T_C = 25°C	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP3N45 MTP3N50		$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$r_{DS(on)}$	—	3	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc) (I_D = 1.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	9 7	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	40	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	30	
Turn-Off Delay Time		$t_{d(off)}$	—	90	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	16 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	10 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

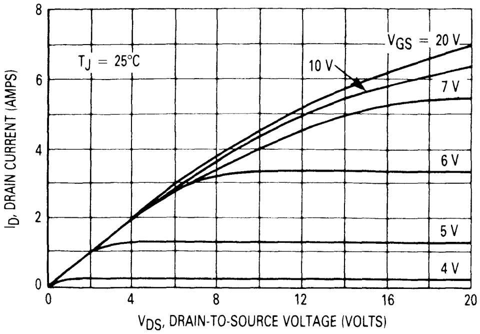


Figure 1. On-Region Characteristics

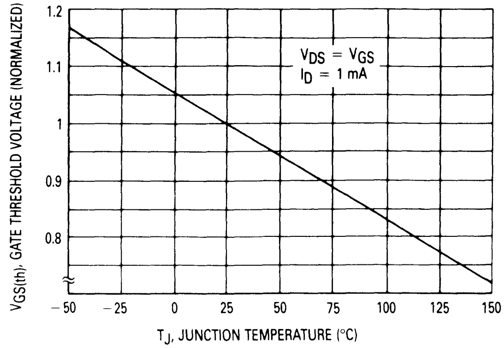


Figure 2. Gate-Threshold Voltage Variation With Temperature

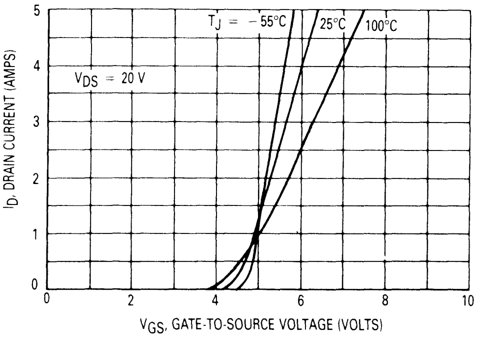


Figure 3. Transfer Characteristics

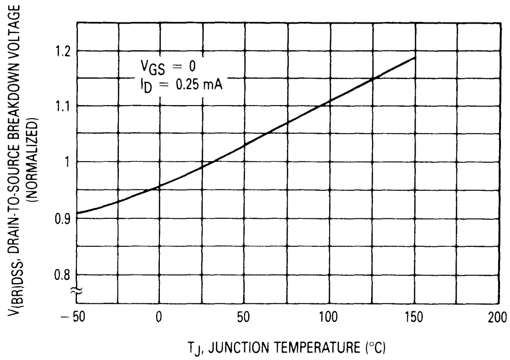


Figure 4. Breakdown Voltage Variation With Temperature

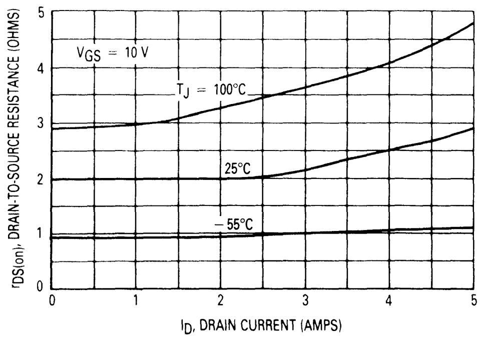


Figure 5. On-Resistance versus Drain Current

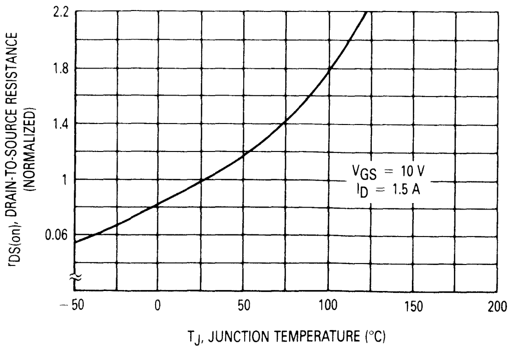


Figure 6. On-Resistance Variation With Temperature

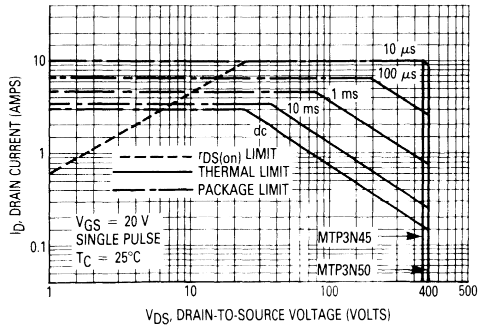


Figure 7. Maximum Rated Forward Biased Safe Operating Area

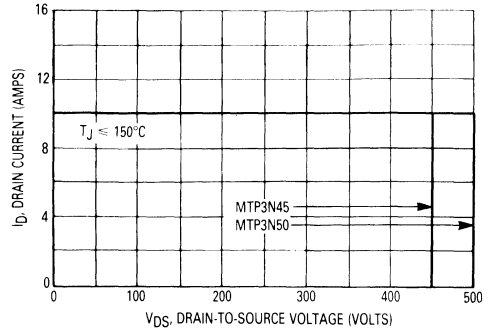


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

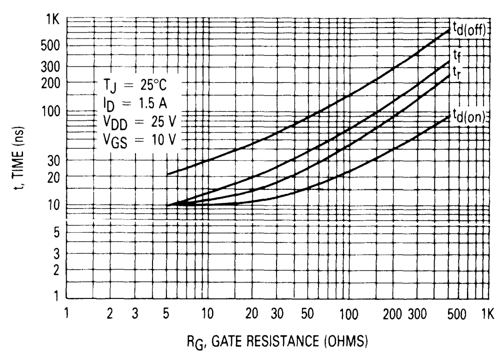


Figure 9. Resistive Switching Time Variation versus Gate Resistance

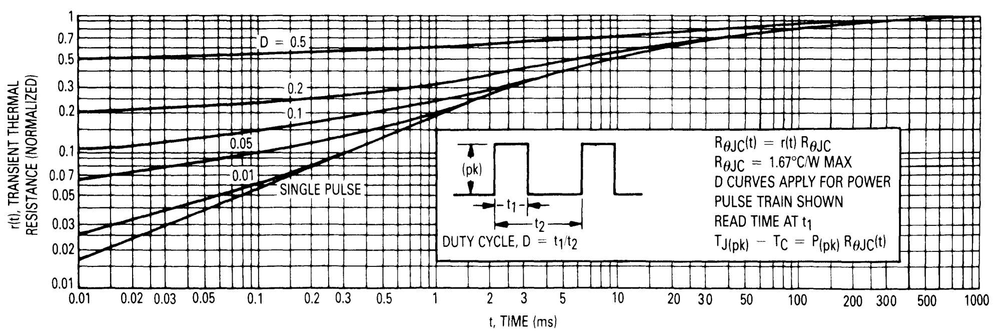


Figure 10. Thermal Response

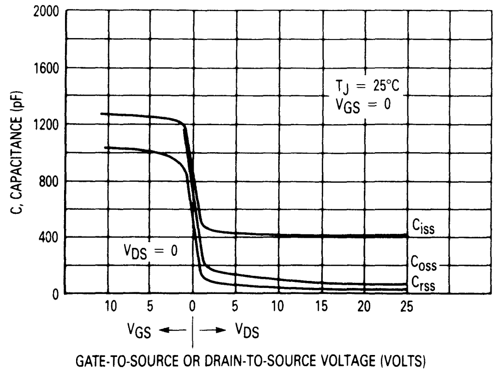


Figure 11. Capacitance Variation

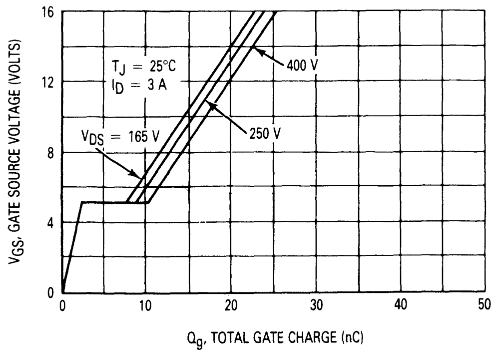


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

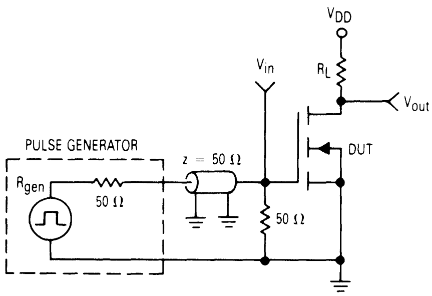


Figure 13. Switching Test Circuit

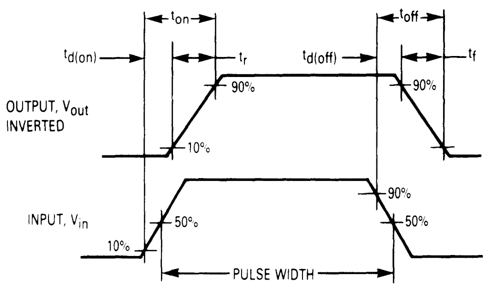
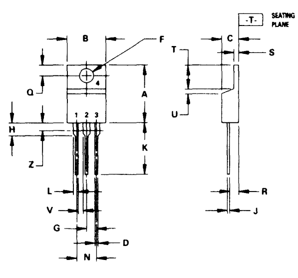


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTP3N95
MTP3N100
MTP4N85
MTP4N90

Designer's Data Sheet

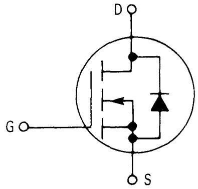
Power Field Effect Transistor

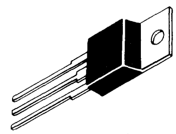
N-Channel Enhancement Mode Silicon Gate TMOS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
3 and 4 AMPERES
$r_{DS(on)}$ = 4 OHMS
850, 900, 950
and 1000 VOLTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP				Unit
		4N85	4N90	3N95	3N100	
Drain-Source Voltage	V_{DSS}	850	900	950	1000	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	850	900	950	1000	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40				Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 4 18		 3 16		Adc
Gate Current — Pulsed	I_{GM}	1.5				Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6				Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150				°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP4N85 MTP4N90 MTP3N95 MTP3N100	$V_{(BR)DSS}$	850 900 950 1000	— — — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc) (V_{GS} = 10 Vdc, I_D = 2 Adc)	MTP3N95/3N100 MTP4N85/4N90	$r_{DS(on)}$	— —	4 4	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 3 Adc) (I_D = 1.5 Adc, T_J = 100°C) (I_D = 4 Adc) (I_D = 2 Adc, T_C = 100°C)	MTP3N95/3N100 MTP4N85/4N90	$V_{DS(on)}$	— — — —	12 10 16 14	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 1.5 A) (V_{DS} = 10 V, I_D = 2 A)	MTP3N95/3N100 MTP4N85/4N90	g_{fs}	2 2	— —	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	1500	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	60	
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figs. 8 and 9.	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	40	
Turn-Off Delay Time		$t_{d(off)}$	—	250	
Fall Time		t_f	—	75	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 Vdc) See Figs. 10 and 11.	Q_g	55 (typ)	85	nC
Gate-Source Charge		Q_{gs}	30 (typ)	—	
Gate-Drain Charge		Q_{gd}	25 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0) See Figs. 16 and 17.	V_{SD}	1.1 (typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	200 (typ)	—	ns
Reverse Recovery Time		t_{rr}	1000 (typ)	—	ns

TYPICAL CHARACTERISTICS

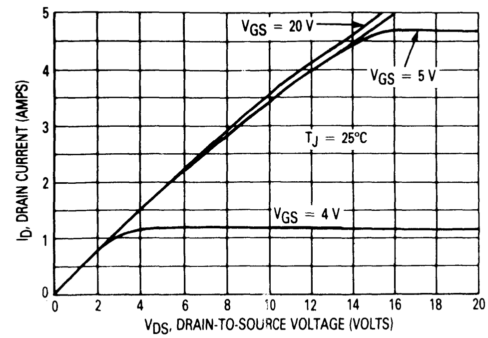


Figure 1. On-Region Characteristics

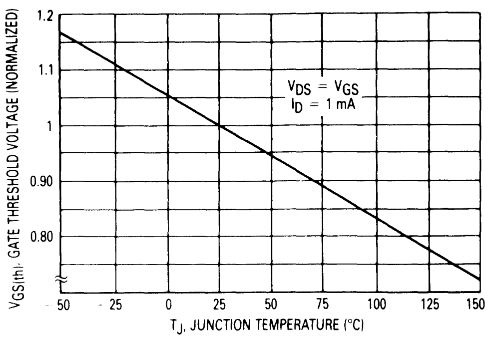


Figure 2. Gate-Threshold Voltage Variation with Temperature

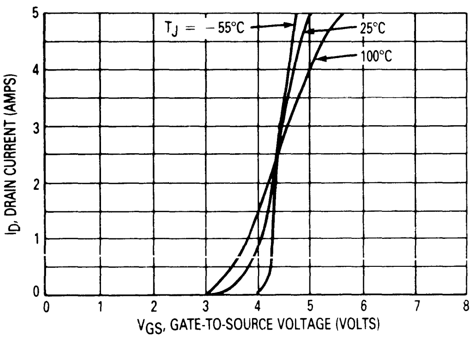


Figure 3. Transfer Characteristics

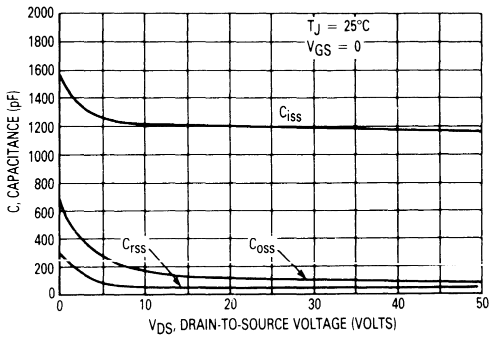


Figure 4. Capacitance Variation

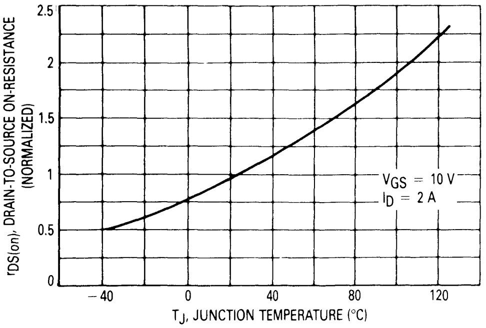


Figure 5. Normalized On-Resistance versus Temperature

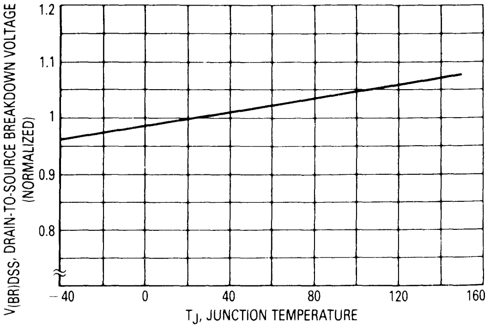


Figure 6. Normalized Breakdown Voltage versus Temperature

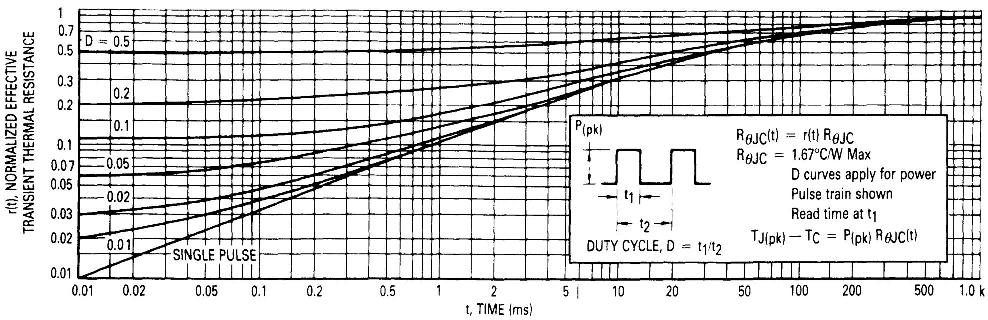


Figure 7. Thermal Response

RESISTIVE SWITCHING

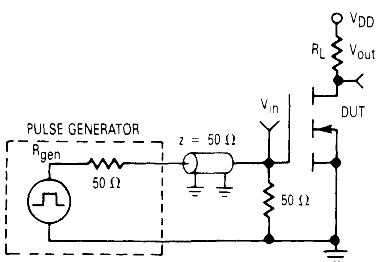


Figure 8. Switching Test Circuit

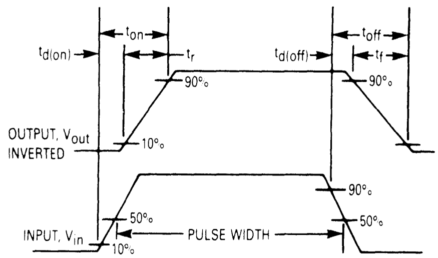


Figure 9. Switching Waveforms

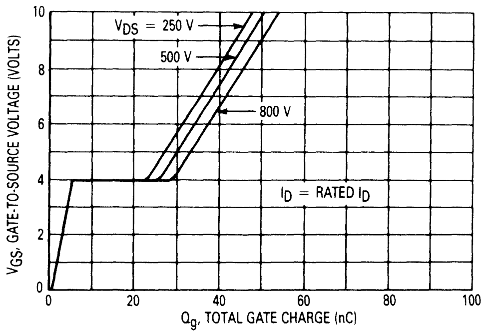
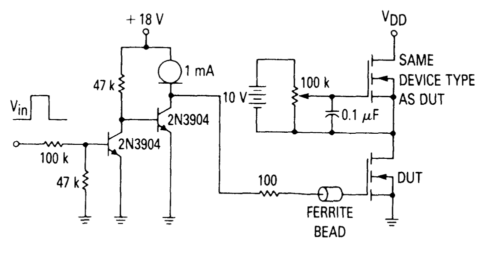


Figure 10. Gate Charge Variation



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 11. Gate Charge Test Circuit

SAFE OPERATING AREA INFORMATION

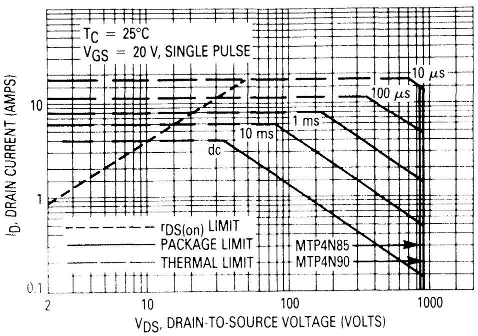


Figure 12. Maximum Rated Forward Biased Safe Operating Area

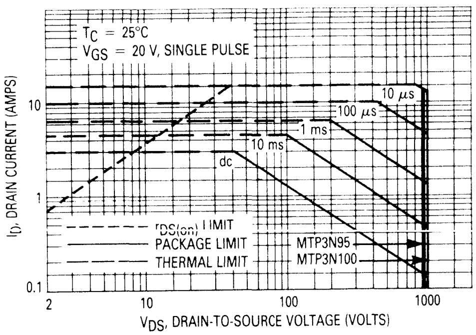


Figure 13. Maximum Rated Forward Biased Safe Operating Area

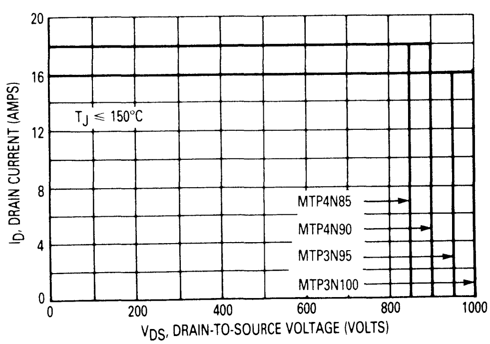


Figure 14. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The dc data of Figures 11 and 12 are based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figures 11 and 12
$T_{J(max)}$ = rated maximum junction temperature
T_C = device case temperature
P_D = rated power dissipation at T_C = 25°C
$R_{\theta JC}$ = rated steady state thermal resistance
$r(t)$ = normalized thermal response from Figure 7

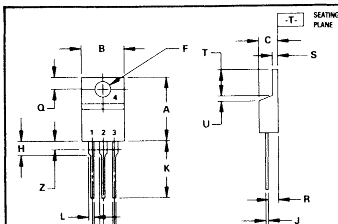
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP4N05L
MTP4N06L

Designer's Data Sheet

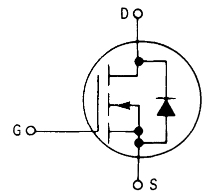
Power Field Effect Transistor

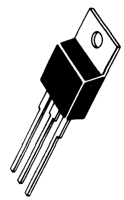
N-Channel Enhancement-Mode Silicon Gate TMOS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
LOGIC LEVEL
4 AMPERES
$r_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	MTP4N05L	MTP4N06L	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±15 ±20		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	4 16		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	25 0.2		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) MTP4N05L MTP4N06L	$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	 1 0.75	 2 1.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 4 Adc) (I_D = 2 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 3 1.8	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 2 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	225	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	600	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	40	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	360	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{oss}	—	100	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 2 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	40	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 4 A, V_{GS} = 5 Vdc) See Figures 11 and 12.	Q_g	4 (typ)	8	nC
Gate-Source Charge		Q_{gs}	1.5 (typ)	—	
Gate-Drain Charge		Q_{gd}	2.5 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = 4 A, V_{GS} = 0) See Figures 14 and 15.	V_{SD}	1.2 (typ)	1.6	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	250 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (typ) 4.5 (typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

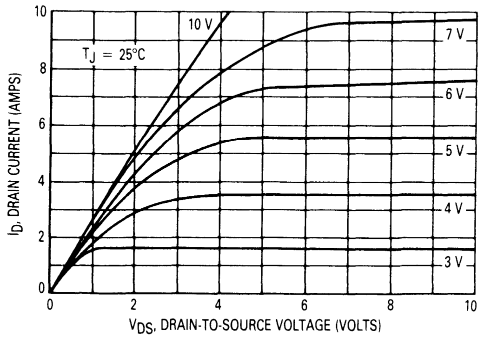


Figure 1. On-Region Characteristics

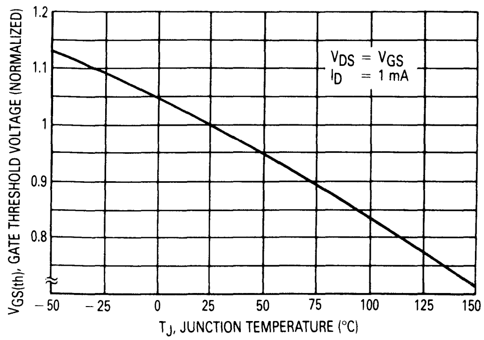


Figure 2. Gate-Threshold Variation With Temperature

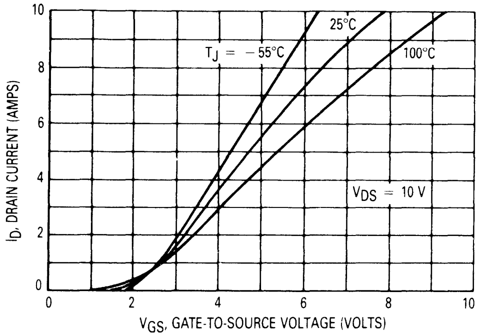


Figure 3. Transfer Characteristics

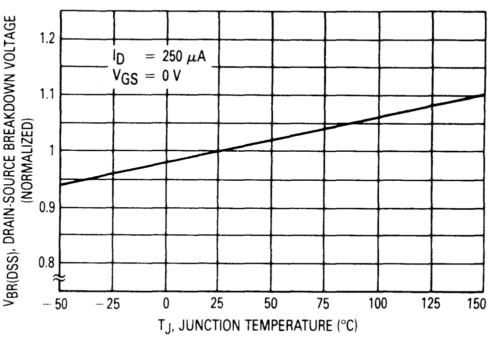


Figure 4. Breakdown Voltage Variation With Temperature

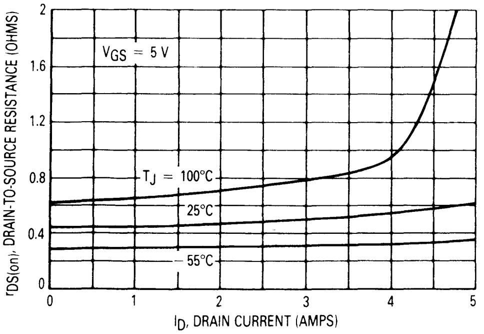


Figure 5. On-Resistance versus Drain Current

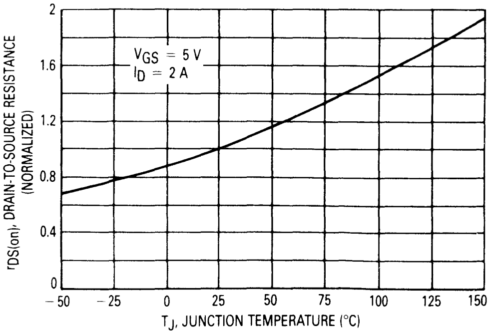


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

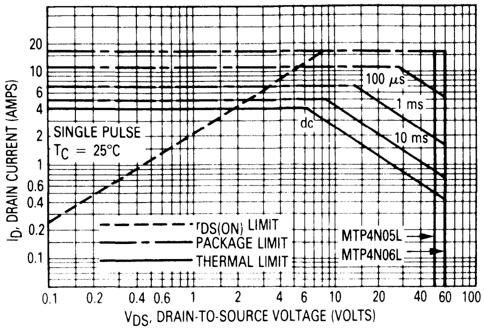


Figure 7. Maximum Rated Forward Biased Safe Operating Area

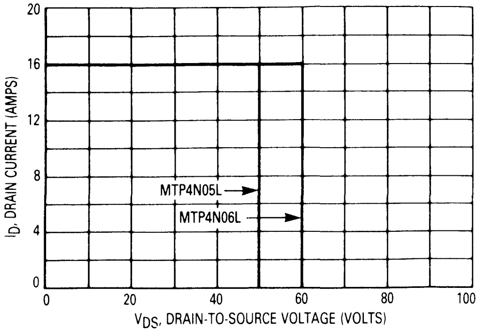


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

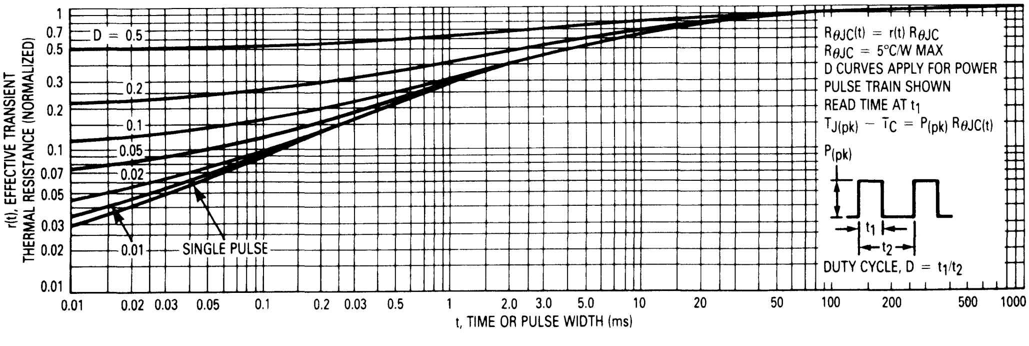


Figure 9. Thermal Response

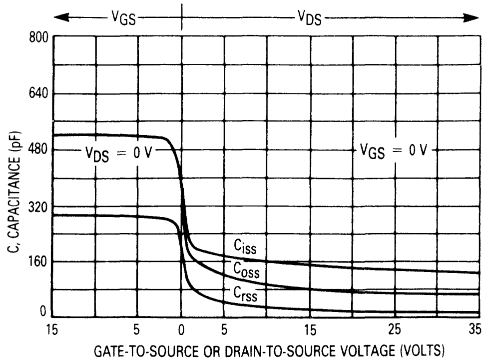


Figure 10. Capacitance Variation

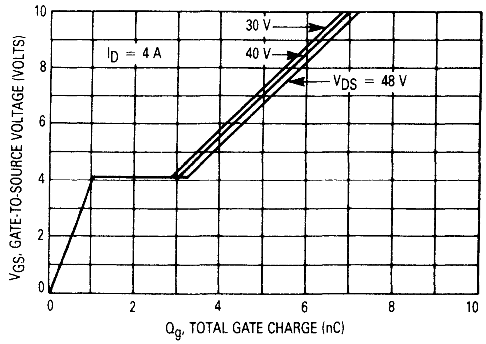
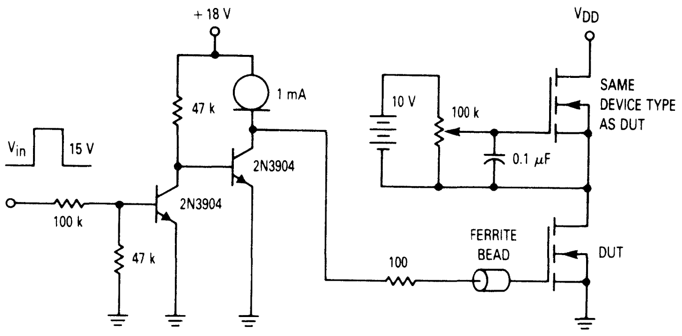


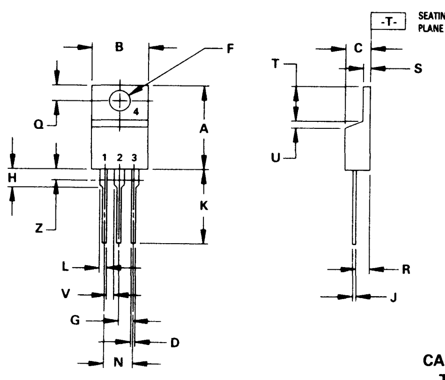
Figure 11. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 12. Gate Charge Test Circuit

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

3

MTP4N08

Designer's Data Sheet

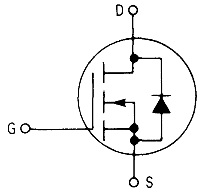
Power Field Effect Transistor

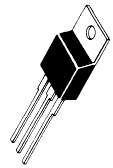
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
4 AMPERES
$r_{DS(on)}$ = 0.8 OHM
80 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	80	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 4 9	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	80	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2 Adc)		$r_{DS(on)}$	—	0.8	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4 Adc) (I_D = 2 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3.6 3.2	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	200	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	80	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	3.75 (Typ)	10	nC
Gate-Source Charge		Q_{gs}	1.75 (Typ)	—	
Gate-Drain Charge		Q_{gd}	2 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.8 (Typ)	2.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

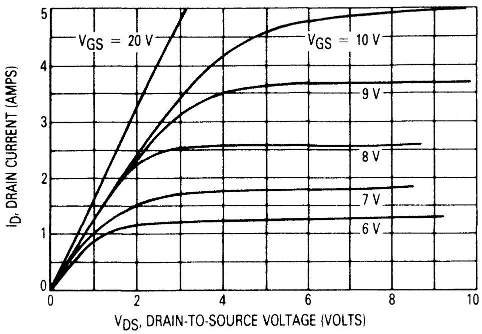


Figure 1. On-Region Characteristics

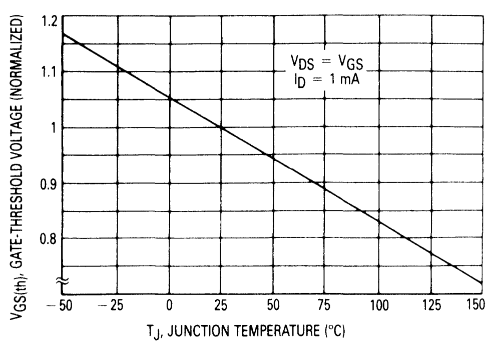


Figure 2. Gate-Threshold Voltage Variation With Temperature

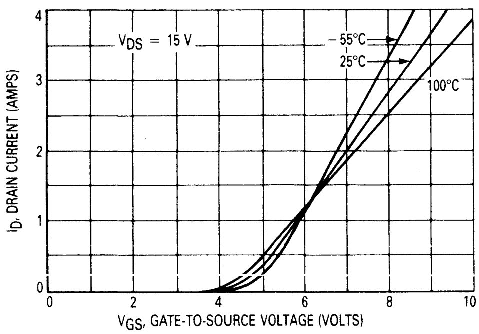


Figure 3. Transfer Characteristics

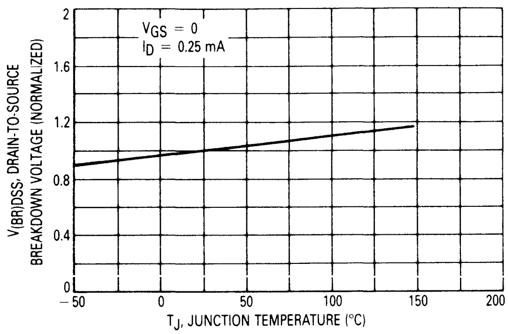


Figure 4. Breakdown Voltage Variation With Temperature

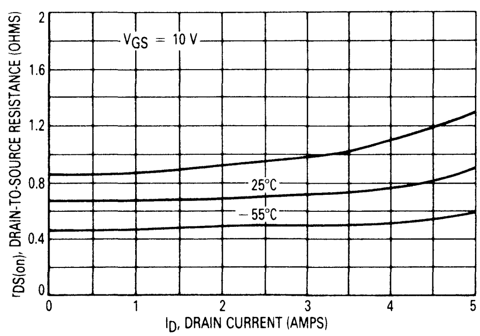


Figure 5. On-Resistance versus Drain Current

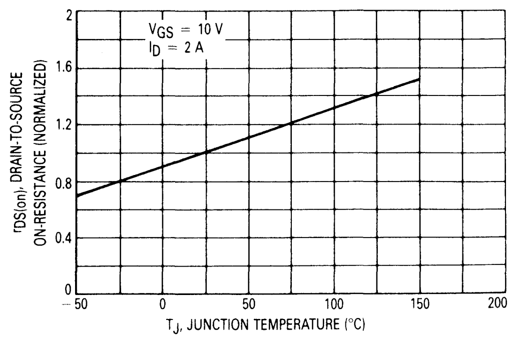


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

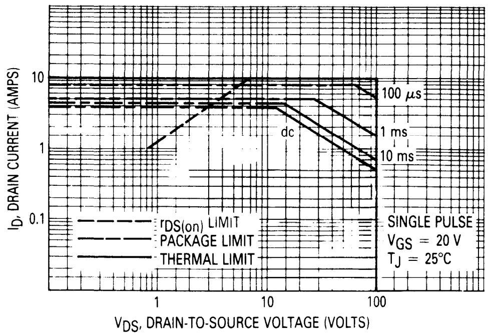


Figure 7. Maximum Rated Forward Biased Safe Operating Area

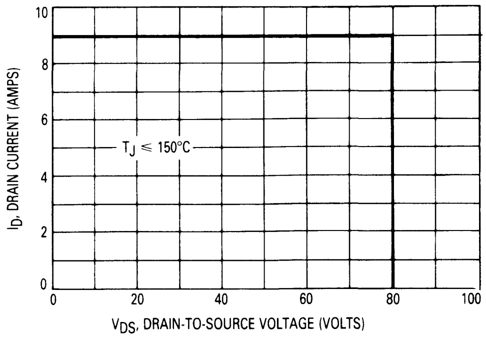


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

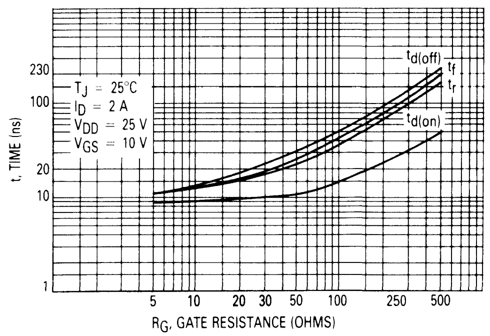


Figure 9. Gate Resistance versus Time

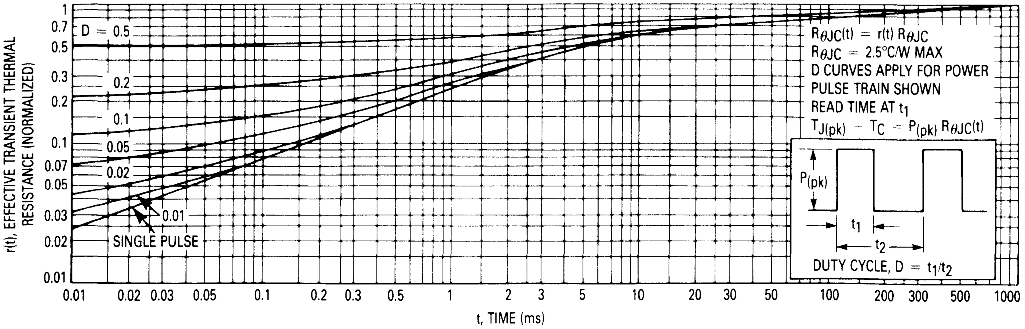


Figure 10. Thermal Response

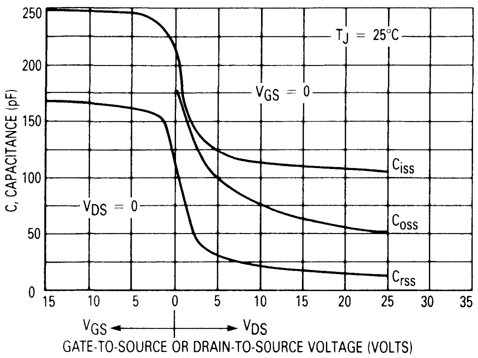


Figure 11. Capacitance Variation

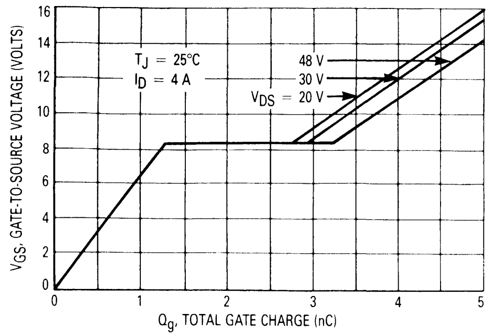


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

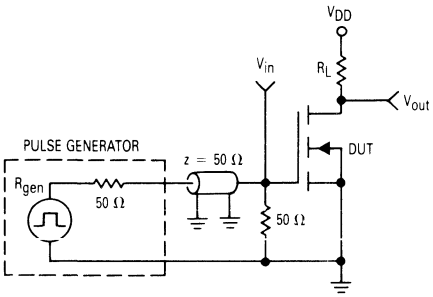


Figure 13. Switching Test Circuit

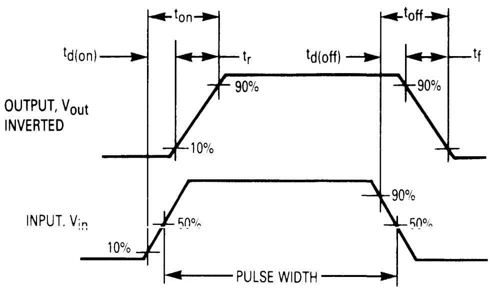
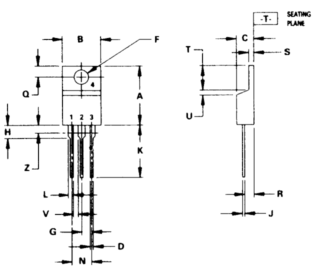


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP5N05
MTP5N06

Designer's Data Sheet

Power Field Effect Transistor

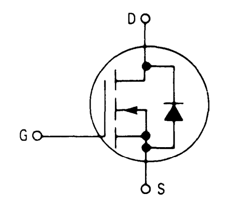
N-Channel Enhancement-Mode Silicon Gate TMOS

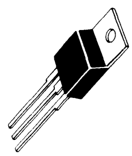
These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
5 AMPERES
$r_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS

3





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 5N05	MTP 5N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 5 10		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP5N05 / MTP5N06		$V_{(BR)DSS}$	50 / 60	— / —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) / (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— / —	10 / 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) / T_J = 100°C		$V_{GS(th)}$	2 / 1.5	4.5 / 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) / (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— / —	3.2 / 3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	200	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	80	
Turn-Off Delay Time		$t_{d(off)}$	—	30	
Fall Time		t_f	—	30	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	3.75 (Typ)	10	nC
Gate-Source Charge		Q_{gs}	1.75 (Typ)	—	
Gate-Drain Charge		Q_{gd}	2 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) / (Measured from the drain lead 0.25" from package to center of die)		L_d	3.5 (Typ) / 4.5 (Typ)	— / —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

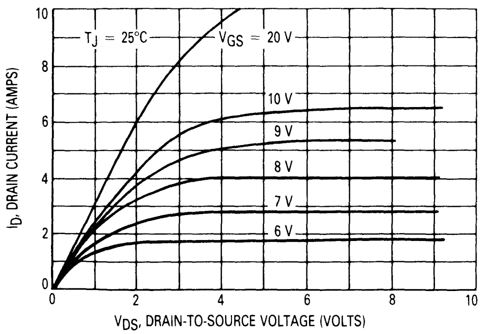


Figure 1. On-Region Characteristics

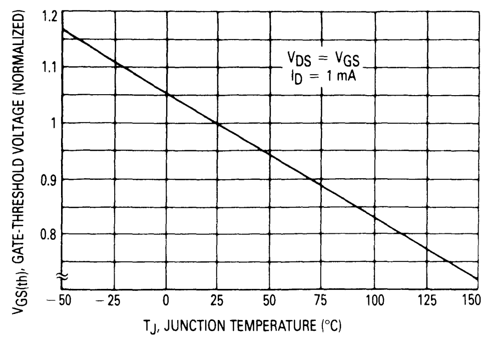


Figure 2. Gate-Threshold Voltage Variation With Temperature

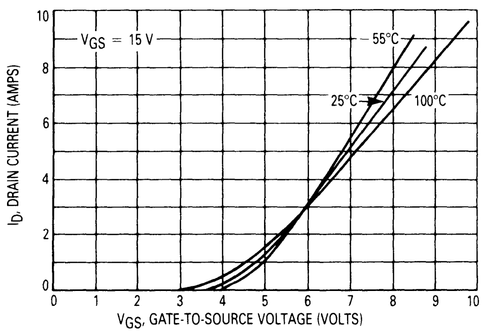


Figure 3. Transfer Characteristics

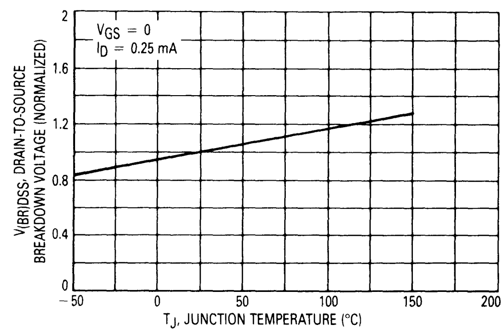


Figure 4. Breakdown Voltage Variation With Temperature

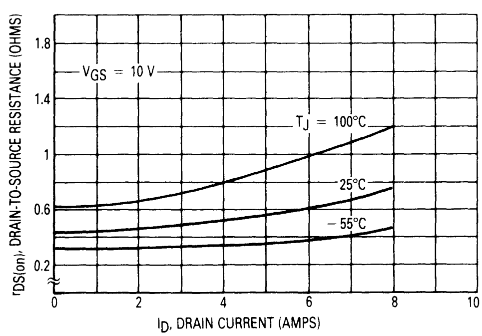


Figure 5. On-Resistance versus Drain Current

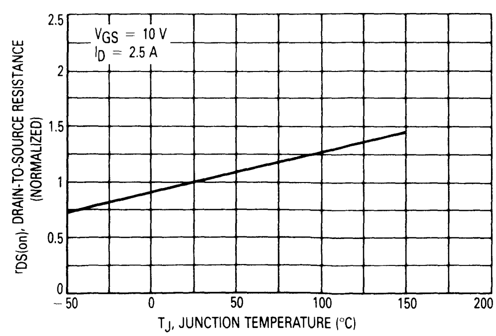


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

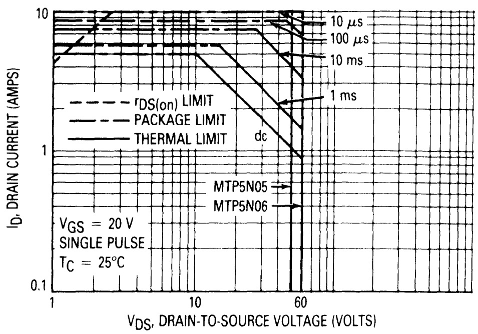


Figure 7. Maximum Rated Forward Biased Safe Operating Area

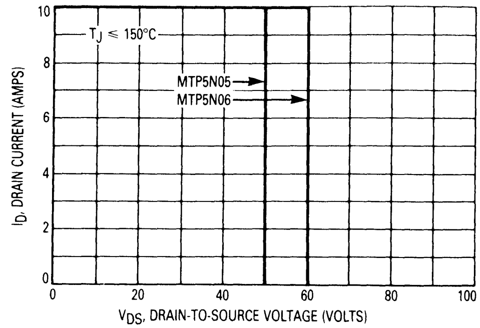


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

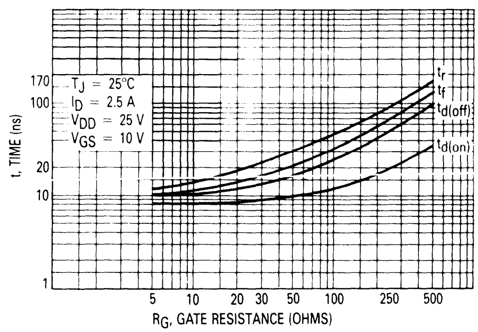


Figure 9. Resistive Switching Time Variation versus Gate Resistance

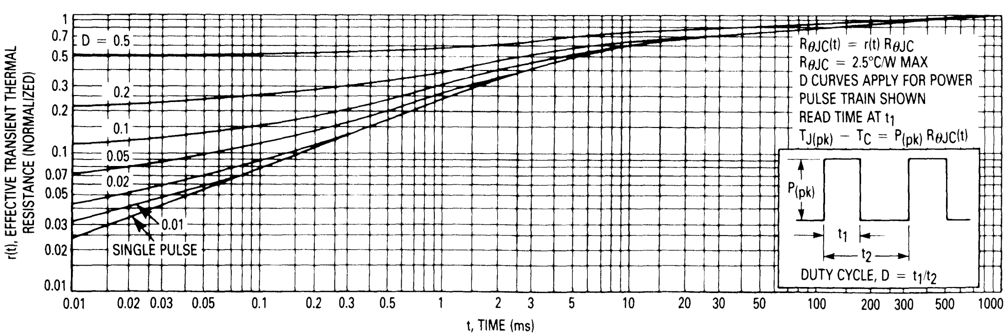


Figure 10. Thermal Response

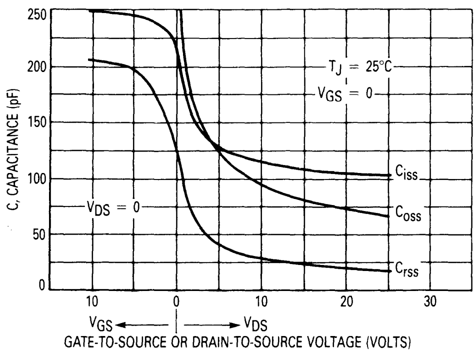


Figure 11. Capacitance Variation

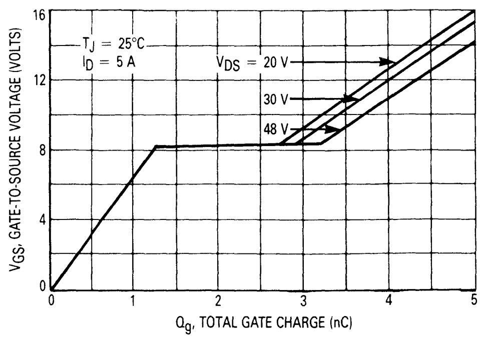


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

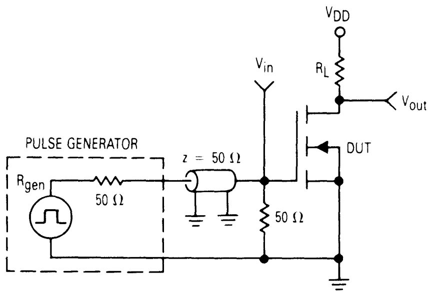


Figure 13. Switching Test Circuit

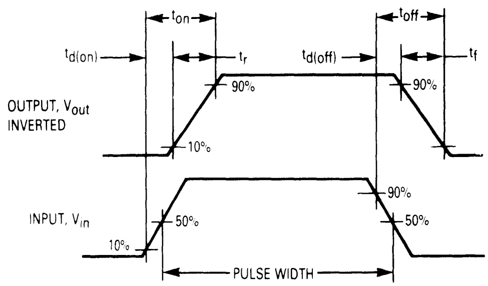
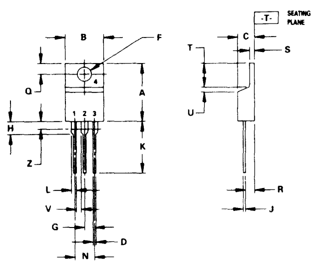


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP5N12

Designer's Data Sheet

Power Field Effect Transistor

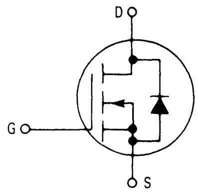
N-Channel Enhancement-Mode Silicon Gate TMOS

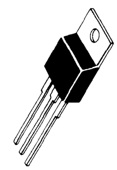
TMOS

TMOS POWER FET
5 AMPERES
$r_{DS(on)}$ = 0.9 OHM
120 VOLTS

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	120	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	120	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 5 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	120	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$r_{DS(on)}$	—	0.9	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	6.4 4.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)		g_{FS}	0.75	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	200	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	20	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	6.5 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	3.5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	3 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

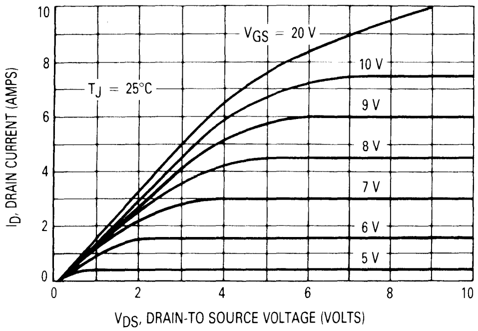


Figure 1. On-Region Characteristics

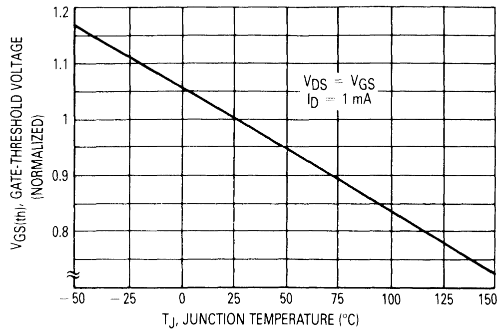


Figure 2. Gate-Threshold Voltage Variation With Temperature

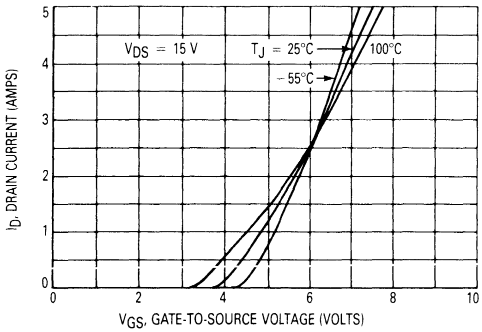


Figure 3. Transfer Characteristics

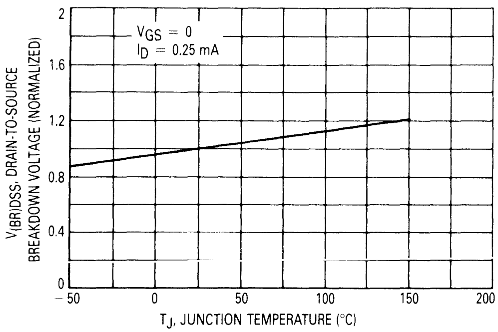


Figure 4. Breakdown Voltage Variation With Temperature

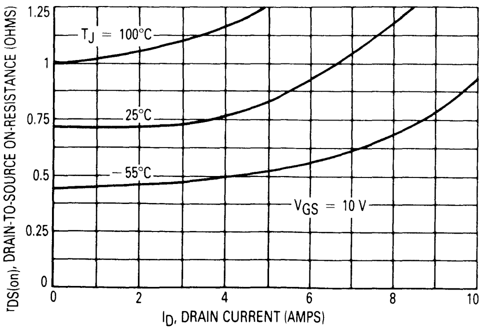


Figure 5. On-Resistance versus Drain Current

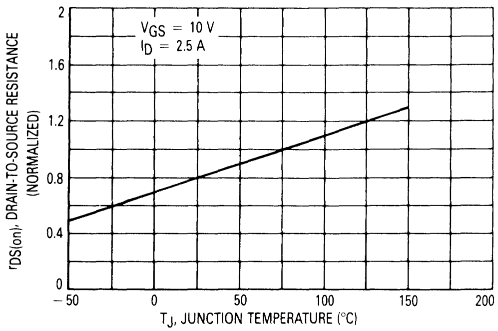


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

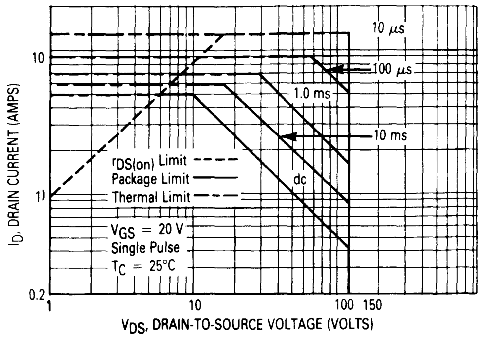


Figure 7. Maximum Rated Forward Biased Safe Operating Area

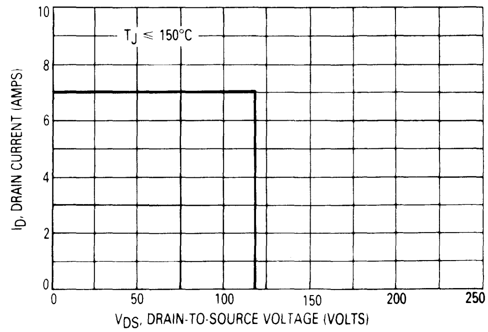


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

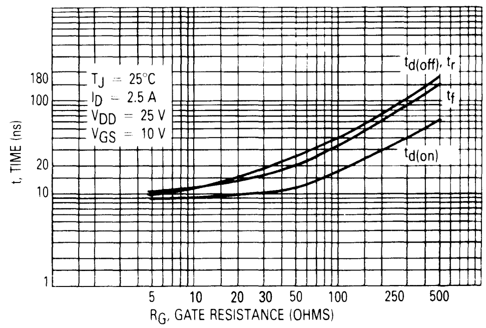


Figure 9. Resistive Switching versus Gate Resistance

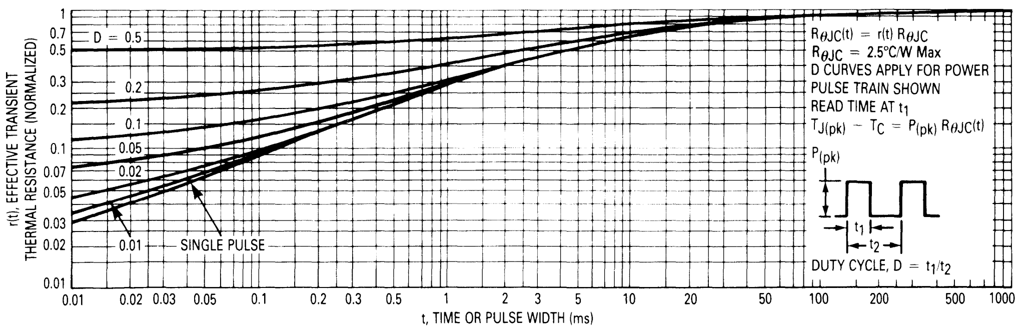


Figure 10. Thermal Response

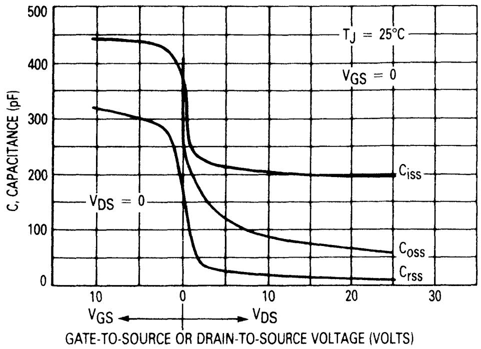


Figure 11. Capacitance Variation

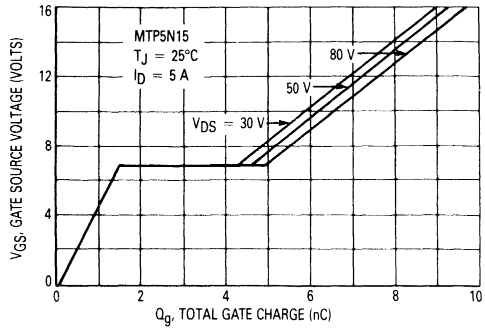


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

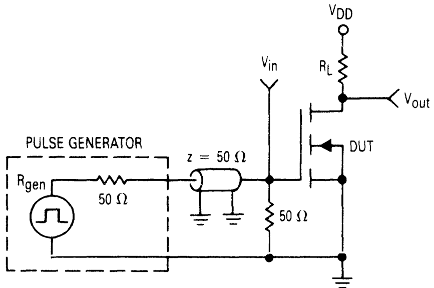


Figure 13. Switching Test Circuit

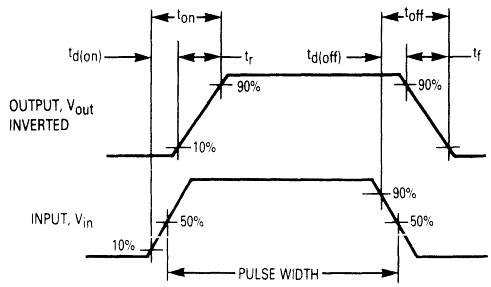
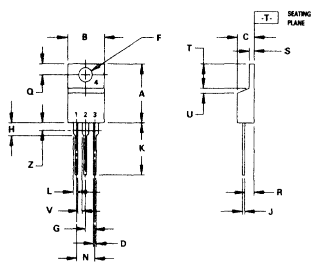


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

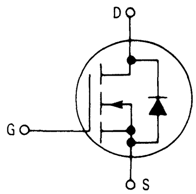
MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP5N20

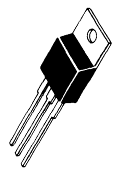
Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



TMOS POWER FET
5 AMPERES
$r_{DS(on)}$ = 1 OHM
200 VOLTS



CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 5 15	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.67	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP5N20	$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C	$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$r_{DS(on)}$	—	1	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 5 Adc) (I_D = 2.5 Adc, T_J = 100°C)	$V_{DS(on)}$	 — —	 6 5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 2.5 A)	g_{FS}	1.5	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	100	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	9 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.2 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

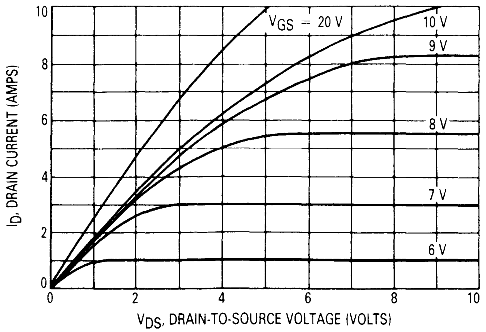


Figure 1. On-Region Characteristics

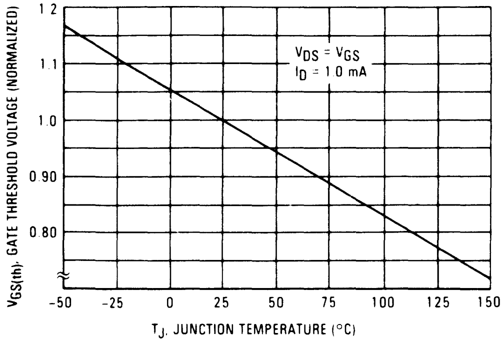


Figure 2. Gate-Threshold Voltage Variation With Temperature

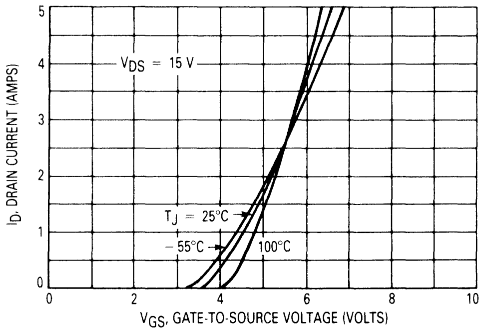


Figure 3. Transfer Characteristics

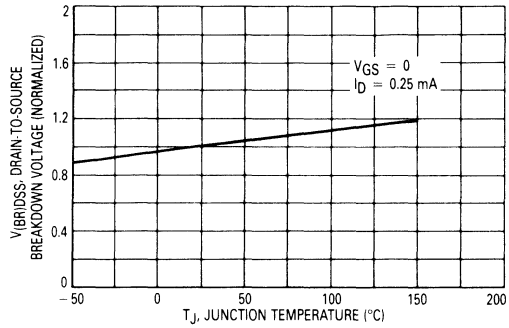


Figure 4. Breakdown Voltage Variation With Temperature

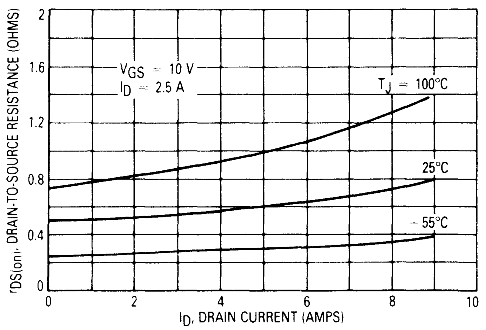


Figure 5. On-Resistance versus Drain Current

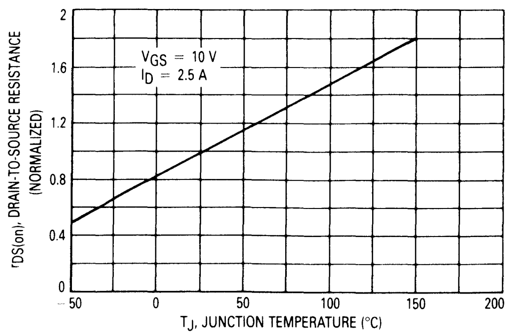


Figure 6. On-Resistance Variation With Temperature

3

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SAFE OPERATING AREA INFORMATION

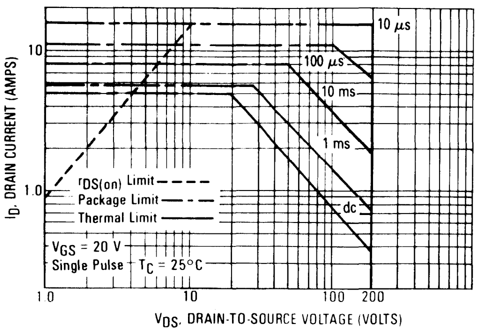


Figure 7. Maximum Rated Forward Biased Safe Operating Area

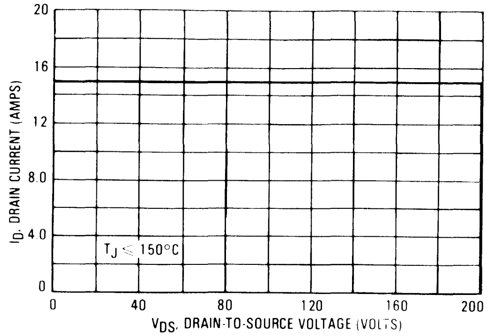


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

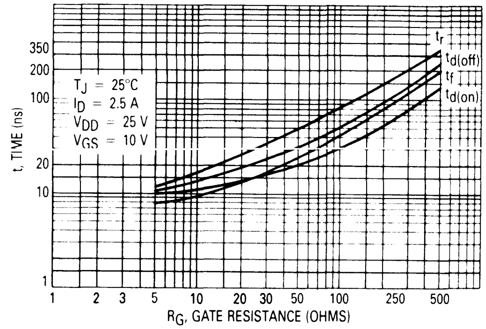


Figure 9. Resistive Switching Time Variation versus Gate Resistance

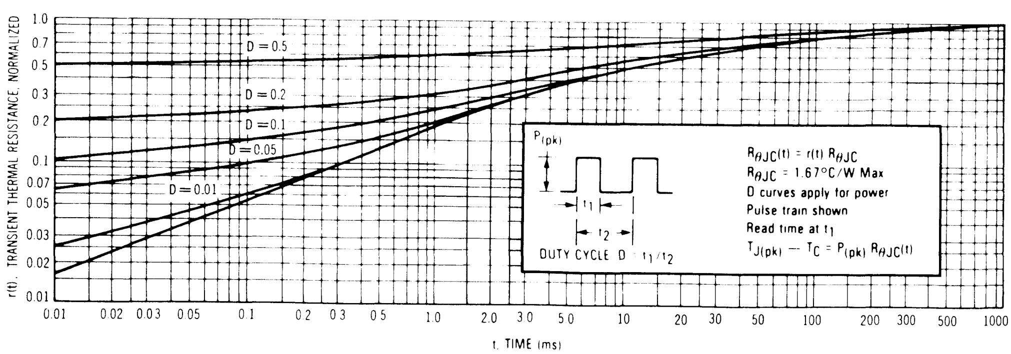


Figure 10. Thermal Response

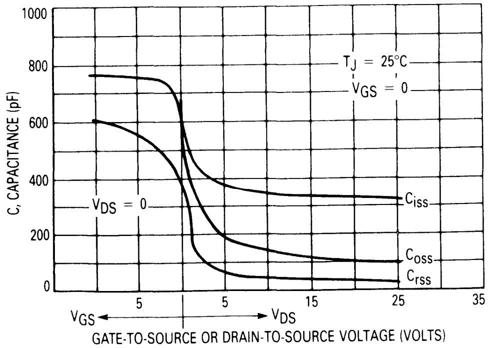


Figure 11. Capacitance Variation

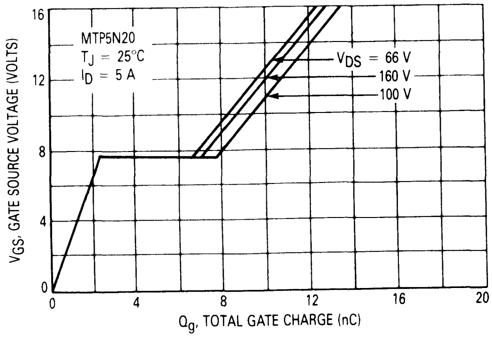


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

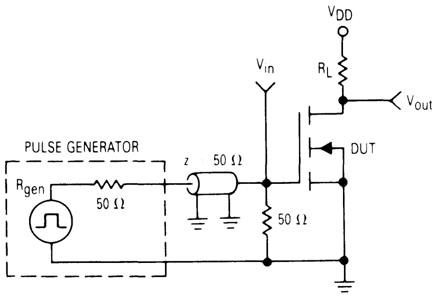


Figure 13. Switching Test Circuit

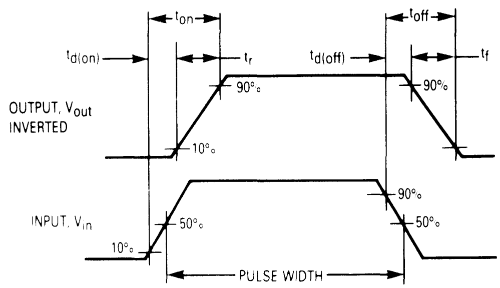
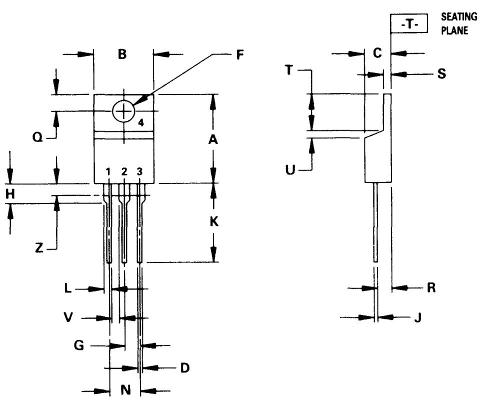


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MTP6N10

Designer's Data Sheet

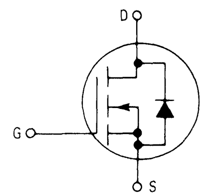
Power Field Effect Transistor

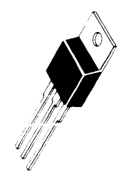
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
6 AMPERES
$r_{DS(on)}$ = 0.6 OHM
100 VOLTS

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 6 12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc)		$V_{DS(on)}$	—	4.2	Vdc
(I_D = 3 Adc, T_J = 100°C)			—	3.6	
Forward Transconductance (V_{DS} = 15 V, I_D = 3 A)		g_{FS}	1	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	200	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	25	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	6.5 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	3.5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	3 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.3 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	250 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

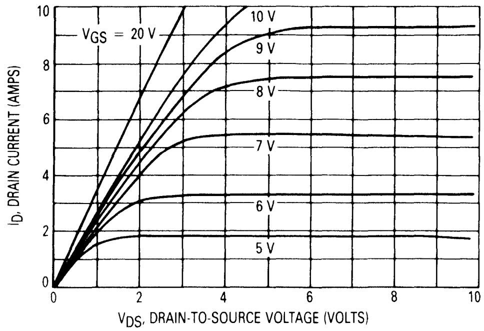


Figure 1. On-Region Characteristics

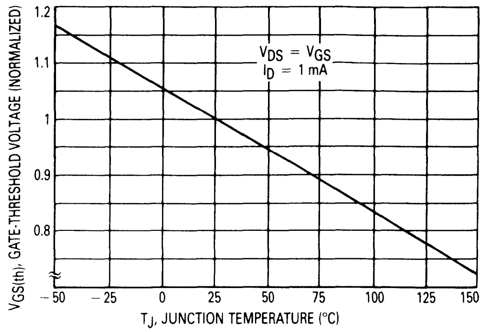


Figure 2. Gate-Threshold Voltage Variation With Temperature

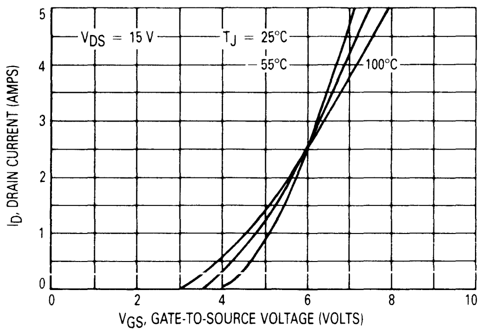


Figure 3. Transfer Characteristics

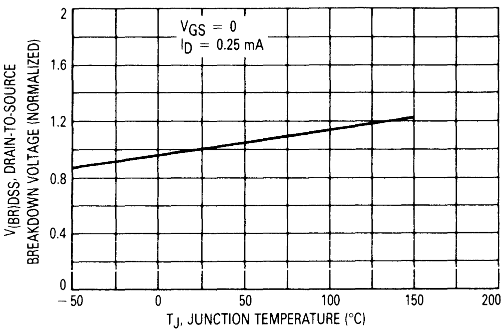


Figure 4. Breakdown Voltage versus Temperature

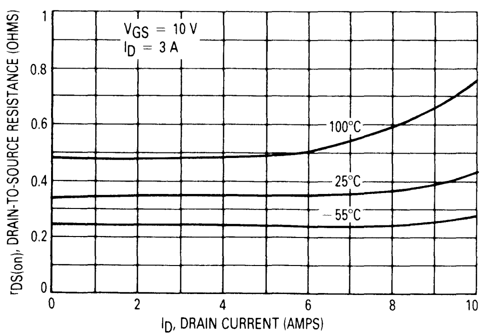


Figure 5. On-Resistance versus Drain Current

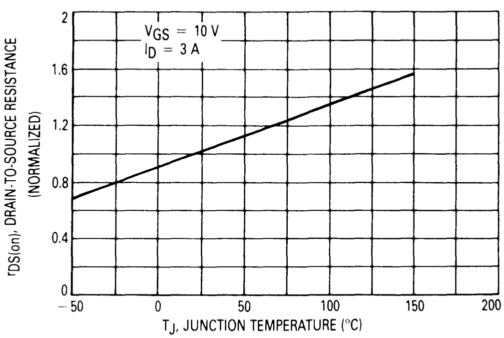


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

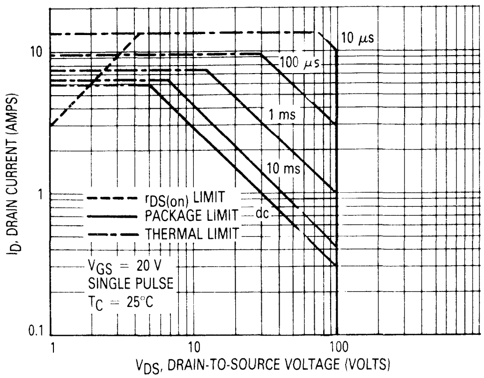


Figure 7. Maximum Rated Forward Biased Safe Operating Area

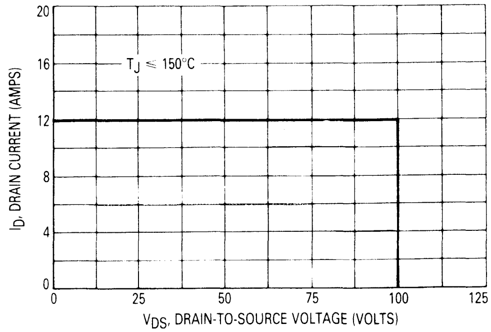


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

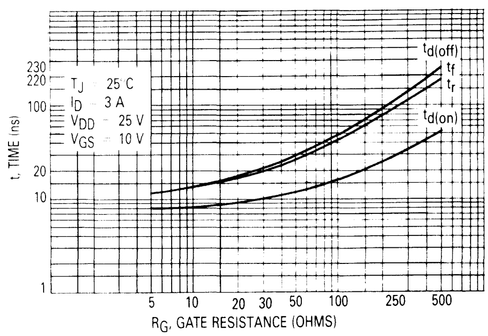


Figure 9. Resistive Switching versus Gate Resistance

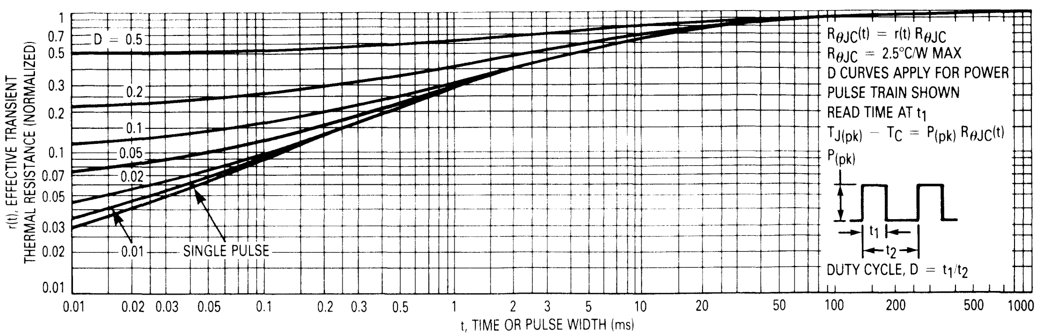


Figure 10. Thermal Response

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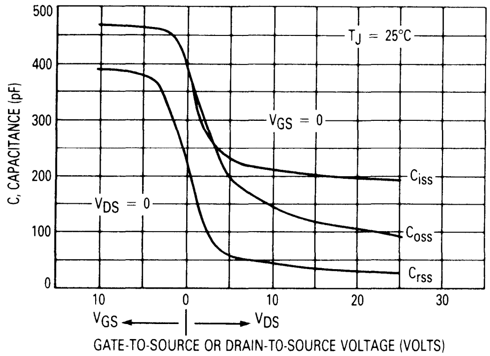


Figure 11. Capacitance Variation

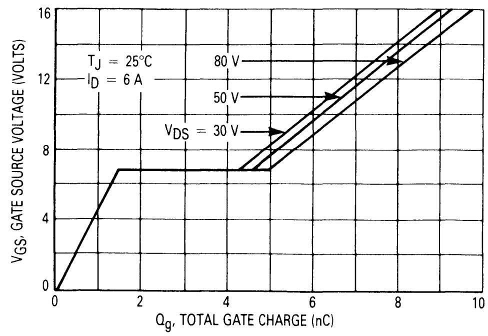


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

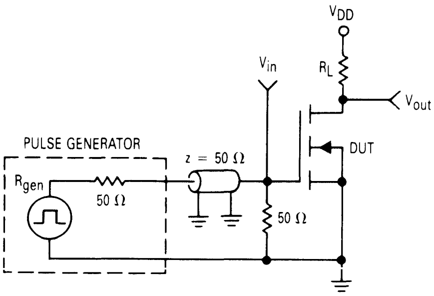


Figure 13. Switching Test Circuit

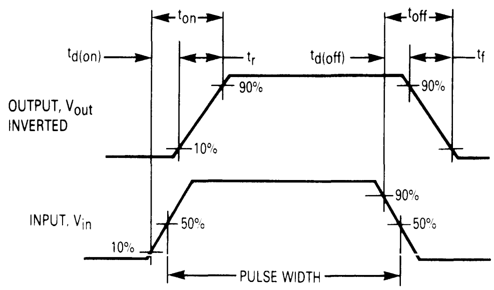
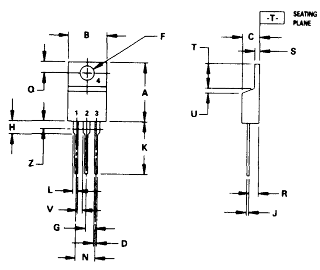


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

MTP6N55
MTP6N60

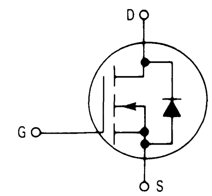
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

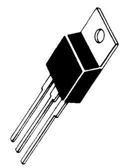
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS

TMOS POWER FETs
6 AMPERES
$r_{DS(on)}$ = 1.2 OHMS
550 and 600 VOLTS

3





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 6N55	MTP 6N60	Unit
Drain-Source Voltage	V_{DSS}	550	600	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	550	600	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 6 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP6N55 / MTP6N60		$V_{(BR)DSS}$	550 / 600	— / —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) / (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— / —	0.2 / 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) / T_J = 100°C		$V_{GS(th)}$	2 / 1.5	4.5 / 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3 Adc)		$r_{DS(on)}$	—	1.2	Ohms
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 6 Adc) / (I_D = 3 Adc, T_J = 100°C)		$V_{DS(on)}$	— / —	8 / 7.2	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 3 A)		g_{FS}	2	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1800	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	45 (Typ)	65	nC
Gate-Source Charge		Q_{gs}	22 (Typ)	—	
Gate-Drain Charge		Q_{gd}	23 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.3 (Typ)	—	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) / (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) / 4.5 (Typ)	— / —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

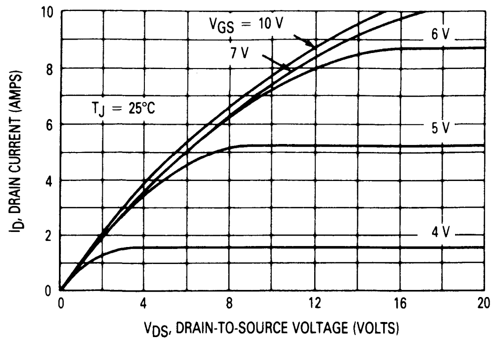


Figure 1. On-Region Characteristics

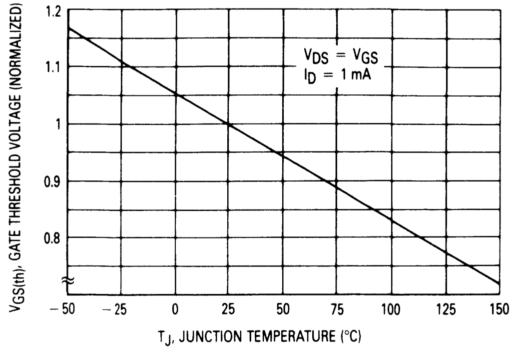


Figure 2. Gate-Threshold Voltage Variation With Temperature

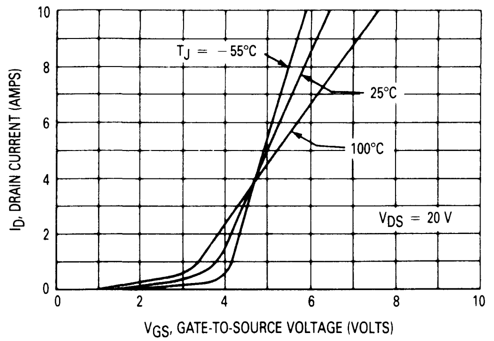


Figure 3. Transfer Characteristics

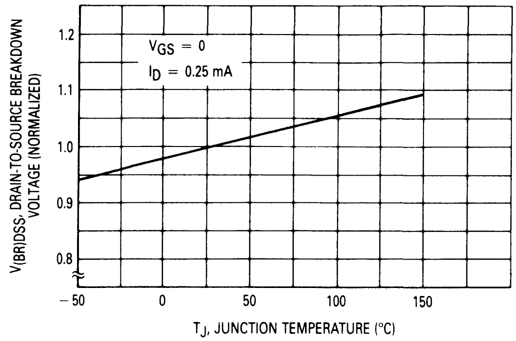


Figure 4. Breakdown Voltage Variation With Temperature

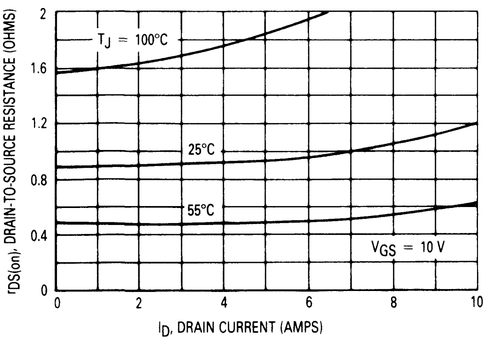


Figure 5. On-Resistance versus Drain Current

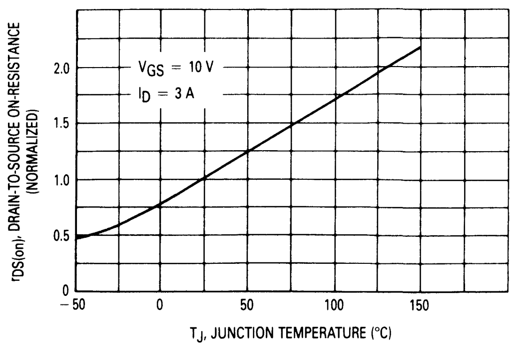


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

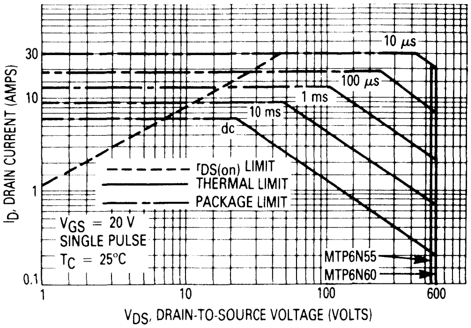


Figure 7. Maximum Rated Forward Biased Safe Operating Area

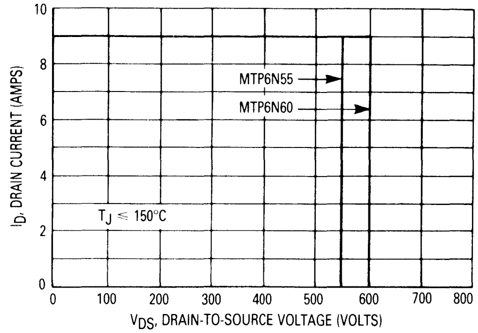


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

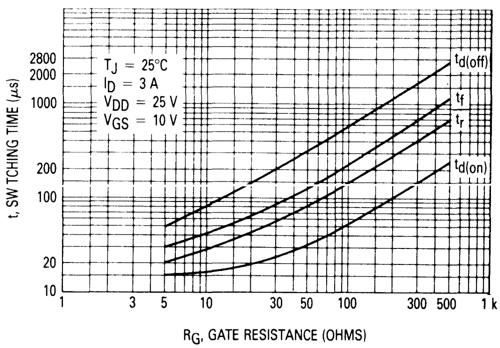


Figure 9. Resistive Switching Time Variation versus Gate Resistance

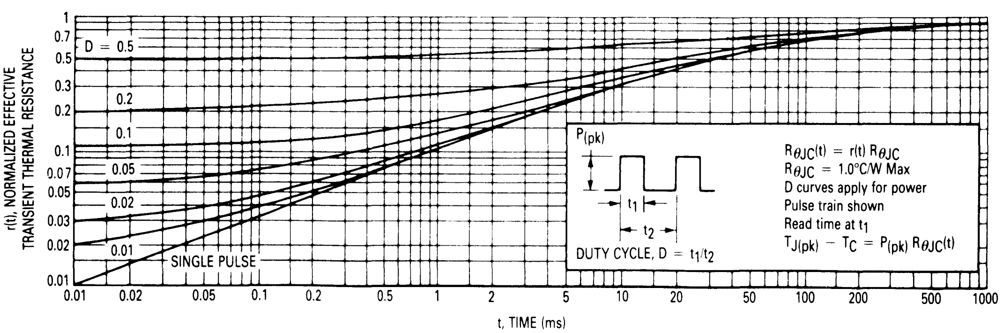


Figure 10. Thermal Response

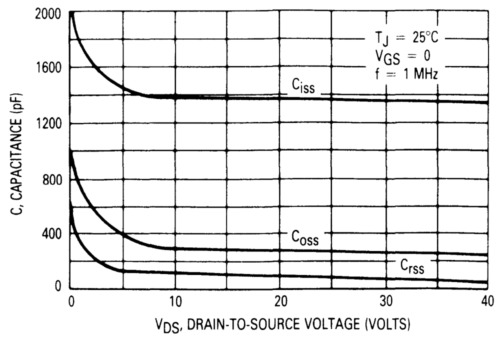


Figure 11. Capacitance Variation

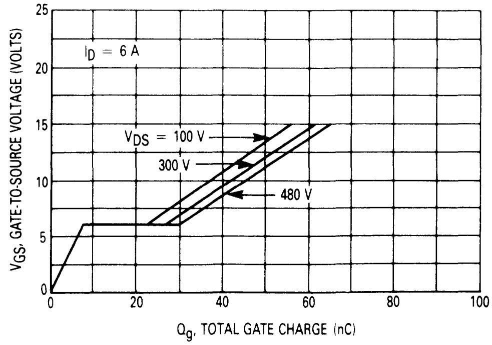


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

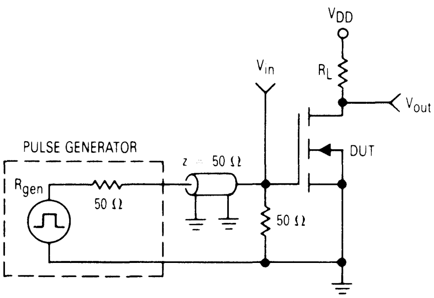


Figure 13. Switching Test Circuit

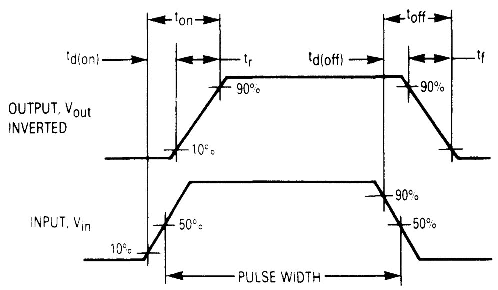
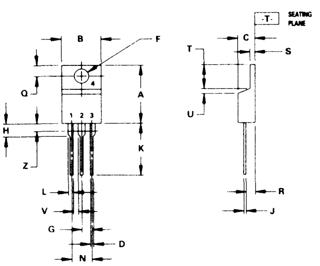


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP7N20

Designer's Data Sheet

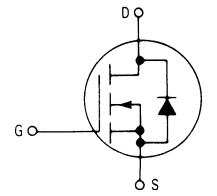
Power Field Effect Transistor

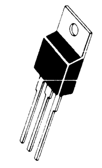
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
7 AMPERES
$r_{DS(on)}$ = 0.7 OHM
200 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20	Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40	Vpk
Drain Current			Adc
Continuous	I_D	7	
Pulsed	I_{DM}	18	
Total Power Dissipation @ T_C = 25°C	P_D	75	Watts
Derate above 25°C		0.6	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$r_{DS(on)}$	—	0.7	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7 Adc)		$V_{DS(on)}$	—	5.9	Vdc
(I_D = 3.5 Adc, T_J = 100°C)			—	5	
Forward Transconductance (V_{DS} = 15 V, I_D = 3.5 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	700	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	9 (Typ)	20	nC
Gate-Source Charge		Q_{gs}	4 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

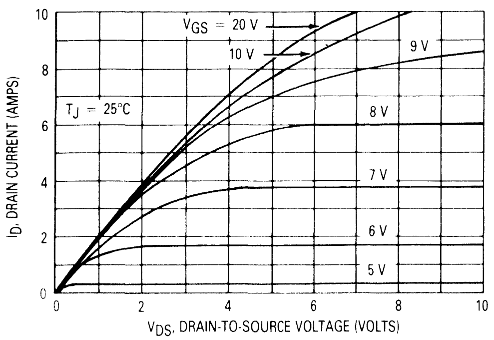


Figure 1. On-Region Characteristics

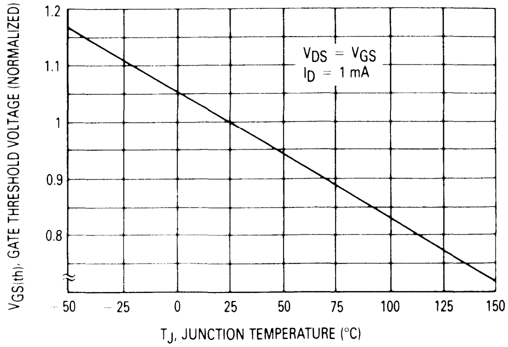


Figure 2. Gate-Threshold Voltage Variation With Temperature

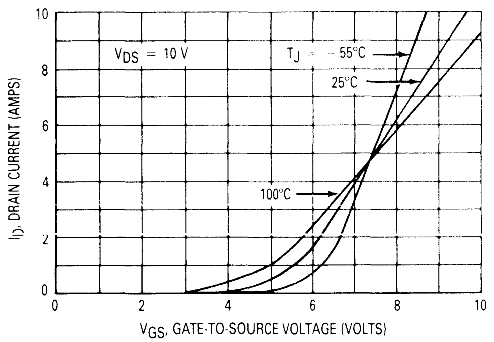


Figure 3. Transfer Characteristics

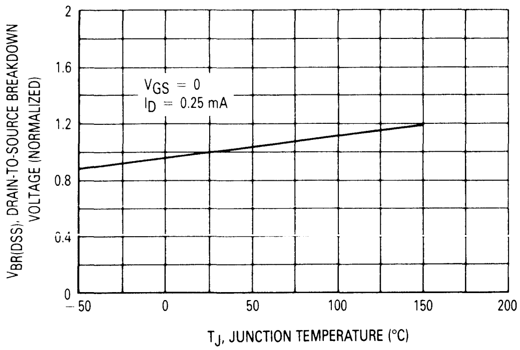


Figure 4. Breakdown Voltage Variation With Temperature

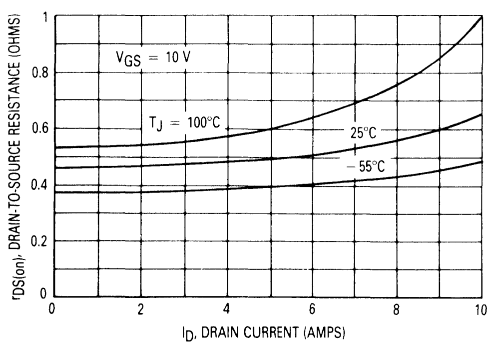


Figure 5. On-Resistance versus Drain Current

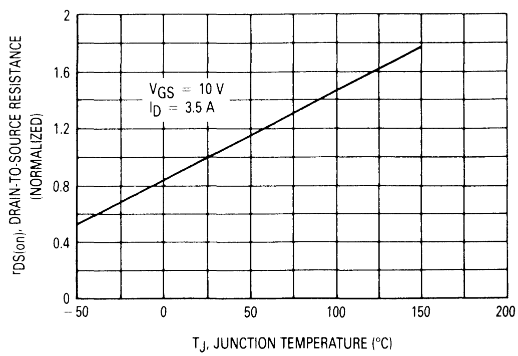


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

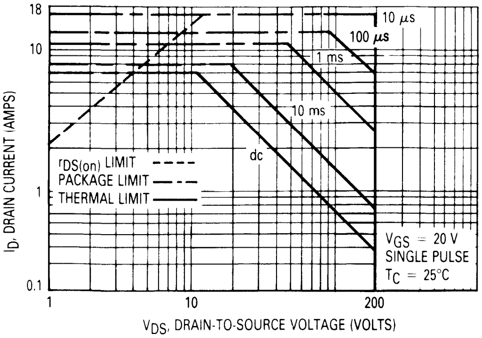


Figure 7. Maximum Rated Forward Biased Safe Operating Area

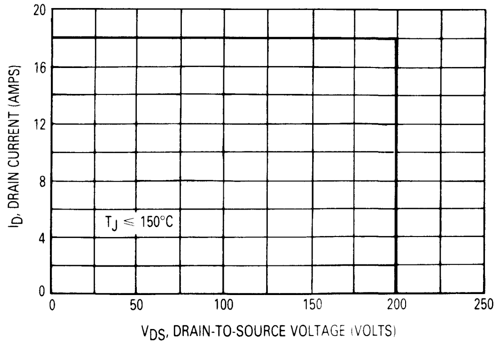


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

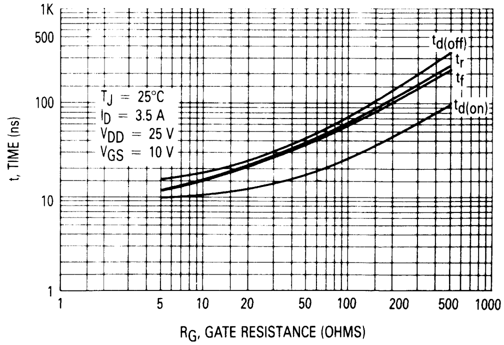


Figure 9. Resistive Switching Time Variation versus Gate Resistance

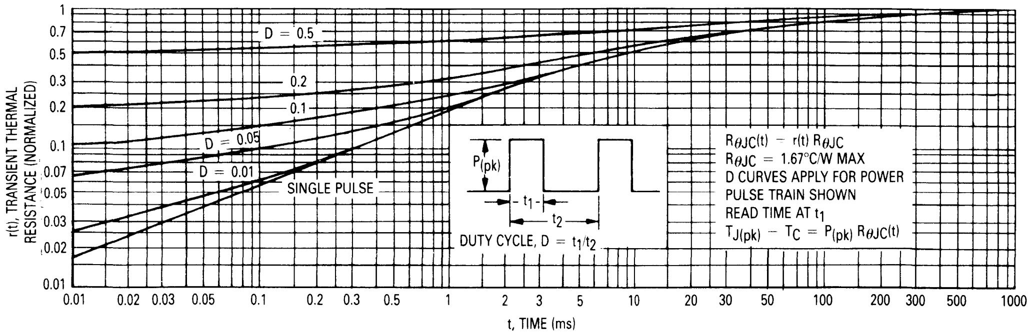


Figure 10. Thermal Response

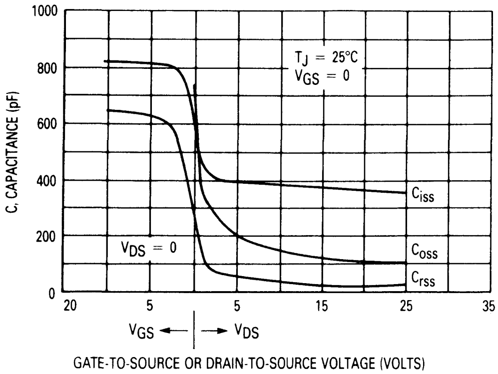


Figure 11. Capacitance Variation

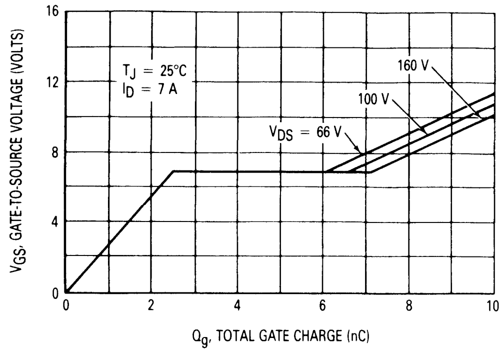


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

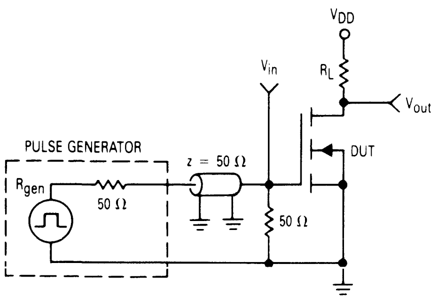


Figure 13. Switching Test Circuit

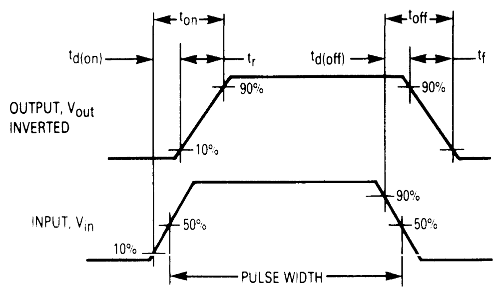
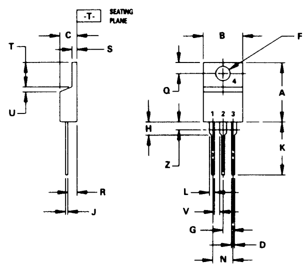


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP7P05
MTP7P06

Designer's Data Sheet

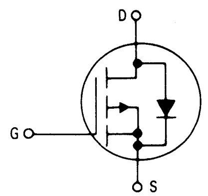
Power Field Effect Transistor

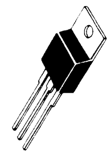
P-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
7 AMPERES
$r_{DS(on)}$ = 0.6 OHM
50 and 60 VOLTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 7P05	MTP 7P06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 7 21		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.67	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP7P05		$V_{(BR)DSS}$	50	—	Vdc
MTP7P06			60	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$r_{DS(on)}$	—	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 7 Adc)		$V_{DS(on)}$	—	4.2	Vdc
(I_D = 3.5 Adc, T_J = 100°C)			—	4	
Forward Transconductance (V_{DS} = 15 V, I_D = 3.5 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	700	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	80	
Fall Time		t_f		70	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	12 (Typ)	16	nC
Gate-Source Charge		Q_{gs}	7 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.8 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

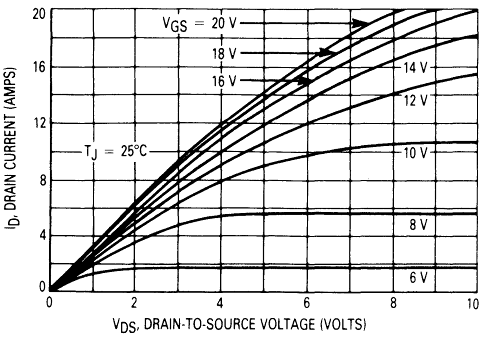


Figure 1. On-Region Characteristics

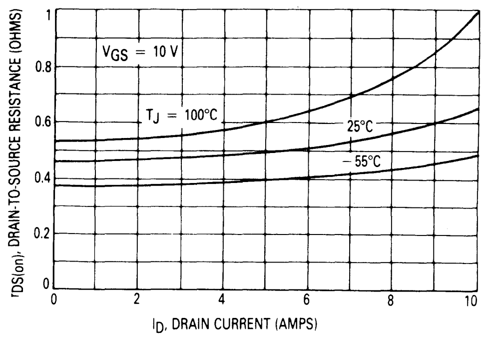


Figure 2. Gate-Threshold Voltage Variation With Temperature

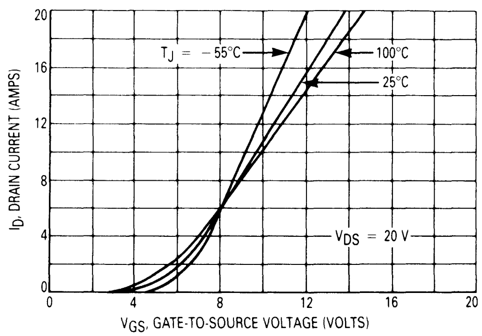


Figure 3. Transfer Characteristics

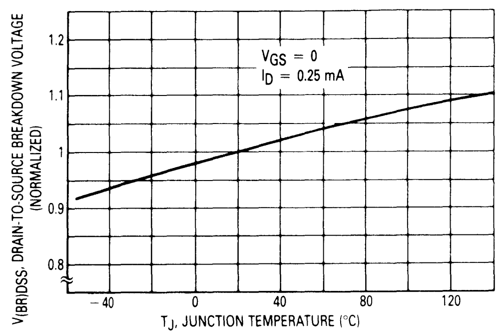


Figure 4. Breakdown Voltage Variation With Temperature

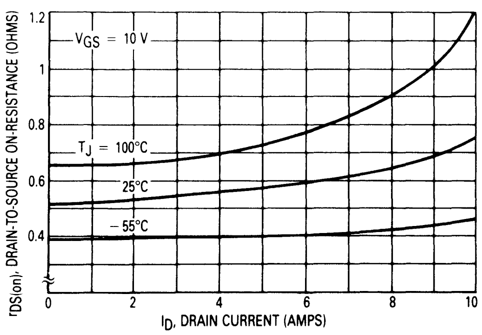


Figure 5. On-Resistance versus Drain Current

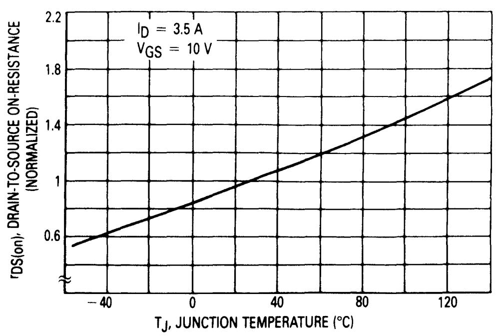


Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

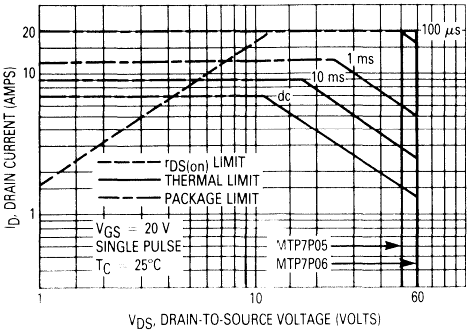


Figure 7. Maximum Rated Forward Biased Safe Operating Area

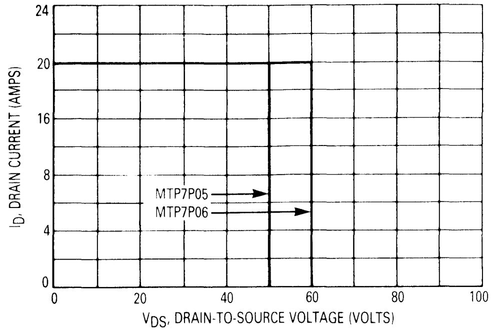


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

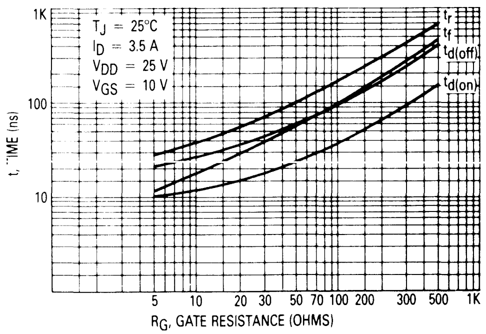


Figure 9. Resistive Switching Time Variation versus Gate Resistance

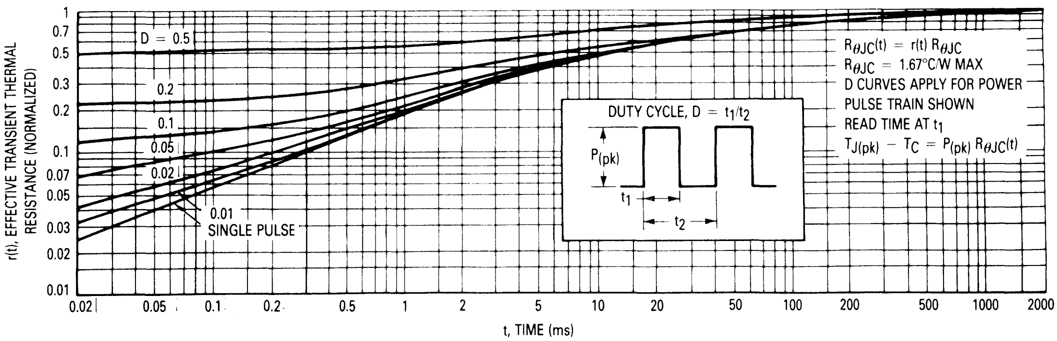


Figure 10. Thermal Response

TYPICAL CHARACTERISTICS

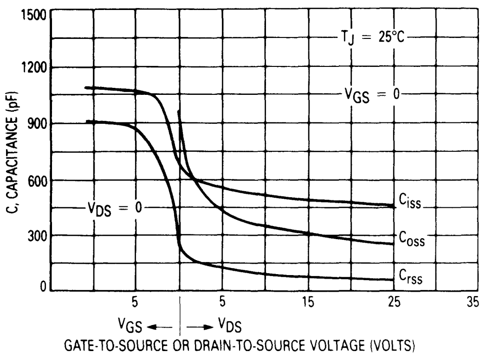


Figure 12. Capacitance Variation

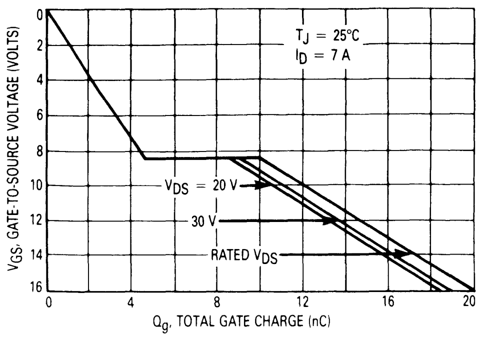


Figure 13. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

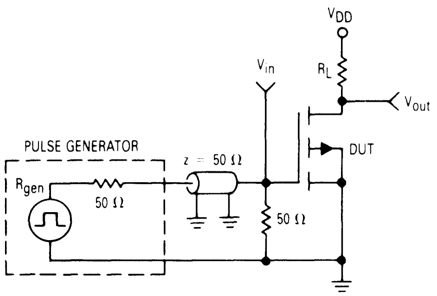


Figure 14. Switching Test Circuit

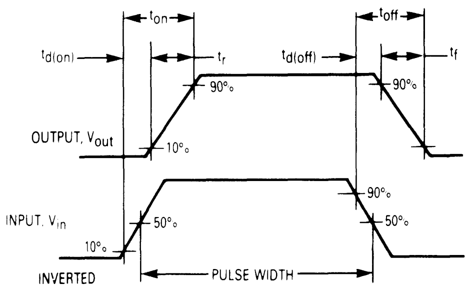
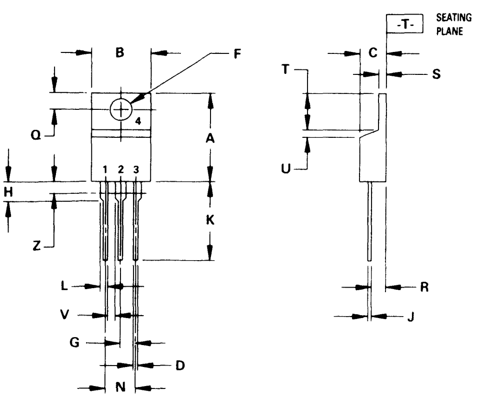


Figure 15. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB

MTP8N08
MTP8N10

Designer's Data Sheet

Power Field Effect Transistor

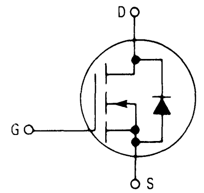
N-Channel Enhancement-Mode Silicon Gate TMOS

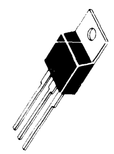
TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.5 OHM
80 and 100 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

3





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM or MTP 8N08	MTM or MTP 8N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 8 20		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP8N08 MTP8N10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.5	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.8 4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)		g_{FS}	1.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	13 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

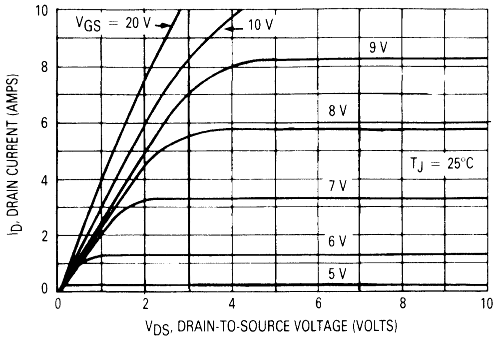


Figure 1. On-Region Characteristics

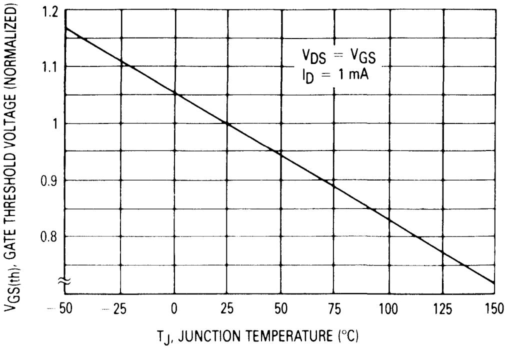


Figure 2. Gate-Threshold Voltage Variation With Temperature

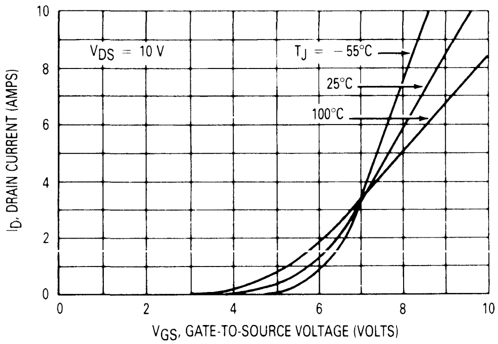


Figure 3. Transfer Characteristics

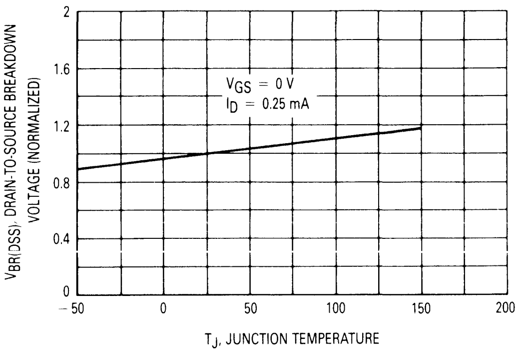


Figure 4. Breakdown Voltage Variation With Temperature

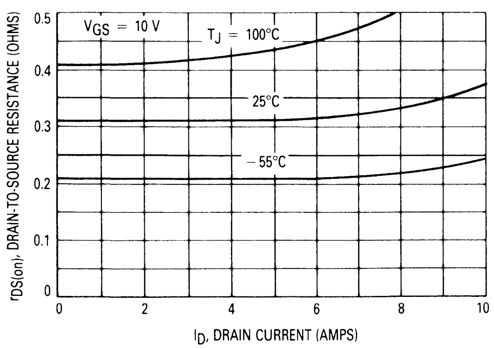


Figure 5. On-Resistance versus Drain Current

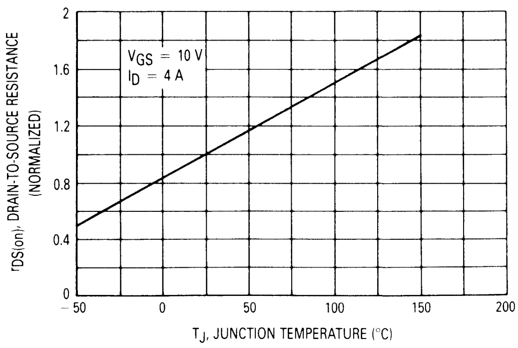


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

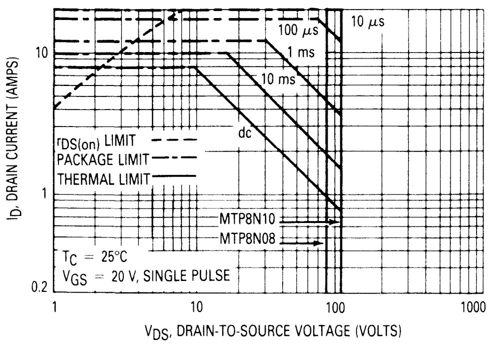


Figure 7. Maximum Rated Forward Biased Safe Operating Area

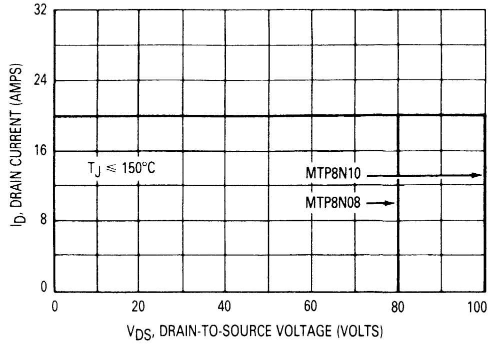


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

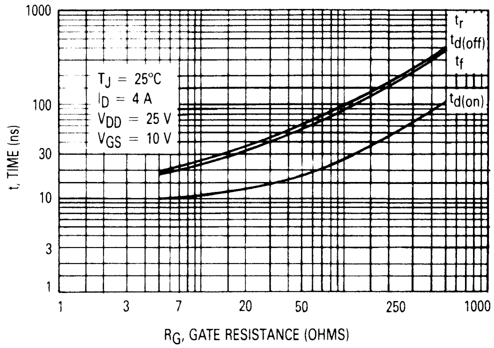


Figure 9. Resistive Switching Time Variation versus Gate Resistance

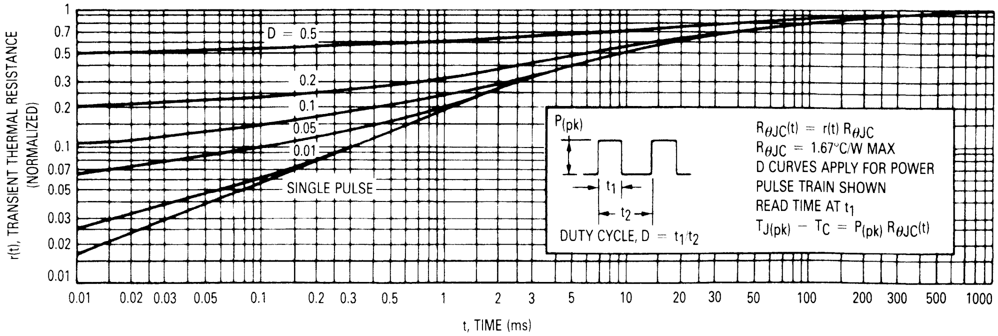


Figure 10. Thermal Response

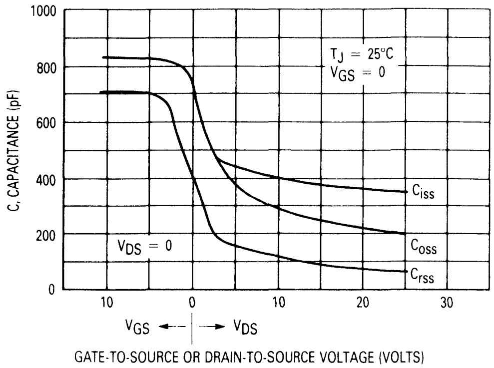


Figure 11. Capacitance Variation

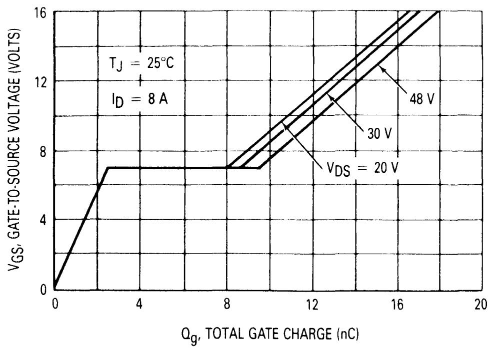


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

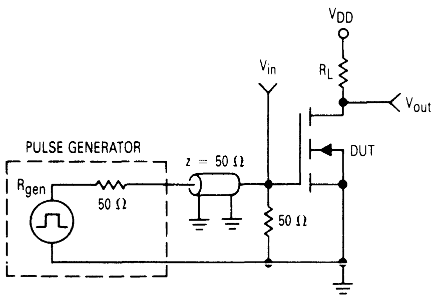


Figure 13. Switching Test Circuit

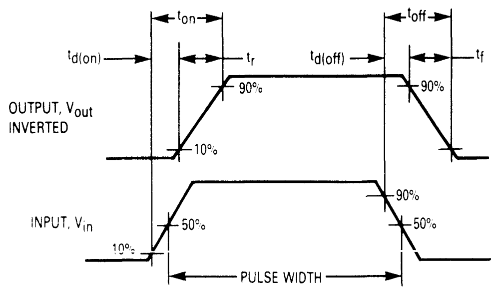
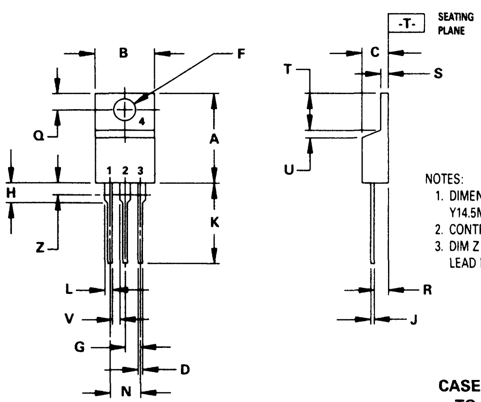


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MTP8N10E

Designer's Data Sheet

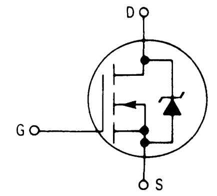
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

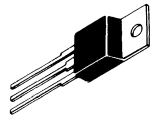
TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.5 OHM
100 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS™





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage	$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)		2	4.5	
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)	$r_{DS(on)}$	—	0.5	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 8 Adc)		—	4.8	
(I_D = 4 Adc, T_J = 100°C)		—	4	
Forward Transconductance (V_{DS} = 15 V, I_D = 4 A)	g_{FS}	4	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15	W_{DSR}			mJ
(I_D = 20 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive)		—	80	
(I_D = 8 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		—	170	
(I_D = 3.2 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		—	70	
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	600	pF
Output Capacitance	C_{oss}	—	400	
Reverse Transfer Capacitance	C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 4 A, R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	50	ns
Rise Time	t_r	—	80	
Turn-Off Delay Time	$t_{d(off)}$	—	100	
Fall Time	t_f	—	80	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	15 (Typ)	30	nC
Gate-Source Charge	Q_{gs}	7.5 (Typ)	—	
Gate-Drain Charge	Q_{gd}	7.5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = 4 A, V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.7	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	70 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE				
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

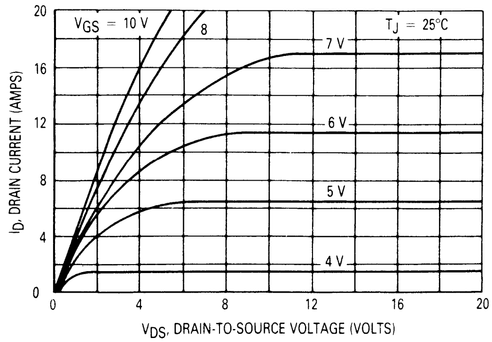


Figure 1. On-Region Characteristics

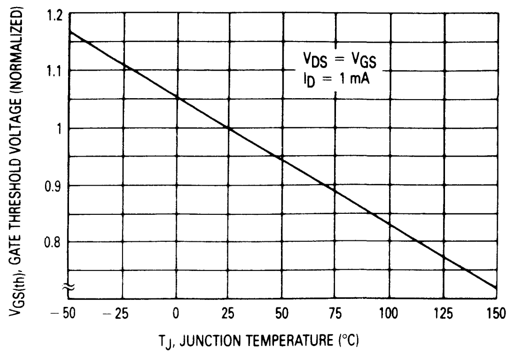


Figure 2. Gate-Threshold Voltage Variation With Temperature

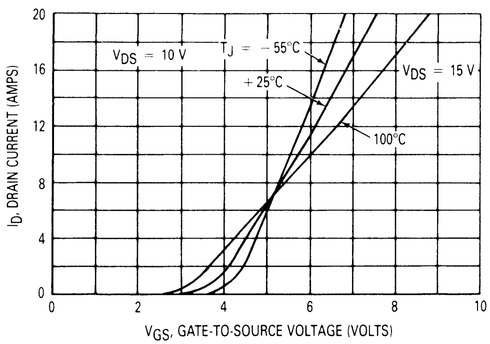


Figure 3. Transfer Characteristics

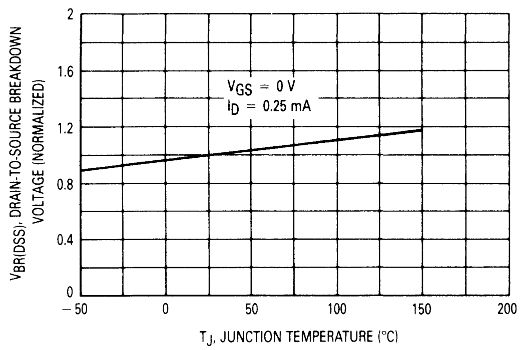


Figure 4. Breakdown Voltage Variation With Temperature

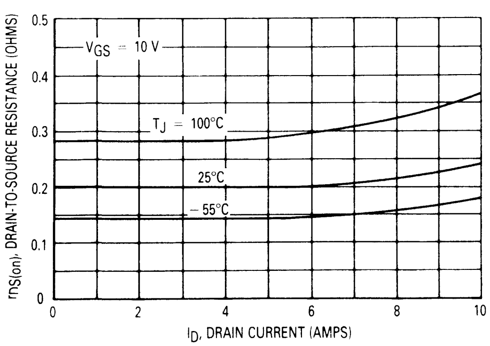


Figure 5. On-Resistance versus Drain Current

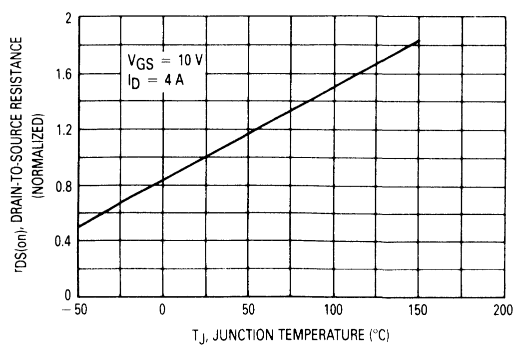


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

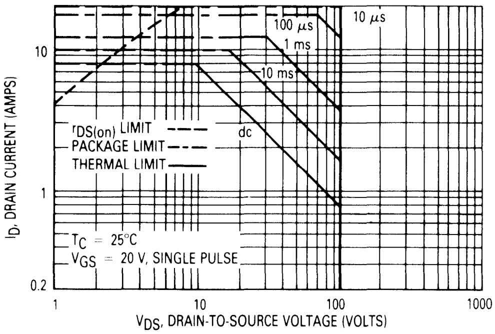


Figure 7. Maximum Rated Forward Biased Safe Operating Area

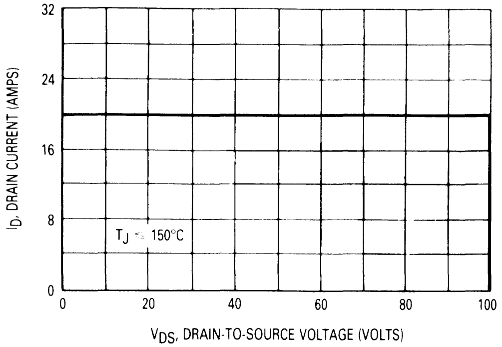


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

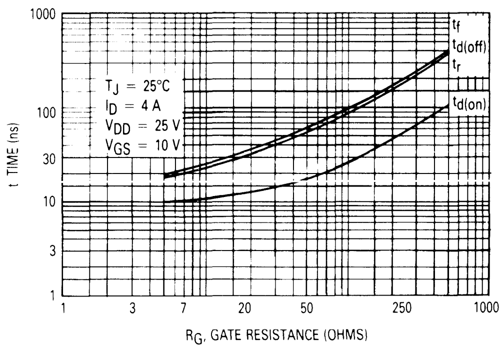


Figure 9. Resistive Switching Time Variation versus Gate Resistance

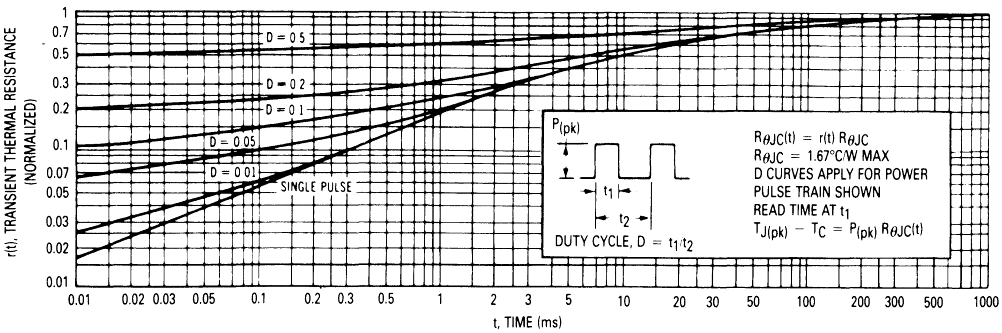


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

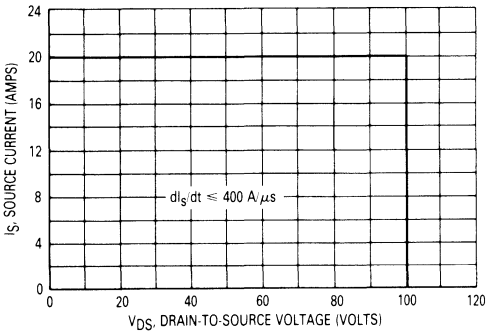


Figure 12. Commutating Safe Operating Area (CSOA)

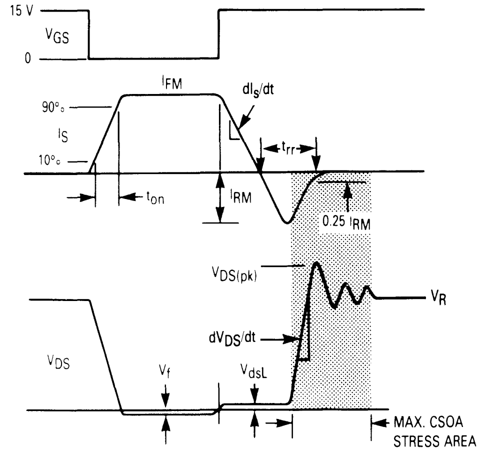


Figure 11. Commutating Waveforms

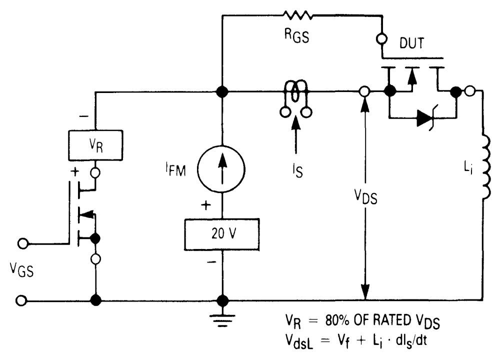


Figure 13. Commutating Safe Operating Area Test Circuit

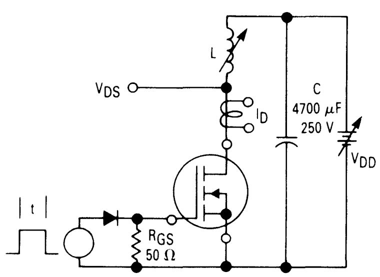
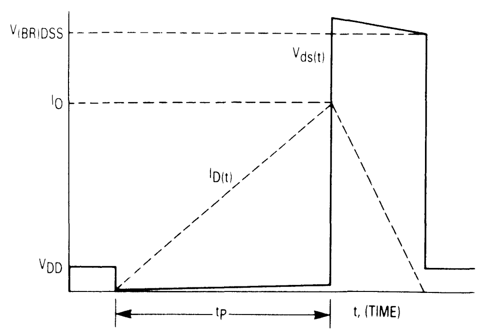


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right) \left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

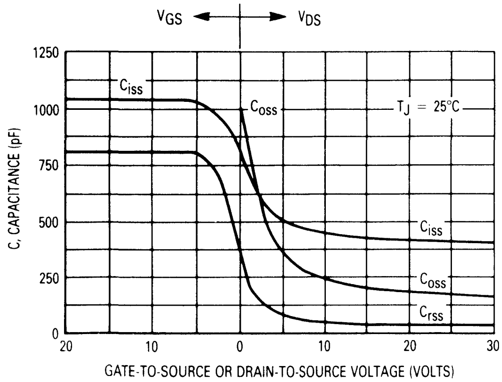


Figure 16. Capacitance Variation

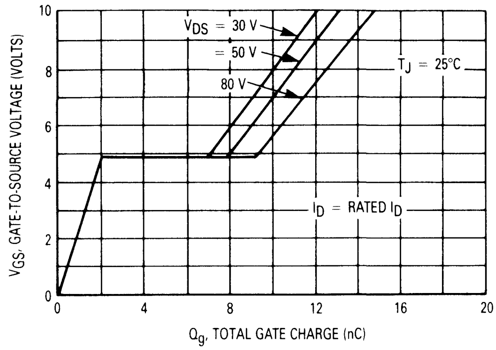
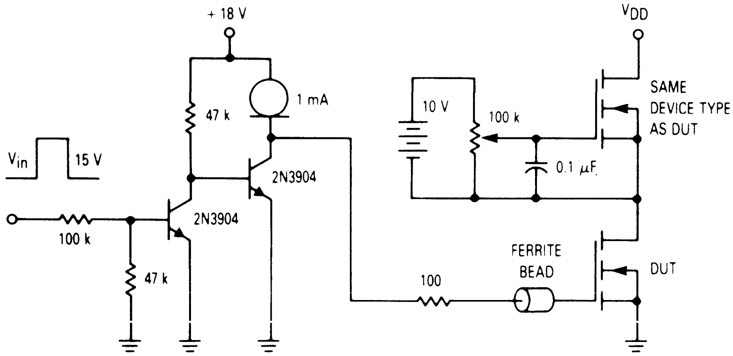


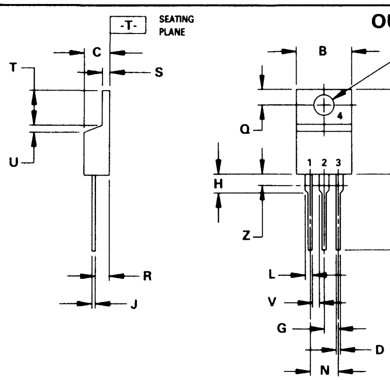
Figure 17. Gate Charge versus Gate-To-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



CASE 221A-04
TO-220AB

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

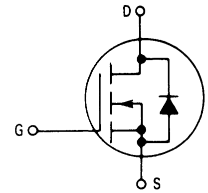
MTP8N15L

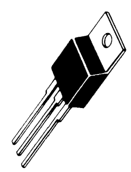
Designer's Data Sheet

Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate L^2 TMOS

TMOS POWER FET
LOGIC LEVEL
10 AMPERES
$r_{DS(on)}$ = 0.45 OHM
150 VOLTS





CASE 221A-04
TO-220AB

This Logic Level TMOS (L^2TMOS) Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers where gate drive voltage is limited.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t_p < 50 μs)	V_{GS} V_{GSM}	±15 ±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	8 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 150 V, V_{GS} = 0) (V_{DS} = 150 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	1 0.75	2 1.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.45	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4 3	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 4 A)		g_{FS}	4.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	560 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		1780 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	20 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		1000 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{oss}	110 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 8 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	14 (Typ)	—	ns
Rise Time		t_r	50 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	60 (Typ)	—	
Fall Time		t_f	46 (Typ)	—	
Total Gate Charge	(V_{DS} = 120 V, I_D = 8 A, V_{GS} = 5 Vdc) See Figures 9 and 10	Q_g	10.5 (Typ)	18	nC
Gate-Source Charge		Q_{gs}	1.8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = 8 A, V_{GS} = 0)	V_{SD}	1.02 (Typ)	1.25	Vdc
Forward Turn-On Time	(I_S = 20 A, dI_S/dt = 100 A/µs, V_R = 70 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	125 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

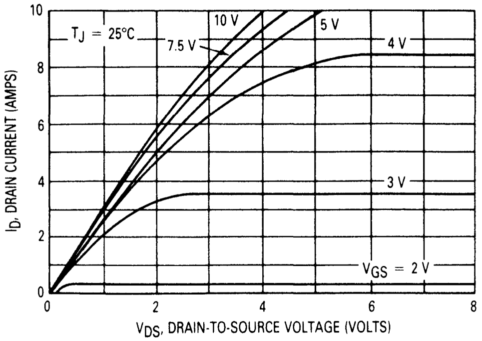


Figure 2. Gate-Threshold Voltage Variation With Temperature

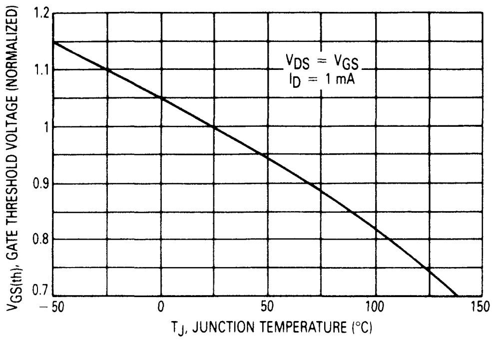


Figure 3. Transfer Characteristics

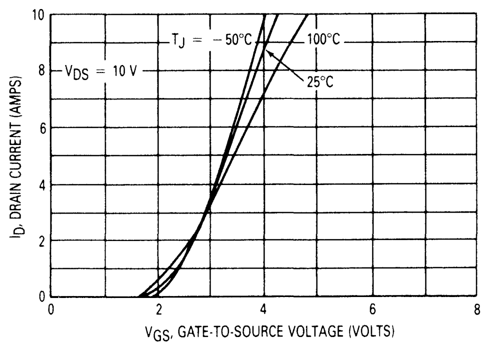


Figure 4. Drain-to-Source Resistance Variation With Drain Current

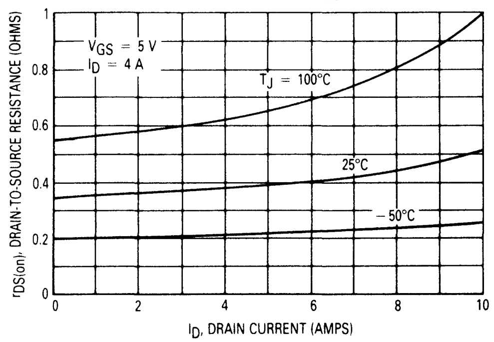


Figure 5. Drain-to-Source Resistance Variation With Gate-to-Source Voltage

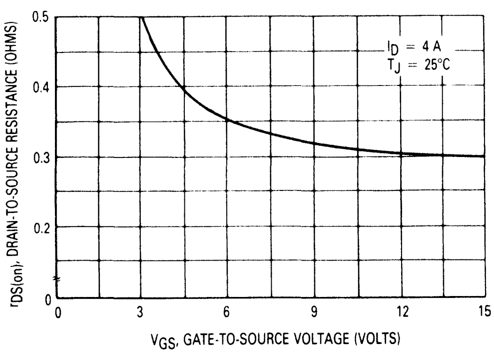


Figure 6. On-Resistance Variation With Temperature

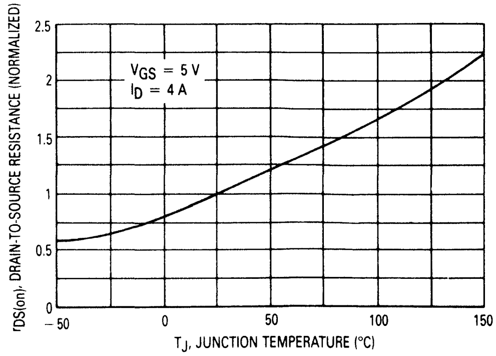


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Figure 7. Drain-to-Source Breakdown Voltage Variation With Temperature

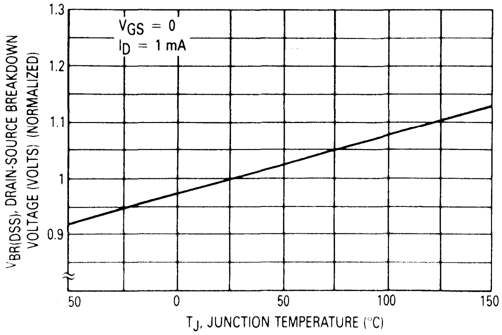


Figure 8. Capacitance Variation With Voltage

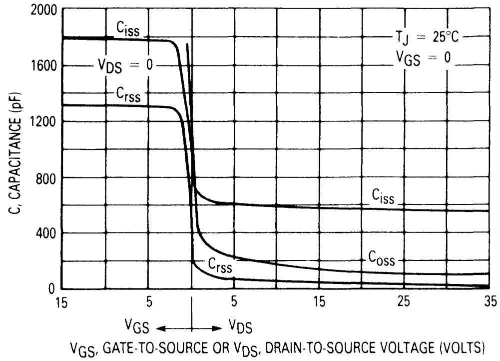
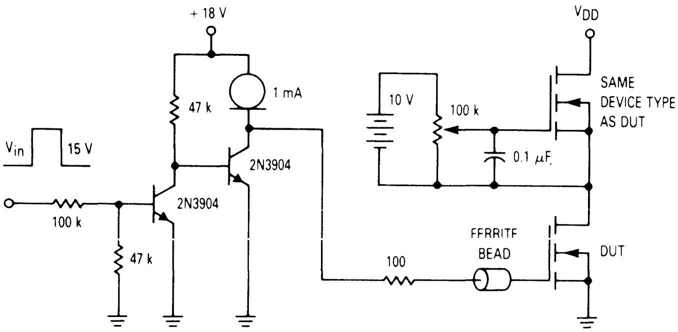
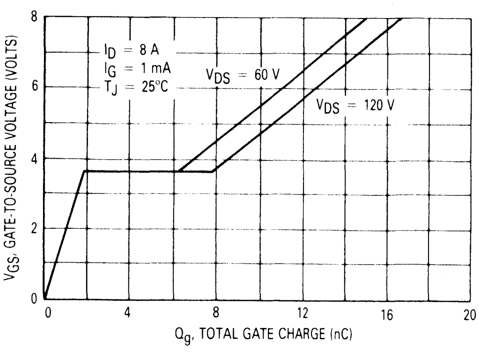


Figure 9. Gate Charge Test Circuit

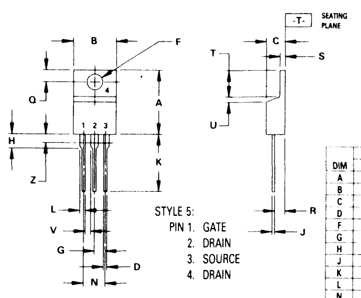


V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge versus Gate-to-Source Voltage



OUTLINE DIMENSIONS

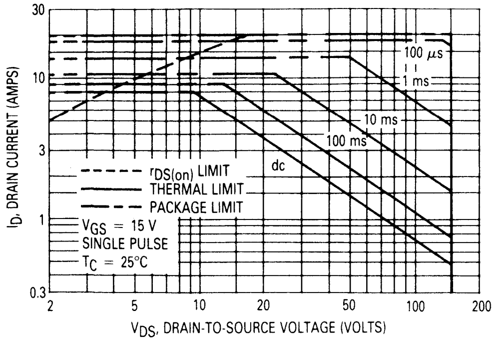


CASE 221A-04
TO-220AB

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

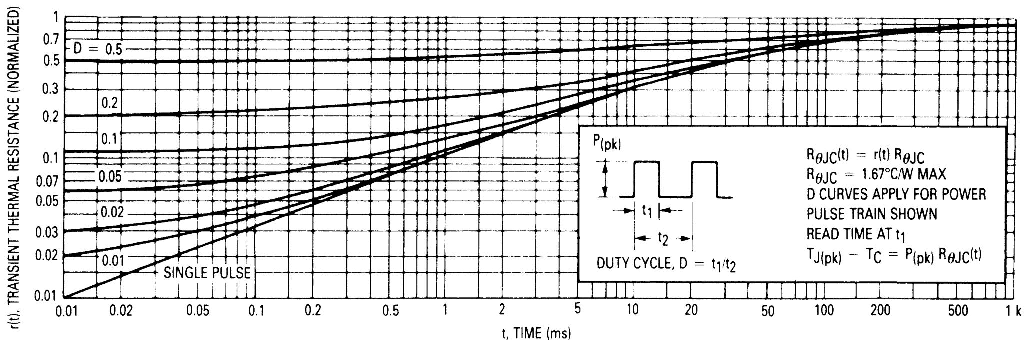
Figure 11. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 12. Thermal Response



RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

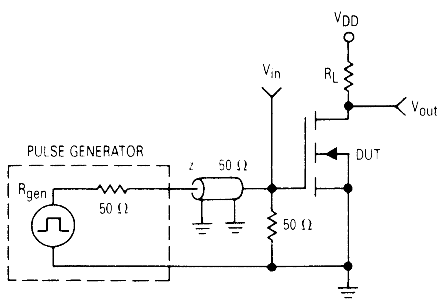
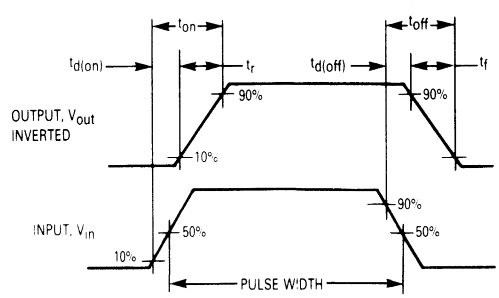


Figure 14. Switching Waveforms



MTP8N45
MTP8N50

Designer's Data Sheet

Power Field Effect Transistor

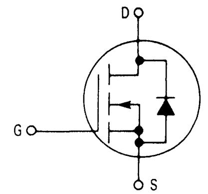
N-Channel Enhancement-Mode
Silicon Gate TMOS

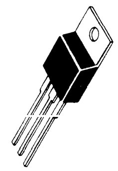
TMOS POWER FETs
8 AMPERES
$r_{DS(on)}$ = 0.8 OHM
450 and 500 VOLTS

These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

3





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 8N45	MTP 8N50	Unit
Drain-Source Voltage	V_{DSS}	450	500	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	450	500	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current				Adc
Continuous	I_D	8		
Pulsed	I_{DM}	32		
Total Power Dissipation @ T_C = 25°C	P_D	125		Watts
Derate above 25°C		1		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP8N45 MTP8N50	$V_{(BR)DSS}$	450 500	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4 Adc)		$r_{DS(on)}$	—	0.8	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 8 Adc) (I_D = 4 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	7.2 6.4	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 4 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.1 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

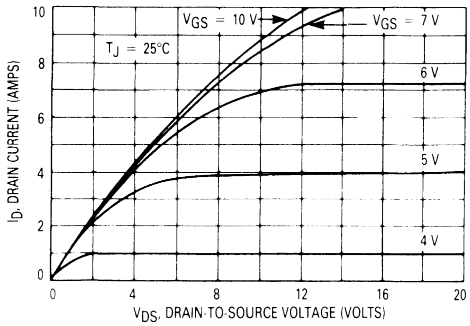


Figure 1. On-Region Characteristics

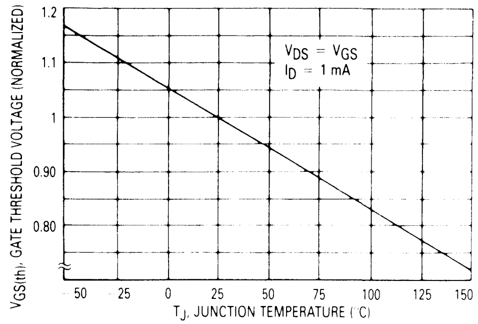


Figure 2. Gate-Threshold Voltage Variation With Temperature

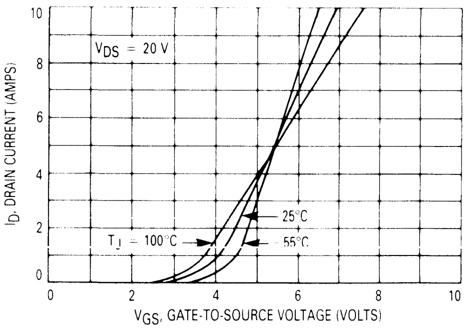


Figure 3. Transfer Characteristics

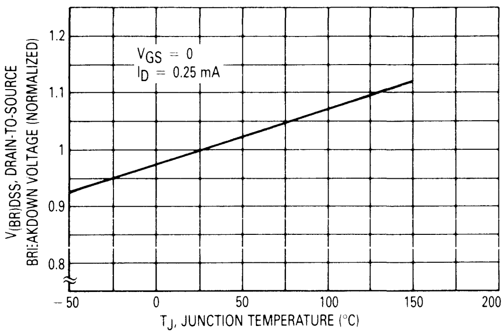


Figure 4. Breakdown Voltage Variation With Temperature

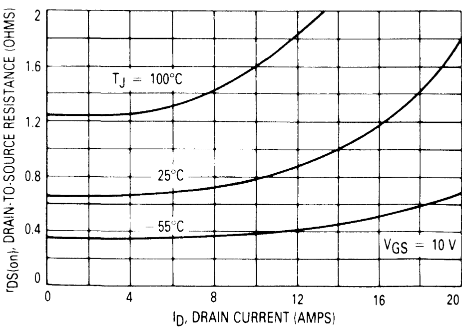


Figure 5. On-Resistance versus Drain Current

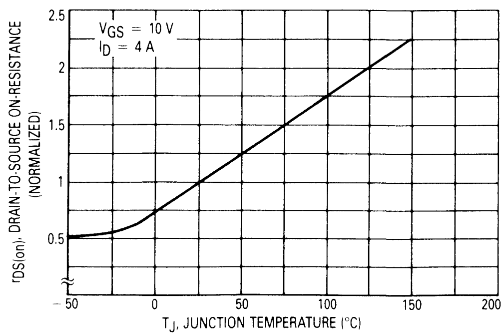


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

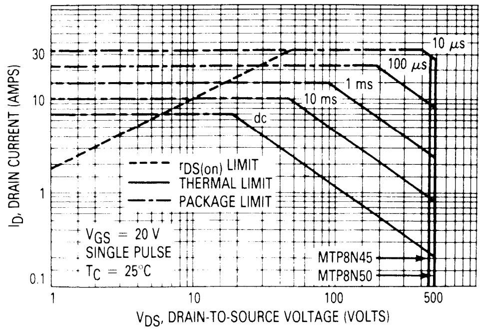


Figure 7. Maximum Rated Forward Biased Safe Operating Area

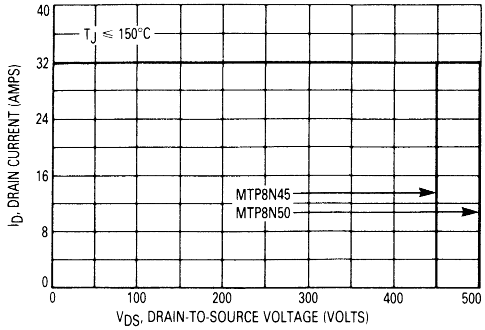


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

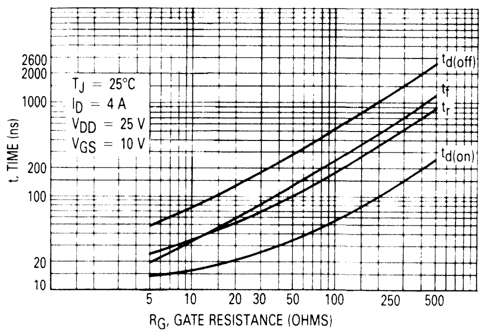


Figure 9. Resistive Switching Time Variation versus Gate Resistance

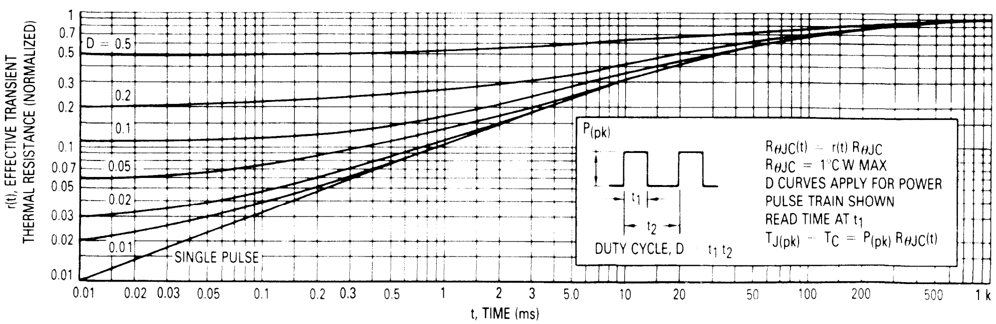


Figure 10. Thermal Response

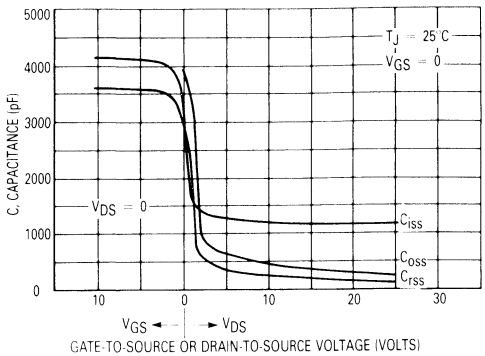


Figure 11. Capacitance Variation

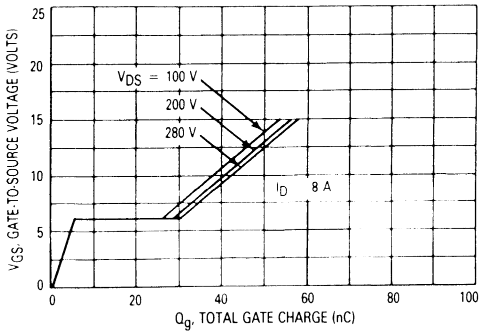


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESIDENTIAL SWITCHING

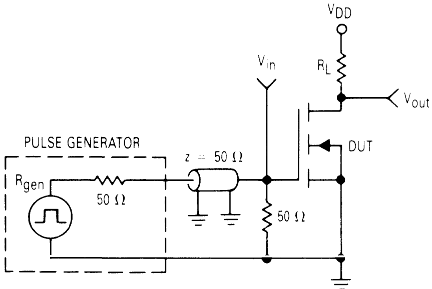


Figure 13. Switching Test Circuit

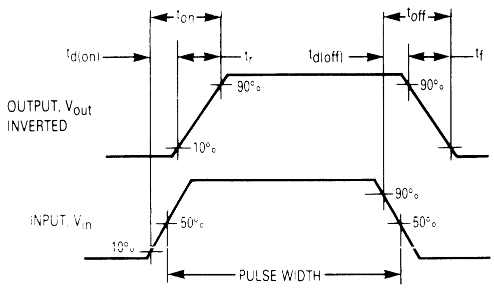
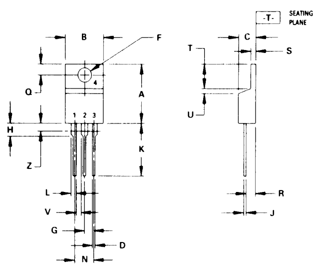


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP10N05
MTP10N06

Designer's Data Sheet

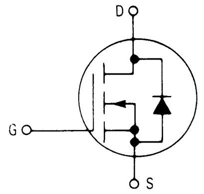
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FETs
10 AMPERES
$r_{DS(on)}$ = 0.28 OHM
50 and 60 VOLTS



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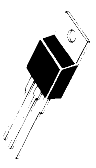
MAXIMUM RATINGS

Rating	Symbol	MTP 10N05	MTP 10N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current				Adc
Continuous	I_D	10		
Pulsed	I_{DM}	28		
Total Power Dissipation @ T_C = 25°C	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C



CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP10N05	$V_{(BR)DSS}$	50	—	Vdc
	MTP10N06		60	—	
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.28	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc)		$V_{DS(on)}$	—	3.4	Vdc
(I_D = 5 Adc, T_J = 100°C)			—	2.8	
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)		g_{FS}	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	120	
Turn-Off Delay Time		$t_{d(off)}$	—	50	
Fall Time		t_f	—	60	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	13 (Typ)	26	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.7 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

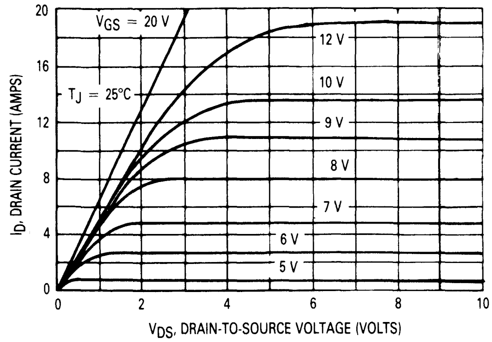


Figure 1. On-Region Characteristics

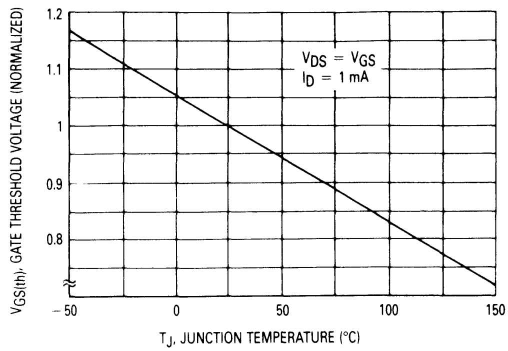


Figure 2. Gate-Threshold Voltage Variation With Temperature

3

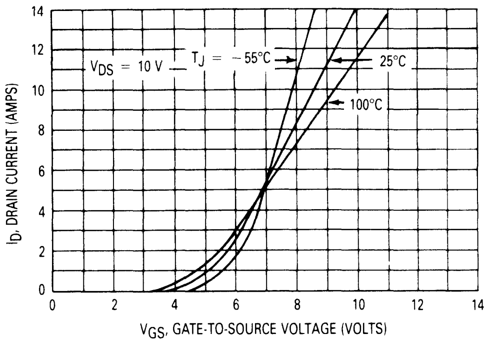


Figure 3. Transfer Characteristics

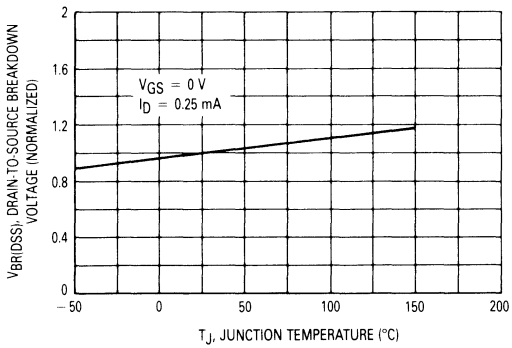


Figure 4. Breakdown Voltage Variation With Temperature

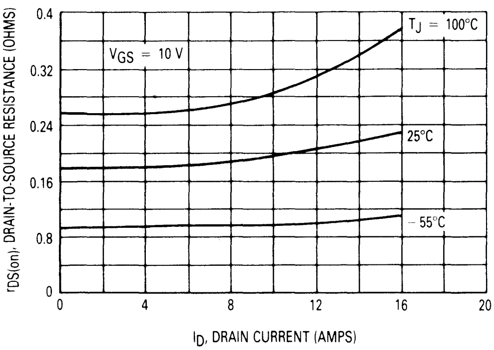


Figure 5. On-Resistance versus Drain Current

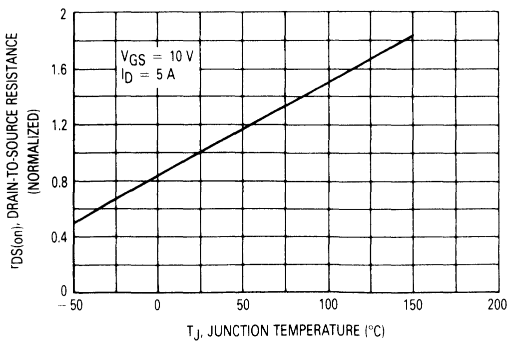


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

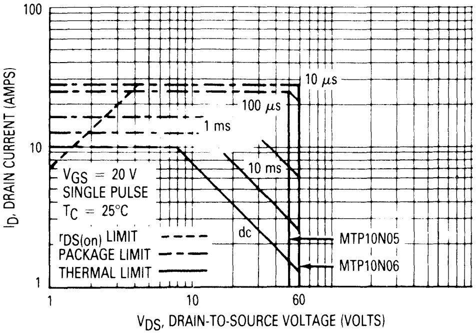


Figure 7. Maximum Rated Forward Biased Safe Operating Area

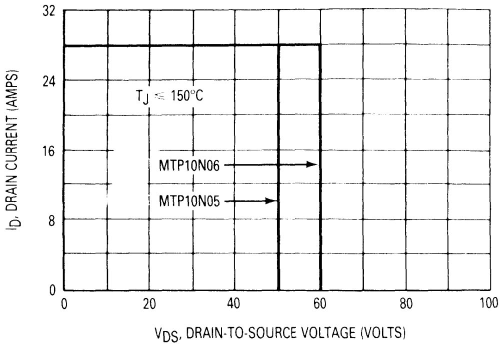


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

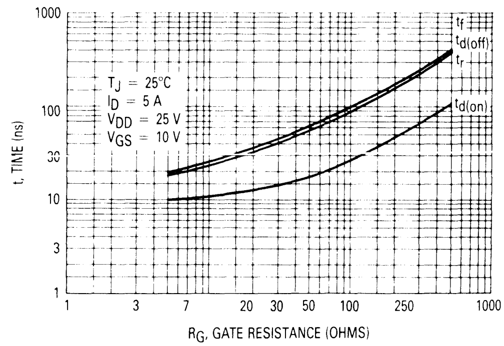


Figure 9. Resistive Switching Time Variation versus Gate Resistance

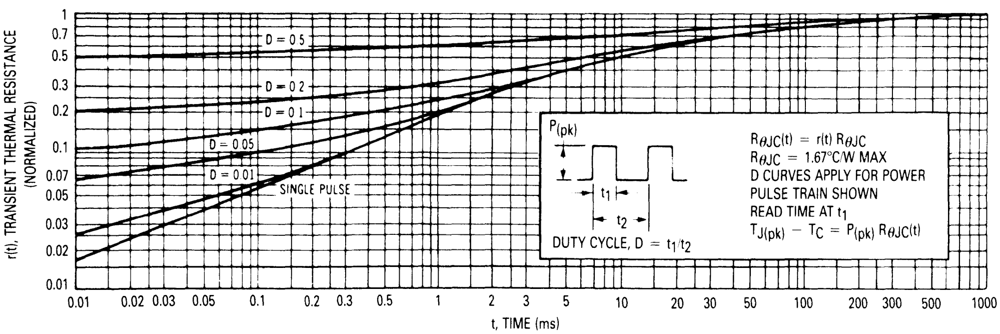


Figure 10. Thermal Response

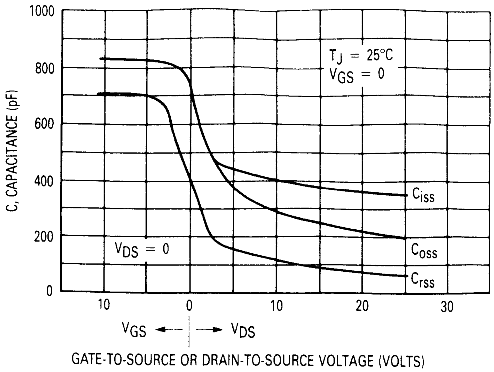


Figure 11. Capacitance Variation

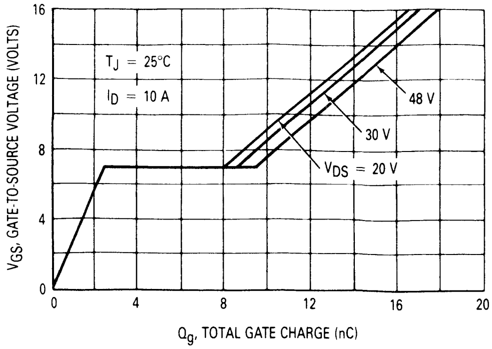


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

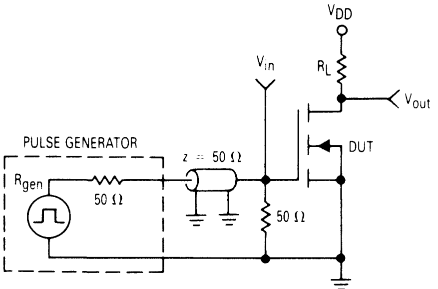


Figure 13. Switching Test Circuit

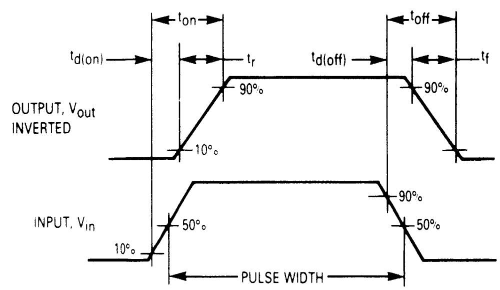
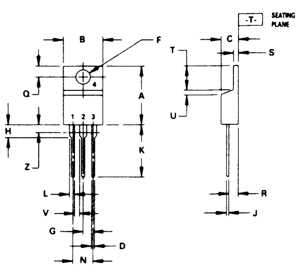


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5.
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTP10N08
MTP10N10

Designer's Data Sheet

Power Field Effect Transistor

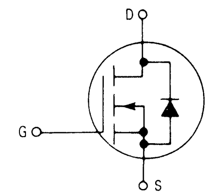
N-Channel Enhancement-Mode Silicon Gate TMOS

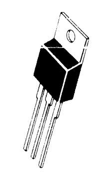
TMOS POWER FETs
10 AMPERES
$r_{DS(on)} = 0.33$ OHM
80 and 100 VOLTS

3

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 10N08	MTP 10N10	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage ($R_{GS} = 1\ M\Omega$)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20		Vdc
— Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GSM}	±40		Vpk
Drain Current — Continuous	I_D	10		Adc
— Pulsed	I_{DM}	25		
Total Power Dissipation @ $T_C = 25°C$	P_D	75		Watts
Derate above 25°C		0.6		W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.67	
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP10N08 MTP10N10	$V_{(BR)DSS}$	80 100	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.33	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc) (I_D = 5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 4 3.3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)		g_{FS}	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	80	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	50	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	13 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.7 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	700 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

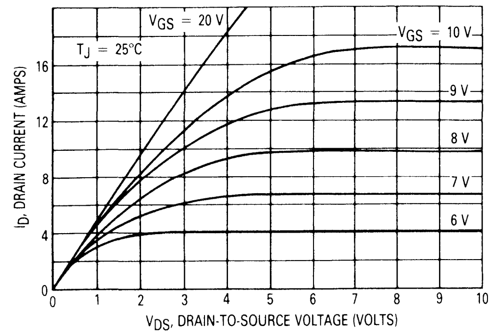


Figure 1. On-Region Characteristics

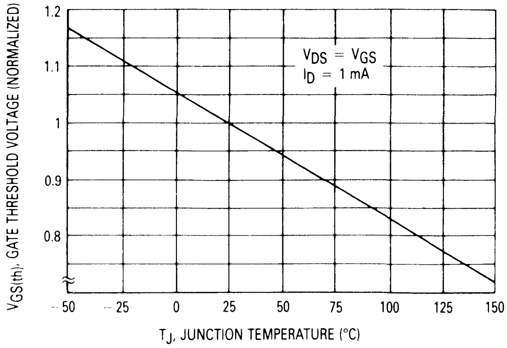


Figure 2. Gate-Threshold Voltage Variation With Temperature

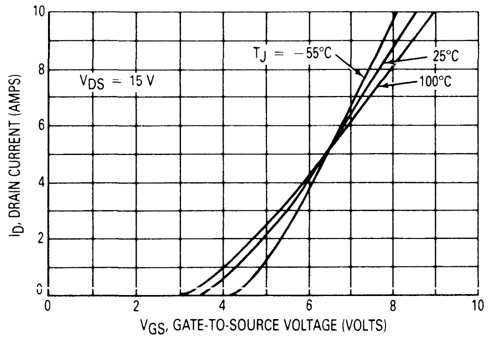


Figure 3. Transfer Characteristics

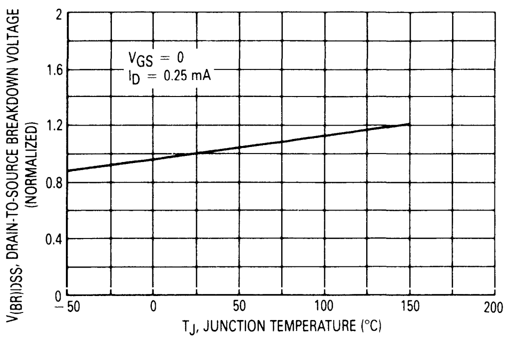


Figure 4. Breakdown Voltage Variation With Temperature

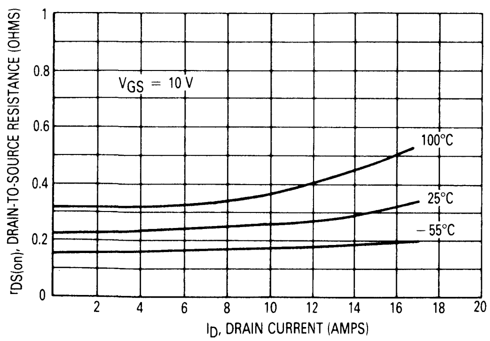


Figure 5. On-Resistance versus Drain Current

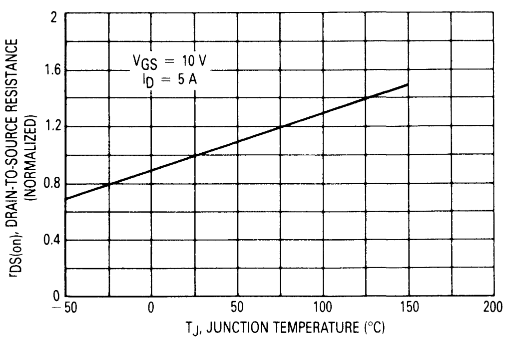


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

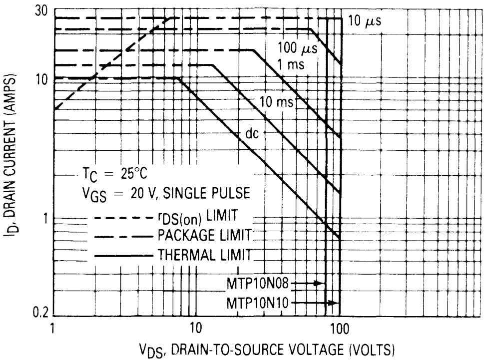


Figure 7. Maximum Rated Forward Biased Safe Operating Area

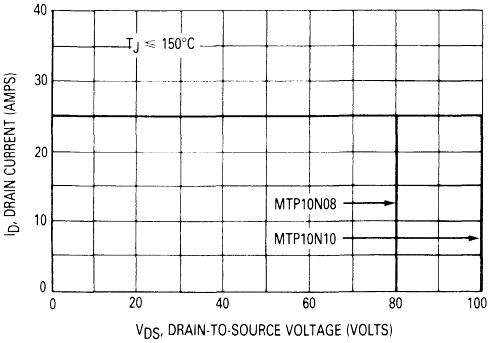


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

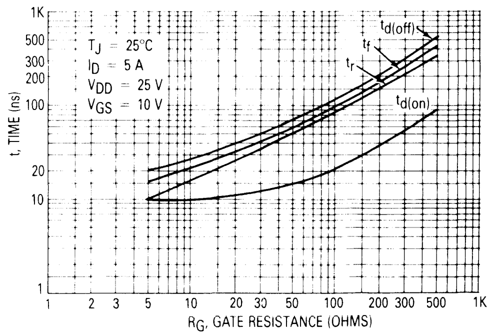


Figure 9. Resistive Switching Time versus Gate Resistance

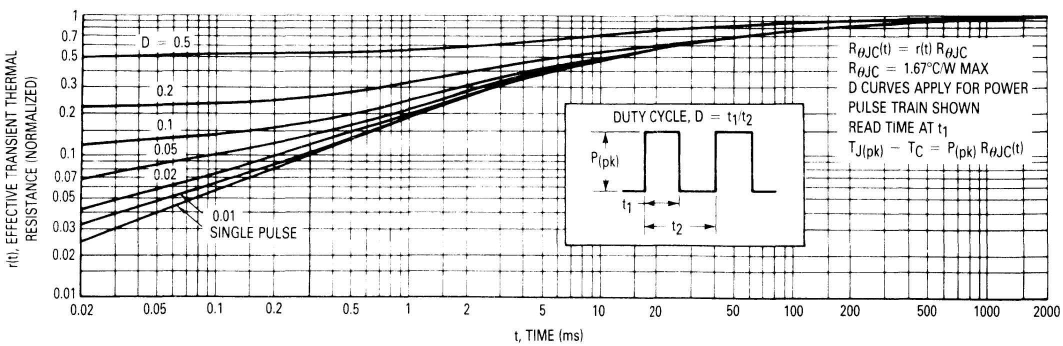


Figure 10. Thermal Response

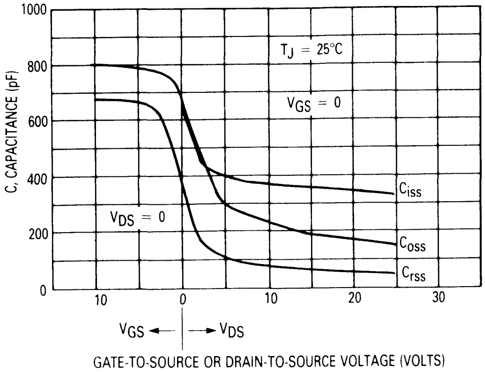


Figure 11. Capacitance Variation

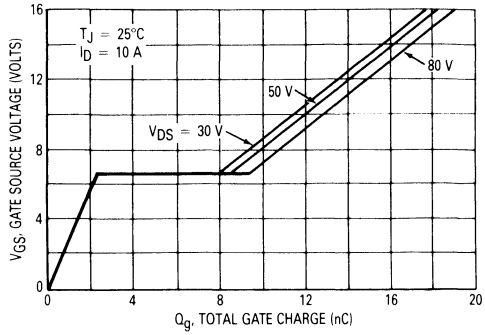


Figure 12. Gate Charge versus Gate-To-Source Voltage

3

RESISTIVE SWITCHING

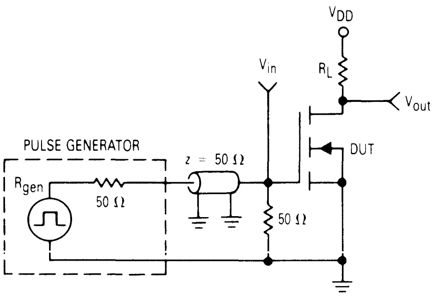


Figure 13. Switching Test Circuit

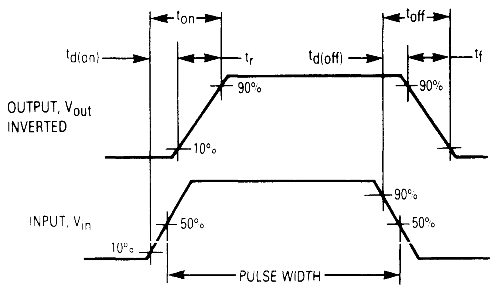
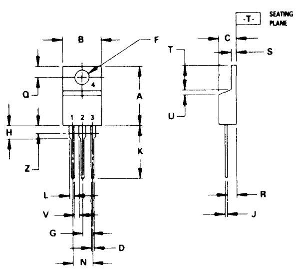


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTP10N10E

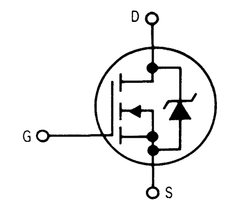
Designer's Data Sheet

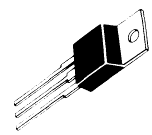
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER FETs
10 AMPERES
$r_{DS(on)}$ = 0.25 OHM
100 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits





CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 25	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage	$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)		2	4.5	
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)	$r_{DS(on)}$	—	0.25	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 10 Adc)		—	2.7	
(I_D = 5 Adc, T_J = 100°C)		—	2.4	
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)	g_{FS}	4	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15	W_{DSR}			mJ
(I_D = 25 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive)		—	60	
(I_D = 10 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		—	100	
(I_D = 4 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		—	40	
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	600	pF
Output Capacitance	C_{oss}	—	400	
Reverse Transfer Capacitance	C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, I_D = 5 A, R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	50	ns
Rise Time	t_r	—	80	
Turn-Off Delay Time	$t_{d(off)}$	—	100	
Fall Time	t_f	—	80	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	15 (Typ)	30	nC
Gate-Source Charge	Q_{gs}	8 (Typ)	—	
Gate-Drain Charge	Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.7	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	70 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE				
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

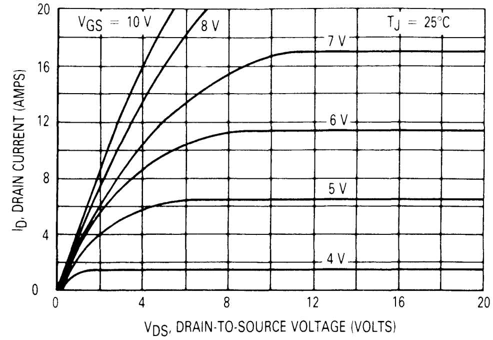


Figure 1. On-Region Characteristics

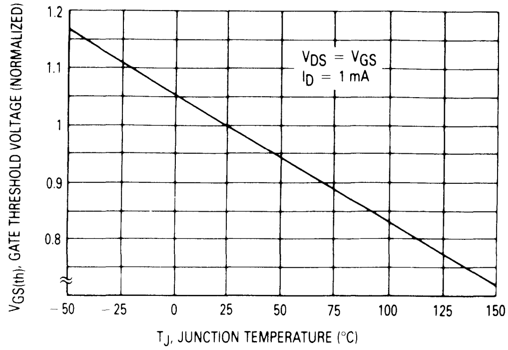


Figure 2. Gate-Threshold Voltage Variation With Temperature

3

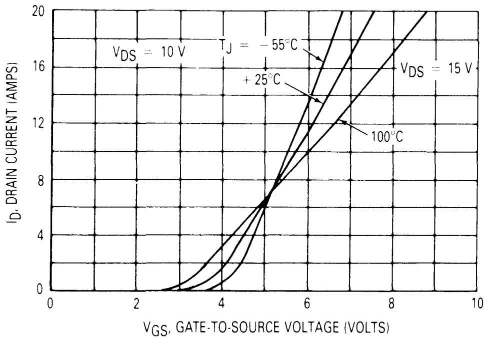


Figure 3. Transfer Characteristics

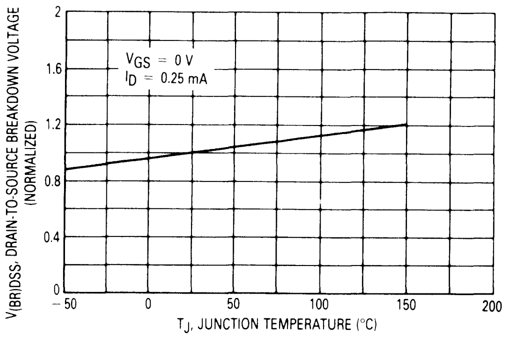


Figure 4. Breakdown Voltage Variation With Temperature

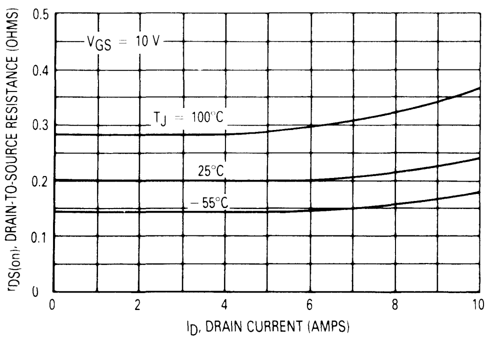


Figure 5. On-Resistance versus Drain Current

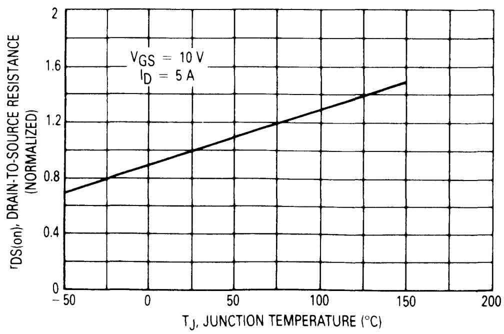


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

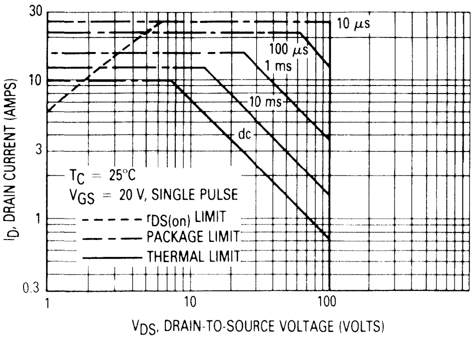


Figure 7. Maximum Rated Forward Biased Safe Operating Area

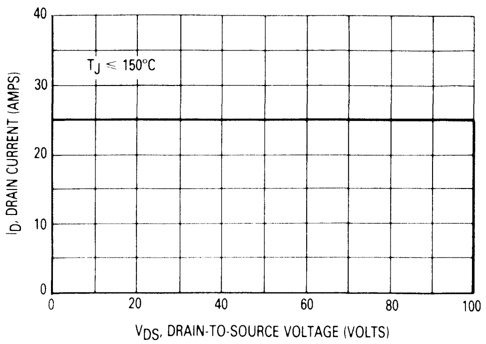


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

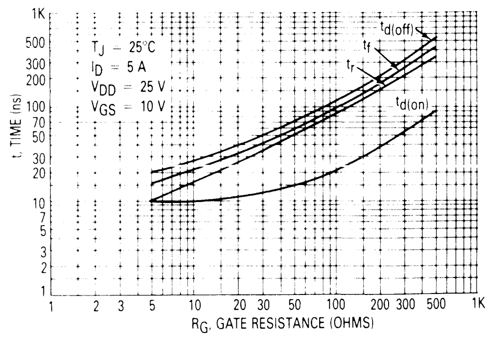


Figure 9. Resistive Switching Time versus Gate Resistance

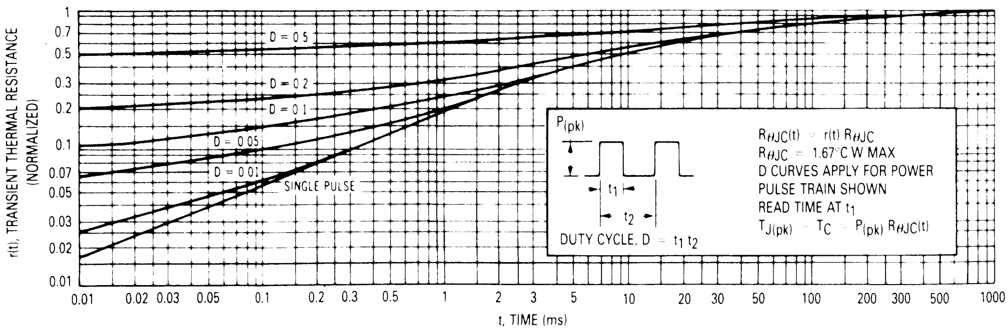


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

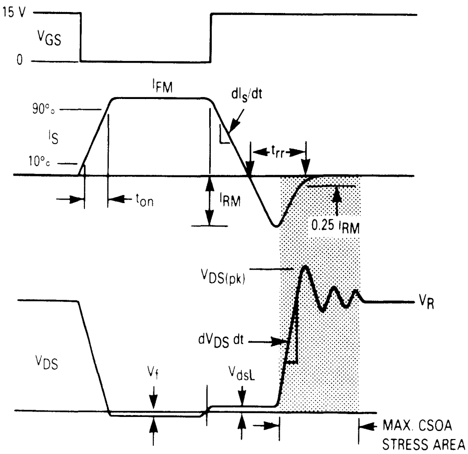


Figure 11. Commutating Waveforms

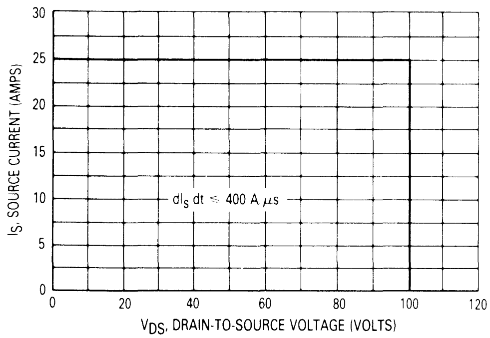


Figure 12. Commutating Safe Operating Area (CSOA)

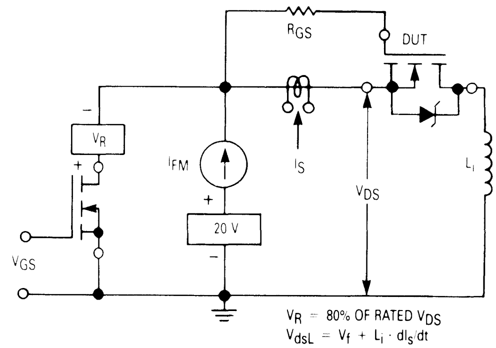


Figure 13. Commutating Safe Operating Area Test Circuit

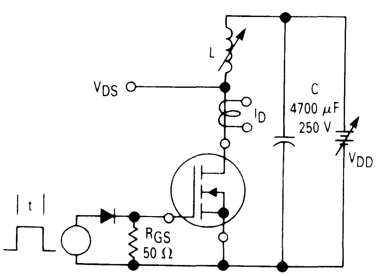
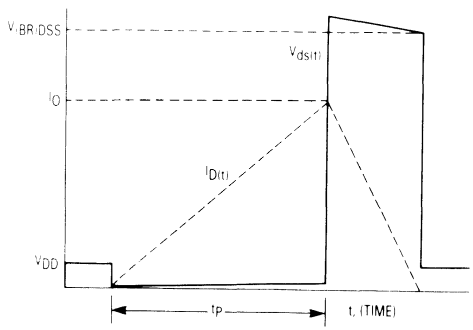


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

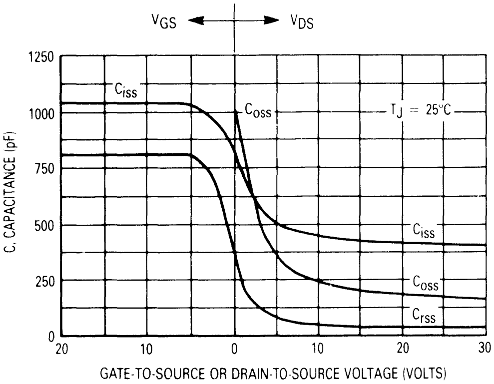


Figure 16. Capacitance Variation

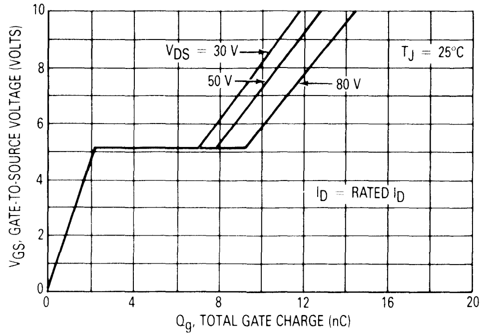
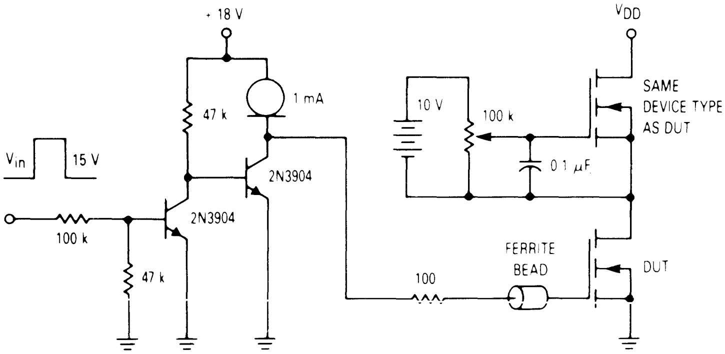


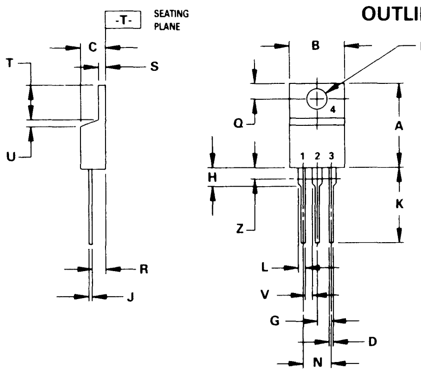
Figure 17. Gate Charge versus Gate-To-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH = 100 μs, DUTY CYCLE = 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



CASE 221A-04
TO-220AB

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP10N10M

Advance Information

Power Field Effect Transistor

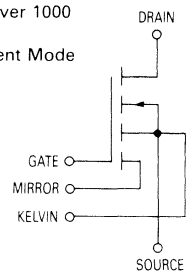
N-Channel Enhancement-Mode Silicon Gate TMOS with Current Sensing Capability

TMOS SENSEFET
10 AMPERES
$r_{DS(on)}$ = 0.25 OHM
100 VOLTS

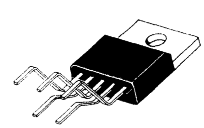
3

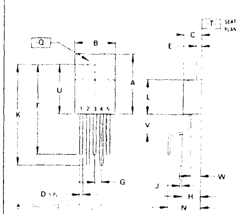
This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with minimum power loss.

- "Lossless" Current Sensing for Maximum Efficiency — Sense Current is Reduced by a Factor of Over 1000
- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy
- Rugged — SOA is Power Dissipation Limited
- Low $r_{DS(on)}$ — 0.25 Ohms Maximum



NOTES:
1. Handling precautions to protect against electrostatic discharge is mandatory.
2. Do not use the mirror FET independent of the power FET.
3. It is recommended that the mirror terminal (M) be shorted to the source terminal (S) when current sensing is not required.





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1:
PIN 1. GATE
2. MIRROR
3. DRAIN
4. KELVIN
5. SOURCE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
F	21.590	23.749	0.850	0.935
G	1.702 BSC		0.067 BSC	
H	4.445	5.080	0.175	0.200
J	0.381	0.635	0.015	0.025
K	22.860	27.940	0.900	1.100
L	8.052	9.398	0.317	0.370
N	7.874	8.509	0.310	0.335
Q	3.556	3.937	0.140	0.155
U	11.888	12.827	0.468	0.505
V	4.699	5.842	0.185	0.230
W	2.286	2.794	0.090	0.110

CASE 314B-02

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	100	Vdc
Drain-to-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-to-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain-to-Mirror Voltage	V_{DMS}	100	Vdc
Gate-to-Mirror Voltage	V_{GM}	±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 25	Adc
Sense Current — Continuous — Pulsed	I_M I_{MM}	6 14	mA
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case Junction-to-Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{MS} = 0 unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	—	Vdc
Drain-to-Mirror Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DMS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}				mAdc
(V_{DS} = 100 V, V_{GS} = 0)		—	—	0.2	
(V_{DS} = 100 V, V_{GS} = 0, T_J = 100°C)		—	—	1	
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage	$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 1 mAdc)		2	3	4.5	
(T_J = 100°C)		1.5	—	4	
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)	$r_{DS(on)}$	—	0.16	0.25	Ohms
Static Drain-to-Mirror On-Resistance (V_{GS} = 10 V, I_D = 10 A, R_{SENSE} = 0)	$r_{DM(on)}$	—	288	—	Ohms
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc)	$V_{DS(on)}$				Vdc
(I_D = 10 A)		—	1.9	2.7	
(I_D = 5 A, T_J = 100°C)		—	—	2.8	
Forward Transconductance (V_{GS} = 10 Vdc, I_D = 5 Adc)	g_{FS}	2.5	—	—	mhos
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 10 A, V_{GS} = 10 V)	n	1750	1800	1850	—

DYNAMIC CHARACTERISTICS

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz, See Figure 6	C_{iss}		—	500	pF
Output Capacitance		C_{oss}	—	—	300	
Transfer Capacitance		C_{rss}	—	—	100	

SWITCHING CHARACTERISTICS*

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Turn-On Delay Time	V_{DD} = 25 V, I_D = 5 A, R_{gen} = 50 Ohms	$t_{d(on)}$	—	—	50	ns
Rise Time		t_r	—	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	50	
Total Gate Charge	V_{DS} = 80 V, I_D = 10 A, V_{GS} = 10 V, See Figure 4	Q_g	—	16	25	nC
Gate-Source Charge		Q_{gs}	—	7	—	
Gate-Drain Charge		Q_{gd}	—	9	—	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Forward On-Voltage	I_S = 10 A	V_{SD}	—	2	—	Vdc
Forward Turn-On Time		t_{on}	—	20	—	ns
Reverse Recovery Time		t_{rr}	—	700	—	

*Indicates Pulse Test: Pulse Width ≤ 300 μs max, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

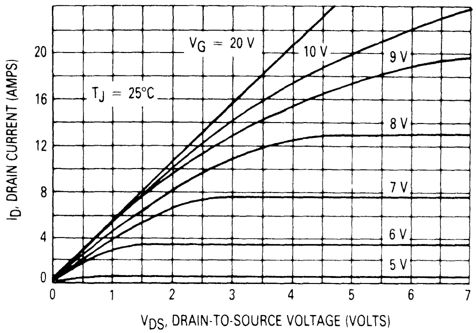


Figure 1. On-Region Characteristics

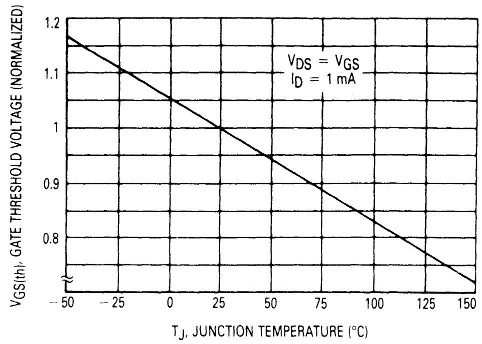


Figure 2. Gate Threshold Voltage Variation with Temperature

3

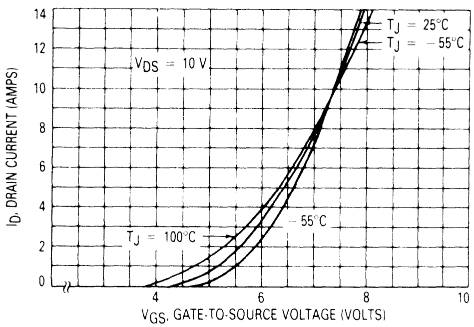


Figure 3. Transfer Characteristics

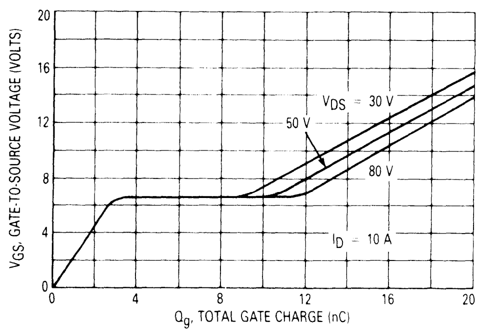


Figure 4. Stored Charge Variation

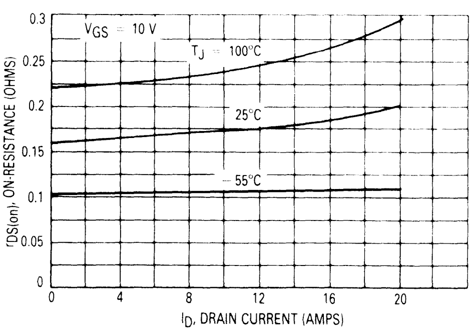


Figure 5. On-Resistance versus Drain Current

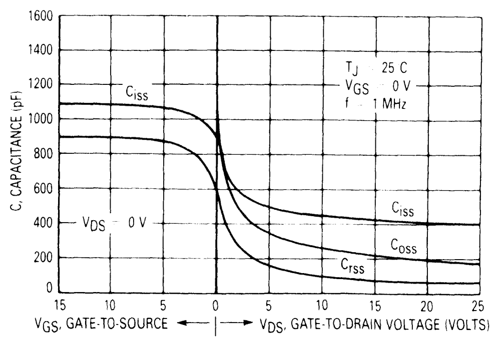


Figure 6. Capacitance Variation

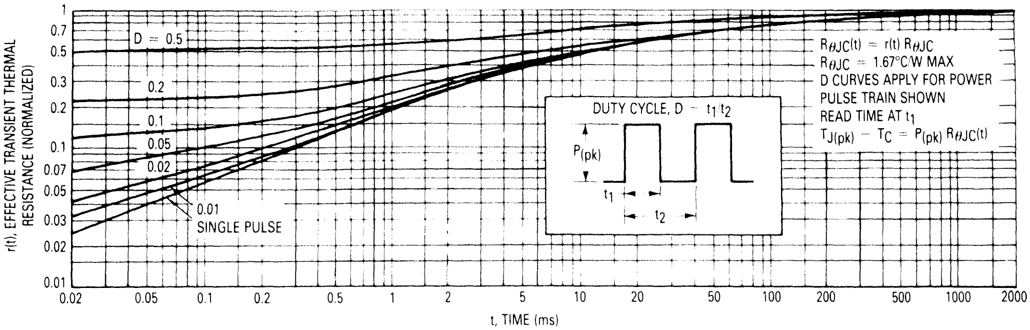


Figure 7. Thermal Response

SAFE OPERATING AREA INFORMATION

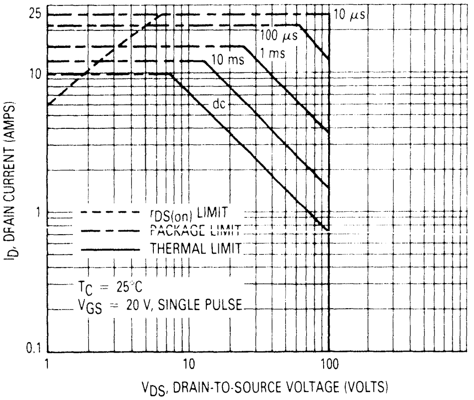


Figure 8. Maximum Rated Forward Biased Safe Operating Area

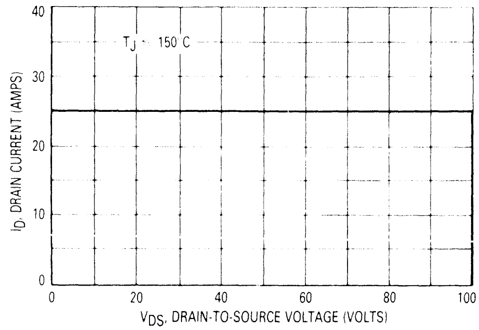


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

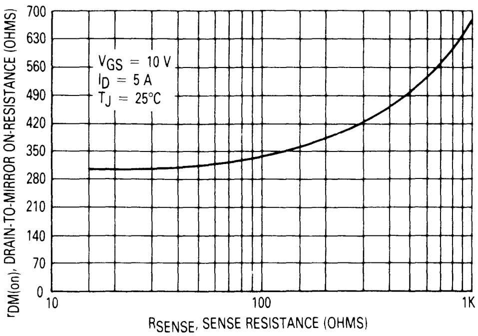


Figure 10. Drain-to-Mirror On-Resistance versus Sense Resistance

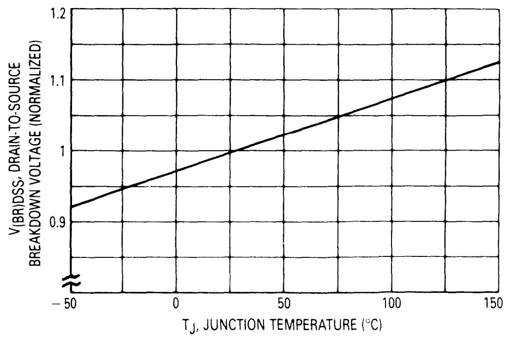


Figure 11. Normalized Drain-To-Source Breakdown Voltage versus Temperature

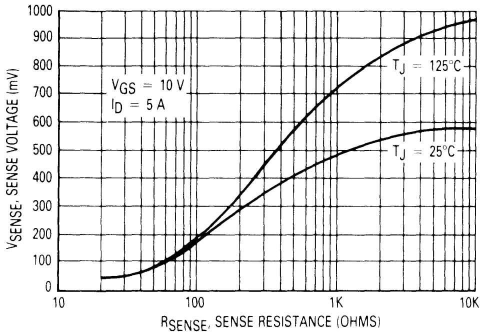


Figure 12. Sense Voltage versus Sense Resistance

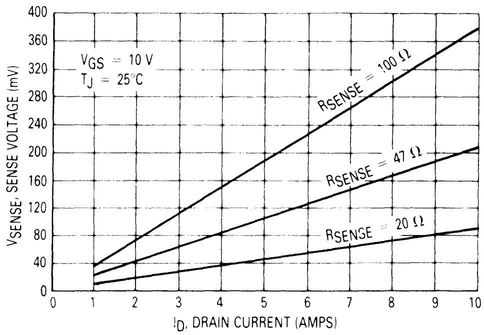


Figure 13. Drain Current versus Sense Voltage

USING SENSEFETs

In practical applications, less sense current will flow than that calculated by using the current mirror ratio, n. Shown in Figure 1 is a model of the SENSEFET. It is seen that R_{SENSE} decreases the voltage across $r_{DM(on)}$ and decreases the sense current. An additional decrease in sense current occurs due to the decreased voltage across the mirror transistors. For this reason, a modified current mirror ratio, n′ must be calculated. The equation to calculate n′ is derived from the MOSFET square law model in the linear region,

$$n' = \frac{n}{1 - \dfrac{V_{SE}(V_{GS} - V_T - 1/2\ V_{SE})}{V_{DS(on)}(V_{GS} - V_T - 1/2\ V_{DS(on)})}}$$

$$n' \approx \frac{n}{1 - V_{SE}/V_{DS(on)}} \qquad (1)$$

(for $V_{SE}, V_{DS(on)} << V_{GS} - V_T$).

Where, V_{GS} = Gate-to-Source Voltage,
V_T = Gate-to-Source Threshold Voltage

and V_{SE} = Sense Voltage $= \dfrac{R_{SENSE}\ I_D}{n'}$. (2)

Hence, n′ can be calculated from equation (1) and the result used in equation (2) to find the value of R_{SENSE}. The value of R_{SENSE} should be kept below 100 Ω for most accurate results.

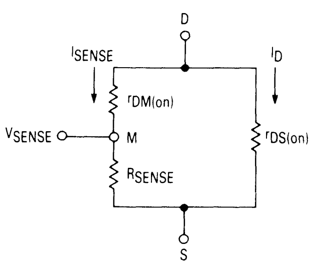


Figure 14. SENSEFET Model

These equations were derived using die level source as the ground reference, neglecting contact and wire bond resistance to the source pin. In practice these parasitic resistances can cause significant errors at high currents, therefore it is mandatory to reference the gate drive signal and measure $V_{DS(on)}$ and V_{SENSE} with respect to the Kelvin pin.

Figure 15 illustrates the correct SENSEFET configuration.

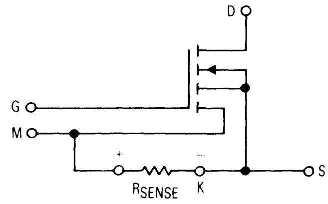
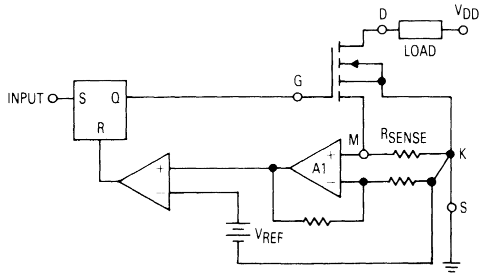


Figure 15. SENSEFET Configuration

SENSEFET APPLICATIONS CONSIDERATIONS

3

- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET is likely due to over-dissipation. By syncing the current limit loop to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Noise Suppression: Noise pickup in the current sensing circuitry of SENSEFET systems can be a first order design issue. Layout, therefore is critical. In addition, some spike limiting capacitance across R_{SENSE} is often desirable, provided that it is placed right at the current sensing circuitry's input terminals. To help with the layout problem, a Kelvin source connection is provided. The Kelvin connection gives SENSEFETs separate power and signal source pins. This feature can be used advantageously with circuits such as the MC34129 current mode controller and MC33034 brushless dc motor drive, which also have dual grounds.
- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop error in this kind of situation is a first order design consideration. In particular, current flowing from the SENSEFET's source into a non-zero ground impedance can easily create voltage drops which are significant with respect to SENSEFET signal levels. Here again, the Kelvin connection is a useful tool. Tying the current limit circuitry's voltage reference to the Kelvin terminal as shown in Figure 16 eliminates errors that can be developed by high currents flowing in a power ground.



Set A1 gain to match sense voltage to V_{REF} at max I_D.

Figure 16. Typical Current Sensing with a SENSEFET

- Temperature Stability: With very low values of R_{SENSE}, temperature tracking depends primarily upon the matching of monolithic devices and is generally within a few percent for a 100°C change in temperature. As R_{SENSE} is increased, however, temperature coefficient becomes less dependent upon matching and more a function of the power section's on-voltage. In the limit where R_{SENSE} is very large, sense voltage approximates $V_{DS(on)}$ and tracks its temperature coefficient. It is not unusual to see V_{SENSE} change less than 5% for a 100°C change in temperature provided that R_{SENSE} is less than 10% of $r_{DM(on)}$. On the other hand, changes of 50% are not unusual when R_{SENSE} exceeds $r_{DM(on)}$.
- There is a parasitic reverse diode on the current mirror MOSFET as well as the power MOSFET. Diode reverse recovery currents will cause a sense voltage spike that may have to be filtered from the sense circuitry.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP10N15

Designer's Data Sheet

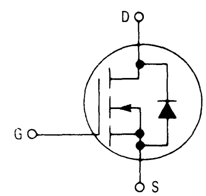
Power Field Effect Transistor

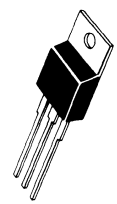
N-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FET
10 AMPERES
$r_{DS(on)}$ = 0.3 OHM
150 VOLTS





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 28	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	 $R_{\theta JC}$	 1.67	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP10N15		$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc) (I_D = 5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3 2.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 5 A)		g_{FS}	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	800	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	180	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	15 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	7 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.2 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

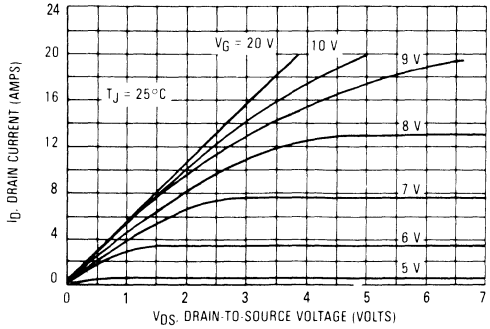


Figure 1. On-Region Characteristics

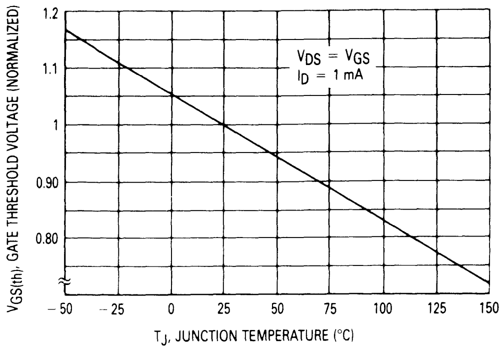


Figure 2. Gate-Threshold Voltage Variation With Temperature

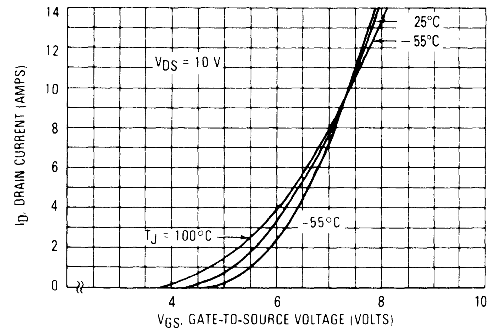


Figure 3. Transfer Characteristics

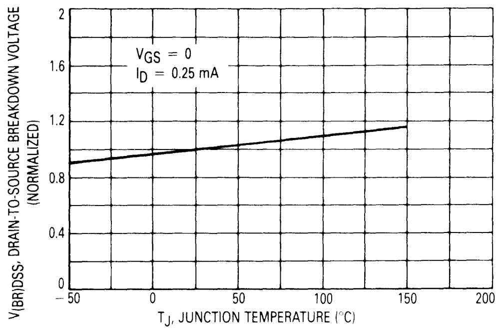


Figure 4. Breakdown Voltage Variation With Temperature

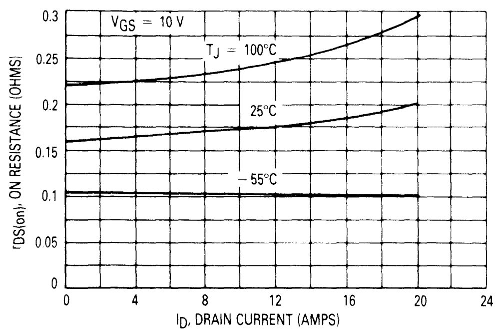


Figure 5. On-Resistance versus Drain Current

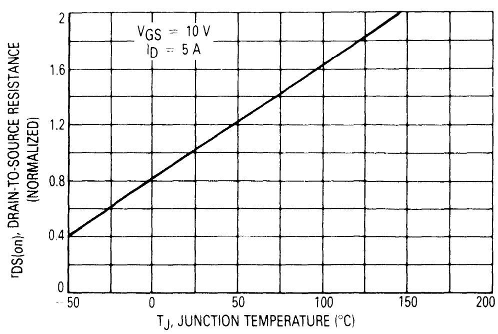


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

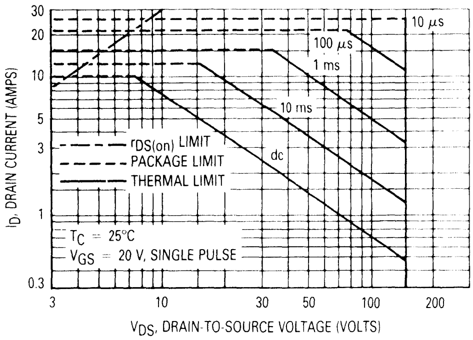


Figure 7. Maximum Rated Forward Biased Safe Operating Area

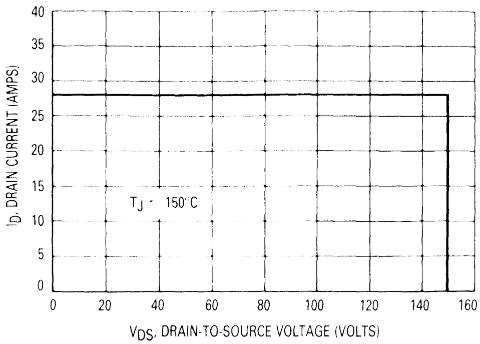


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

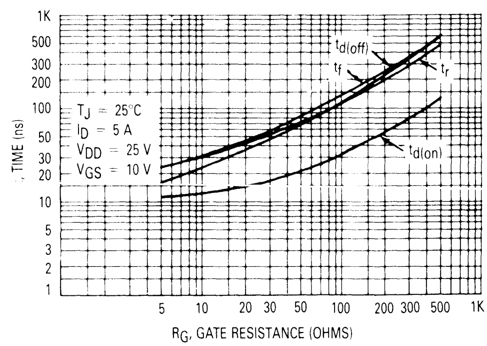


Figure 9. Resistive Switching Time Variation versus Gate Resistance

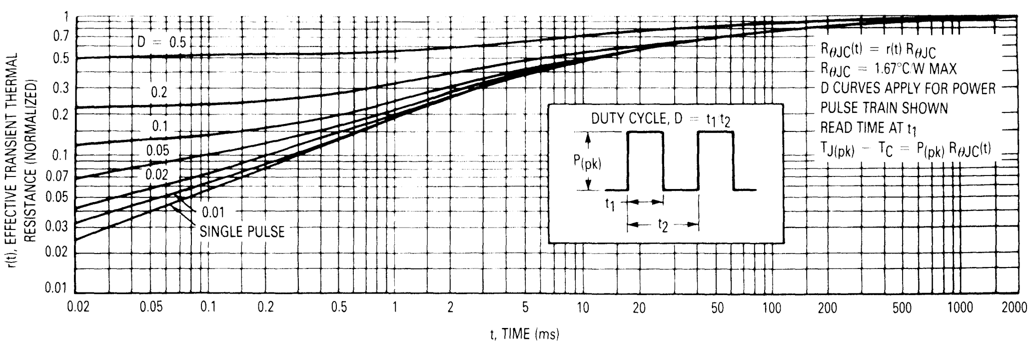


Figure 10. Thermal Response

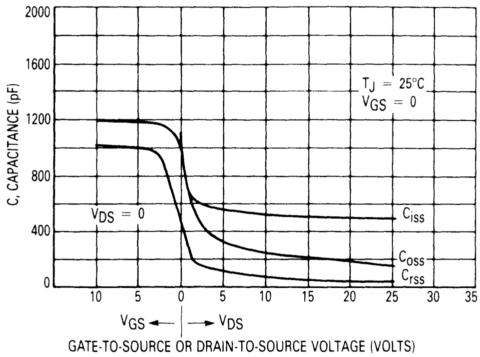


Figure 11. Capacitance Variation

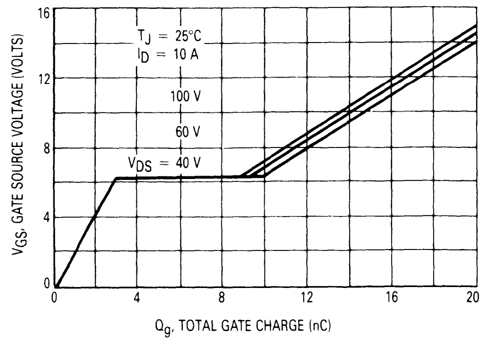


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

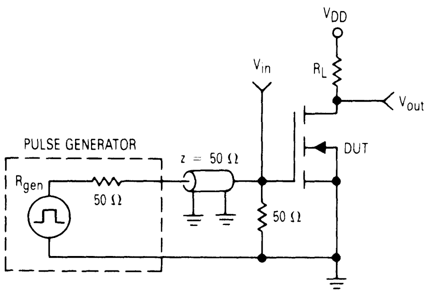


Figure 13. Switching Test Circuit

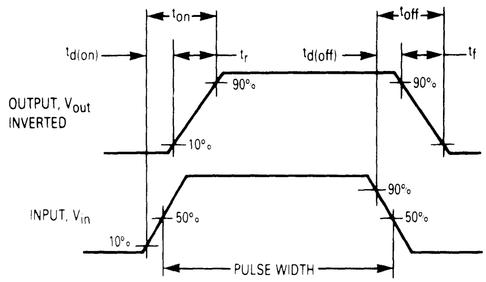
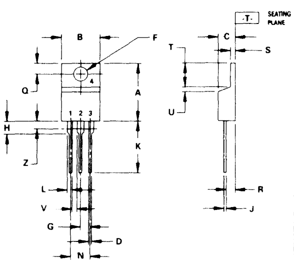


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP10N35
MTP10N40

Designer's Data Sheet

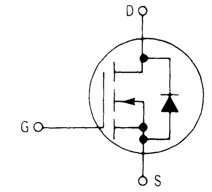
Power Field Effect Transistor

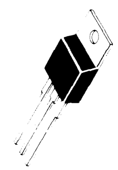
N-Channel Enhancement-Mode
Silicon Gate TMOS

TMOS POWER FETs
10 AMPERES
$r_{DS(on)}$ = 0.55 OHM
350 and 400 VOLTS

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 10N35	MTP 10N40	Unit
Drain-Source Voltage	V_{DSS}	350	400	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	350	400	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t_p ≤ 50 μs)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 10 40		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	MTP10N35 MTP10N40	$V_{(BR)DSS}$	350 400	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	0.2 1	mAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 Adc)		$r_{DS(on)}$	—	0.55	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 10 Adc) (I_D = 5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	6 4.75	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 5 A)		g_{FS}	4	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	350	
Reverse Transfer Capacitance		C_{rss}	—	150	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.1 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	600 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

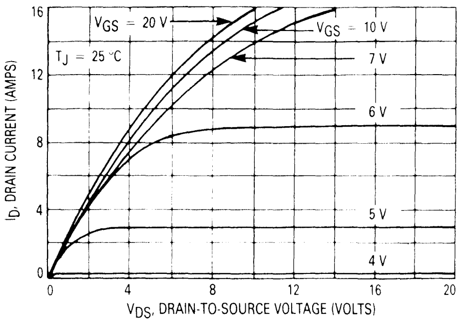


Figure 1. On-Region Characteristics

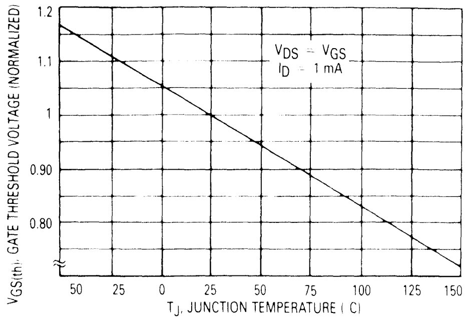


Figure 2. Gate-Threshold Voltage Variation With Temperature

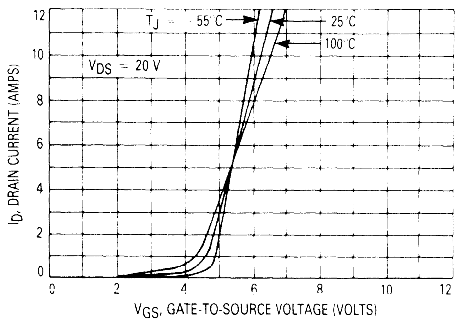


Figure 3. Transfer Characteristics

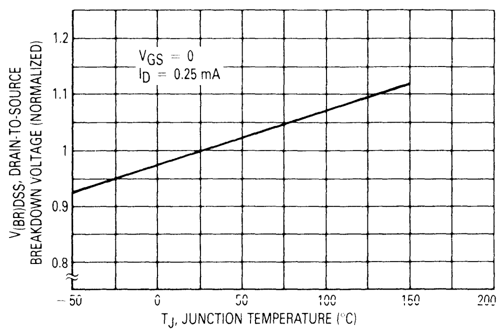


Figure 4. Breakdown Voltage Variation With Temperature

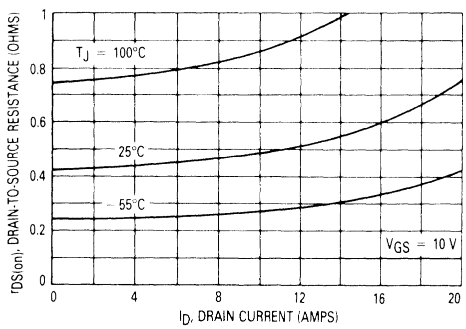


Figure 5. On-Resistance versus Drain Current

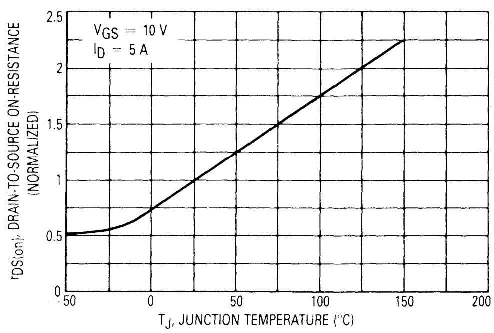


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

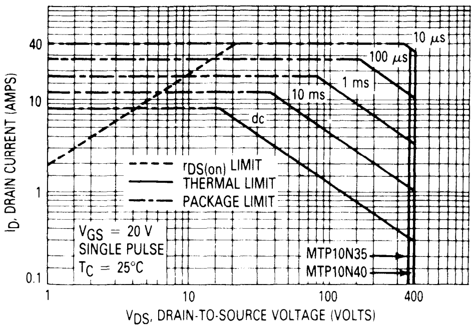


Figure 7. Maximum Rated Forward Biased Safe Operating Area

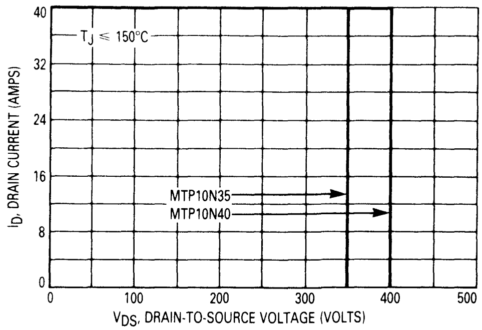


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

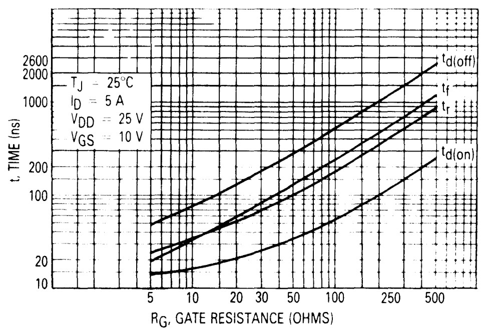


Figure 9. Resistive Switching Time Variation versus Gate Resistance

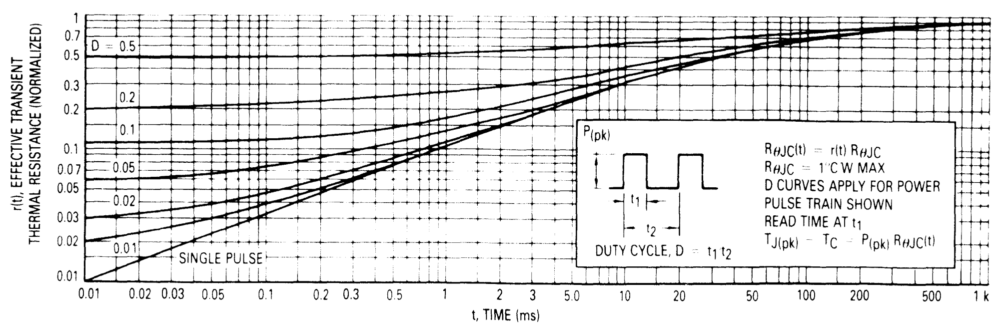


Figure 10. Thermal Response

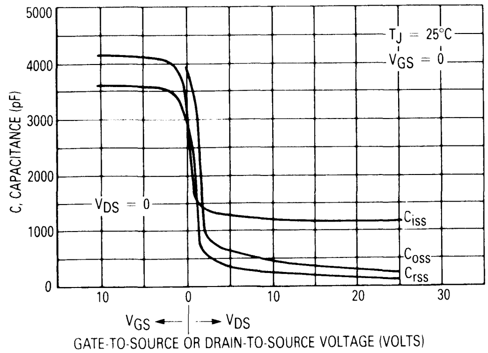


Figure 11. Capacitance Variation

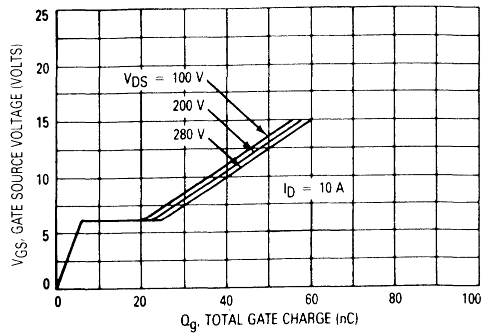


Figure 12. Gate Charge versus Gate-to-Source Voltage

RESISTIVE SWITCHING

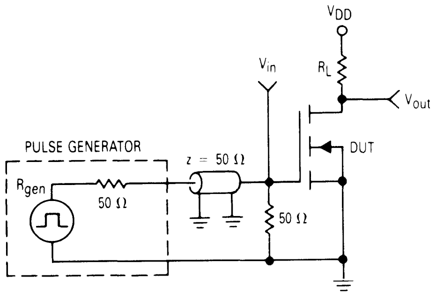


Figure 13. Switching Test Circuit

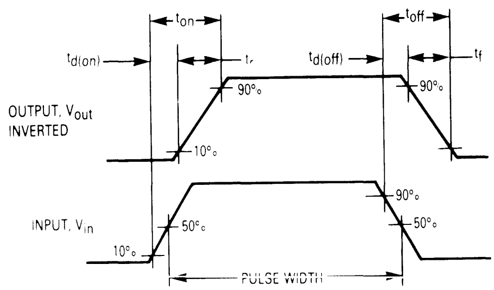
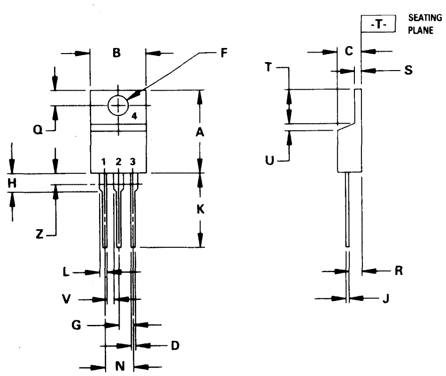


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 221A-04
TO-220AB

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

MTP12N08L
MTP12N10L

Designer's Data Sheet

Power Field Effect Transistor

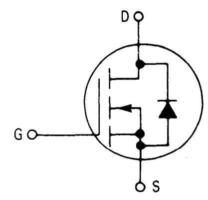
N-Channel Enhancement-Mode
Silicon Gate TMOS

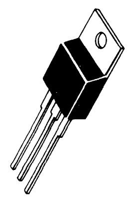
TMOS POWER FETs
LOGIC LEVEL
12 AMPERES
$r_{DS(on)}$ = 0.18 OHM
80 and 100 VOLTS

These Logic Level TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP12N08L	MTP12N10L	Unit
Drain-Source Voltage	V_{DSS}	80	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±15 ±20		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 30		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) MTP12N08L MTP12N10L	$V_{(BR)DSS}$	 80 100	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	2	Vdc
(T_J = 100°C)			0.75	1.5	
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 12 Adc)		$V_{DS(on)}$	—	2.4	Vdc
(I_D = 6 Adc, T_J = 100°C)			—	1.6	
Forward Transconductance (V_{DS} = 10 V, I_D = 6 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	800	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	2600	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	—	350	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz		—	1600	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{oss}	—	100	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	130	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 11 and 12.	Q_g	15 (typ)	25	nC
Gate-Source Charge		Q_{gs}	3.7 (typ)	—	
Gate-Drain Charge		Q_{gd}	11.3 (typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1 (typ)	1.25	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			3.5 (typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

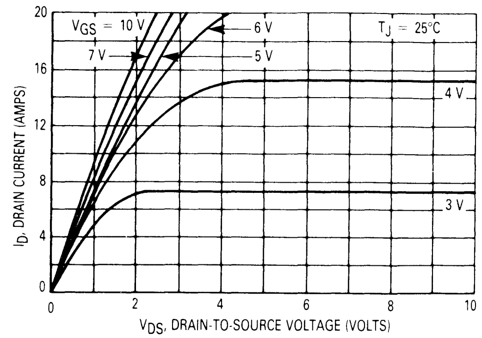


Figure 1. On-Region Characteristics

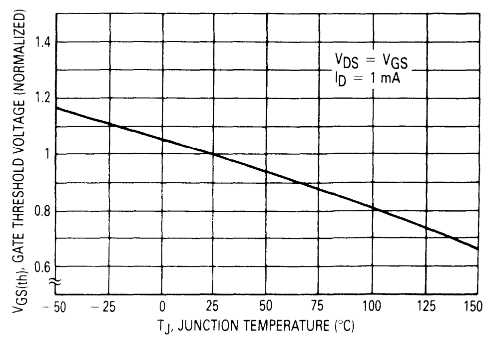


Figure 2. Gate-Threshold Voltage Variation With Temperature

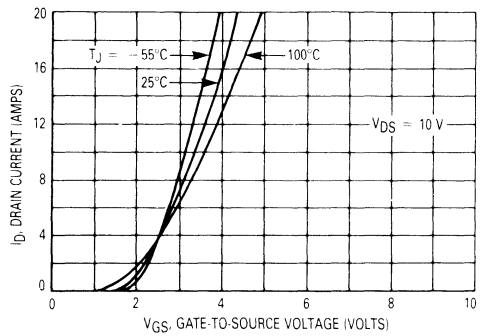


Figure 3. Transfer Characteristics

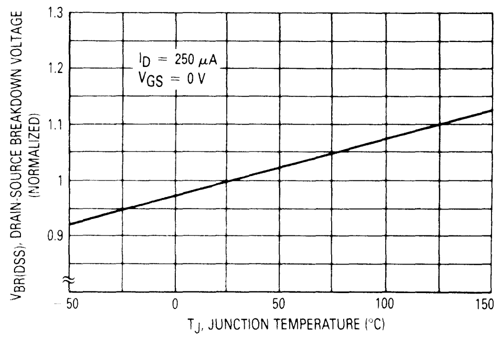


Figure 4. Breakdown Voltage Variation With Temperature

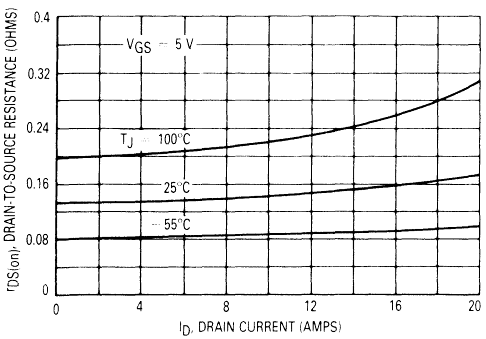


Figure 5. On-Resistance Variation With Drain Current

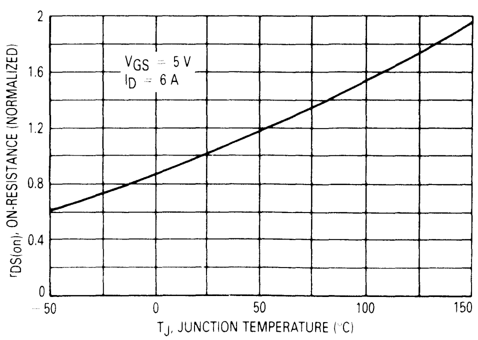


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

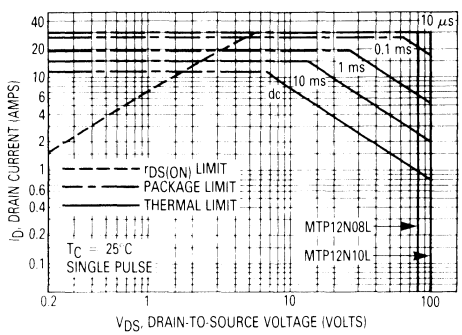


Figure 7. Maximum Rated Forward Biased Safe Operating Area

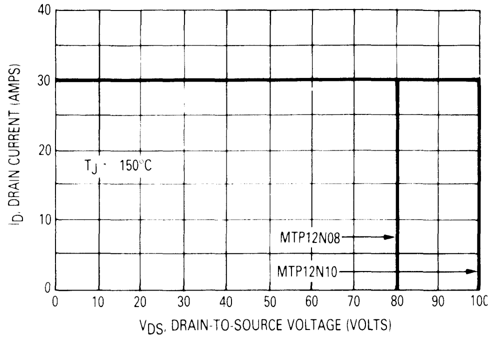


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

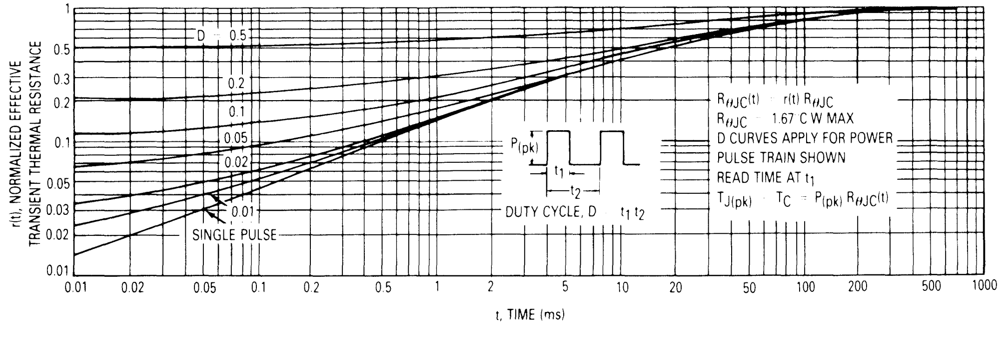


Figure 9. Thermal Response

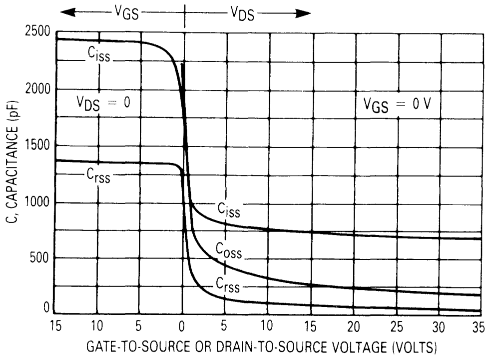


Figure 10. Capacitance Variation With Voltage

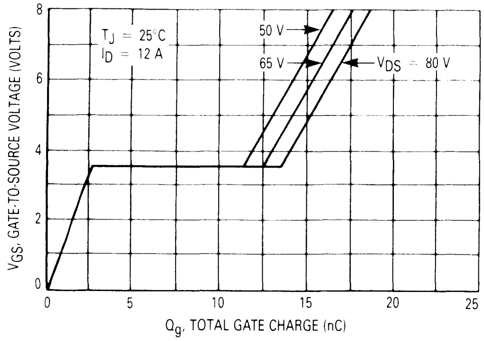
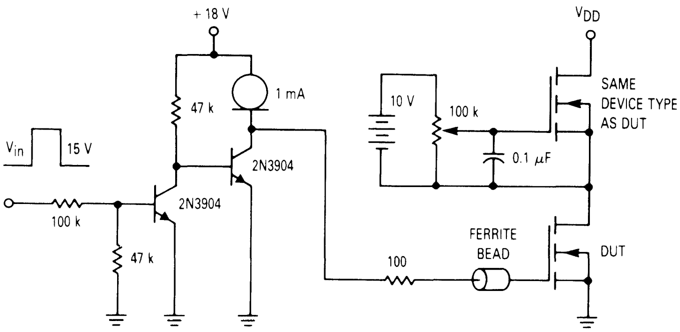


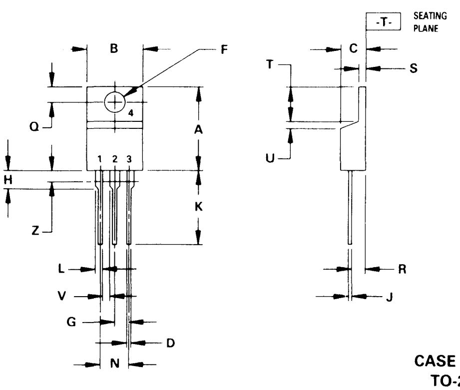
Figure 11. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 12. Gate Charge Test Circuit

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

MTP12N20

Designer's Data Sheet

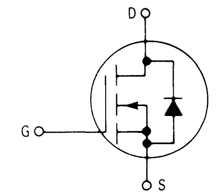
Power Field Effect Transistor

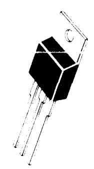
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
12 AMPERES
$r_{DS(on)}$ = 0.35 OHM
200 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	200	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate-Source Voltage — Continuous — Non-repetitive (t_p ≤ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 40	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	200	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0)		I_{DSS}	—	10	μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.35	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc)		$V_{DS(on)}$	—	5	Vdc
(I_D = 6 Adc, T_J = 100°C)			—	4.2	
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)		g_{FS}	4.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	24 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	13 (Typ)	—	
Gate-Drain Charge		Q_{gd}	11 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	3	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	3.5 (Typ)	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

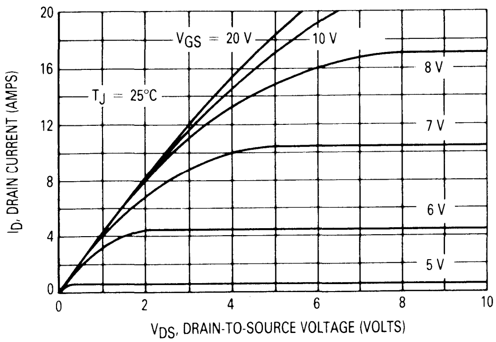


Figure 1. On-Region Characteristics

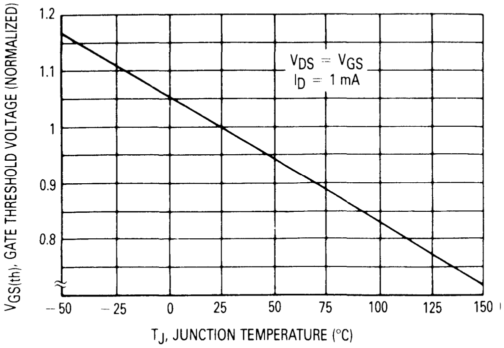


Figure 2. Gate-Threshold Voltage Variation With Temperature

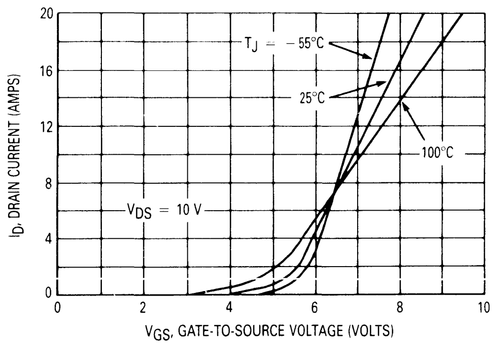


Figure 3. Transfer Characteristics

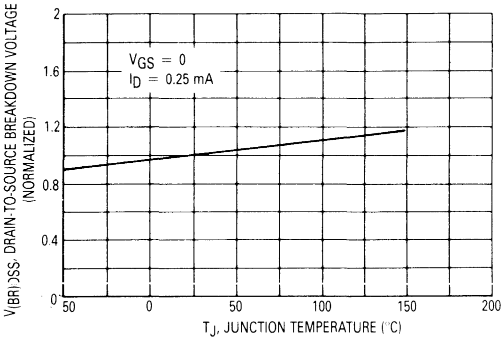


Figure 4. Breakdown Voltage Variation With Temperature

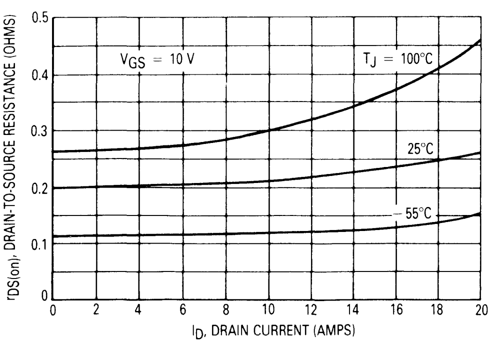


Figure 5. On-Resistance versus Drain Current

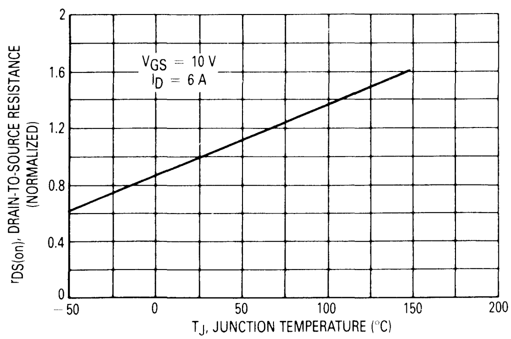


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

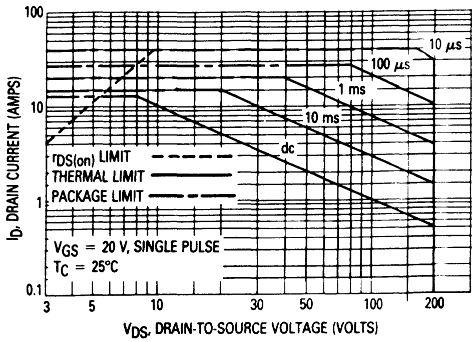


Figure 7. Maximum Rated Forward Biased Safe Operating Area

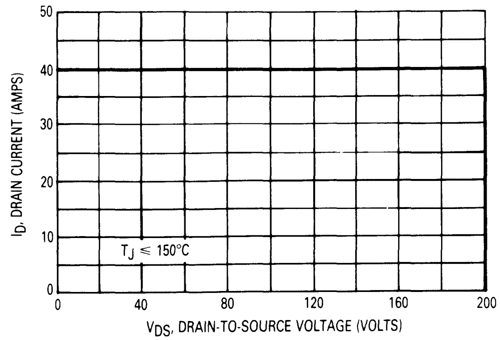


Figure 8. Maximum Rated Switching Safe Operating Area

3

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

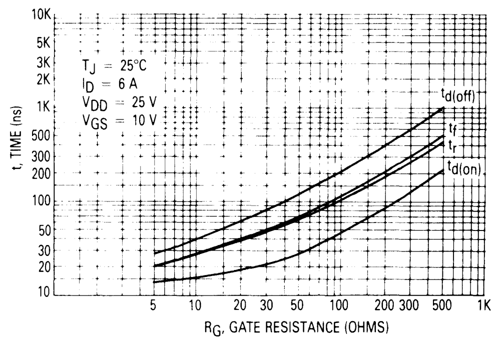


Figure 9. Resistive Switching Time Variation versus Gate Resistance

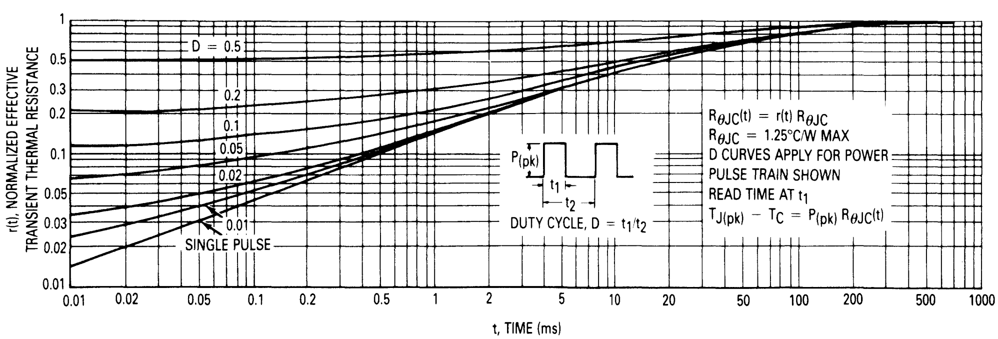


Figure 10. Thermal Response

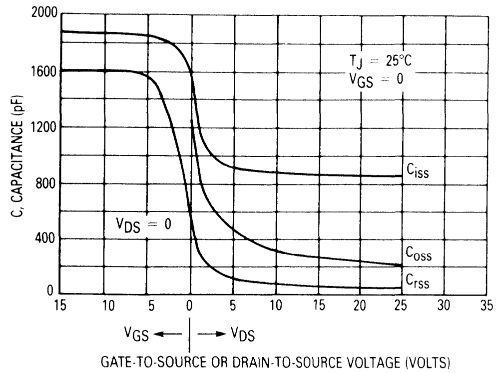


Figure 11. Capacitance Variation

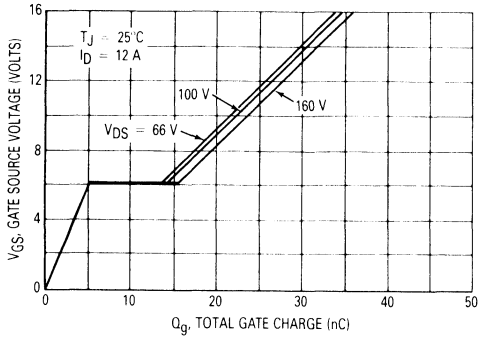


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

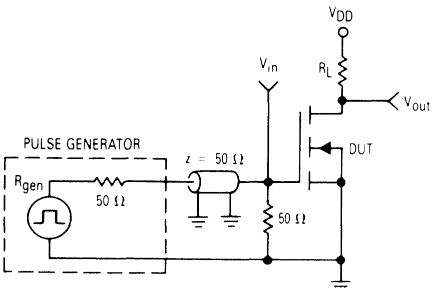


Figure 13. Switching Test Circuit

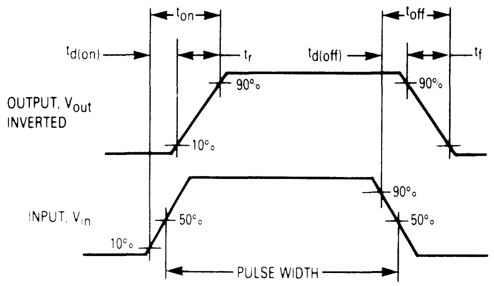
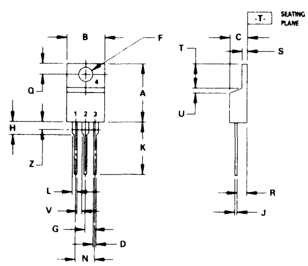


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

CASE 221A-04
TO-220AB

MTP15N05
MTP15N06

Designer's Data Sheet

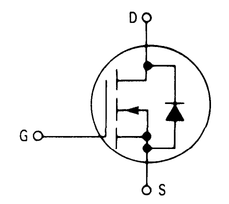
Power Field Effect Transistor

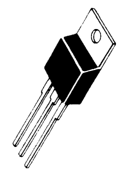
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FETs
15 AMPERES
$r_{DS(on)}$ = 0.16 OHM
50 and 60 VOLTS

These TMOS Power FETs are designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTP 15N05	MTP 15N06	Unit
Drain-Source Voltage	V_{DSS}	50	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40		Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 40		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA) MTP15N05 / MTP15N06		$V_{(BR)DSS}$	50 60	— —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) / (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) / T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.16	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc) / (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	2.9 2.4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	3.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	700	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn-Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	17 (Typ)	35	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	9 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.8 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	320 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) / (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

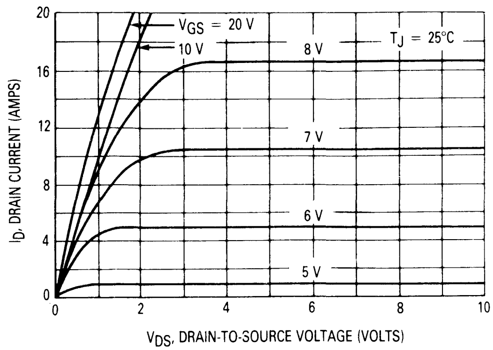


Figure 1. On-Region Characteristics

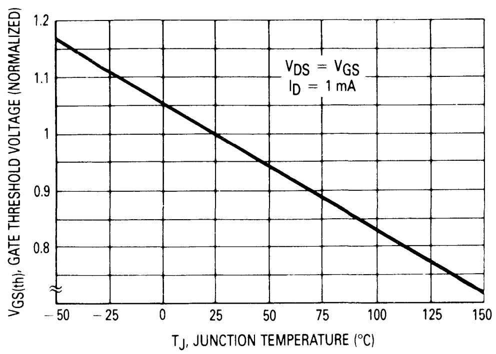


Figure 2. Gate-Threshold Voltage Variation With Temperature

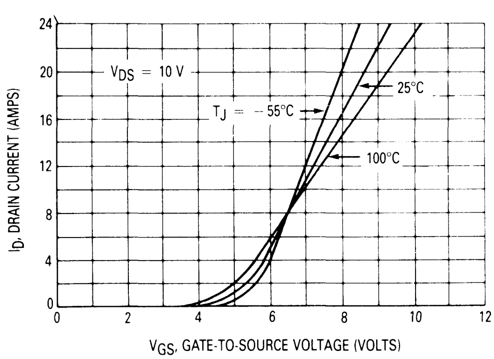


Figure 3. Transfer Characteristics

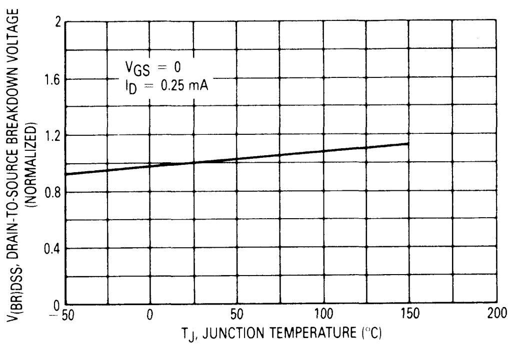


Figure 4. Breakdown Voltage Variation With Temperature

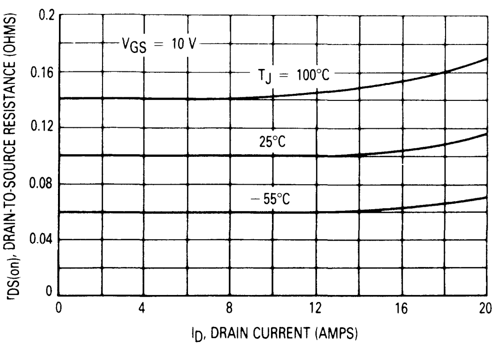


Figure 5. On-Resistance versus Drain Current

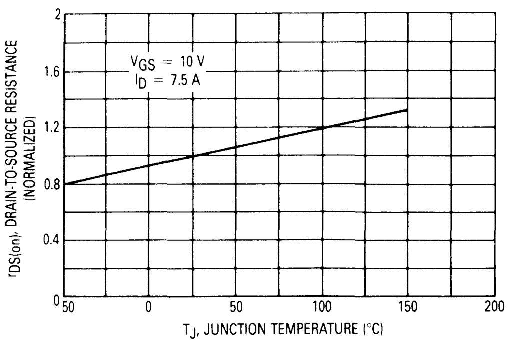


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

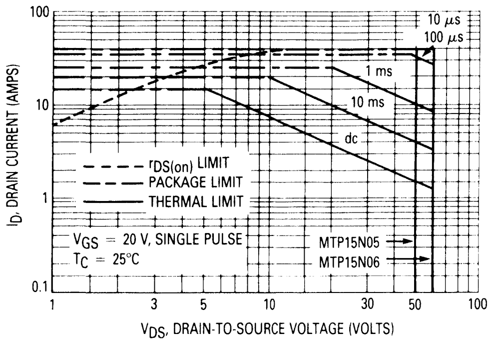


Figure 7. Maximum Rated Forward Biased Safe Operating Area

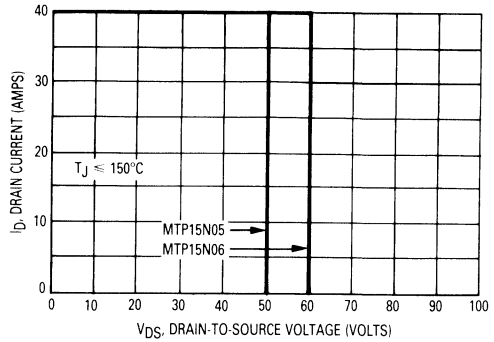


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

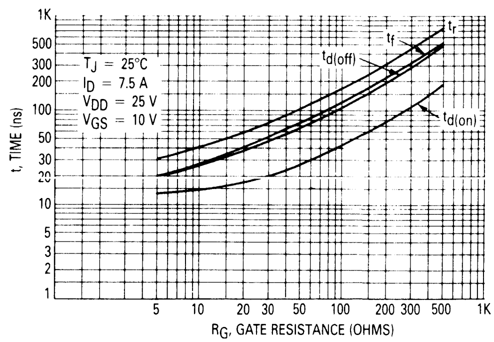


Figure 9. Resistive Switching Time versus Gate Resistance

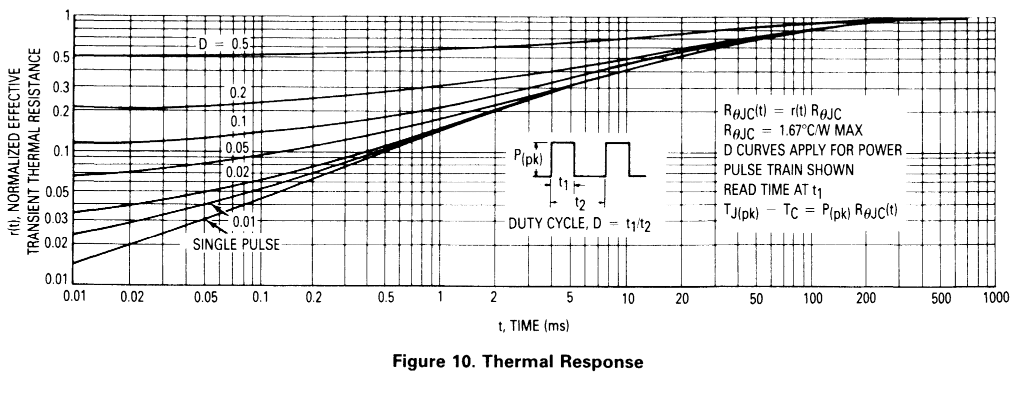


Figure 10. Thermal Response

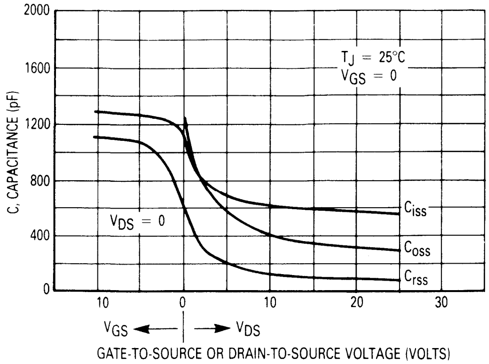


Figure 11. Capacitance Variation

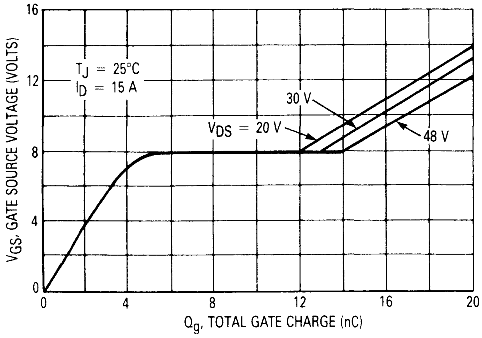


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESISTIVE SWITCHING

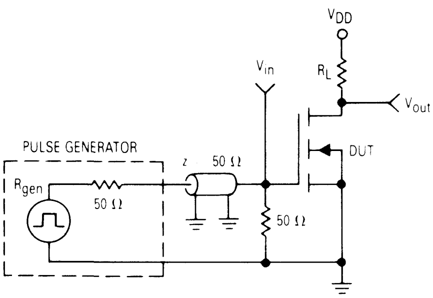


Figure 13. Switching Test Circuit

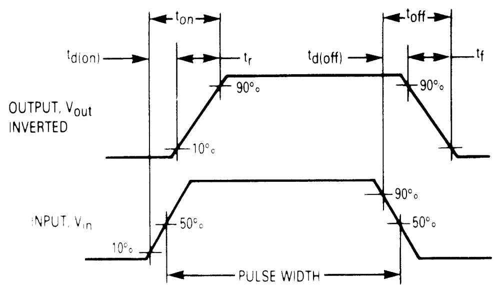
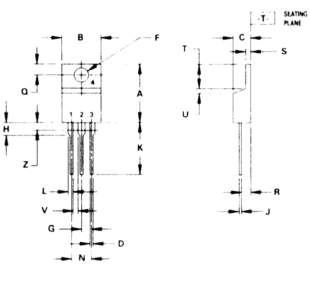


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MTP15N08L

Designer's Data Sheet

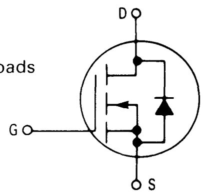
Power Field Effect Transistors

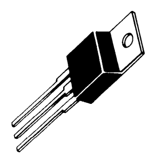
N-Channel Enhancement-Mode Silicon Gate TMOS

This Logic Level TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts Max
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

**TMOS POWER FET
LOGIC LEVEL
15 AMPERES
$r_{DS(on)}$ = 0.135 OHM
80 VOLTS**





**CASE 221A-04
TO-220AB**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	80	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	Vdc
Gate-Source Voltage — Continuous — Non-Repetitive ($t_p \le 50\ \mu s$)	V_{GS}	±15 ±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 45	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)	$V_{(BR)DSS}$	80	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 80 Volts, V_{GS} = 0) (V_{DS} = 80 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	1 50	μAdc

(continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) (T_J = 100°C)		$V_{GS(th)}$	 1 0.75	 2 1.75	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.135	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2.5 1.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	6	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	750 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 8		2500 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	65 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 8		1400 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 8	C_{oss}	240 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 7.5 A, V_{GS} = 5 V, R_{gen} = 50 ohms) See Figures 13 and 14	$t_{d(on)}$	16 (Typ)	—	ns
Rise Time		t_r	85 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	85 (Typ)	—	
Fall Time		t_f	75 (Typ)	—	
Total Gate Charge	(V_{DD} = 60 V, I_D = 15 A, V_{GS} = 5 Vdc) See Figures 9 and 10	Q_g	12.5 (Typ)	22	nC
Gate-Source Charge		Q_{gs}	2 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	I_S = 15 A, V_{GS} = 0	V_{SD}	1.06 (Typ)	1.2	Vdc
Forward Turn-On Time	I_S = 15 A, dI_S/dt = dI_S/dt = 100 A/μs, V_R = 30 V See Figures 16 and 17	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	85 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

3

3

Figure 1. On-Region Characteristics

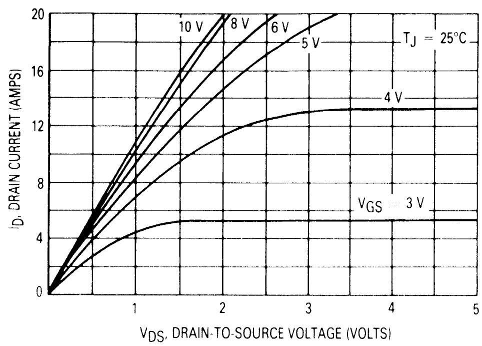


Figure 2. Gate-Threshold Voltage Variation With Temperature

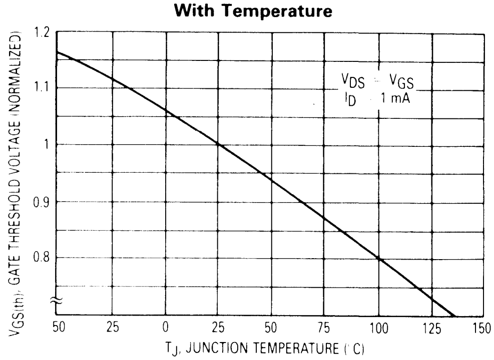


Figure 3. Transfer Characteristics

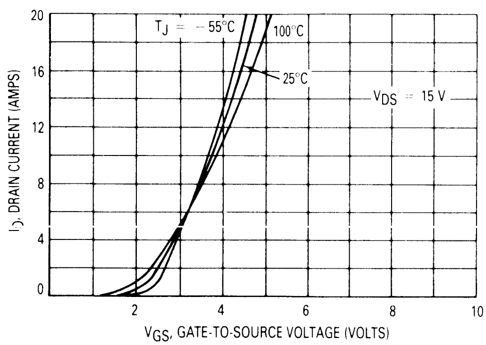


Figure 4. On-Resistance Variation With Drain Current

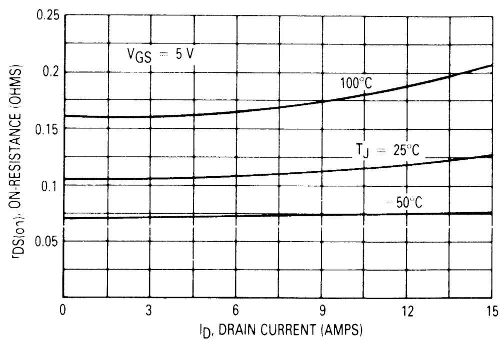


Figure 5. On-Resistance versus Gate-to-Source Voltage

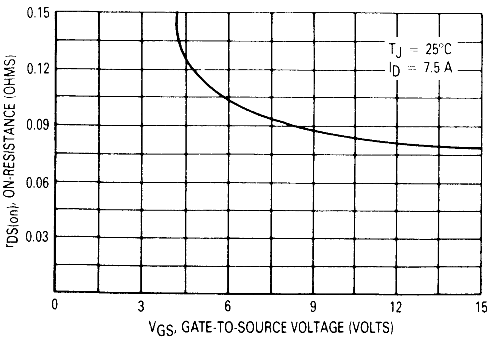


Figure 6. On-Resistance Variation With Temperature

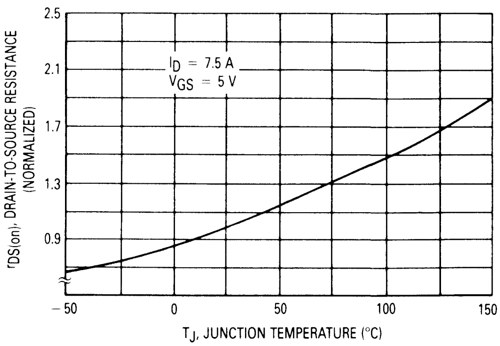


Figure 7. Drain-Source Breakdown Voltage Variation with Temperature

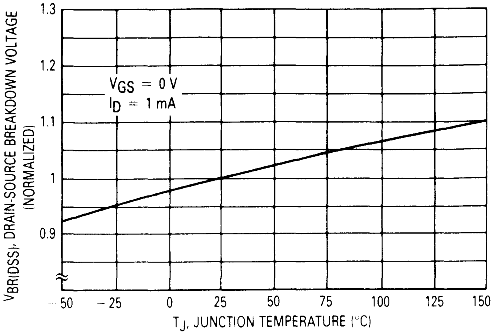


Figure 8. Capacitance Variation With Voltage

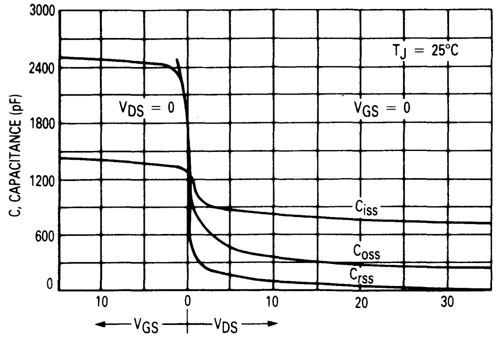
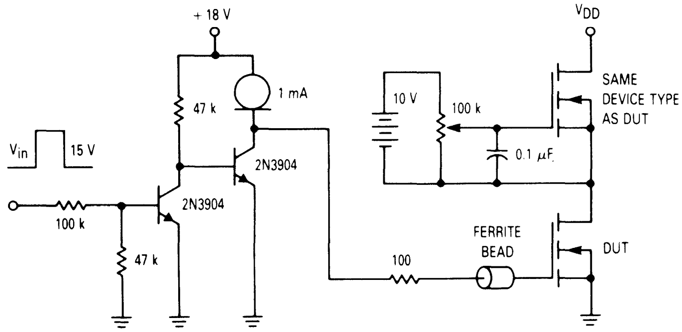
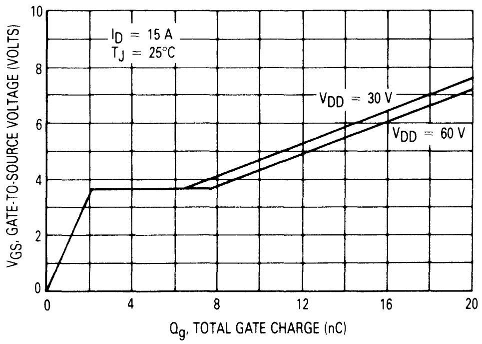


Figure 9. Gate Charge Test Circuit

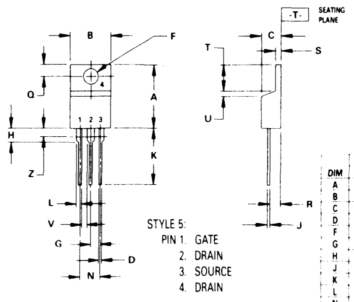


V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Gate Charge Variation



OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH
3 DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED

CASE 221A-04
TO-220AB

PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

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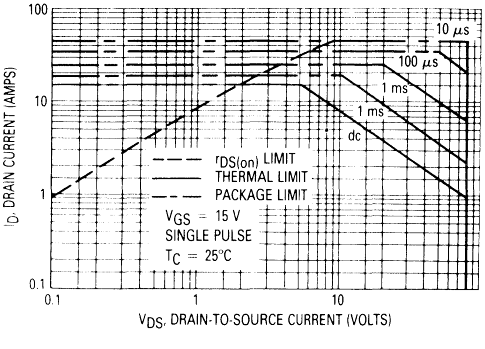
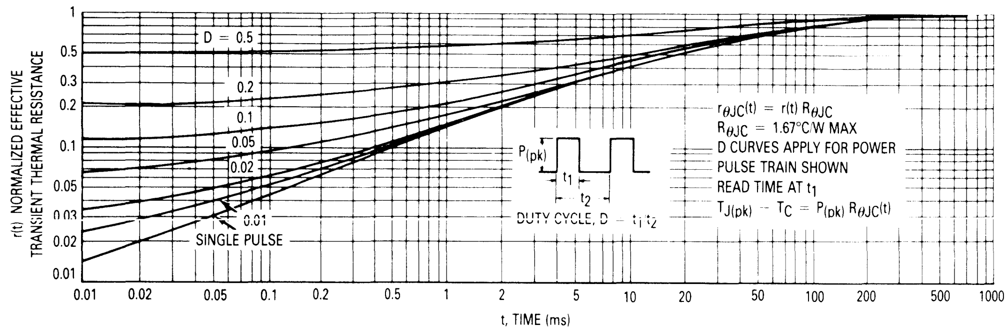
Figure 11. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 12. Thermal Response



RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

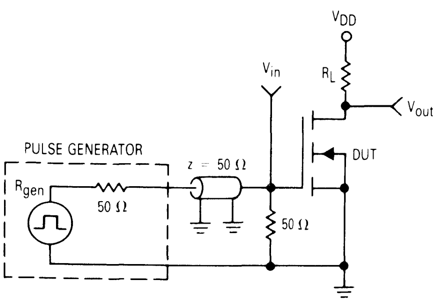
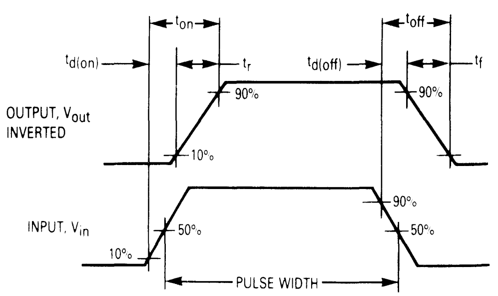


Figure 14. Switching Waveforms



MTP15N15

Designer's Data Sheet

Power Field Effect Transistor

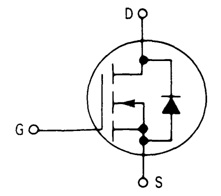
N-Channel Enhancement-Mode Silicon Gate TMOS

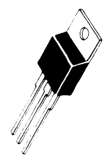
TM
TMOS

TMOS POWER FET
15 AMPERES
$r_{DS(on)}$ = 0.25 OHM
150 VOLTS

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	150	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	150	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	15 48	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.25	°C/W
Junction to Ambient TO-220	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$r_{DS(on)}$	—	0.25	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.5 3.75	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 7.5 A)		g_{FS}	5.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	120	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 12	Q_g	23 (Typ)	45	nC
Gate-Source Charge		Q_{gs}	11 (Typ)	—	
Gate-Drain Charge		Q_{gd}	12 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.2 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

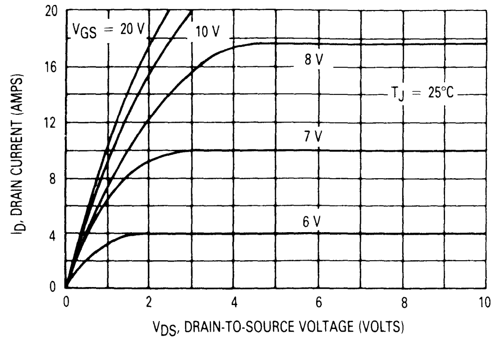


Figure 1. On-Region Characteristics

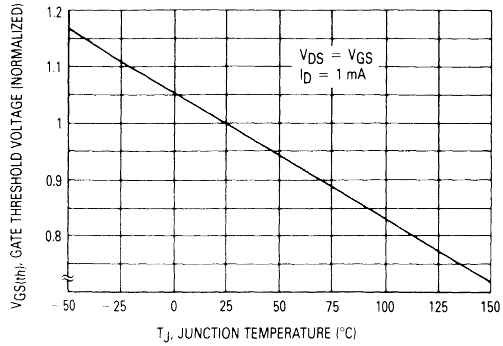


Figure 2. Gate-Threshold Voltage Variation With Temperature

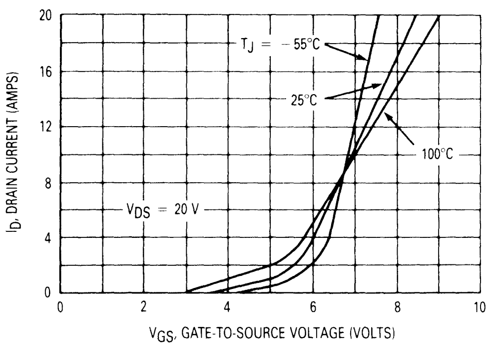


Figure 3. Transfer Characteristics

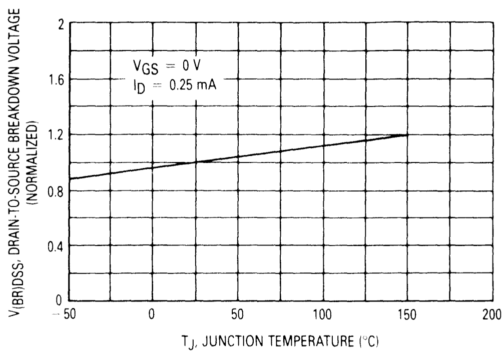


Figure 4. Breakdown Voltage Variation With Temperature

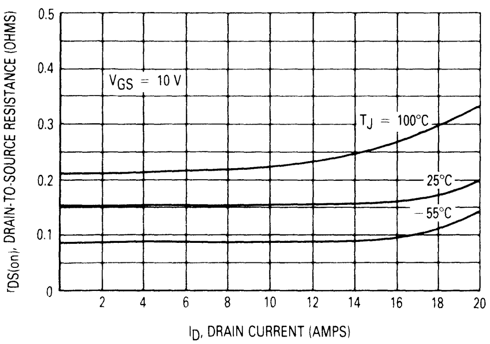


Figure 5. On-Resistance versus Drain Current

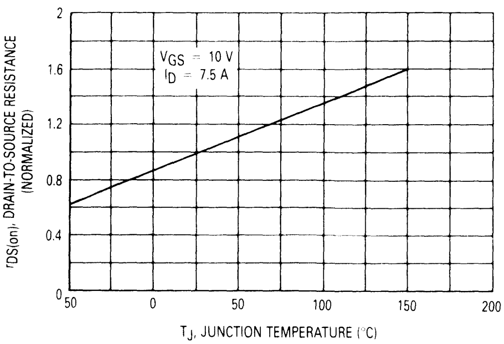


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

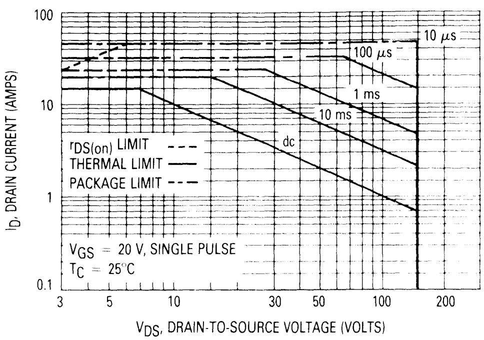


Figure 7. Maximum Rated Forward Biased Safe Operating Area

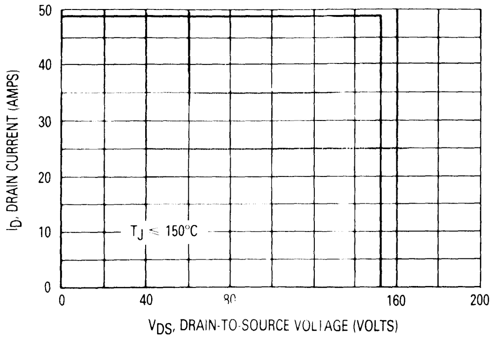


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

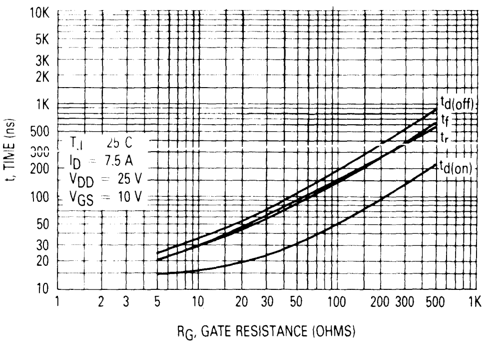


Figure 9. Resistive Switching Time Variation versus Gate Resistance

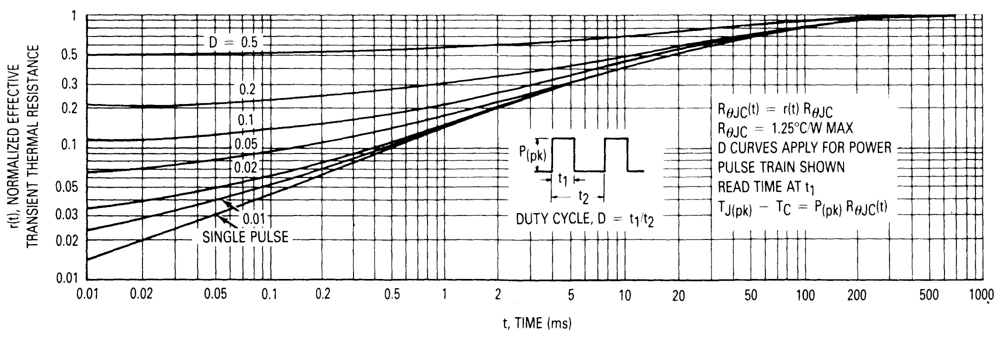


Figure 10. Thermal Response

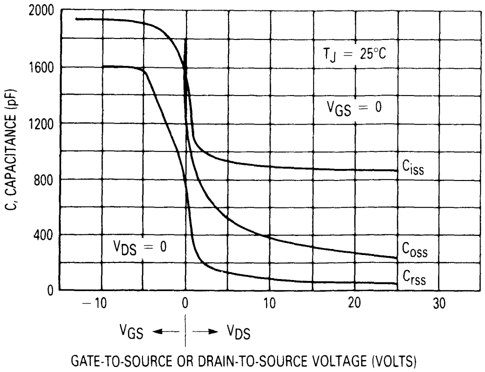


Figure 11. Capacitance Variation

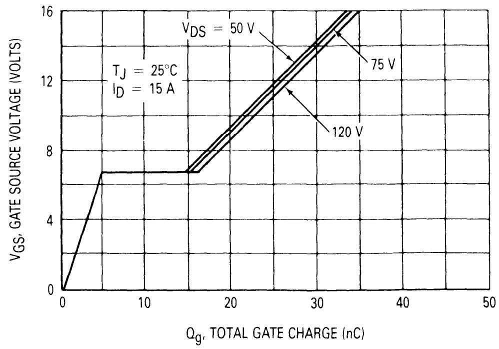


Figure 12. Gate Charge versus Gate-to-Source Voltage

3

RESISTIVE SWITCHING

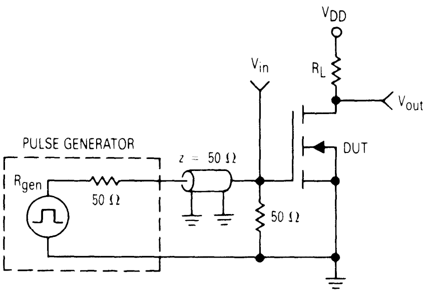


Figure 13. Switching Test Circuit

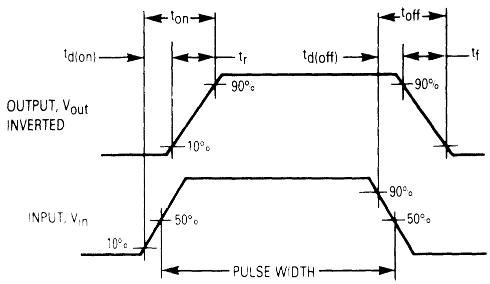
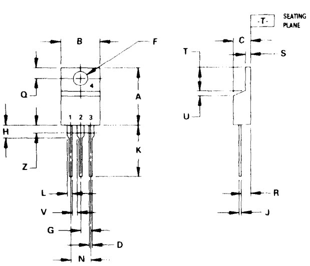


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z		2.04	—	0.080

STYLE 5
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

MTP20N10E

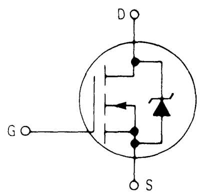
Designer's Data Sheet

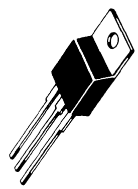
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER FET
20 AMPERES
$r_{DS(on)}$ = 0.15 OHM
100 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \le 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	20 60	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.67	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 175	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_J \le 175°C$)

Single Pulse Drain-to-Source Avalanche Energy Repetitive Pulse Drain-to-Source Avalanche Energy	W_{DSS} (1) W_{DSS} (2) W_{DSR} (3)	400 100 10	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 25 V, I_D = 20 A, L = 1.5 mH, Initial T_C = 25°C
(2) V_{DD} = 25 V, I_D = 20 A, L = 380 µH, Initial T_C = 100°C
(3) f = 10 kHz

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 80	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	3.6 3	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 10 A)		g_{FS}	6	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	600	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	28 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	15 (Typ)	—	
Gate-Drain Charge		Q_{gd}	13 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.9	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

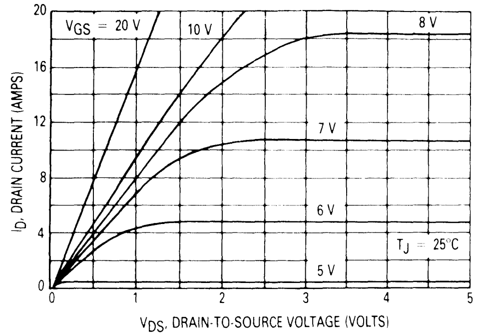


Figure 2. Gate-Threshold Voltage Variation With Temperature

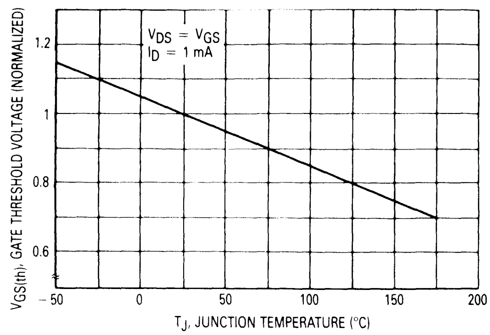


Figure 3. Transfer Characteristics

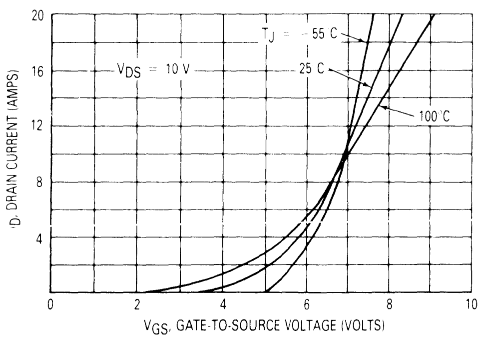


Figure 4. Breakdown Voltage Variation With Temperature

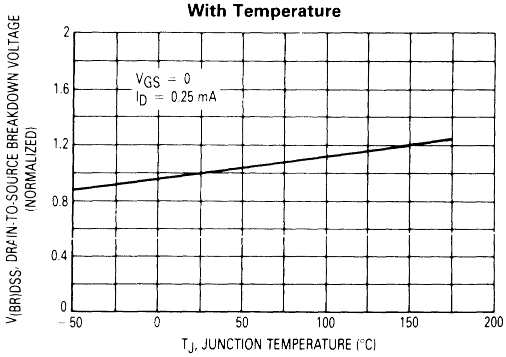


Figure 5. On-Resistance versus Drain Current

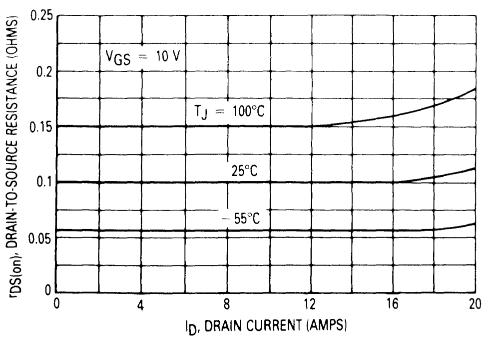
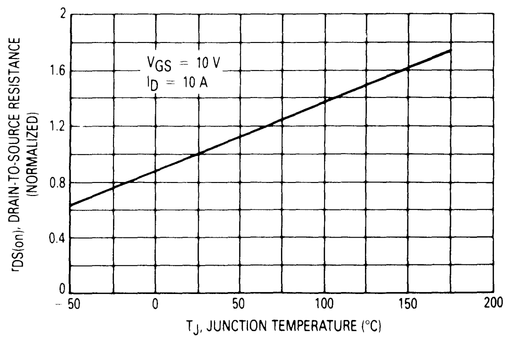


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

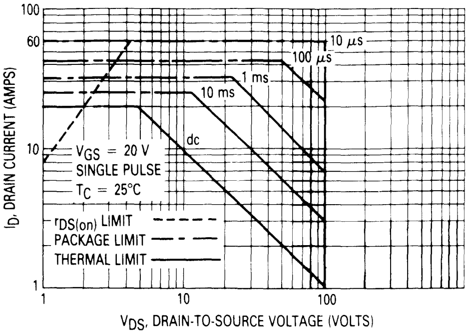
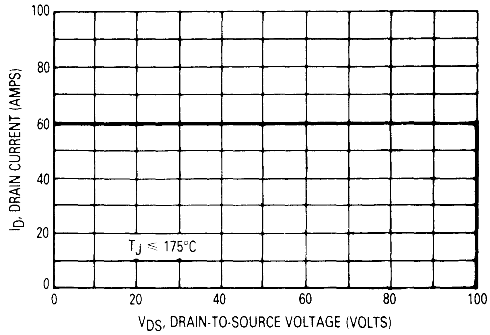


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time Variation versus Gate Resistance

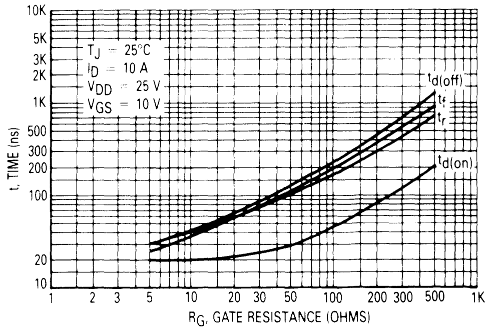
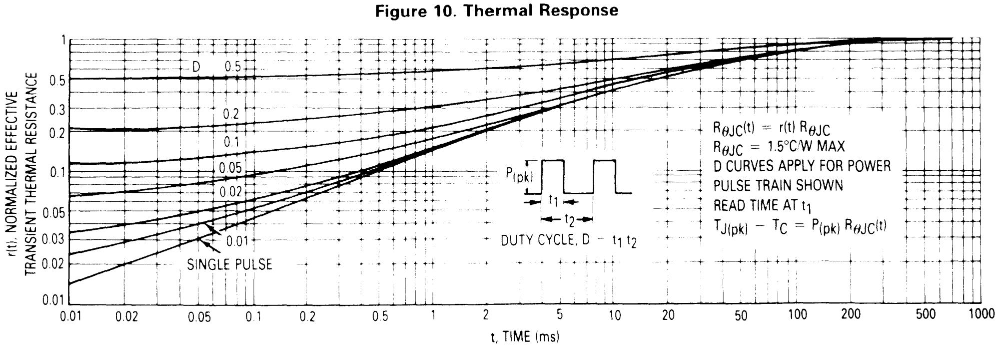


Figure 10. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

Figure 11. Commutating Waveforms

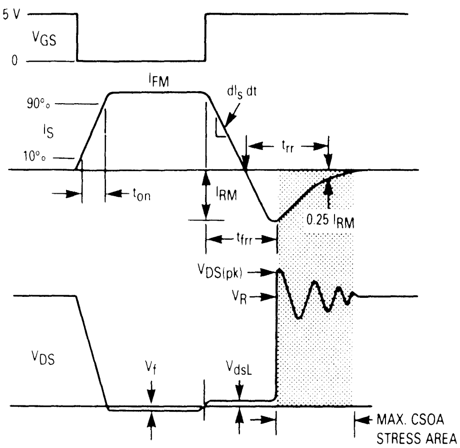


Figure 12. Commutating Safe Operating Area (CSOA)

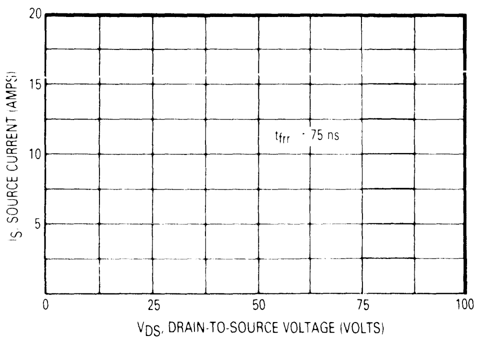


Figure 13. Commutating Safe Operating Area Test Circuit

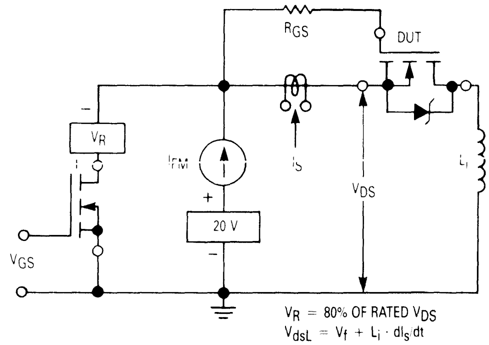


Figure 14. Unclamped Inductive Switching Test Circuit

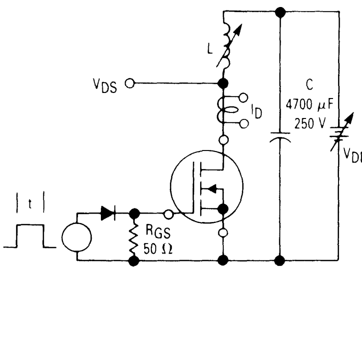
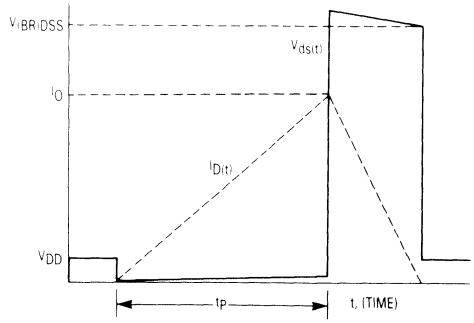


Figure 15. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 16. Capacitance Variation

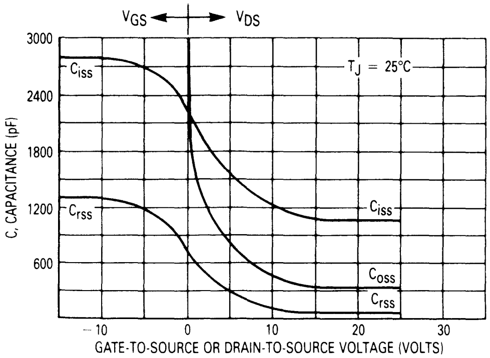


Figure 17. Gate Charge versus Gate-to-Source Voltage

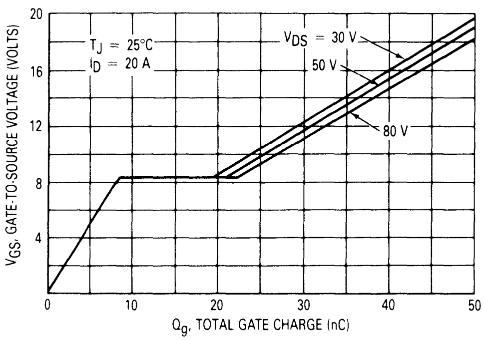
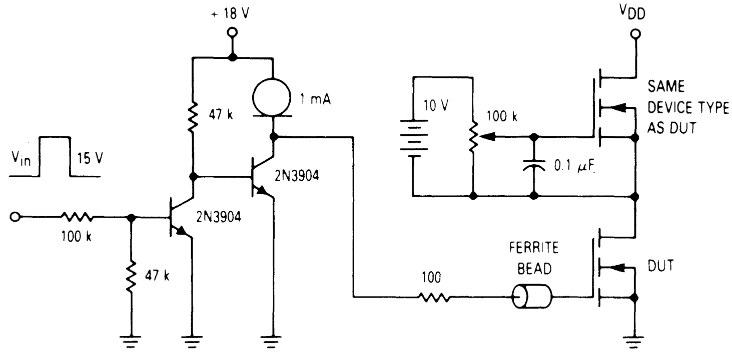
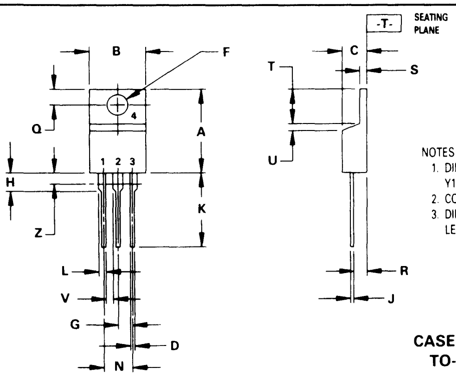


Figure 18. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

MTP20P06

Advance Information

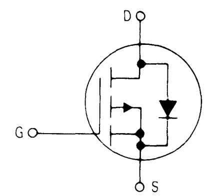
Power Field Effect Transistor

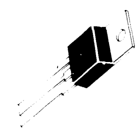
P-Channel Enhancement-Mode Silicon Gate TMOS

This TMOS Power FET is designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS POWER FET
20 AMPERES
$r_{DS(on)}$ = 0.2 OHM
60 VOLTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	20 72	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.25	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS*					
Gate Threshold Voltage ($V_{DS} = V_{GS}$, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$r_{DS(on)}$	—	0.2	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	4.2 4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 10 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	1400	pF
Output Capacitance		C_{oss}	—	700	
Reverse Transfer Capacitance		C_{rss}	—	300	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 10 Amp, R_{gen} = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	350	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	160	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = 20 Amp, V_{GS} = 10 V) See Figure 12	Q_g	30 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	10 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 20 Amp, V_{GS} = 0)	V_{SD}	4 (Typ)	4.2	Vdc
Forward Turn-On Time		t_{on}	100 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	120 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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TYPICAL ELECTRICAL CHARACTERISTICS

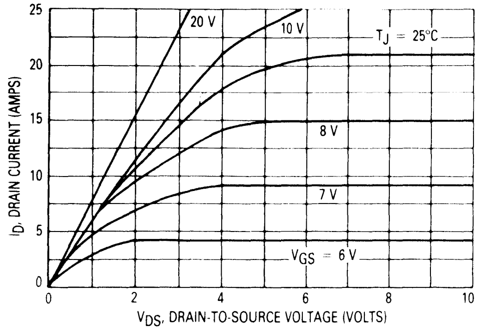


Figure 1. On-Region Characteristics

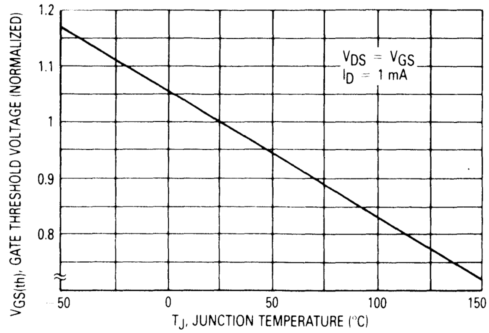


Figure 2. Gate-Threshold Variation With Temperature

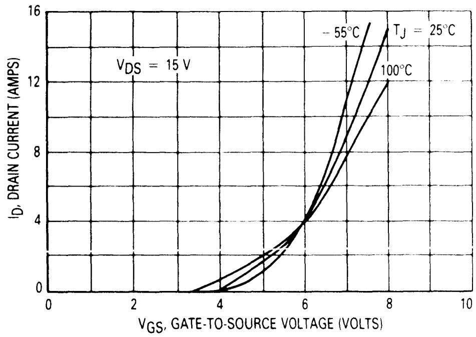


Figure 3. Transfer Characteristics

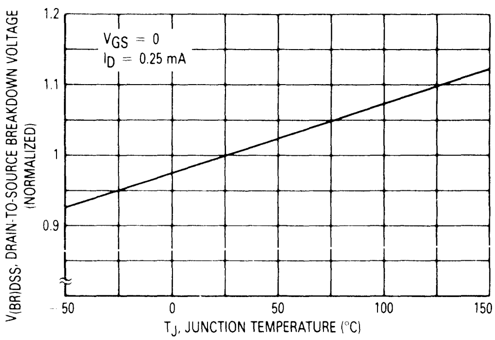


Figure 4. Breakdown Voltage Variation With Temperature

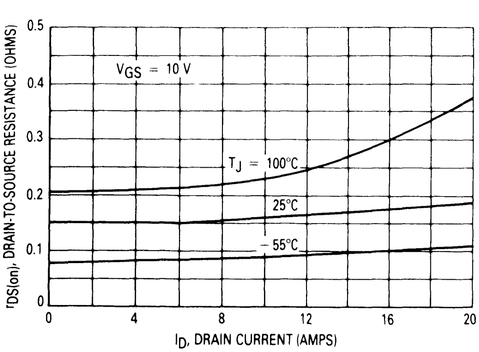


Figure 5. On-Resistance versus Drain Current

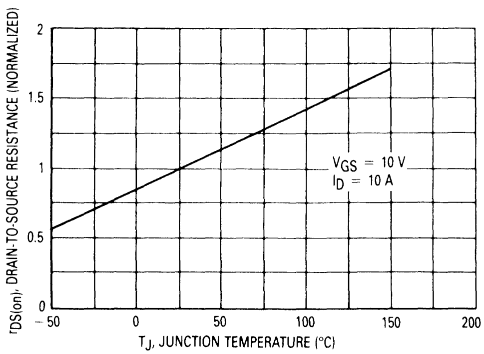


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

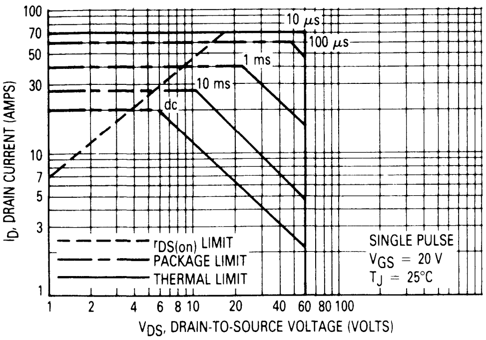


Figure 7. Maximum Rated Forward Biased Safe Operating Area

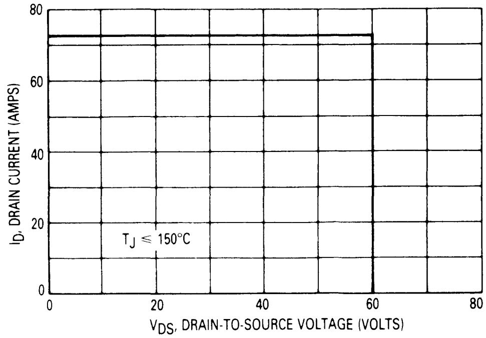


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

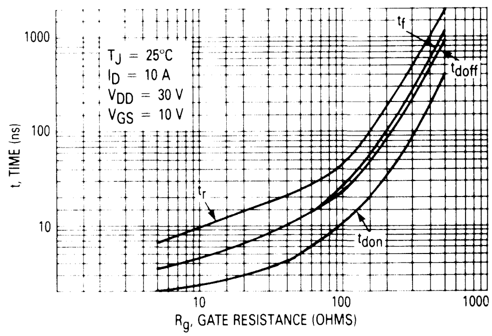


Figure 9. Resistive Switching Time Variation versus Gate Resistance

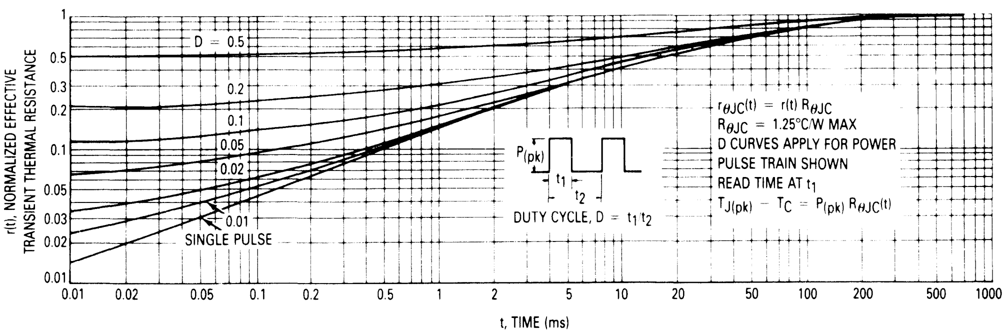


Figure 10. Thermal Response

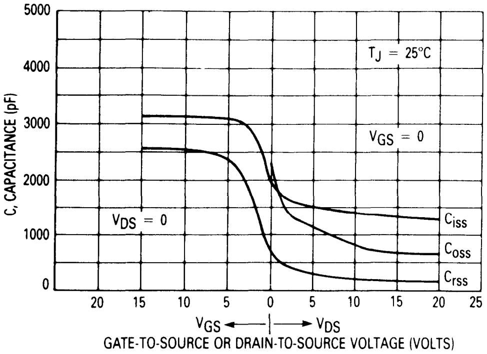


Figure 11. Capacitance Variation

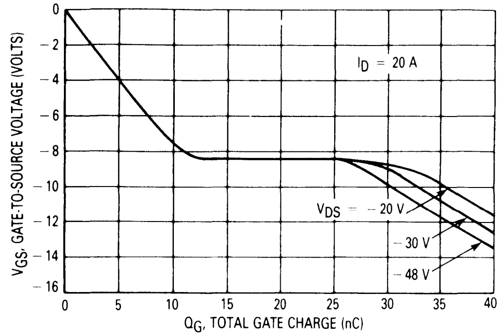


Figure 12. Gate Charge versus Gate-To-Source Voltage

RESITIVE SWITCHING

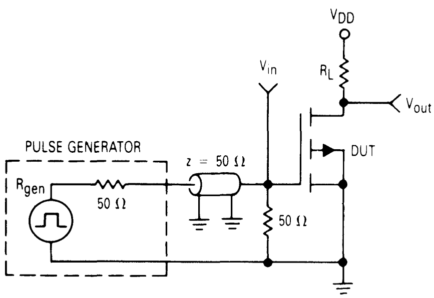


Figure 13. Switching Test Circuit

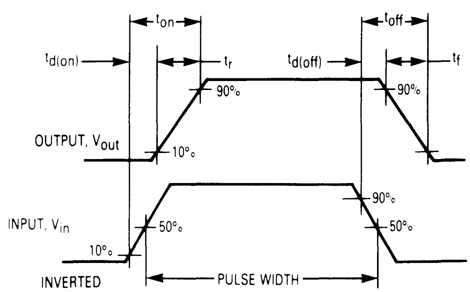
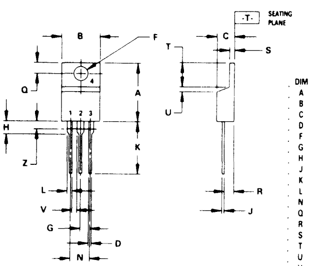


Figure 14. Switching Waveforms

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

STYLE 5
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

Designer's Data Sheet

TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

MTP25N05E

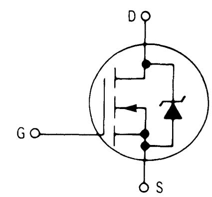
TMOS POWER FETs
25 AMPERES
$r_{DS(on)}$ = 0.07 OHM
50 VOLTS

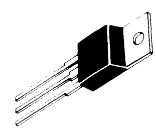
3

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS™





CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 80	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 100	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA, T_J = 100°C)		$V_{GS(th)}$	2 1.5	4 3.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$r_{DS(on)}$	—	0.07	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 25 Adc) (I_D = 12.5 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2 1	Vdc
Forward Transconductance (V_{DS} = 1.75 V, I_D = 16 A)		g_{FS}	9	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15 (I_D = 80 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 25 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 10 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		W_{DSR}	 — — —	 90 200 90	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	800	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 16 A R_{gen} = 15 ohms) See Figure 9	$t_{d(on)}$	—	25	ns
Rise Time		t_r	—	35	
Turn-Off Delay Time		$t_{d(off)}$	—	45	
Fall Time		t_f	—	35	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	26 (Typ)	30	nC
Gate-Source Charge		Q_{gs}	14 (Typ)	—	
Gate-Drain Charge		Q_{gd}	12 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 25 A V_{GS} = 0)	V_{SD}	1.3 (Typ)	1.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	160 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

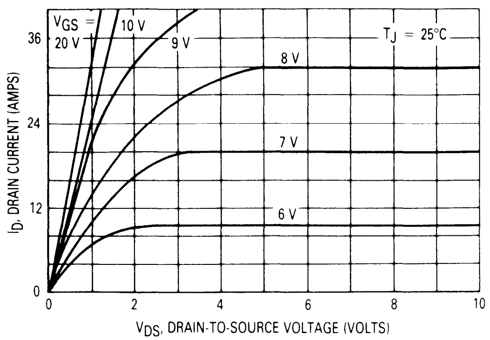


Figure 1. On-Region Characteristics

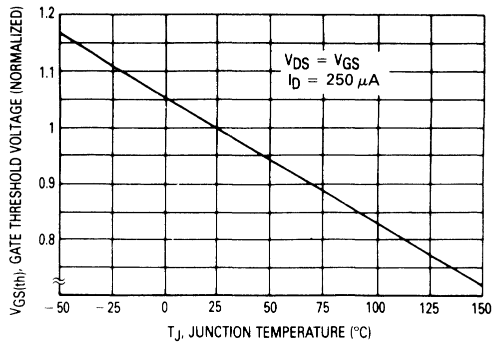


Figure 2. Gate-Threshold Voltage Variation With Temperature

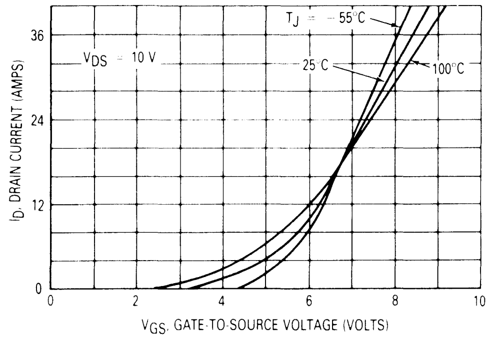


Figure 3. Transfer Characteristics

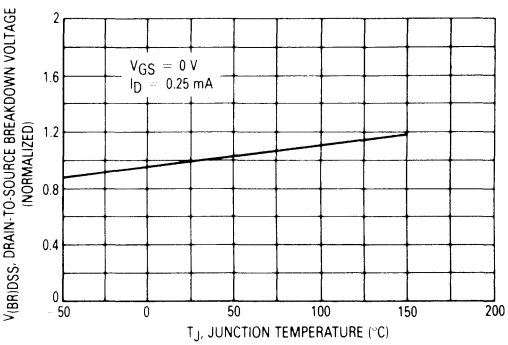


Figure 4. Breakdown Voltage Variation With Temperature

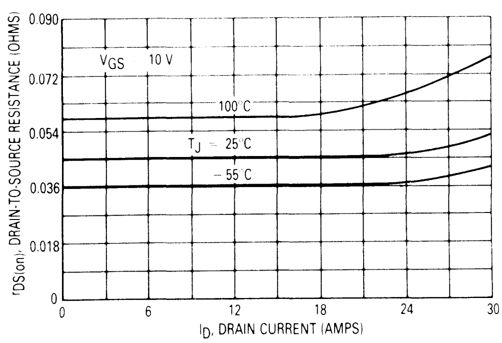


Figure 5. On-Resistance versus Drain Current

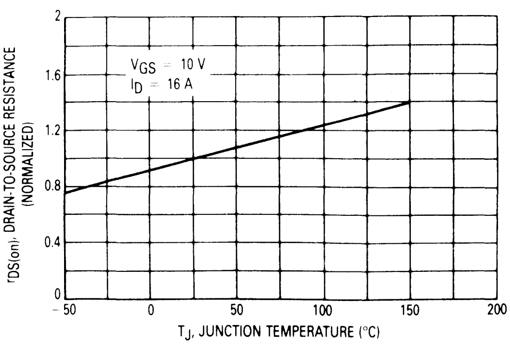


Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

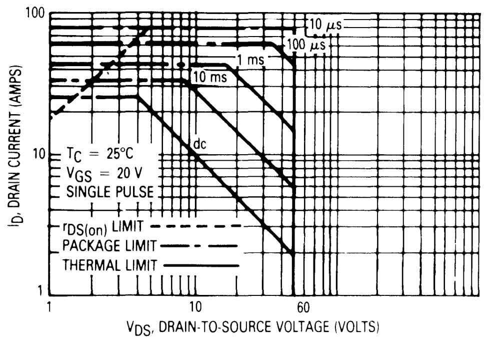


Figure 7. Maximum Rated Forward Biased Safe Operating Area

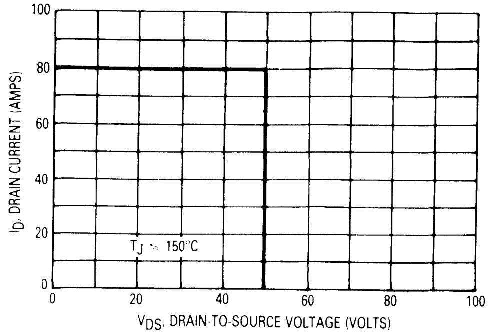


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

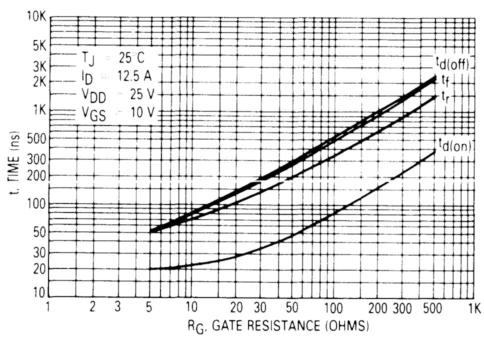


Figure 9. Resistive Switching Time Variation versus Gate Resistance

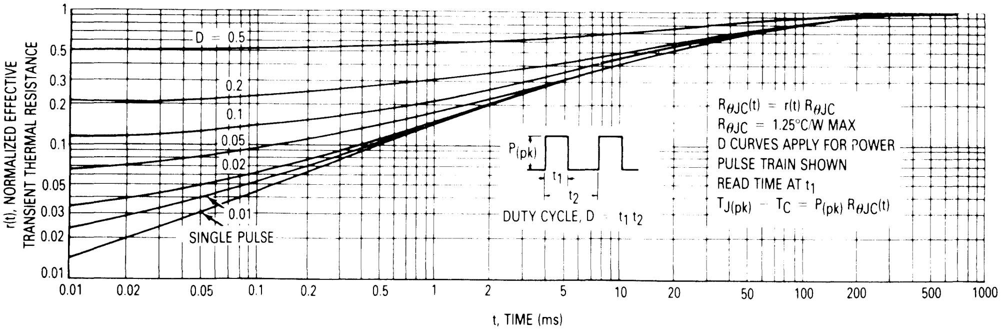


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

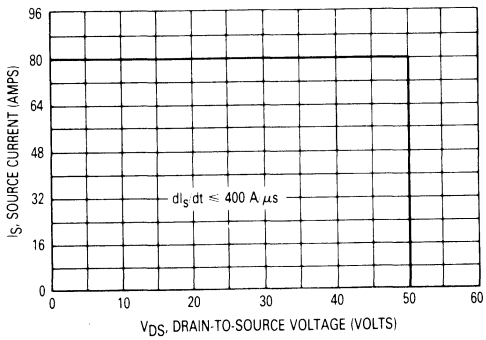


Figure 12. Commutating Safe Operating Area (CSOA)

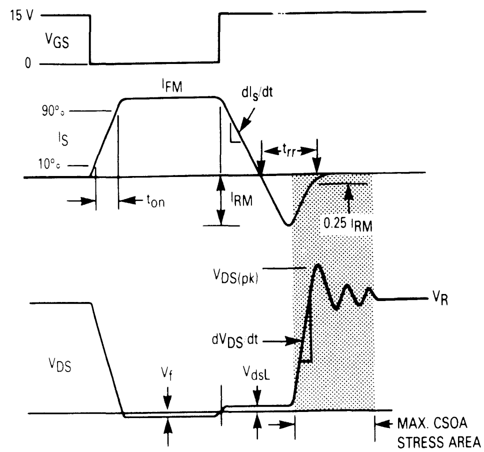


Figure 11. Commutating Waveforms

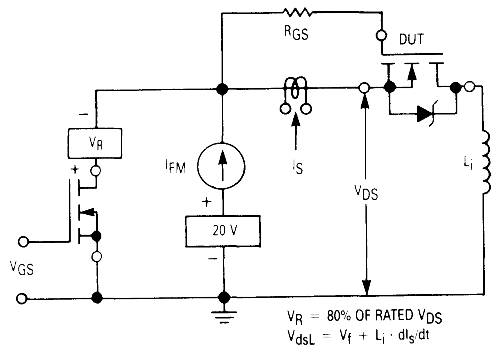


Figure 13. Commutating Safe Operating Area Test Circuit

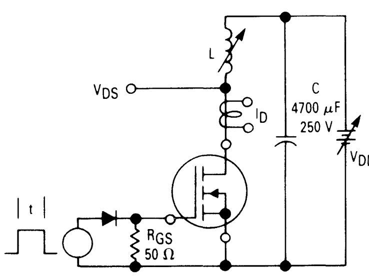
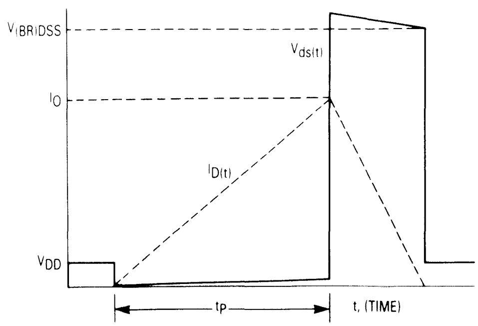


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

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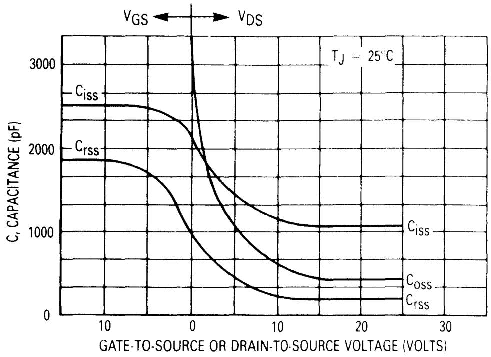


Figure 16. Capacitance Variation

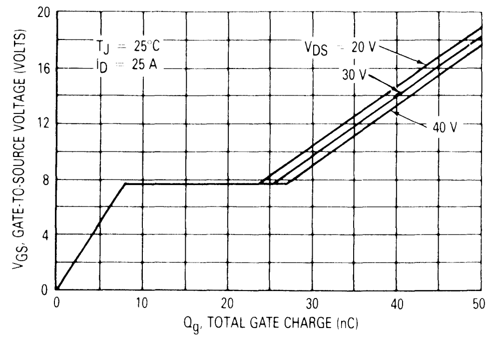
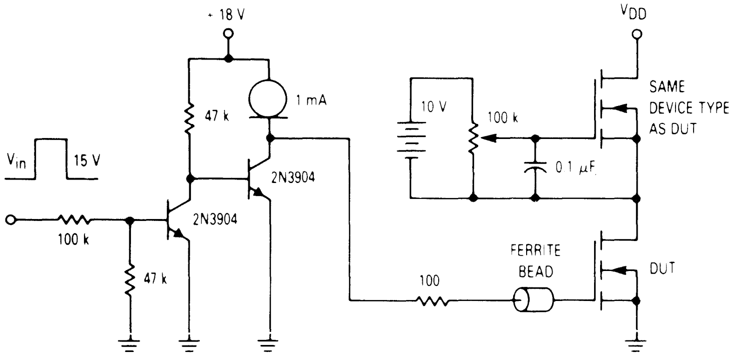


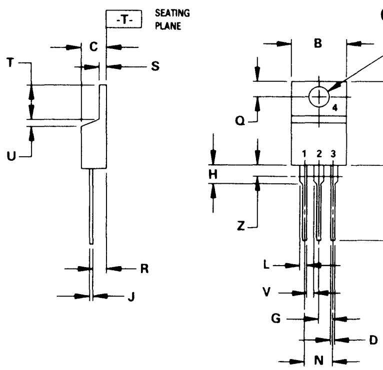
Figure 17. Gate Charge versus Gate-to-Source Voltage



$V_{in} = 15\ V_{pk}$; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



CASE 221A-04
TO-220AB

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MTP25N06E

Designer's Data Sheet

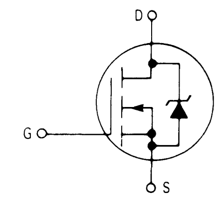
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

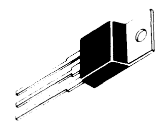
TMOS POWER FETs
25 AMPERES
$r_{DS(on)}$ = 0.08 OHM
60 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS™





CASE 221A-04
TO-220AB

3

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 80	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	100 0.8	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.25 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)			—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage		$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)			2	4.5	
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$r_{DS(on)}$	—	0.08	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 25 Adc)			—	2.4	
(I_D = 12.5 Adc, T_J = 100°C)			—	2	
Forward Transconductance (V_{DS} = 15 V, I_D = 12.5 A)		g_{FS}	6	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15		W_{DSR}			mJ
(I_D = 80 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive)			—	80	
(I_D = 25 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 70 μs, Duty Cycle ≤ 1%)			—	120	
(I_D = 10 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 60 μs, Duty Cycle ≤ 1%)			—	40	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	1000	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	200	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	30 (Typ)	50	nC
Gate-Source Charge		Q_{gs}	15 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.9	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

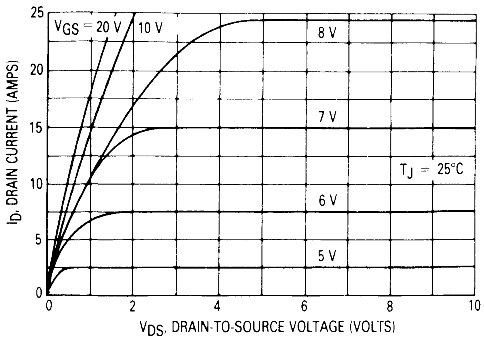


Figure 1. On-Region Characteristics

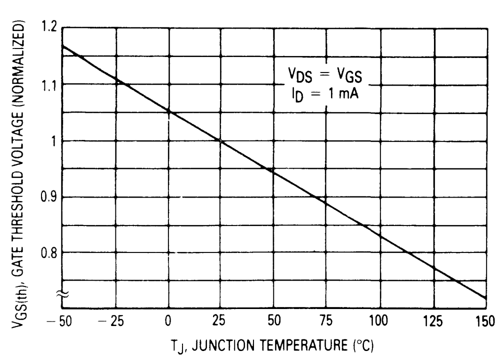


Figure 2. Gate-Threshold Voltage Variation With Temperature

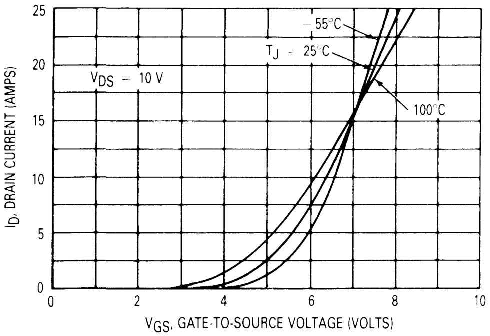


Figure 3. Transfer Characteristics

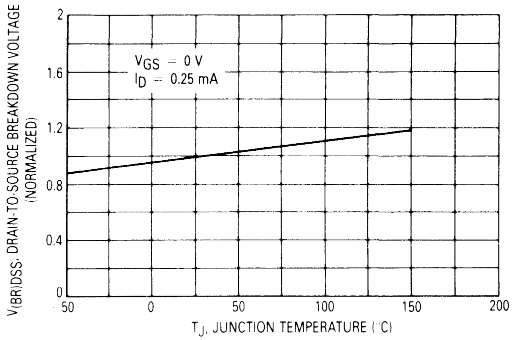


Figure 4. Breakdown Voltage Variation With Temperature

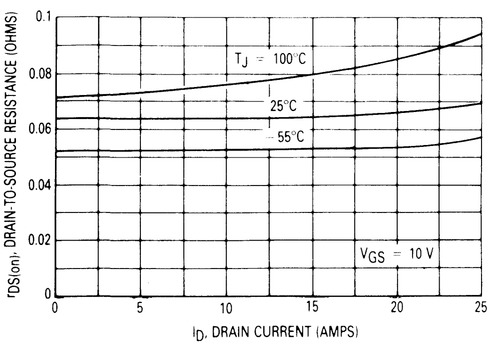


Figure 5. On-Resistance versus Drain Current

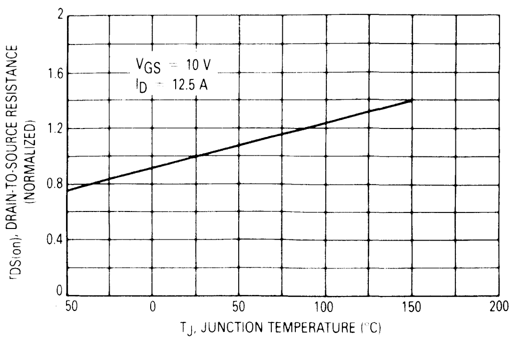


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

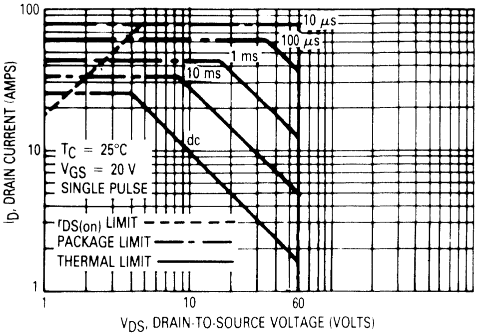


Figure 7. Maximum Rated Forward Biased Safe Operating Area

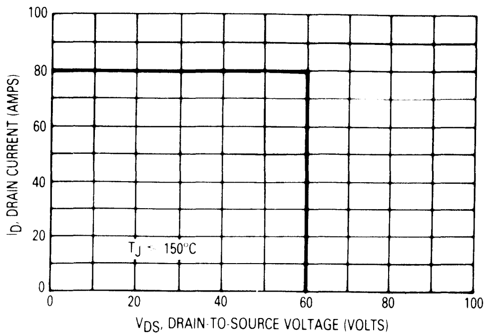


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

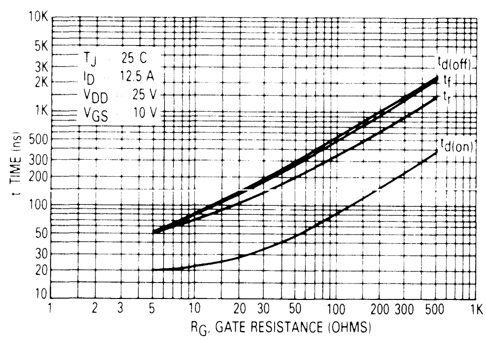


Figure 9. Resistive Switching Time Variation versus Gate Resistance

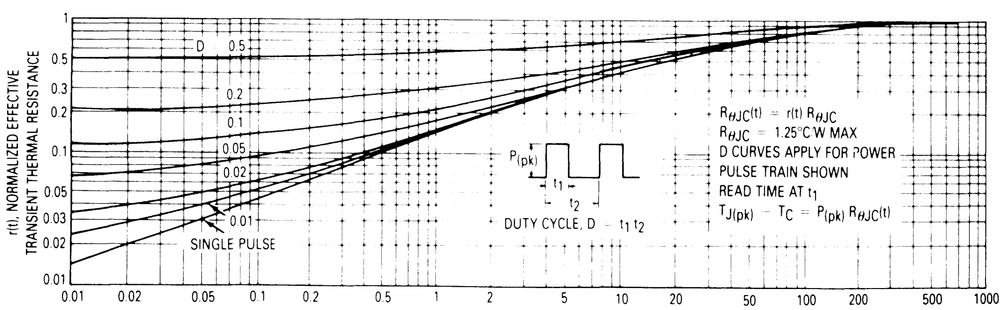


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

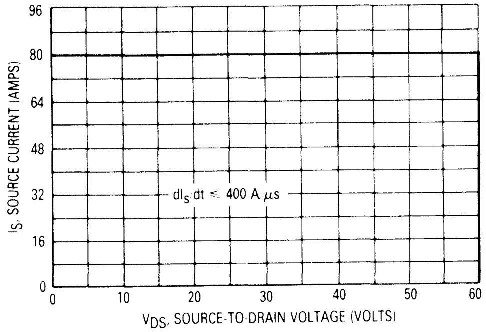


Figure 12. Commutating Safe Operating Area (CSOA)

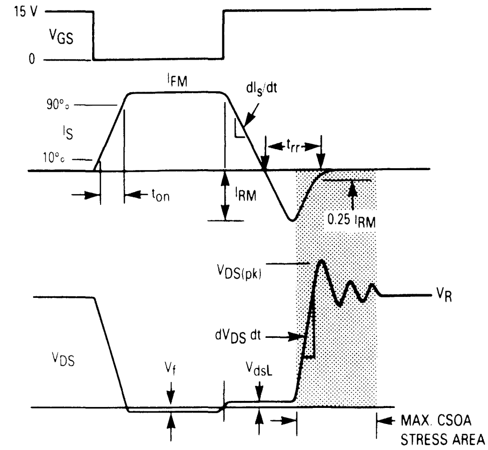


Figure 11. Commutating Waveforms

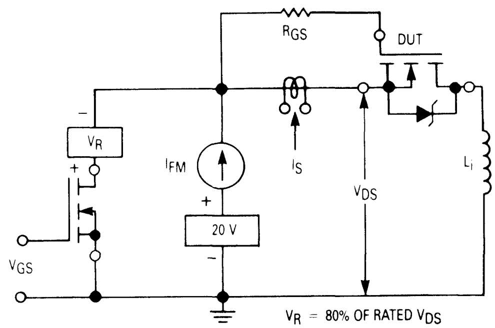


Figure 13. Commutating Safe Operating Area Test Circuit

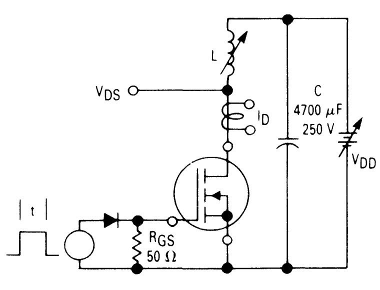
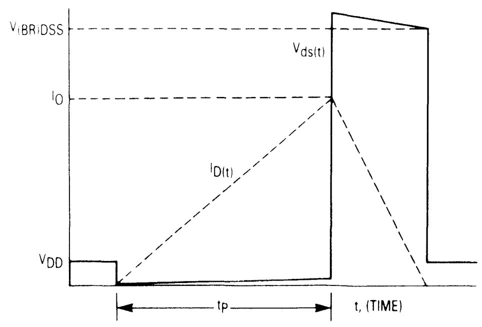


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

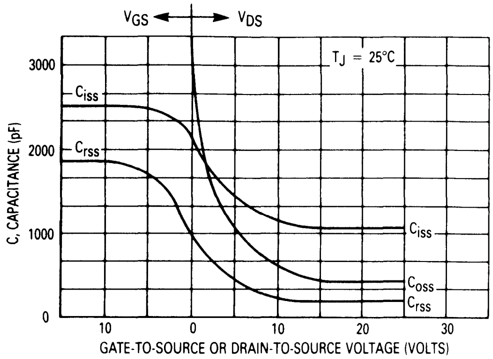


Figure 16. Capacitance Variation

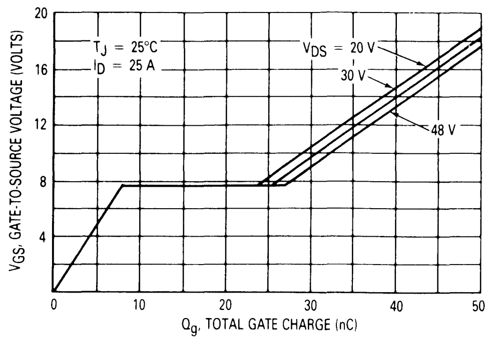
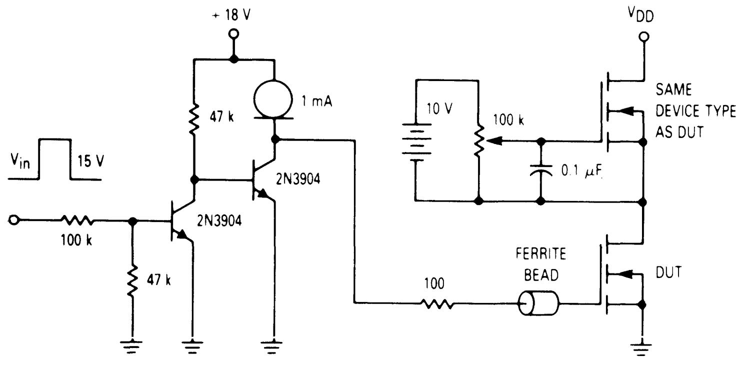


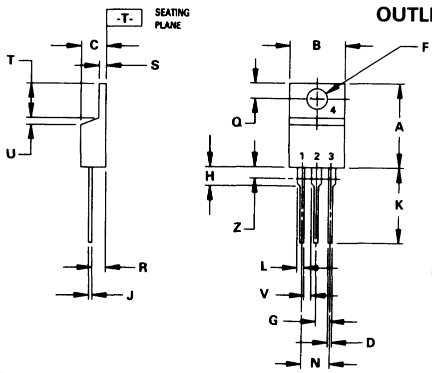
Figure 17. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



CASE 221A-04
TO-220AB

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MTP25N10

Designer's Data Sheet

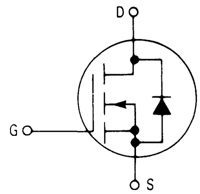
Power Field Effect Transistor

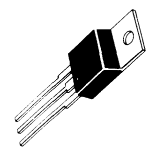
N-Channel Enhancement-Mode Silicon Gate TMOS

TMOS POWER FET
25 AMPERES
$r_{DS(on)}$ = 0.085 OHM
100 VOLTS

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 25 100	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}			μAdc
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage	$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1 mA)		2	4.5	
T_J = 100°C		1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)	$r_{DS(on)}$	—	0.085	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 25 Adc)		—	2.25	
(I_D = 12.5 Adc, T_J = 100°C)		—	1.8	
Forward Transconductance (V_{DS} = 10 V, I_D = 12.5 A)	g_{FS}	5	—	mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 4	C_{iss}	—	1600	pF
Output Capacitance		C_{oss}	—	800	
Reverse Transfer Capacitance		C_{rss}	—	300	

SWITCHING CHARACTERISTICS* (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 12.5 A, R_{gen} = 50 ohms) See Figures 11 and 12	$t_{d(on)}$	—	60	ns
Rise Time		t_r		450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	(V_{DS} = 80 V, I_D = 25 A, V_{GS} = 10 V) See Figures 6 and 9	Q_g	40 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	20 (Typ)	—	
Gate-Drain Charge		Q_{gd}	20 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = 25 A, V_{GS} = 0) See Figures 14 and 15	V_{SD}	1.5 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	50 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Characteristic	Symbol	Min	Max	Unit
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL CHARACTERISTICS

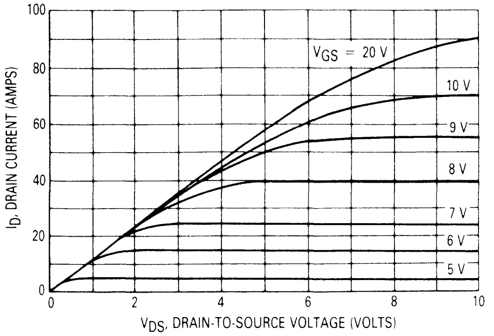


Figure 1. On-Region Characteristics

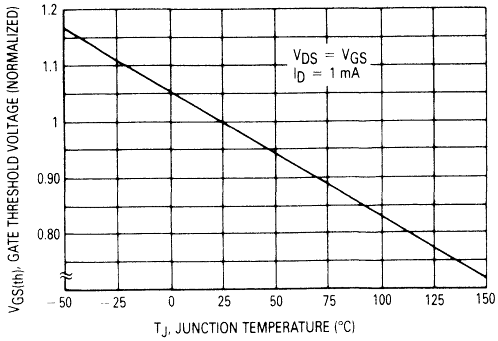


Figure 2. Gate-Threshold Voltage Variation With Temperature

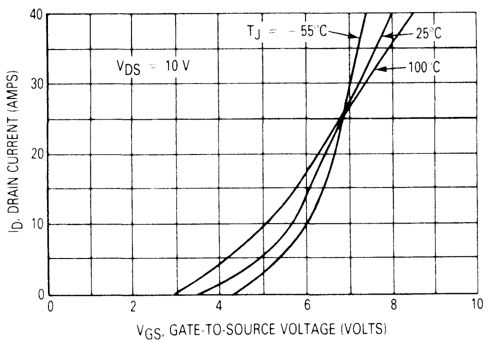


Figure 3. Transfer Characteristics

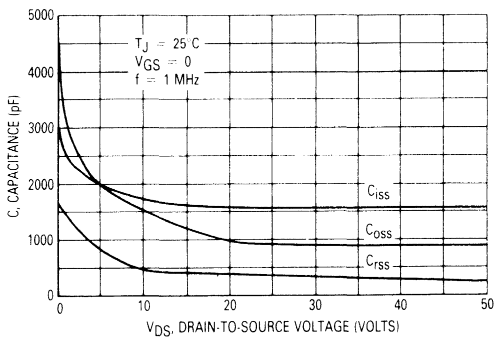


Figure 4. Capacitance Variation

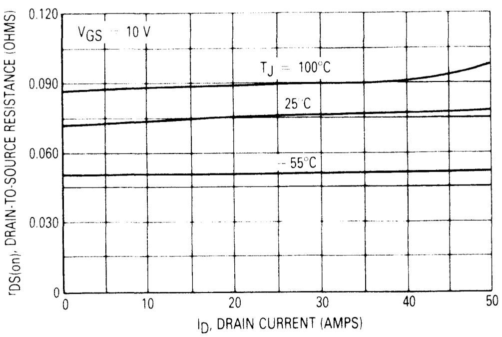


Figure 5. On-Resistance versus Drain Current

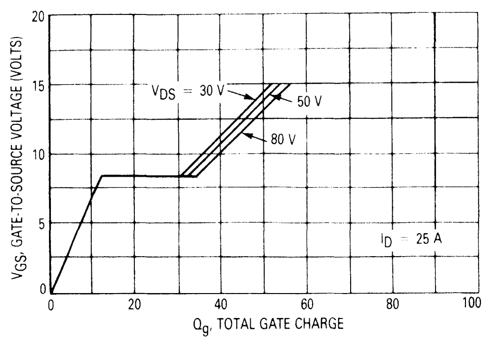


Figure 6. Gate Charge versus Gate-To-Source Voltage

SAFE OPERATING AREA INFORMATION

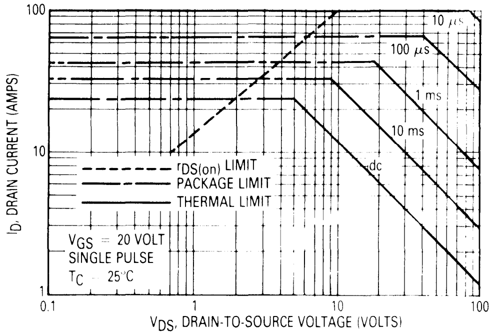


Figure 7. Maximum Rated Forward Biased Safe Operating Area

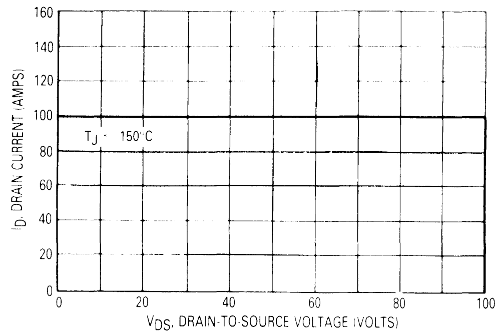


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

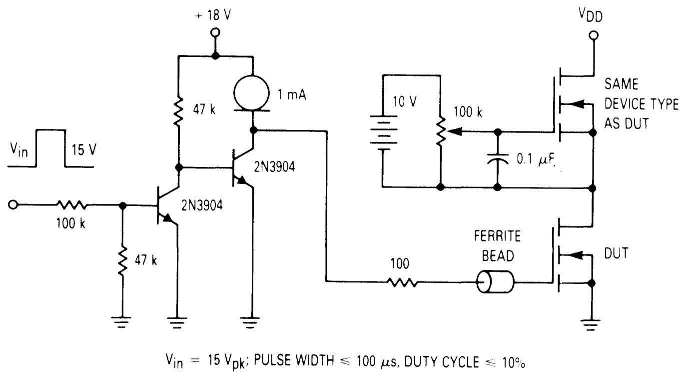
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 9. Gate Charge Test Circuit

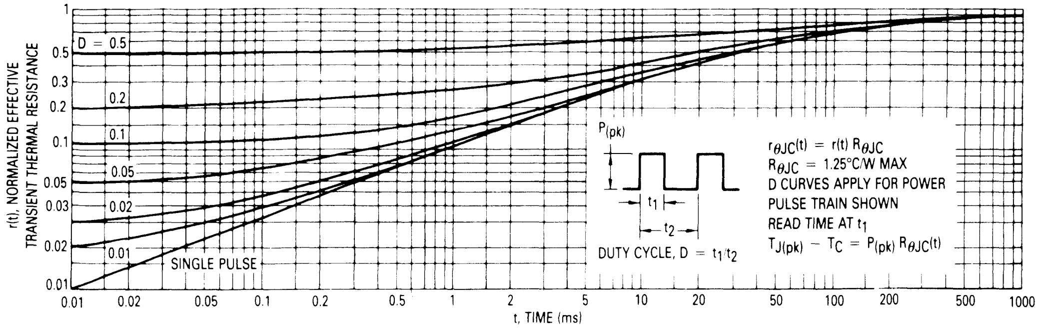


Figure 10. Thermal Response

RESISTIVE SWITCHING

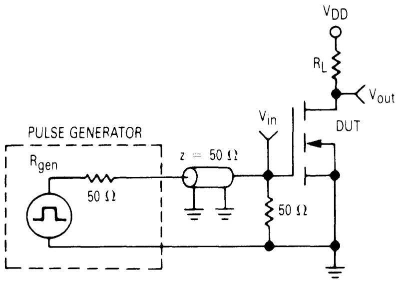


Figure 11. Switching Test Circuit

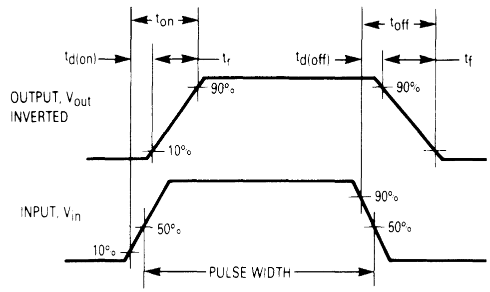
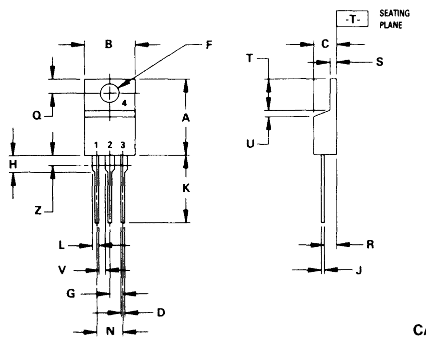


Figure 12. Switching Waveforms

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP25N10E

Designer's Data Sheet

TMOS IV

Power Field Effect Transistor

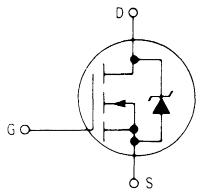
N-Channel Enhancement-Mode Silicon Gate

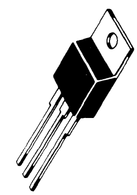
TMOS POWER FET
25 AMPERES
$r_{DS(on)}$ = 0.075 OHM
100 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	25 120	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 175	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_J \leq$ 175°C)

Single Pulse Drain-to-Source Avalanche Energy Repetitive Pulse Drain-to-Source Avalanche Energy	W_{DSS} (1) W_{DSS} (2) W_{DSR} (3)	850 200 15	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 25 V, I_D = 25 A, L = 2.1 mH, Initial T_C = 25°C
(2) V_{DD} = 25 V, I_D = 25 A, L = 500 μH, Initial T_C = 100°C
(3) f = 10 kHz

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	10 80	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$r_{DS(on)}$	—	0.075	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 25 Adc) (I_D = 12.5 Adc, T_J = 100°C)		$V_{DS(on)}$	— —	2.25 1.8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 12.5 A)		g_{FS}	10	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	800	
Reverse Transfer Capacitance		C_{rss}	—	300	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	65 (Typ)	90	nC
Gate-Source Charge		Q_{gs}	30 (Typ)	—	
Gate-Drain Charge		Q_{gd}	35 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D V_{GS} = 0)	V_{SD}	1.5 (Typ)	1.8	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	450 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	3.5 (Typ) 4.5 (Typ)	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

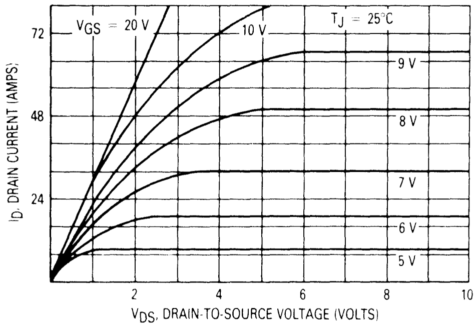


Figure 2. Gate Threshold Voltage Variation With Temperature

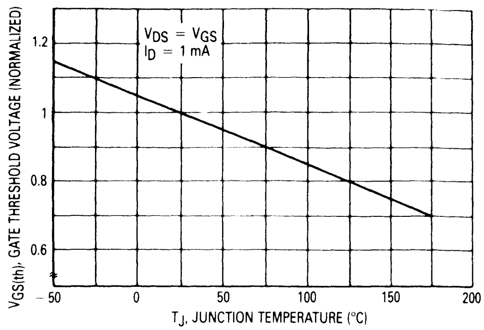


Figure 3. Transfer Characteristics

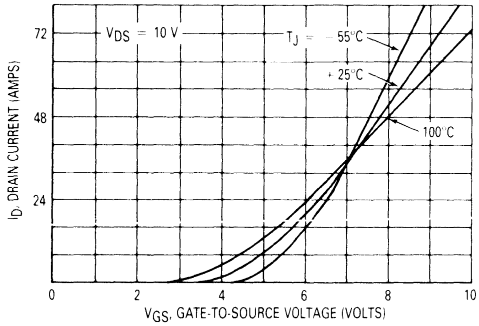


Figure 4. Breakdown Voltage Variation With Temperature

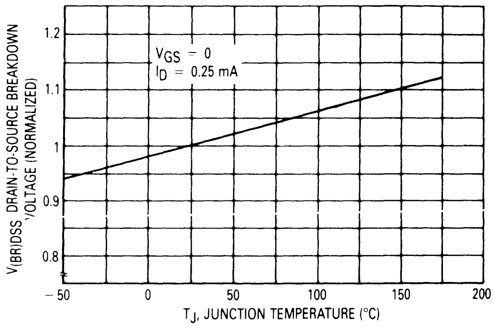


Figure 5. On-Resistance versus Drain Current

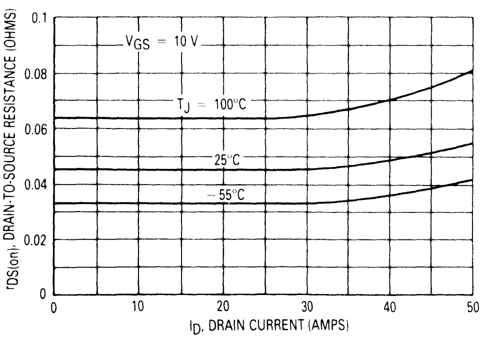
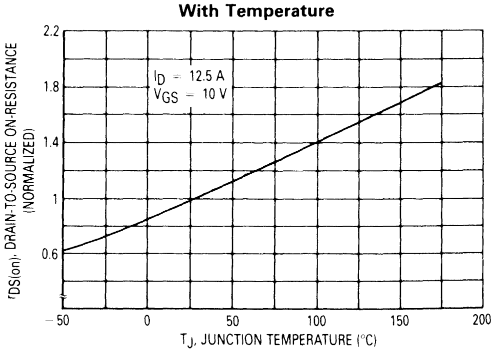


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

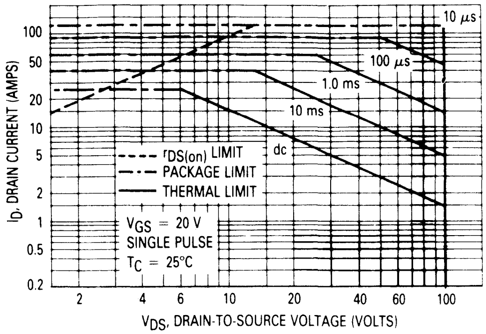


Figure 7. Maximum Rated Forward Biased Safe Operating Area

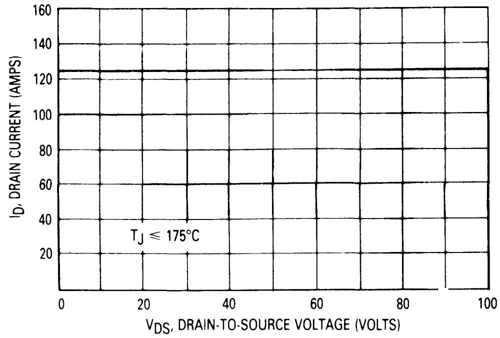


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

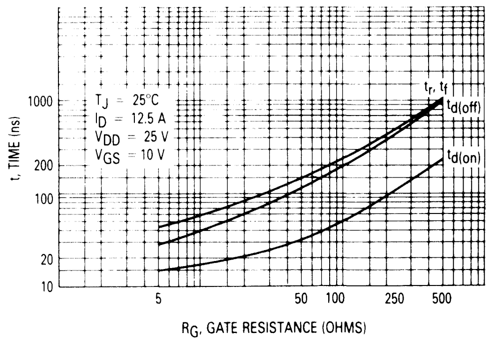
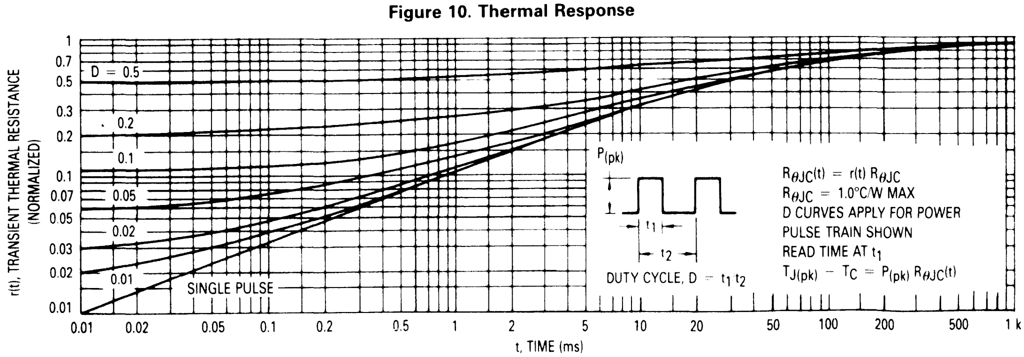


Figure 9. Resistive Switching Time Variation versus Gate Resistance

Figure 10. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

Figure 12. Commutating Safe Operating Area (CSOA)

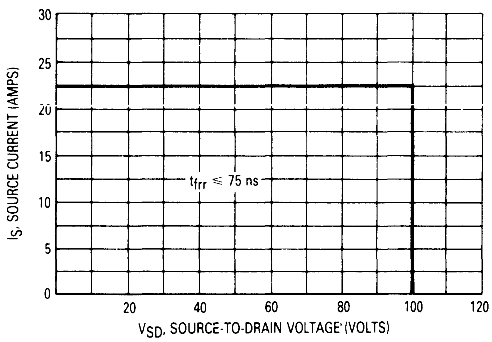


Figure 14. Unclamped Inductive Switching Test Circuit

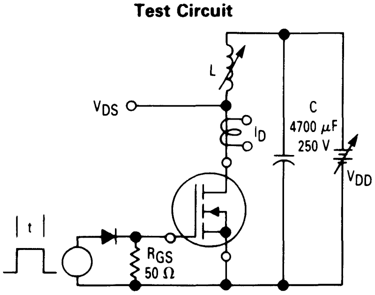


Figure 11. Commutating Waveforms

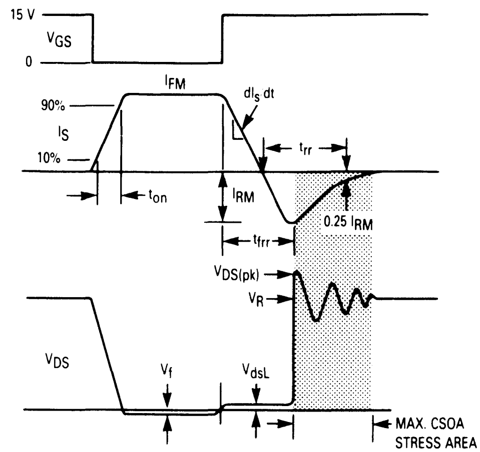


Figure 13. Commutating Safe Operating Area Test Circuit

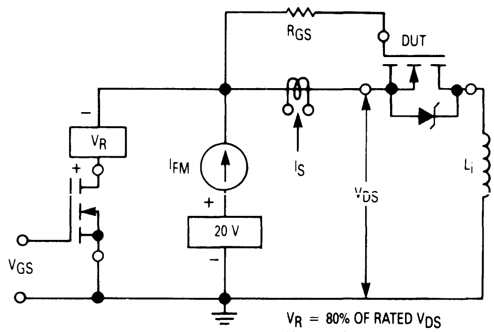
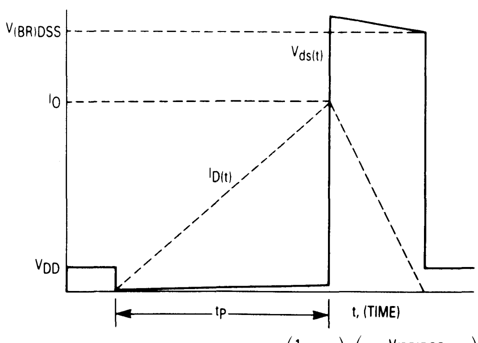


Figure 15. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 16. Capacitance Variation

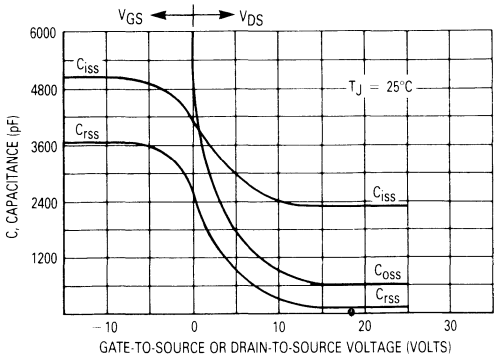


Figure 17. Gate Charge versus Gate-to-Source Voltage

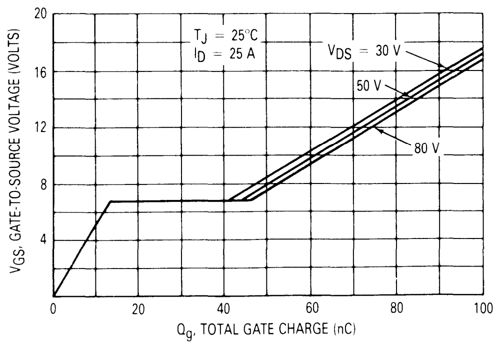
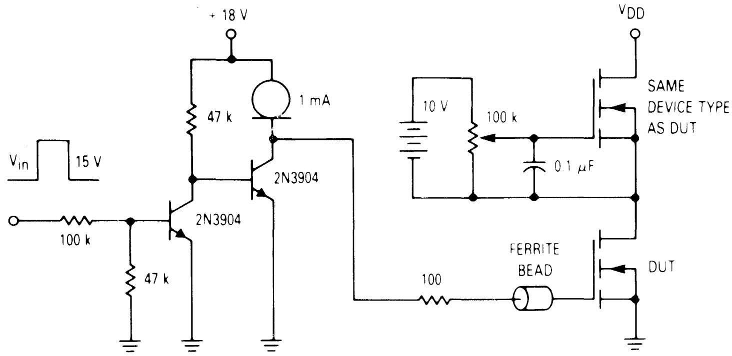
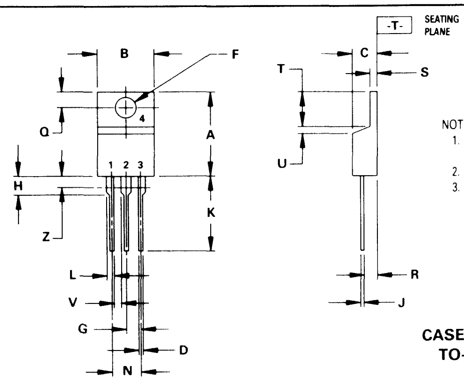


Figure 18. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP30N05E

Designer's Data Sheet

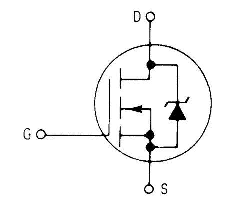
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

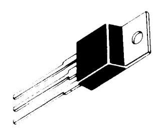
TMOS POWER FETs
30 AMPERES
$r_{DS(on)}$ = 0.05 OHM
50 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- Equivalent to IRFZ30

TMOS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leqq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 80	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current	I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)		—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		—	100	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μA)	$V_{GS(th)}$	2	4	Vdc
T_J = 100°C		1.5	3.5	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)	$r_{DS(on)}$	—	0.05	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)	$V_{DS(on)}$			Vdc
(I_D = 30 Adc)		—	1.65	
(I_D = 16 Adc, T_J = 100°C)		—	1.4	
Forward Transconductance (V_{DS} = 15 V, I_D = 16 A)	g_{FS}	9	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 14 and 15	W_{DSR}			mJ
(I_D = 80 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive)		—	90	
(I_D = 30 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)		—	180	
(I_D = 12 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)		—	70	
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	1600	pF
Output Capacitance	C_{oss}	—	800	
Reverse Transfer Capacitance	C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)				
Turn-On Delay Time (V_{DD} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 9	$t_{d(on)}$	—	25	ns
Rise Time	t_r	—	35	
Turn-Off Delay Time	$t_{d(off)}$	—	45	
Fall Time	t_f	—	35	
Total Gate Charge (V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	26 (Typ)	30	nC
Gate-Source Charge	Q_{gs}	14 (Typ)	—	
Gate-Drain Charge	Q_{gd}	12 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*				
Forward On-Voltage (I_S = 30 A, V_{GS} = 0)	V_{SD}	—	1.6	Vdc
Forward Turn-On Time	t_{on}	Limited by stray inductance		
Reverse Recovery Time	t_{rr}	160 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE				
Internal Drain Inductance	L_d			nH
(Measured from the contact screw on tab to center of die)		3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)		4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

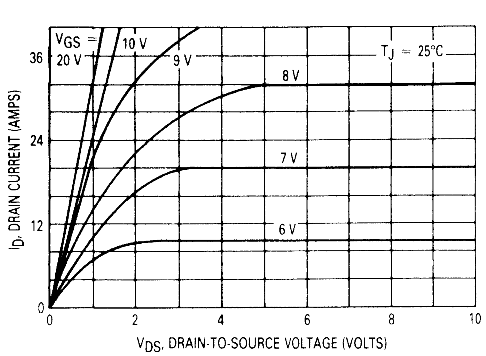


Figure 1. On-Region Characteristics

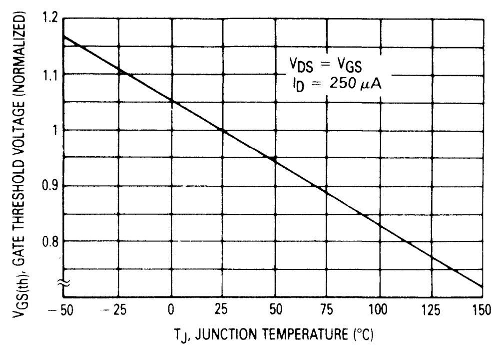


Figure 2. Gate-Threshold Voltage Variation With Temperature

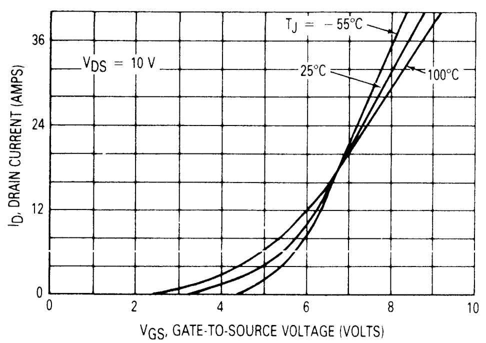


Figure 3. Transfer Characteristics

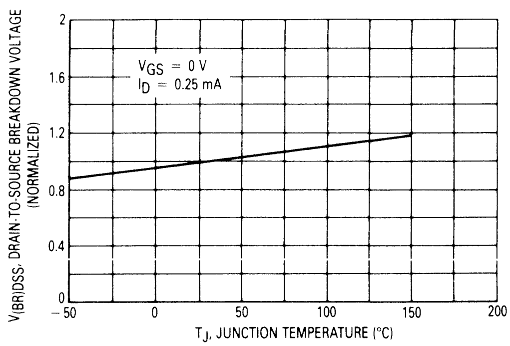


Figure 4. Breakdown Voltage Variation With Temperature

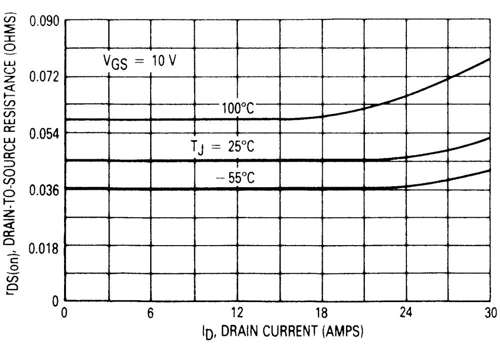


Figure 5. On-Resistance versus Drain Current

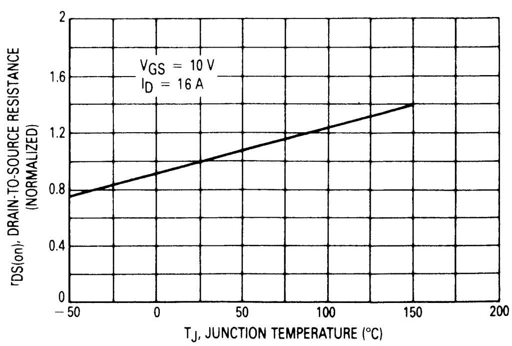


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

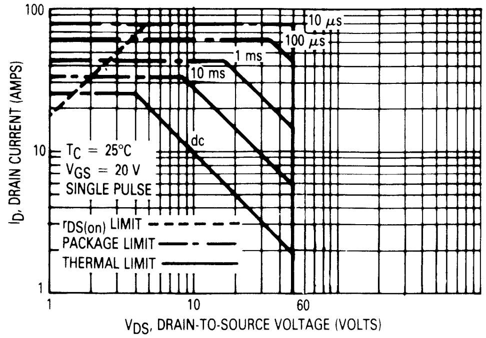


Figure 7. Maximum Rated Forward Biased Safe Operating Area

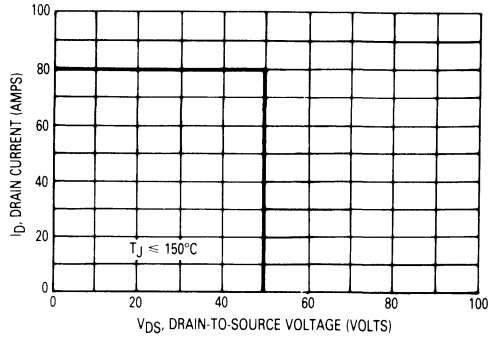


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

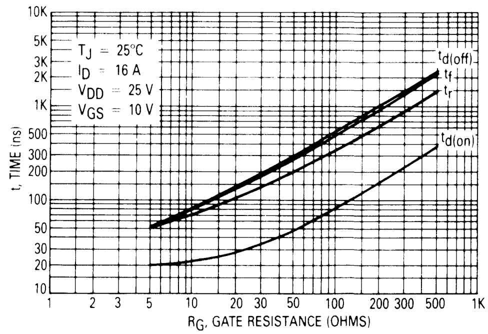


Figure 9. Resistive Switching Time Variation versus Gate Resistance

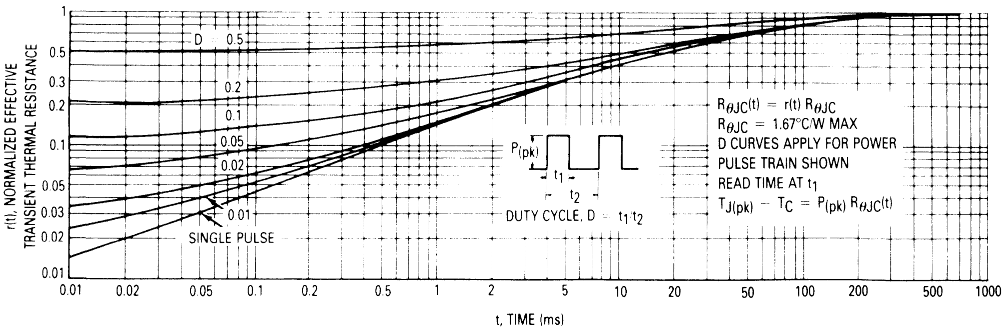


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

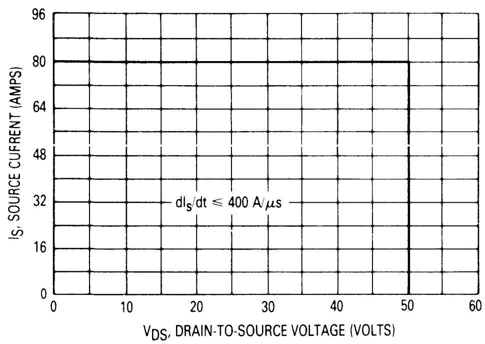


Figure 12. Commutating Safe Operating Area (CSOA)

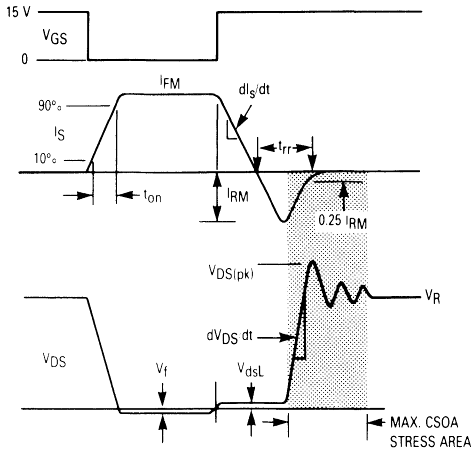


Figure 11. Commutating Waveforms

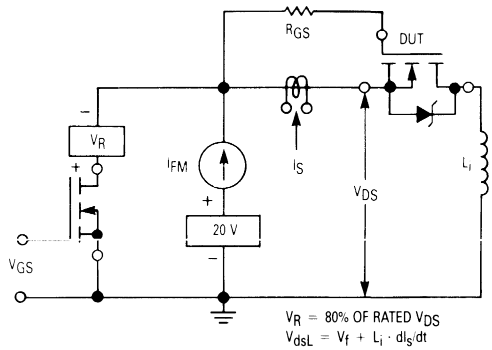


Figure 13. Commutating Safe Operating Area Test Circuit

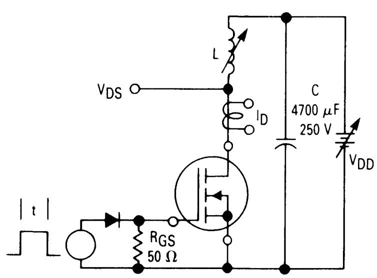


Figure 14. Unclamped Inductive Switching Test Circuit

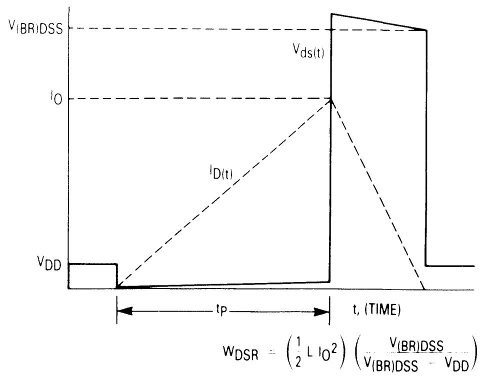


Figure 15. Unclamped Inductive Switching Waveforms

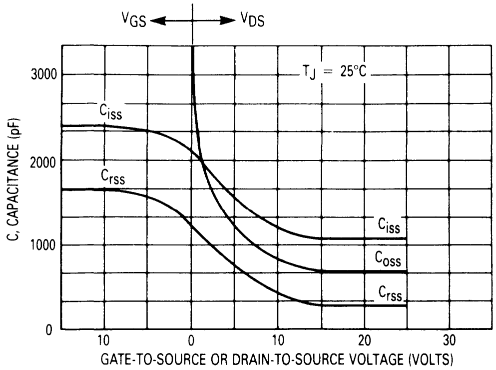


Figure 16. Capacitance Variation

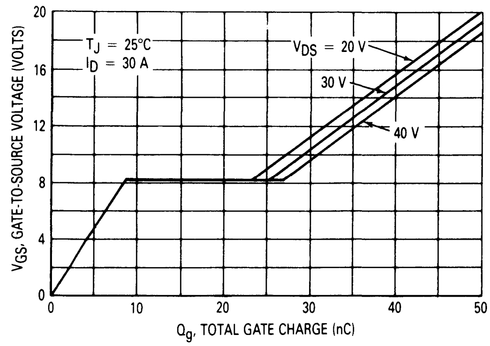
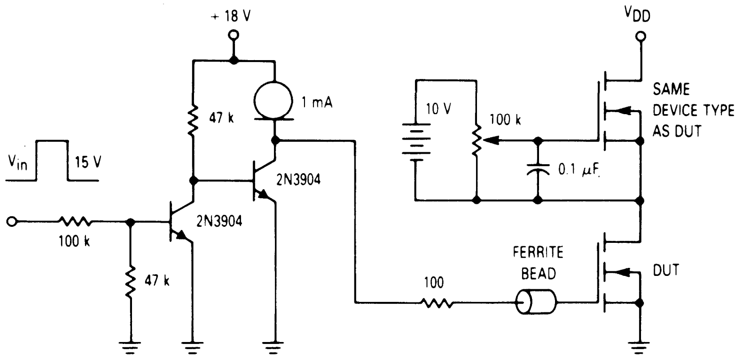


Figure 17. Gate Charge versus Gate-to-Source Voltage

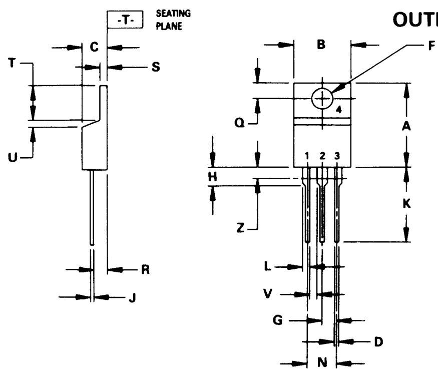
3



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



CASE 221A-04
TO-220AB

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP30N08M

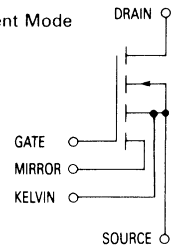
Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS with Current Sensing Capability

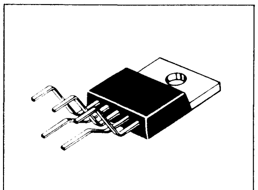
TMOS SENSEFET
30 AMPERES
$r_{DS(on)}$ = 0.065 OHM
80 VOLTS

This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with a minimum of power loss.

- "Lossless" Current Sensing for Maximum Efficiency
  — Sense Current is Reduced by a Factor of 900
- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy
- Rugged — SOA is Power Dissipation Limited
- Low $r_{DS(on)}$ — 0.065 Ohms Maximum



NOTES:
1. Handling precautions to protect against electrostatic discharge is mandatory.
2. Do not use the mirror FET independent of the power FET.
3. It is recommended that the mirror terminal (M) be shorted to the Kelvin Terminal (K) when current sensing is not required.



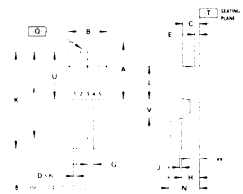
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	80	Vdc
Drain-to-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	80	Vdc
Gate-to-Source Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±20 ±40	Vdc
Drain-to-Mirror Voltage	V_{DMS}	80	Vdc
Gate-to-Mirror Voltage — Continuous — Non-Repetitive ($t_p \leq 50\ \mu s$)	V_{GM}	±20 ±40	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	30 90	Amps
Sense Current — Continuous — Pulsed	I_M I_{MM}	33 100	mA
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case Junction-to-Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

OUTLINE DIMENSIONS



NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH.

PIN 1. GATE
2. MIRROR
3. DRAIN
4. KELVIN
5. SOURCE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
F	21.590	23.749	0.850	0.935
G	1.702 BSC		0.067 BSC	
H	4.445	5.080	0.175	0.200
J	0.381	0.635	0.015	0.025
K	22.860	27.940	0.900	1.100
L	8.052	9.398	0.317	0.370
N	7.874	8.509	0.310	0.335
Q	3.556	3.937	0.140	0.155
U	11.888	12.827	0.468	0.505
V	4.699	5.842	0.185	0.230
W	2.286	2.794	0.090	0.110

CASE 314B-02

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{MK} = 0 unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	80	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 80 V, V_{GS} = 0) (V_{DS} = 80 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mAdc) (T_J = 125°C)		$V_{GS(th)}$	2 1.5	2.5 —	4 3.5	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$r_{DS(on)}$	—	0.05	0.065	Ohms
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc) (I_D = 30 A) (I_D = 15 A, T_J = 125°C)		$V_{DS(on)}$	— —	1.5 —	1.95 1.95	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 15 Adc)		g_{fs}	10	—	—	mhos
CURRENT SENSING CHARACTERISTICS						
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 15 A, V_{GS} = 10 V)		n	900	—	960	—
Mirror Compliance Ratio (V_{GS} = 10 Vdc, I_D = 15 Adc)		K_{mc}	—	0.65	—	—
Source Active Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc, R_S = 10 megohm)		$r_{a(on)}$	—	26	—	mΩ
Mirror Active Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$r_{m(on)}$	—	24	—	Ohms
DYNAMIC CHARACTERISTICS						
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	—	1800	pF
Output Capacitance		C_{oss}	—	—	900	
Transfer Capacitance		C_{rss}	—	—	400	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	V_{DD} = 30 V, I_D = 15 A, R_{gen} = 50 Ohms	$t_{d(on)}$	—	25	60	ns
Rise Time		t_r	—	110	200	
Turn-Off Delay Time		$t_{d(off)}$	—	120	200	
Fall Time		t_f	—	65	150	
Total Gate Charge	V_{DS} = 64 V, I_D = 30 A, V_{GS} = 10 V	Q_g	—	62	75	nC
Gate-Source Charge		Q_{gs}	—	8	—	
Gate-Drain Charge		Q_{gd}	—	35	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	I_S = 30 A	V_{SD}	—	1.6	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance			ns
Reverse Recovery Time		t_{rr}	—	200	—	

*Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

3

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

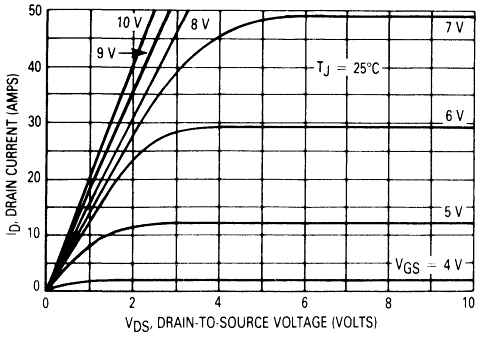


Figure 2. Gate Threshold Voltage Variation with Temperature

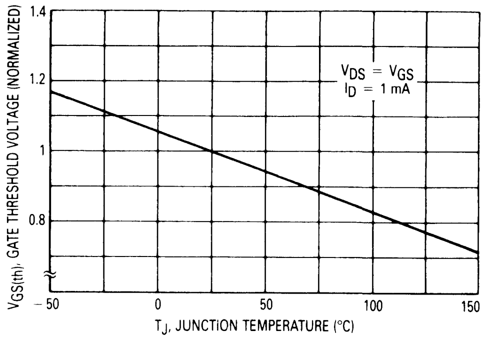


Figure 3. Transfer Characteristics

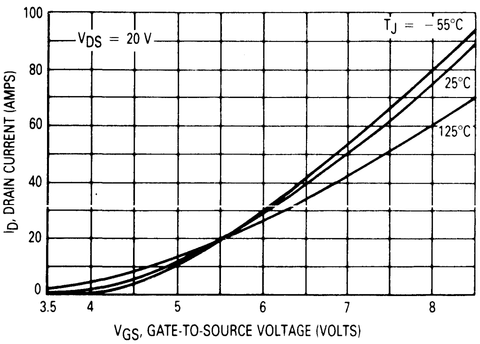


Figure 4. Stored Charge Variation

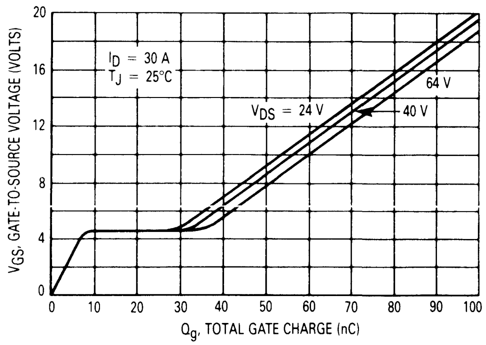


Figure 5. On-Resistance versus Drain Current

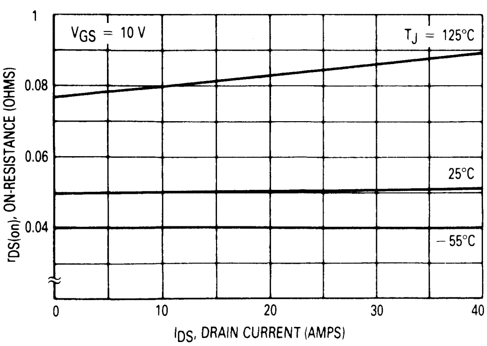
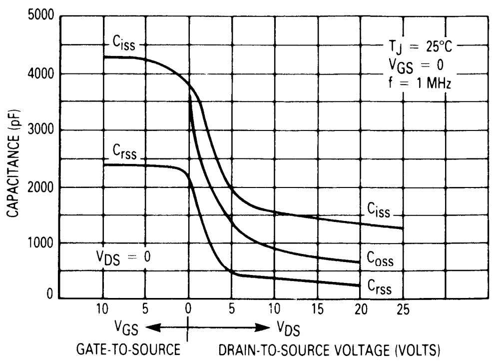
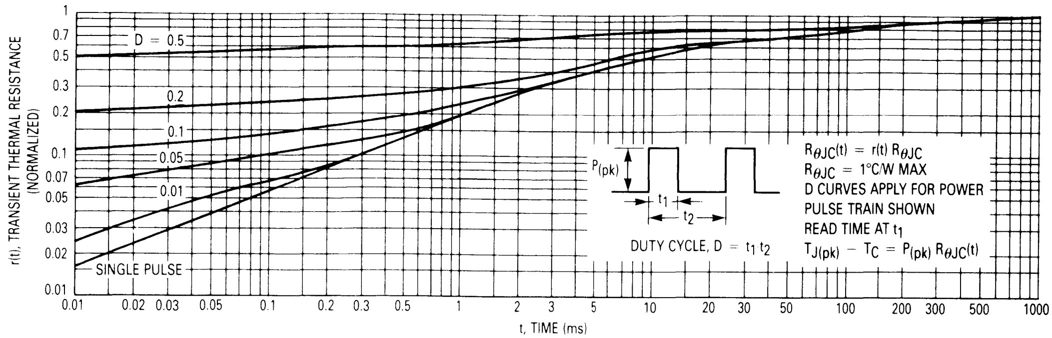


Figure 6. Capacitance Variation



TYPICAL CHARACTERISTICS

Figure 7. Thermal Response



SAFE OPERATING AREA INFORMATION

Figure 8. Maximum Rated Forward Biased Safe Operating Area

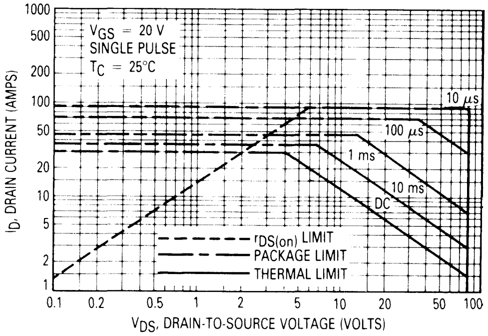
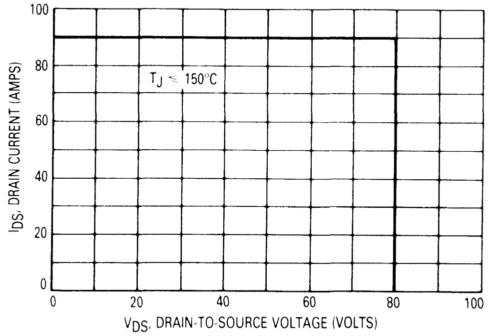


Figure 9. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

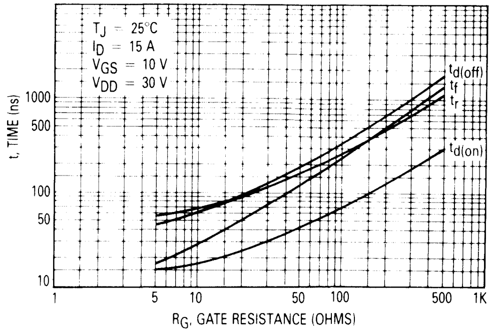
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 10. Resistive Switching Time Variation with Gate Resistance



SAFE OPERATING AREA INFORMATION

Figure 11. On-Resistance Variation with Temperature

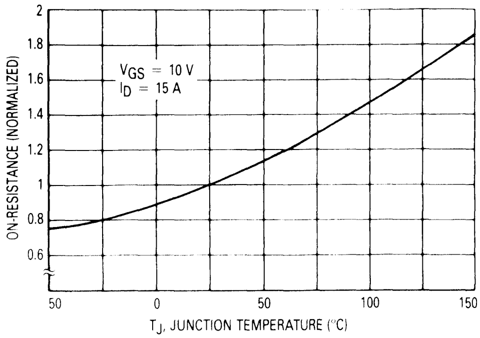


Figure 12. Breakdown Variation with Temperature

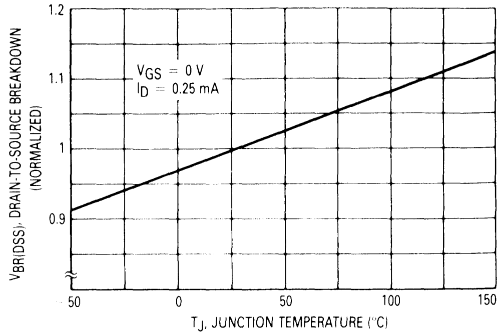


Figure 13. Sense Voltage Variation with Sense Resistance

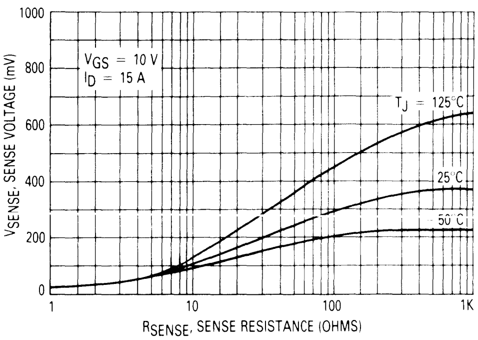


Figure 14. Sense Voltage Variation with Drain Current

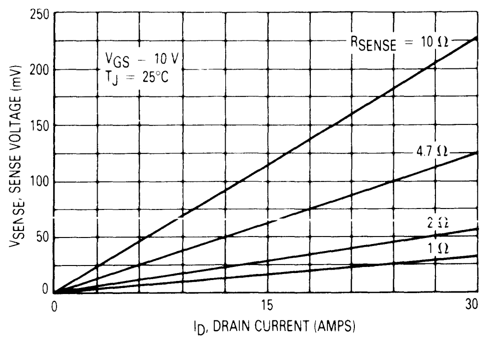


Figure 15. Sense Voltage Variation with Temperature

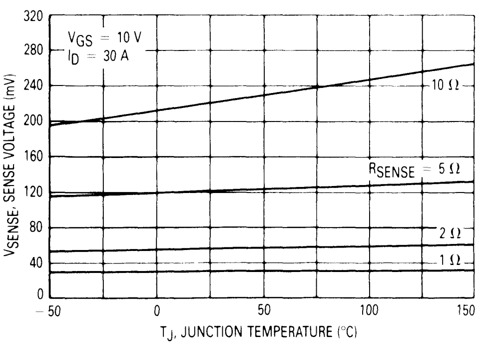


Figure 16. Sense Voltage Variation with Gate-to-Source Voltage

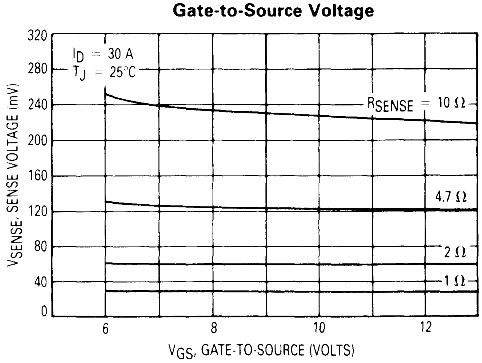


Figure 17. Current Mirror Ratio Variation with Drain Current

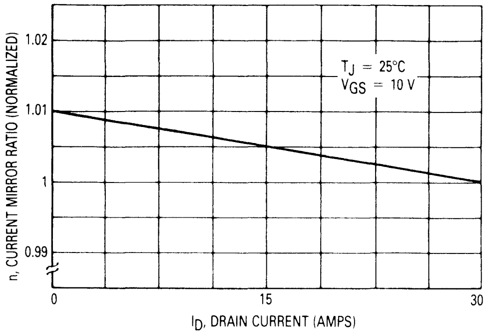


Figure 18. Current Mirror Ratio Variation with Gate-to-Source Voltage

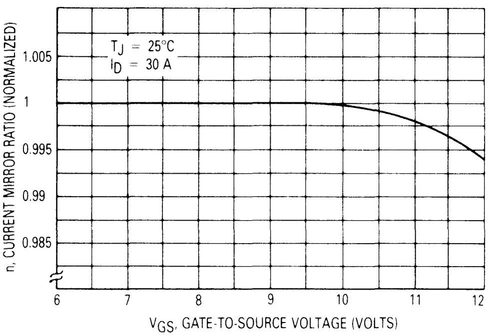
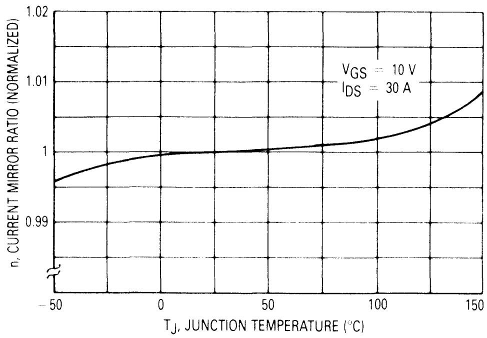


Figure 19. Current Mirror Ratio Variation with Temperature



LOSSLESS CURRENT SENSING

Assuming a fully switched on SENSEFET, current sensing can be modeled with the simple resistor divider network shown in Figure 20. In this model, r_b is the bulk drain resistance, $r_{m(on)}$ is the active mirror on-resistance, $r_{a(on)}$ is the power section's active on-resistance and r_w is the source wire bond resistance. Using values for $r_{a(on)}$ and $r_{m(on)}$ from the electrical characteristics table; V_{SENSE}, R_{SENSE}, and drain current may be calculated from the following sensing equations.

SENSING EQUATIONS:

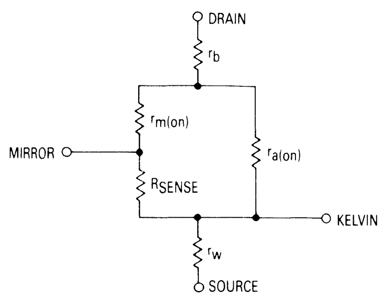
1. $V_{SENSE} = I_D\, r_{a(on)}\, R_{SENSE}/[R_{SENSE} + r_{m(on)}]$
2. $R_{SENSE} = V_{SENSE}\, r_{m(on)}/[I_D\, r_{a(on)} - V_{SENSE}]$
3. $I_D = V_{SENSE}\,(R_{SENSE} + r_{m(on)})/r_{a(on)}\, R_{SENSE}$
4. $n = I_D/I_{SENSE}$; where $R_{SENSE} = 0$
5. $r_{a(on)} = r_{m(on)}/n$

When using these equations there are several factors to keep in mind.

They are described as follows:

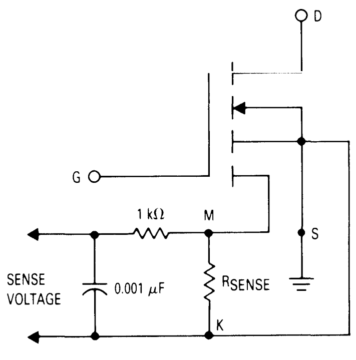
- Maximum Sense Voltage: The maximum sense voltage that can appear at the mirror terminal is $(r_{a(on)}/r_{a(on)} + r_b) \times V_{DS(on)}$. This ratio is called the mirror compliance ratio, K_{MC}, and defines the upper boundary for sense voltage.
- Accuracy: Accurate current sensing is based upon the inherent matching of $r_{m(on)}$ with the power section's active on-resistance, $r_{a(on)}$. When $R_{SENSE} = 0$, matching and current sensing accuracy are within ±3%. As R_{SENSE} is increased, sensing accuracy is reduced since mirror current becomes dependent on the ratio of internal on-resistance to an external R_{SENSE}. From a practical point of view, relatively good sensing accuracy (±10%) is maintained up to $R_{SENSE} = r_{m(on)}/2$. As R_{SENSE} is increased beyond $r_{m(on)}$, sensing accuracy decreases rapidly.

Figure 20. SENSEFET Model



- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop errors in this kind of an application is a first order design consideration. Internal wire bond resistance, contact resistance, and external wiring resistance are all significant. Therefore, it is important to reference sense voltage measurement circuitry to the Kelvin pin rather than power ground. In addition, referencing gate drive to the Kelvin pin rather than power ground will provide faster switching speeds.
- Noise Suppression: Switching noise is also a first order design issue. Layout, therefore, is critical. In addition, a single pole RC filter between R_{SENSE} and the current sensing circuitry's input terminals is often desirable. A 1 μsec time constant is generally long enough to provide adequate noise suppression and short enough to provide adequate protection during overloads. An illustration is provided in Figure 21.
- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET is likely due to excessive power dissipation. By syncing current limiting to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Parasitic Diode: In addition to the power section's usual source-drain diode, there is a mirror-drain diode in the sense cells. Like the source-drain diode, the mirror-drain diode conducts during the reverse-mode operation, however, current sense characteristics are defined only in the forward-mode operation.
- Reverse Recovery: In bridge circuits, when a SENSEFET's source-drain diode is commutated a voltage spike is produced at the mirror. This spike is short since it lasts only for the drain-source diode's reverse recovery time. However, its amplitude can be an order of magnitude larger than normal sense voltages and produce unwanted overcurrent trips. Blanking, filtering, or other suppression techniques may be required in some applications.

Figure 21. SENSEFET with Noise Suppression



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP35N06E

Designer's Data Sheet

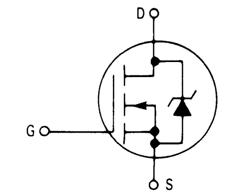
TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER FET
35 AMPERES
$r_{DS(on)}$ = 0.055 OHM
60 VOLTS

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

TMOS™



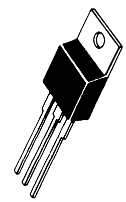
3

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq$ 50 μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	35 120	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C



CASE 221A-04
TO-220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)			—	10	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)			—	80	
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	4.5	Vdc
T_J = 100°C			1.5	4	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 17.5 Adc)		$r_{DS(on)}$	—	0.055	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 35 Adc)			—	2.3	
(I_D = 17.5 Adc, T_J = 100°C)			—	1.9	
Forward Transconductance (V_{DS} = 15 V, I_D = 17.5 A)		g_{FS}	14	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Inductive Switching Energy See Figures 14 and 15		W_{DSR}			mJ
(I_D = 120 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non-repetitive)			—	80	
(I_D = 35 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 70 μs, Duty Cycle ≤ 1%)			—	175	
(I_D = 14 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 60 μs, Duty Cycle ≤ 1%)			—	65	
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 16	C_{iss}	—	3000	pF
Output Capacitance		C_{oss}	—	1500	
Reverse Transfer Capacitance		C_{rss}	—	500	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D R_{gen} = 50 ohms) See Figure 9	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	450	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	300	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	60 (Typ)	90	nC
Gate-Source Charge		Q_{gs}	33 (Typ)	—	
Gate-Drain Charge		Q_{gd}	35 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 35 A V_{GS} = 0) dI_S/dt = 100 A/μs	V_{DS}	1.7 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	200 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance		L_d			nH
(Measured frrom the contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

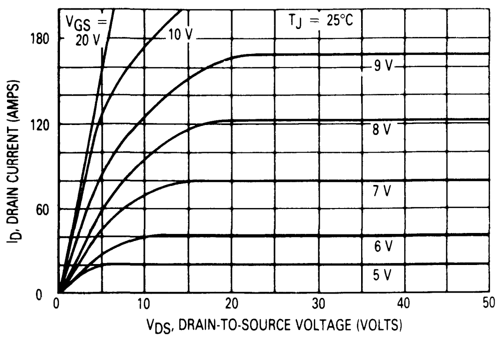


Figure 1. On-Region Characteristics

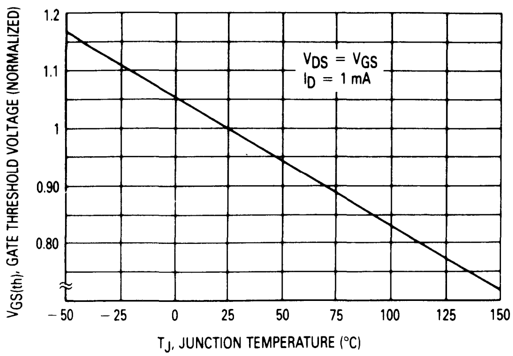
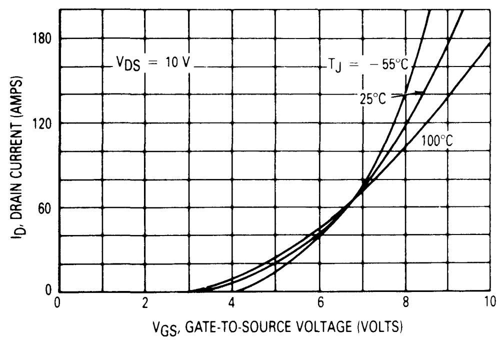


Figure 2. Gate-Threshold Voltage Variation With Temperature



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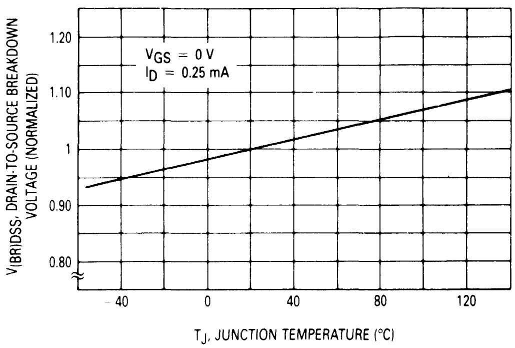

Figure 4. Breakdown Voltage Variation With Temperature

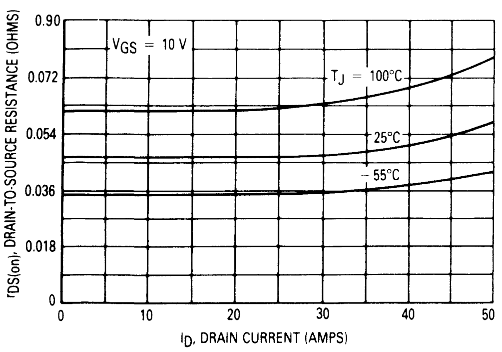

Figure 5. On-Resistance versus Drain Current

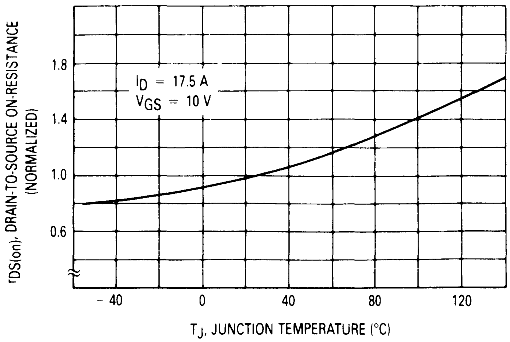

Figure 6. On-Resistance Variation With Temperature

3

SAFE OPERATING AREA INFORMATION

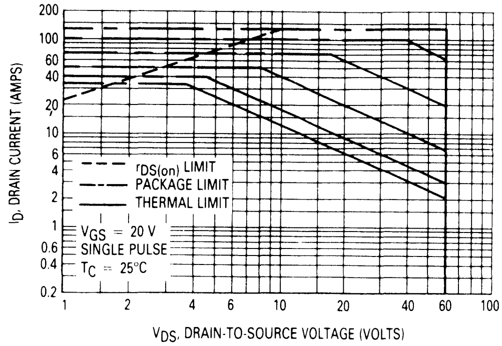

Figure 7. Maximum Rated Forward Biased Safe Operating Area

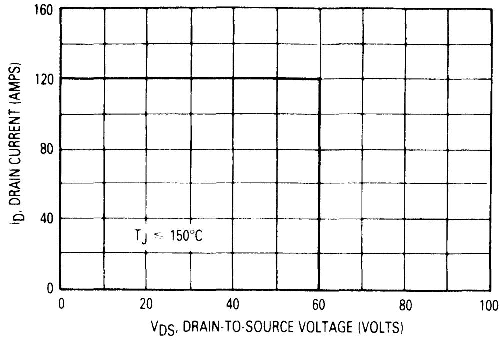

Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

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The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

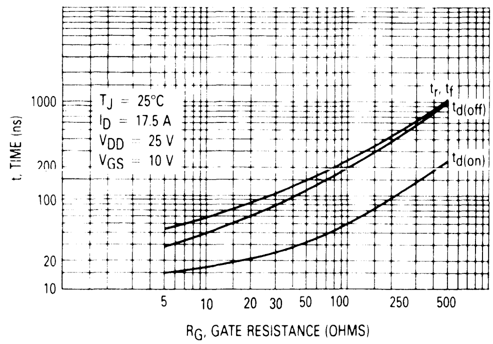


Figure 9. Resistive Switching Time Variation versus Gate Resistance

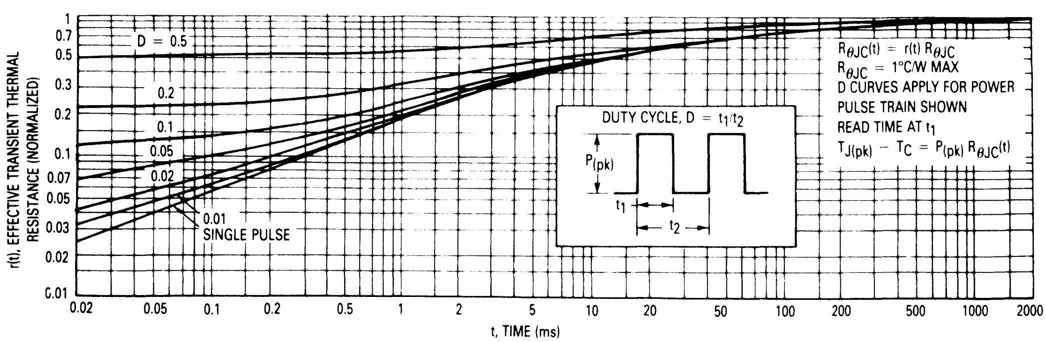


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

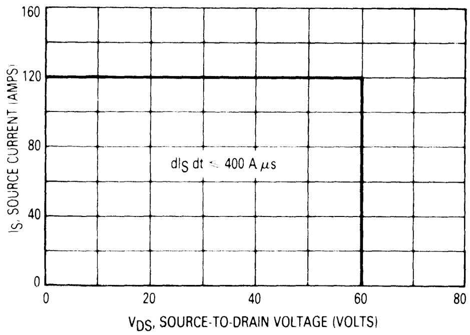


Figure 12. Commutating Safe Operating Area (CSOA)

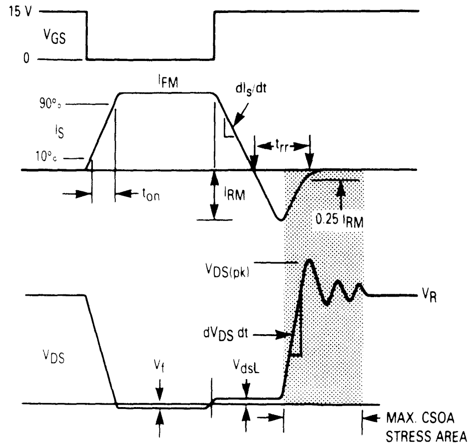


Figure 11. Commutating Waveforms

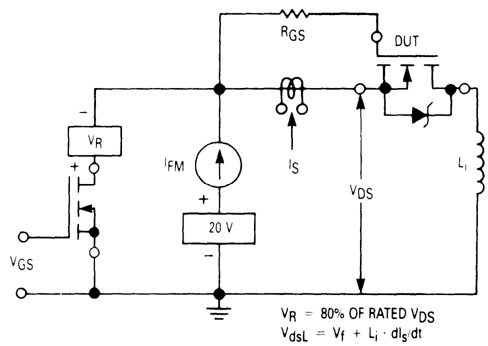


Figure 13. Commutating Safe Operating Area Test Circuit

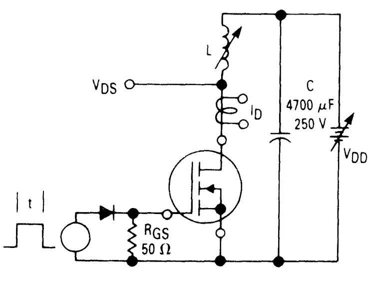
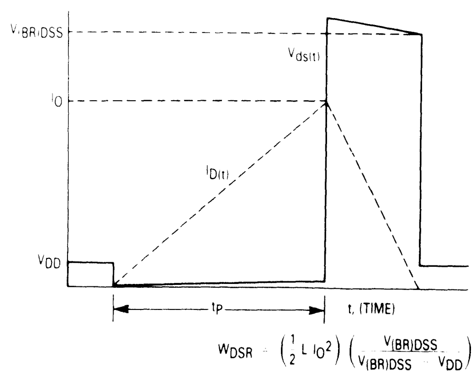


Figure 14. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Unclamped Inductive Switching Waveforms

3

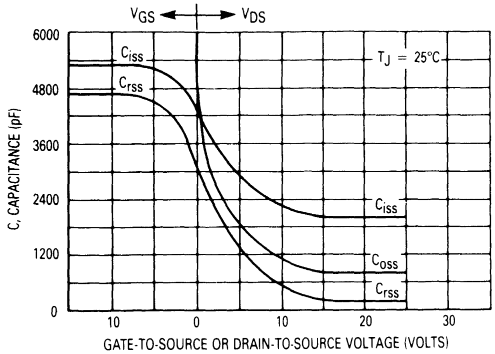


Figure 16. Capacitance Variation

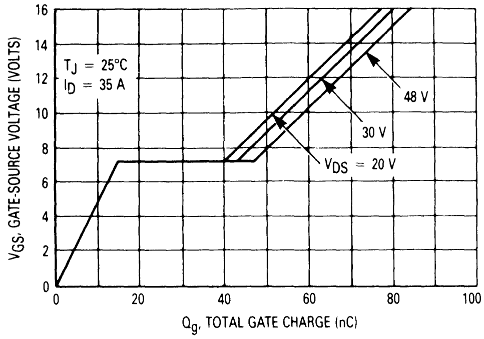
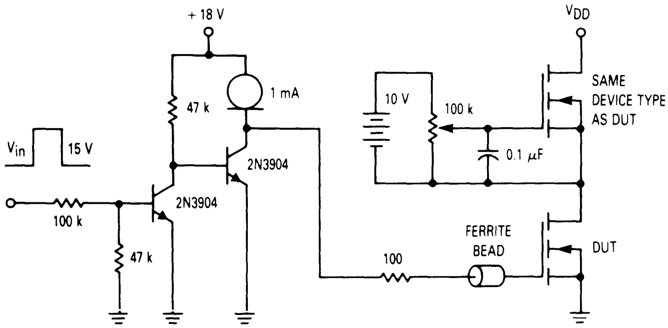


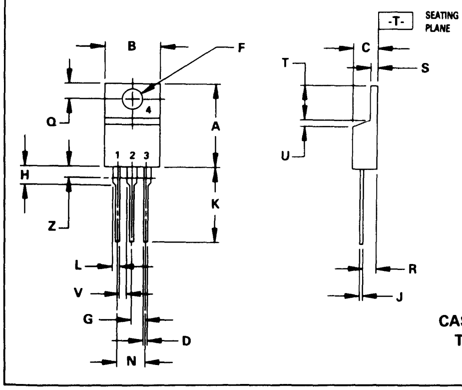
Figure 17. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet

Logic Level TMOS (L^2TMOS) E-FET Power Field Effect Transistor

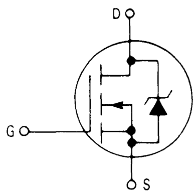
N-Channel Enhancement-Mode Silicon Gate

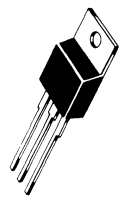
MTP40N06EL

TMOS POWER FET
LOGIC LEVEL
40 AMPERES
$r_{DS(on)}$ = 0.04 OHM
60 VOLTS

This advanced E-FET is an L^2TMOS power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5.0 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2.0 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A-04
TO-220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Pulsed	V_{GS}	±15 ±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	40 130	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 175	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 175°C)

Single Pulse Drain-to-Source Avalanche Energy Repetitive Pulse Drain-to-Source Avalanche Energy	W_{DSS} (1) W_{DSS} (2) W_{DSR} (3)	250 62 15	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 25 V, I_D = 40 A, L = 180 μH, Initial T_C = 25°C
(2) V_{DD} = 25 V, I_D = 40 A, L = 180 μH, Initial T_C = 100°C
(3) f = 10 kHz

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = 60 V, V_{GS} = 0)			—	1.0	
(V_{DS} = 60 V, V_{GS} = 0, T_J = 125°C)			—	50	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage		$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1.0 mA)			1.0	2.0	
T_J = 150°C			0.75	1.75	
Static Drain-Source On-Resistance (V_{GS} = 5.0 Vdc, I_D = 20 Adc)		$r_{DS(on)}$	—	0.04	Ohm
Drain-Source On-Voltage (V_{GS} = 5.0 V)		$V_{DS(on)}$			Vdc
(I_D = 40 Adc)			—	1.8	
(I_D = 20 Adc, T_J = 100°C)			—	1.3	
Forward Transconductance (V_{DS} = 5.0 V, I_D = 20 A)		g_{FS}	12	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{iss}	2500 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1.0 MHz See Figure 15		6100 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{rss}	115 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1.0 MHz See Figure 15		3200 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz See Figure 15	C_{oss}	750 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 20 A, V_{GS} = 5.0 V, R_{gen} = 50 Ohms, R_{GS} = 5.2 Ohms)	$t_{d(on)}$	26 (Typ)	—	ns
Rise Time		t_r	215 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	54 (Typ)	—	
Fall Time		t_f	112 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 40 A, V_{GS} = 5.0 Vdc) See Figures 16 and 17	Q_g	32 (Typ)	45	nC
Gate-Source Charge		Q_{gs}	8 (Typ)	—	
Gate-Drain Charge		Q_{gd}	18 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 40 A, V_{GS} = 0)	V_{SD}	1.2 (Typ)	1.45	Vdc
Forward Turn-On Time	(I_S = 40 A, V_{GS} = 0, dI_S/dt = 100 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	80 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

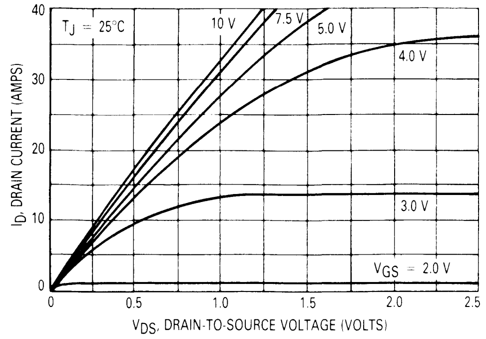


Figure 2. Gate-Threshold Voltage Variation With Temperature

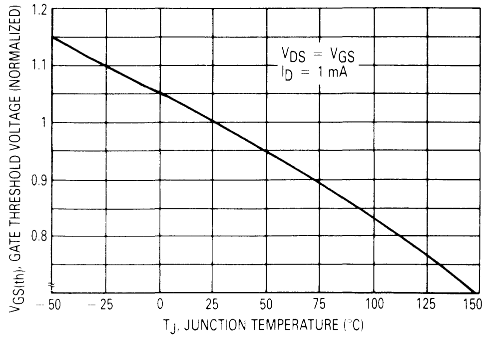


Figure 3. Transfer Characteristics

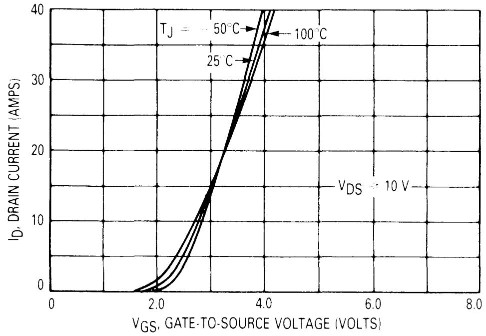


Figure 4. On-Resistance versus Drain Current

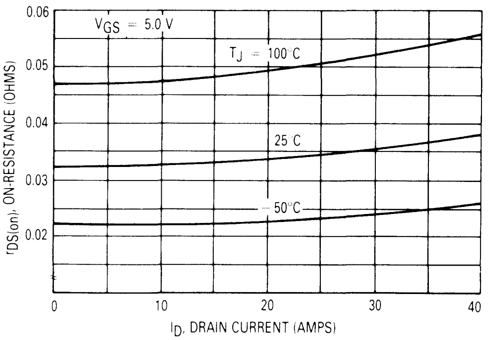


Figure 5. On-Resistance versus Gate-To-Source Voltage

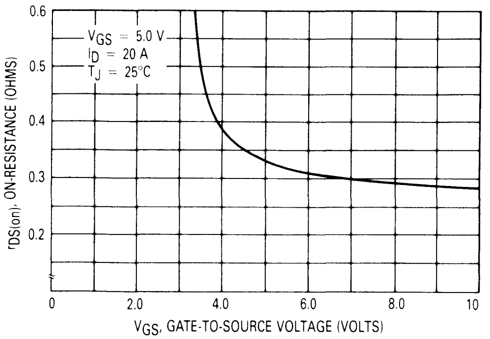
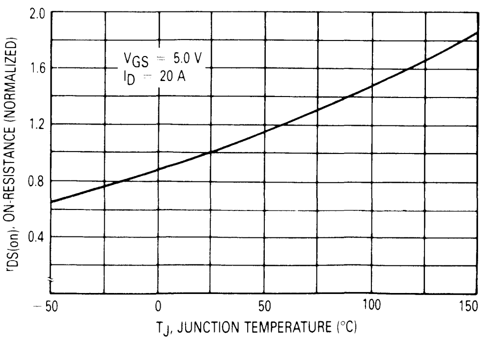


Figure 6. On-Resistance Variation With Temperature



3

Figure 7. Breakdown Voltage Variation With Temperature

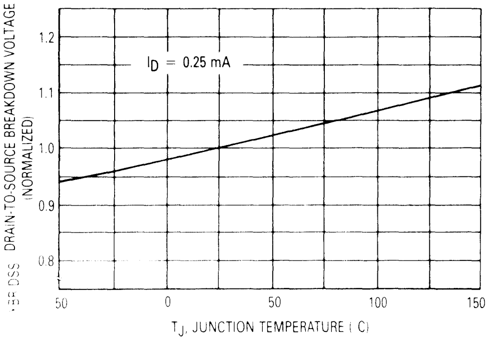
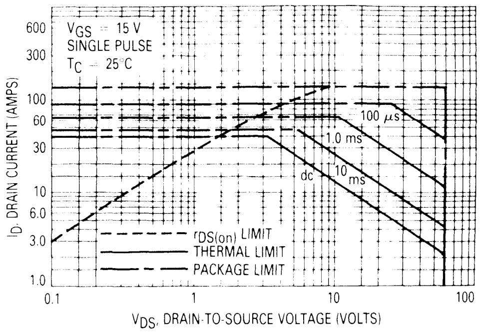


Figure 8. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

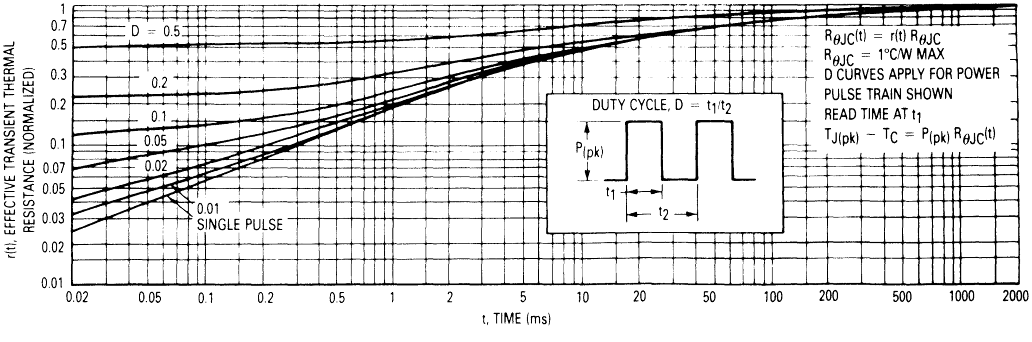
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

The switching safe operating area fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. This is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 11 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 250 A/μs.

Figure 10. Commutating Waveforms

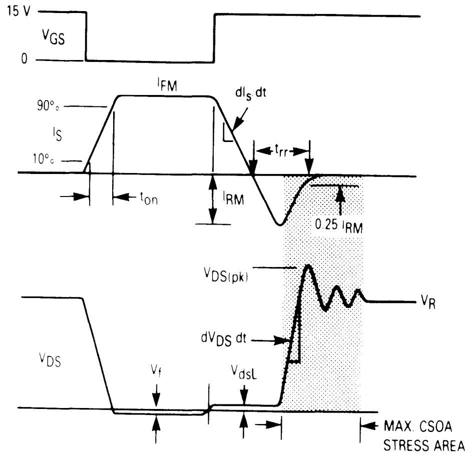


Figure 11. Commutating Safe Operating Area (CSOA)

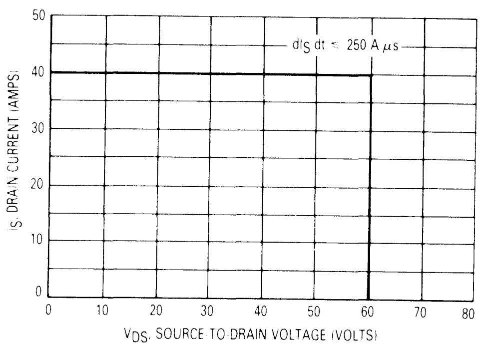


Figure 12. Commutating Safe Operating Area Test Circuit

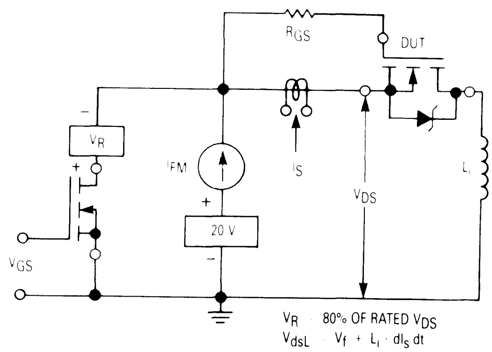


Figure 13. Unclamped Inductive Switching Test Circuit

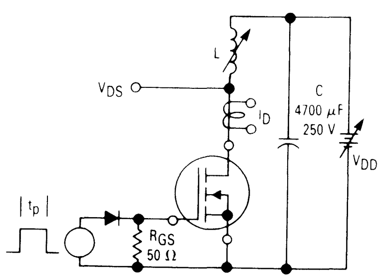


Figure 14. Unclamped Inductive Switching Waveforms

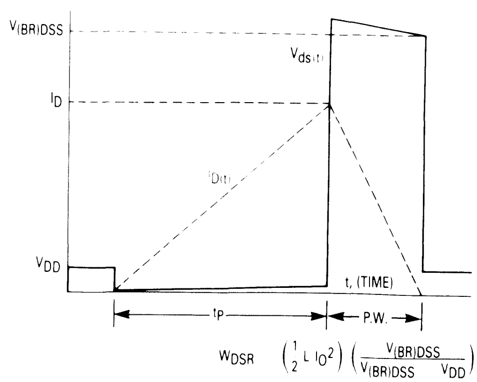


Figure 15. Capacitance Variation With Voltage

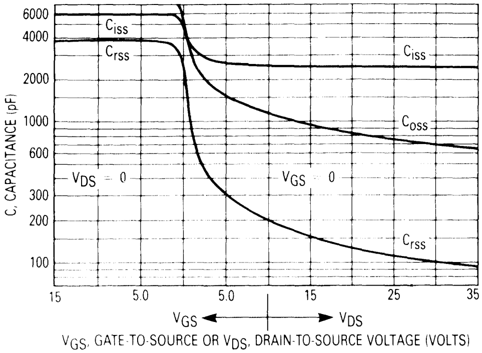


Figure 16. Gate Charge versus Gate-To-Source Voltage

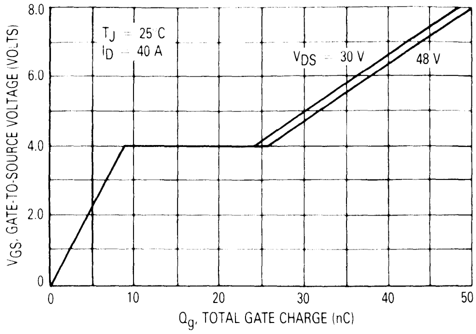
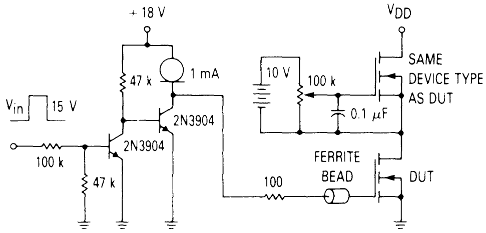
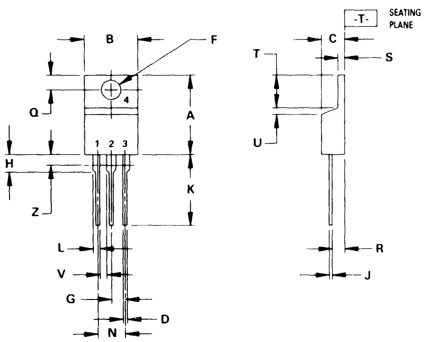


Figure 17. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP40N06M

Advance Information

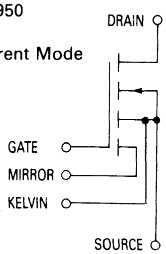
Power Field Effect Transistor

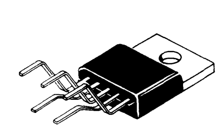
N-Channel Enhancement-Mode Silicon Gate TMOS with Current Sensing Capability

TMOS SENSEFET
40 AMPERES
$r_{DS(on)}$ = 0.04 OHM
60 VOLTS

This TMOS Power FET with current sensing capability is designed for all power control applications where it is desirable to sense current such as in power supplies and motor controls. This device allows current sensing with a minimum of power loss.

- "Lossless" Current Sensing for Maximum Efficiency — Sense Current is Reduced by a Factor of 950
- Ideal for Short Circuit/Overload Protection
- Simplifies Many Circuits When Used With Current Mode Integrated Circuits Such as the MC34129
- Kelvin Source Contact to Maximize Accuracy
- Rugged — SOA is Power Dissipation Limited
- Low $r_{DS(on)}$ — 0.04 Ohms Maximum





NOTES:
1. Handling precautions to protect against electrostatic discharge is mandatory.
2. Do not use the mirror FET independent of the power FET.
3. It is recommended that the mirror terminal (M) be shorted to the Kelvin Terminal (K) when current sensing is not required.

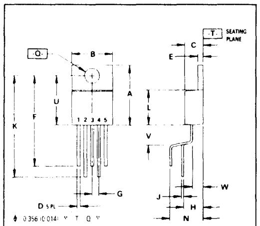
MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-to-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	20 ±40	Vdc Vpk
Drain-to-Mirror Voltage	V_{DMS}	60	Vdc
Gate-to-Mirror Voltage	V_{GM}	20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	40 120	Amps
Sense Current — Continuous — Pulsed	I_M I_{MM}	45 130	mA
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case Junction-to-Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

This is advance information on a new introduction and specifications are subject to change without notice.



NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

STYLE 1
PIN 1. GATE
2. MIRROR
3. DRAIN
4. KELVIN
5. SOURCE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.169	1.397	0.046	0.055
F	21.590	23.749	0.850	0.935
G	1.702 BSC		0.067 BSC	
H	4.445	5.080	0.175	0.200
J	0.381	0.635	0.015	0.025
K	22.860	27.940	0.900	1.100
L	8.052	9.398	0.317	0.370
N	7.874	8.509	0.310	0.335
Q	3.556	3.937	0.140	0.155
U	11.888	12.827	0.468	0.505
V	4.699	5.842	0.185	0.230
W	2.286	2.794	0.090	0.110

CASE 314B-02

3

ELECTRICAL CHARACTERISTICS (T_C = 25°C, V_{MK} = 0 unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0) (V_{DS} = 60 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mAdc) (T_J = 125°C)	$V_{GS(th)}$	2 1.5	2.5 —	4 3.5	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc)	$r_{DS(on)}$	—	0.03	0.04	Ohms
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc) (I_D = 40 A) (I_D = 20 A, T_J = 100°C)	$V_{DS(on)}$	— —	1.2 —	1.8 1.8	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 20 Adc)	g_{fs}	12	—	—	mhos
CURRENT SENSING CHARACTERISTICS					
Current Mirror Ratio (Cell Ratio) (R_{SENSE} = 0, I_D = 10 A, V_{GS} = 10 V)	n	900	—	960	—
Mirror Compliance Ratio (V_{GS} = 10 Vdc, I_D = 20 Adc)	K_{mc}	—	0.67	—	—
Source Active Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc, R_S = 10 megohm)	$r_{a(on)}$	—	17	—	mΩ
Mirror Active Resistance (V_{GS} = 10 Vdc, I_D = 20 Adc)	$r_{m(on)}$	—	16	—	Ohms
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	—	1800	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	—	900	pF
Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	—	400	pF
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time (V_{DD} = 25 V, I_D = 20 A, R_{gen} = 50 Ohms)	$t_{d(on)}$	—	20	40	ns
Rise Time (V_{DD} = 25 V, I_D = 20 A, R_{gen} = 50 Ohms)	t_r	—	20	40	ns
Turn-Off Delay Time (V_{DD} = 25 V, I_D = 20 A, R_{gen} = 50 Ohms)	$t_{d(off)}$	—	60	100	ns
Fall Time (V_{DD} = 25 V, I_D = 20 A, R_{gen} = 50 Ohms)	t_f	—	30	60	ns
Total Gate Charge (V_{DS} = 48 V, I_D = 40 A, V_{GS} = 10 V)	Q_g	—	62	75	nC
Gate-Source Charge (V_{DS} = 48 V, I_D = 40 A, V_{GS} = 10 V)	Q_{gs}	—	27	—	nC
Gate-Drain Charge (V_{DS} = 48 V, I_D = 40 A, V_{GS} = 10 V)	Q_{gd}	—	35	—	nC
SOURCE-DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage (I_S = 80 A)	V_{SD}	—	1.1	1.5	Vdc
Forward Turn-On Time (I_S = 80 A)	t_{on}	—	260	—	ns
Reverse Recovery Time (I_S = 80 A)	t_{rr}	—	200	—	ns

*Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

TYPICAL CHARACTERISTICS

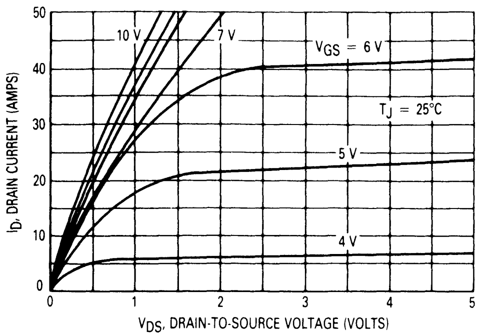


Figure 1. On-Region Characteristics

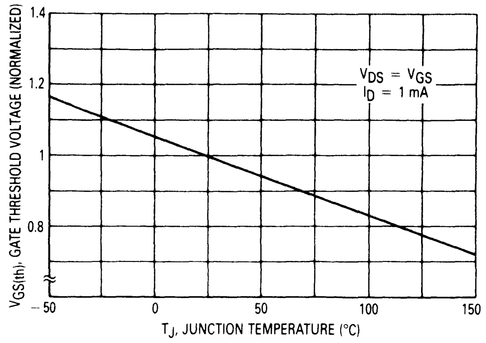


Figure 2. Gate Threshold Voltage Variation with Temperature

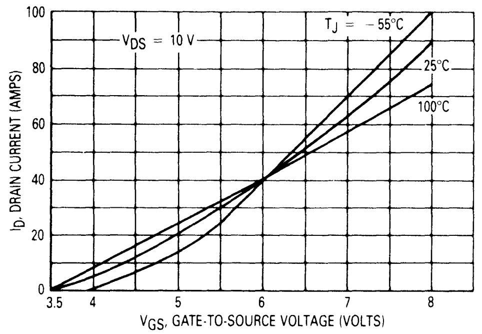


Figure 3. Transfer Characteristics

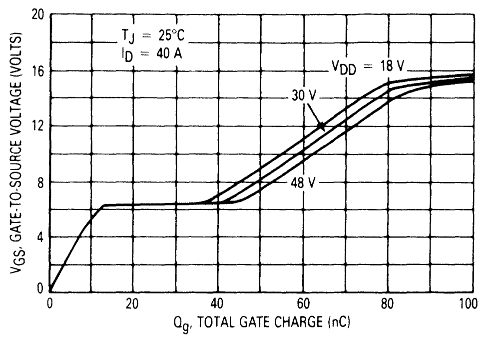


Figure 4. Stored Charge Variation

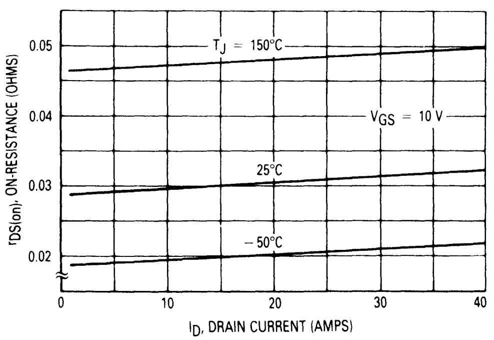


Figure 5. On-Resistance versus Drain Current

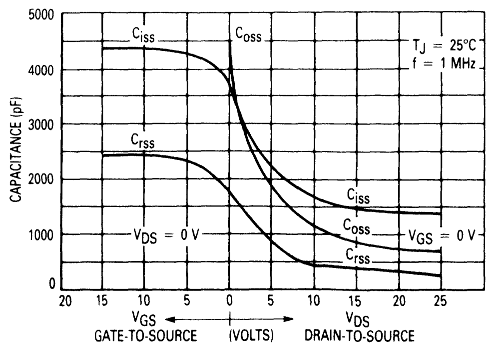


Figure 6. Capacitance Variation

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TYPICAL CHARACTERISTICS

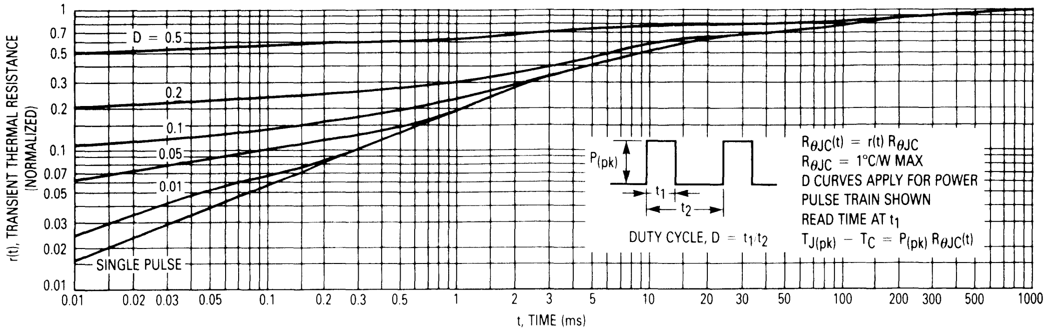

Figure 7. Thermal Response

SAFE OPERATING AREA INFORMATION

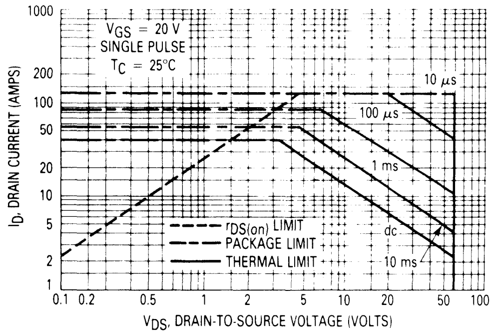

Figure 8. Maximum Rated Forward Biased Safe Operating Area

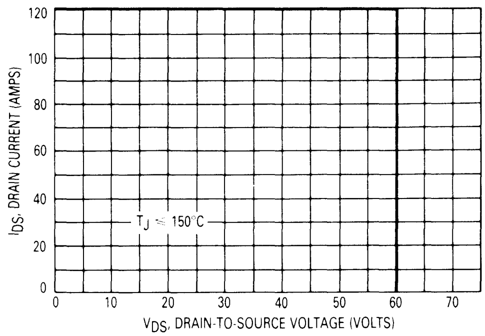

Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

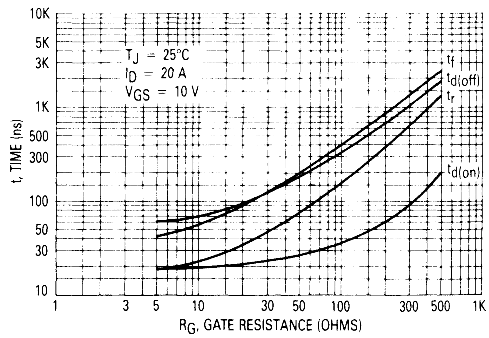

Figure 10. Resistive Switching Time Variation with Gate Resistance

SAFE OPERATING AREA INFORMATION

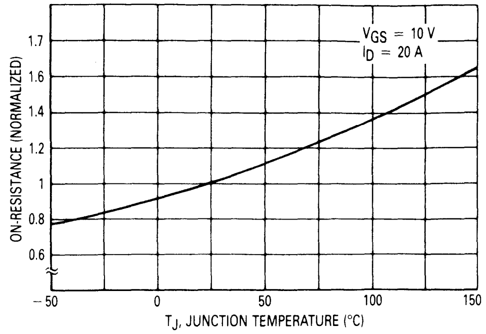

Figure 11. On-Resistance Variation with Temperature

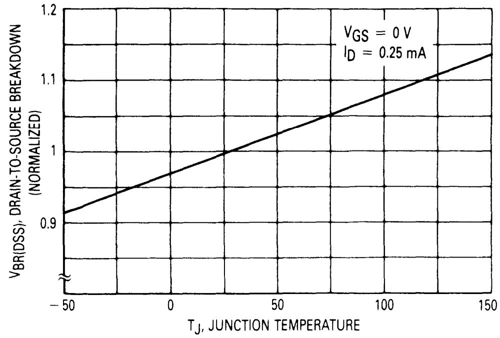

Figure 12. Breakdown Variation with Temperature

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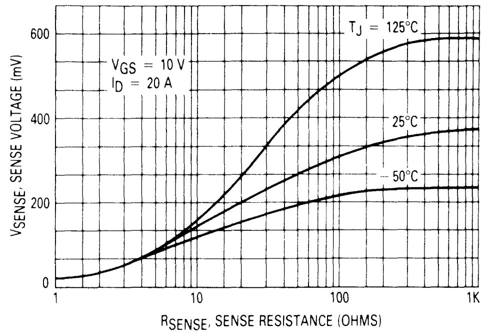

Figure 13. Sense Voltage Variation with Sense Resistance

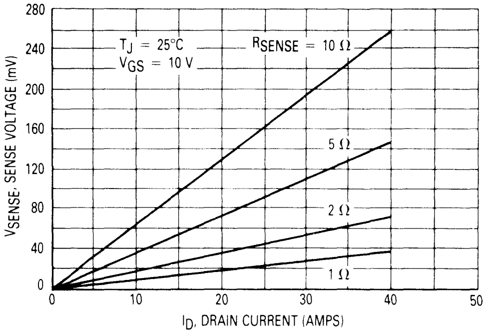

Figure 14. Sense Voltage Variation with Drain Current

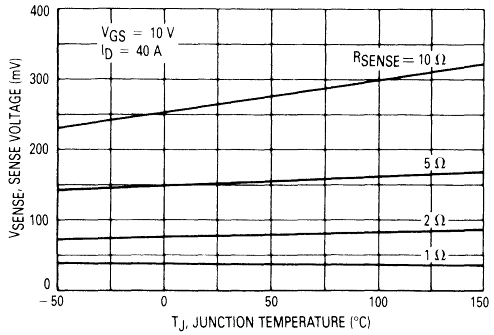

Figure 15. Sense Voltage Variation with Temperature

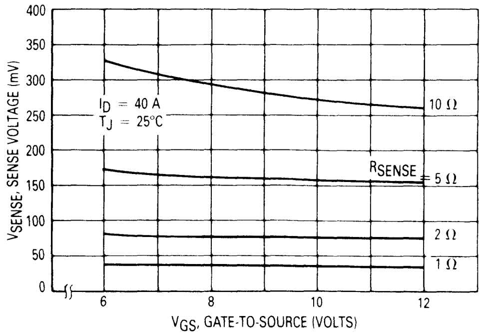

Figure 16. Sense Voltage Variation with Gate-to-Source Voltage

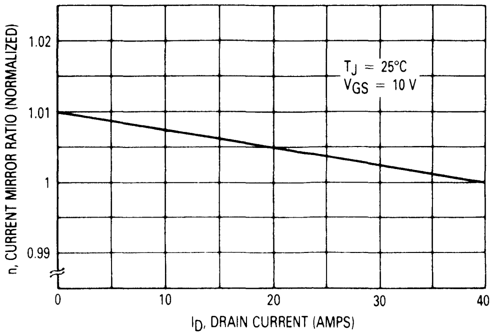

Figure 17. Current Mirror Ratio Variation with Drain Current

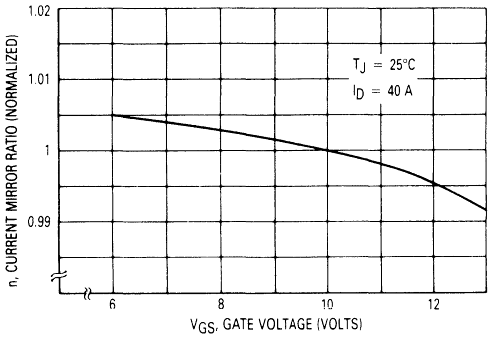

Figure 18. Current Mirror Ratio Variation with Gate-to-Source Voltage

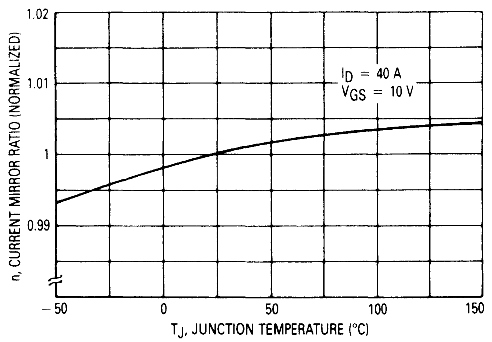

Figure 19. Current Mirror Ratio Variation with Temperature

LOSSLESS CURRENT SENSING

Assuming a fully switched on SENSEFET, current sensing can be modeled with the simple resistor divider network shown in Figure 20. In this model, r_b is the bulk drain resistance, $r_{m(on)}$ is the active mirror on-resistance, $r_{a(on)}$ is the power section's active on-resistance and r_w is the source wire bond resistance. Using values for $r_{a(on)}$ and $r_{m(on)}$ from the electrical characteristics table; V_{SENSE}, R_{SENSE}, and drain current may be calculated from the following sensing equations.

SENSING EQUATIONS:

1. $V_{SENSE} = I_D\, r_{a(on)}\, R_{SENSE}/[R_{SENSE} + r_{m(on)}]$
2. $R_{SENSE} = V_{SENSE}\, r_{m(on)}/[I_D\, r_{a(on)} - V_{SENSE}]$
3. $I_D = V_{SENSE}\, (R_{SENSE} + r_{m(on)})/r_{a(on)}\, R_{SENSE}$
4. $n = I_D/I_{SENSE}$; where $R_{SENSE} = 0$
5. $r_{a(on)} = r_{m(on)}/n$

When using these equations there are several factors to keep in mind.

They are described as follows:

- Maximum Sense Voltage: The maximum sense voltage that can appear at the mirror terminal is $(r_{a(on)}/r_{a(on)} + r_b) \times V_{DS(on)}$. This ratio is called the mirror compliance ratio, K_{MC}, and defines the upper boundary for sense voltage.
- Accuracy: Accurate current sensing is based upon the inherent matching of $r_{m(on)}$ with the power section's active on-resistance, $r_{a(on)}$. When $R_{SENSE} = 0$, matching and current sensing accuracy are within ±3%. As R_{SENSE} is increased, sensing accuracy is reduced since mirror current becomes dependent on the ratio of internal on-resistance to an external R_{SENSE}. From a practical point of view, relatively good sensing accuracy (±10%) is maintained up to $R_{SENSE} = r_{m(on)}/2$. As R_{SENSE} is increased beyond $r_{m(on)}$, sensing accuracy decreases rapidly.

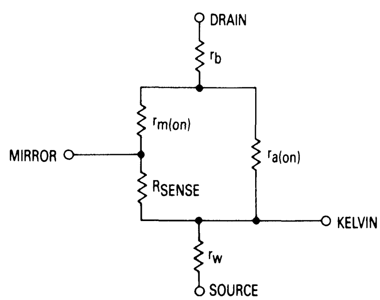

Figure 20. SENSEFET Model

- Ground Loop Errors: Lossless current sensing is a technique that looks for 100 mV signals in a loop that may carry tens or even hundreds of amps. The potential for ground loop errors in this kind of an application is a first order design consideration. Internal wire bond resistance, contact resistance, and external wiring resistance are all significant. Therefore, it is important to reference sense voltage measurement circuitry to the Kelvin pin rather than power ground. In addition, referencing gate drive to the Kelvin pin rather than power ground will provide faster switching speeds.
- Noise Suppression: Switching noise is also a first order design issue. Layout, therefore, is critical. In addition, a single pole RC filter between R_{SENSE} and the current sensing circuitry's input terminals is often desirable. A 1 μsec time constant is generally long enough to provide adequate noise suppression and short enough to provide adequate protection during overloads. An illustration is provided in Figure 21.
- Double Pulse Suppression: In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET is likely due to excessive power dissipation. By syncing current limiting to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- Parasitic Diode: In addition to the power section's usual source-drain diode, there is a mirror-drain diode in the sense cells. Like the source-drain diode, the mirror-drain diode conducts during the reverse-mode operation, however, current sense characteristics are defined only in the forward-mode operation.
- Reverse Recovery: In bridge circuits, when a SENSEFET's source-drain diode is commutated a voltage spike is produced at the mirror. This spike is short since it lasts only for the drain-source diode's reverse recovery time. However, its amplitude can be an order of magnitude larger than normal sense voltages and produce unwanted overcurrent trips. Blanking, filtering, or other suppression techniques may be required in some applications.

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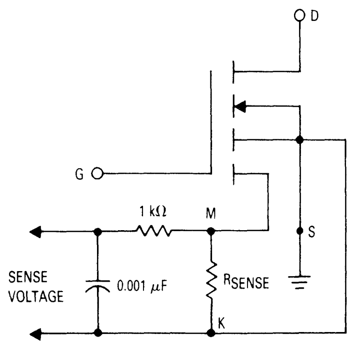


Figure 21. SENSEFET with Noise Suppression

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTP50N05EL

Designer's Data Sheet

Logic Level TMOS (L^2TMOS) E-FET Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

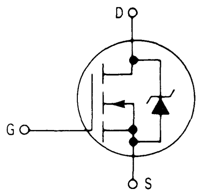
TMOS POWER FET
LOGIC LEVEL
50 AMPERES
$r_{DS(on)}$ = 0.032 OHM
50 VOLTS

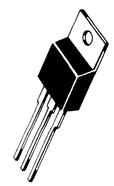
This advanced L^2TMOS E-FET is a power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5.0 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

3

TMOS

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2.0 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive	V_{GS} V_{GSM}	±15 ±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	50 160	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 175	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J ≤ 175°C)

Single Pulse Drain-to-Source Avalanche Energy Repetitive Pulse Drain-to-Source Avalanche Energy	W_{DSS} (1) W_{DSS} (2) W_{DSR} (3)	200 50 15	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 25 V, I_D = 50 A, L = 80 μH, Initial T_C = 25°C
(2) V_{DD} = 25 V, I_D = 50 A, L = 80 μH, Initial T_C = 100°C
(3) f = 10 kHz

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = 50 V, V_{GS} = 0)			—	1.0	
(V_{DS} = 50 V, V_{GS} = 0, T_J = 125°C)			—	50	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage		$V_{GS(th)}$			Vdc
(V_{DS} = V_{GS}, I_D = 1.0 mA)			1.0	2.0	
T_J = 100°C			0.75	1.75	
Static Drain-Source On-Resistance (V_{GS} = 5.0 Vdc, I_D = 25 Adc)		$r_{DS(on)}$	—	0.032	Ohm
Drain-Source On-Voltage (V_{GS} = 5.0 V)		$V_{DS(on)}$			Vdc
(I_D = 50 Adc)			—	1.8	
(I_D = 25 Adc, T_J = 100°C)			—	1.2	
Forward Transconductance (V_{DS} = 5.0 V, I_D = 25 A)		g_{FS}	16	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{iss}	2500 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1.0 MHz See Figure 15		6600 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz	C_{rss}	215 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1.0 MHz See Figure 15		3600 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz See Figure 15	C_{oss}	965 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 25 A, V_{GS} = 5.0 V, R_{gen} = 50 Ohms, R_{GS} = 5.2 Ohms)	$t_{d(on)}$	27 (Typ)	—	ns
Rise Time		t_r	220 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	60 (Typ)	—	
Fall Time		t_f	110 (Typ)	—	
Total Gate Charge	(V_{DS} = 40 V, I_D = 50 A, V_{GS} = 5.0 Vdc) See Figures 16 and 17	Q_g	38 (Typ)	48	nC
Gate-Source Charge		Q_{gs}	12 (Typ)	—	
Gate-Drain Charge		Q_{gd}	30 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = 50 A, V_{GS} = 0)	V_{SD}	1.3 (Typ)	1.5	Vdc
Forward Turn-On Time	(I_S = 50 A, V_{GS} = 0, dI_S/dt = 100 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	50 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

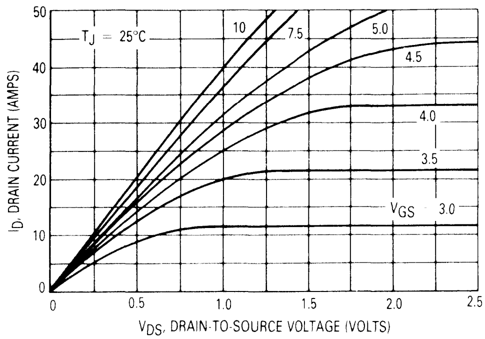


Figure 2. Gate-Threshold Voltage Variation With Temperature

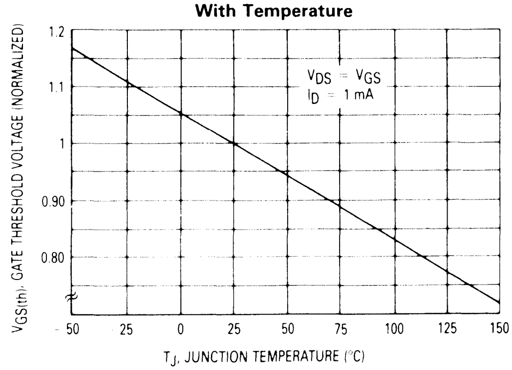


Figure 3. Transfer Characteristics

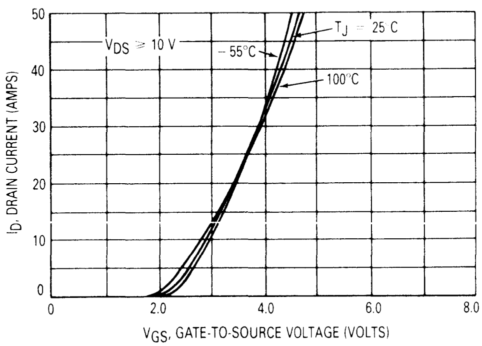


Figure 4. On-Resistance versus Drain Current

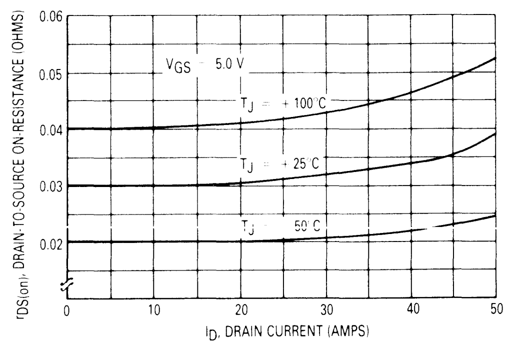


Figure 5. Drain-To-Source On-Resistance versus Gate-To-Source Voltage

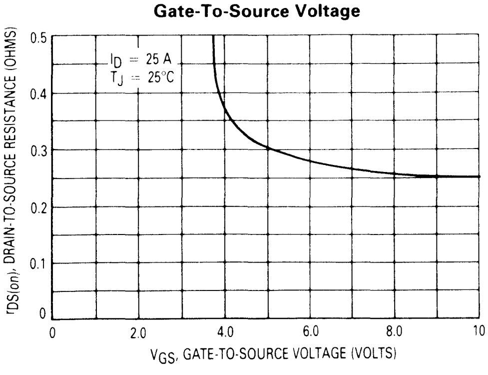
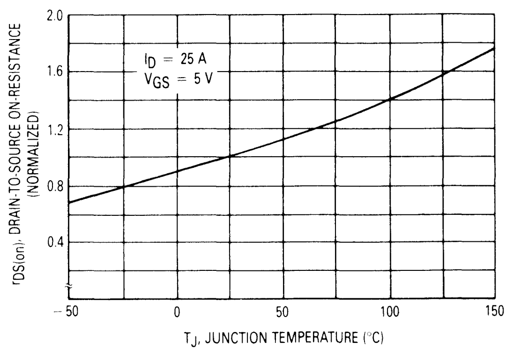


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Breakdown Voltage Variation With Temperature

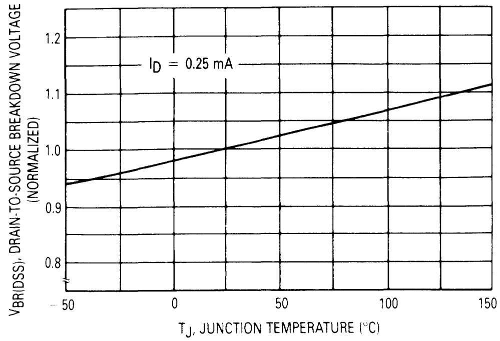
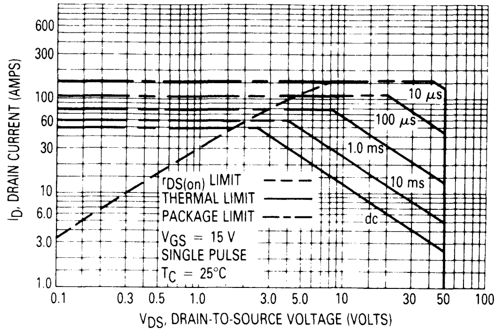


Figure 8. Maximum Rated Forward Biased Safe Operating Area



3

FORWARD BIASED SAFE OPERATING AREA

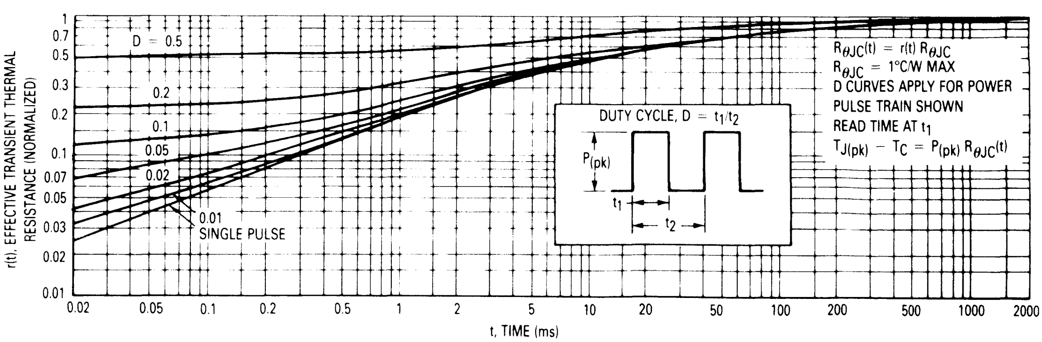
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

The switching safe operating area fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. This is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 11 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

Figure 10. Commutating Waveforms

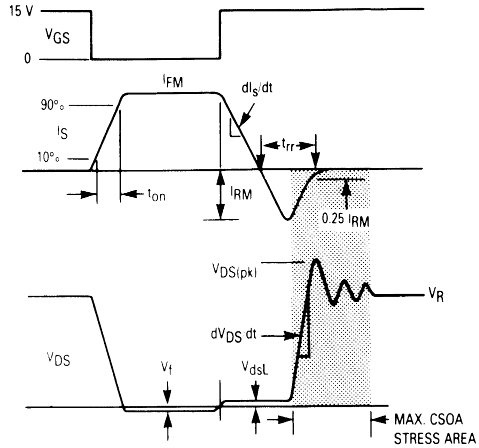


Figure 11. Commutating Safe Operating Area (CSOA)

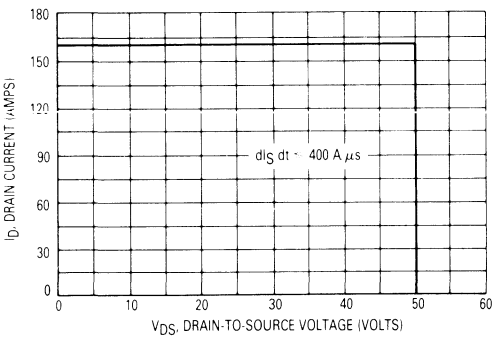
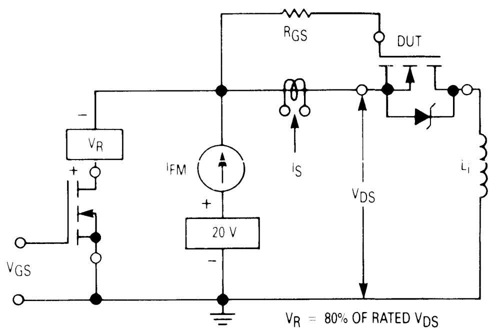


Figure 12. Commutating Safe Operating Area Test Circuit



V_R = 80% OF RATED V_{DS}

$V_{dsL} = V_f + L_i \cdot dI_S/dt$

Figure 13. Unclamped Inductive Switching Test Circuit

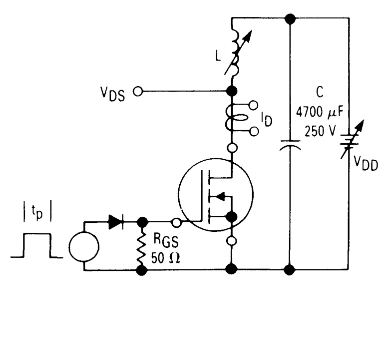
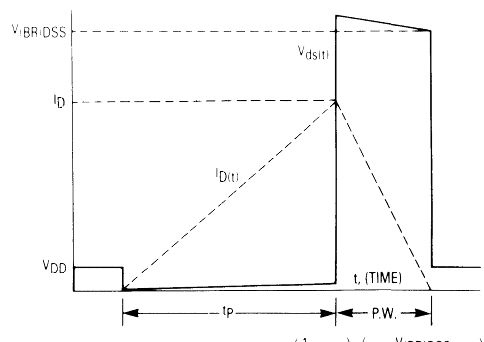


Figure 14. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Capacitance Variation With Voltage

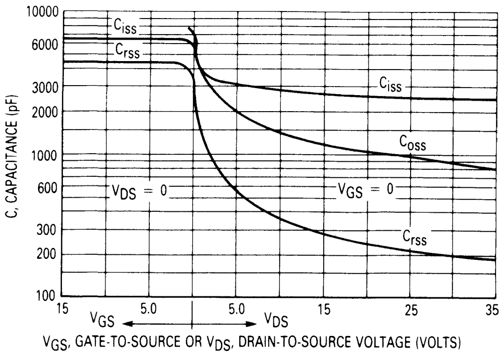


Figure 16. Gate Charge versus Gate-To-Source Voltage

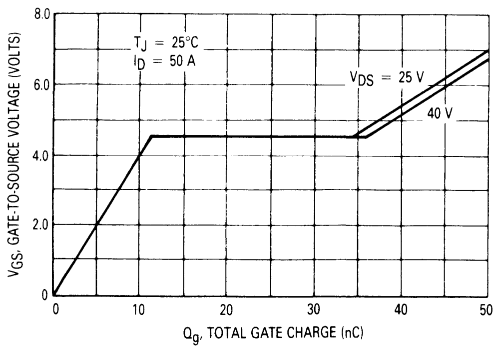


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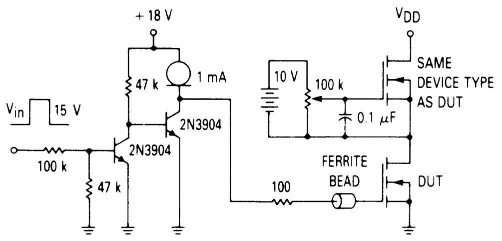
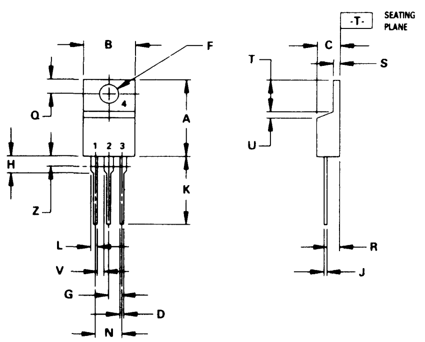
Figure 17. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

CASE 221A-04
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

MTP2955

Designer's Data Sheet

Power Field Effect Transistor

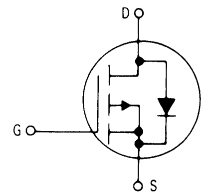
P-Channel Enhancement-Mode Silicon Gate TMOS

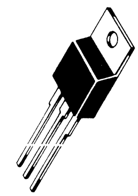
TMOS POWER FET
12 AMPERES
$r_{DS(on)}$ = 0.3 OHM
60 VOLTS

3

This TMOS Power FET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- P-Channel — Can Be Used as Complement to MTP3055E





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±15 ±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case	$R_{\theta JC}$	1.67	°C/W
— Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μAdc
(V_{DS} = 60 Volts, V_{GS} = 0)			—	10	
(V_{DS} = 60 Volts, V_{GS} = 0, T_J = 125°C)			—	80	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = −15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	2.0	4.5	Vdc
T_J = 100°C			1.5	4.0	
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.3	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V)		$V_{DS(on)}$			Vdc
(I_D = 12 Adc)			—	3.9	
(I_D = 6.0 Adc, T_J = 100°C)			—	3.2	
Forward Transconductance (V_{DS} = 10 V, I_D = 6.0 A)		g_{FS}	3.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 12	C_{iss}	600 (Typ)	—	pF
Output Capacitance		C_{oss}	300 (Typ)	—	
Reverse Transfer Capacitance		C_{rss}	135 (Typ)	—	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{GS} = 10 V, V_{DD} = 25 V, I_D = 6.0 Amps, R_g = 50 ohms) See Figures 9, 13 and 14	$t_{d(on)}$	10 (Typ)	—	ns
Rise Time		t_r	75 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	75 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DD} = 48 V, I_D = 12 A, V_{GS} = 10 V) See Figure 11	Q_g	26 (Typ)	45	nC
Gate-Source Charge		Q_{gs}	3.5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	15 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	I_S = 12 A, V_{GS} = 0	V_{SD}	3.0 (Typ)	3.8	Vdc
Forward Turn-On Time	I_S = 12 A, dI_S/dt = 100 A/μs, V_R = 30 V	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	110 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance		L_d			nH
(Measured from contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of pad)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

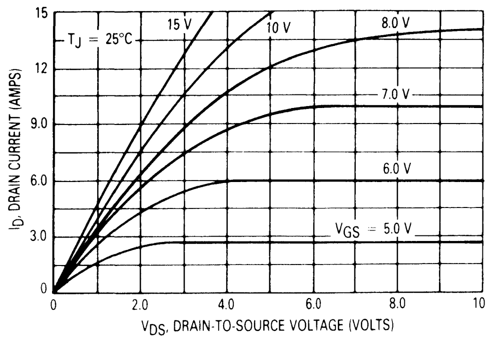


Figure 2. Gate Threshold Variation With Temperature

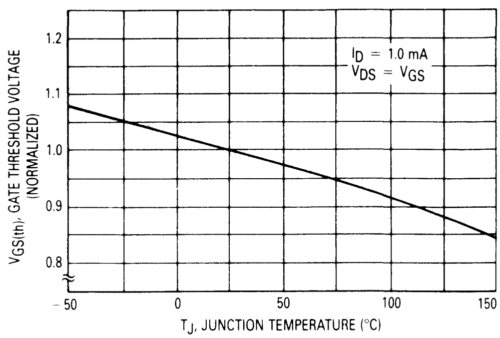


Figure 3. Transfer Characteristics

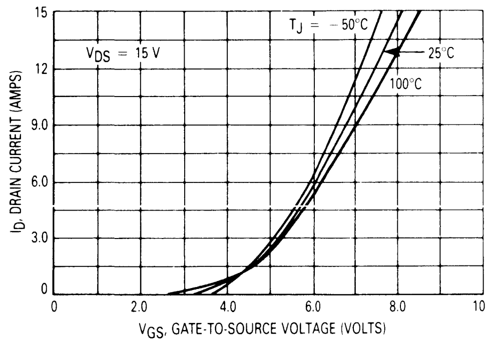


Figure 4. Breakdown Voltage Variation With Temperature

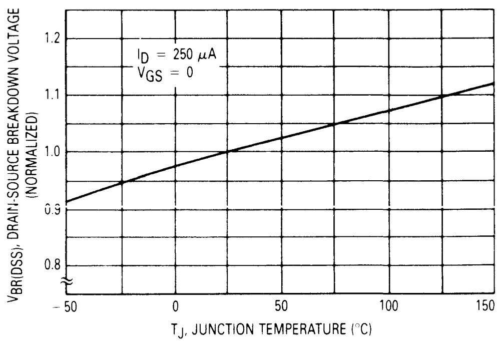


Figure 5. On-Resistance Variation With Drain Current

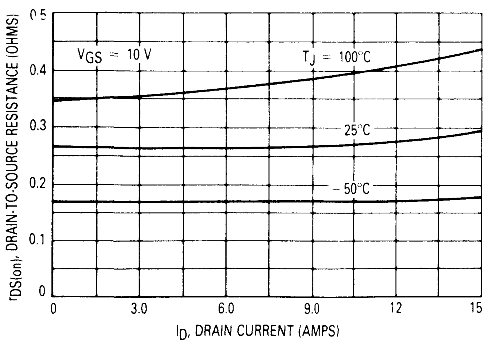
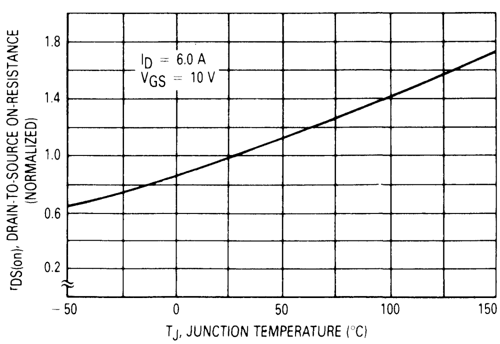


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

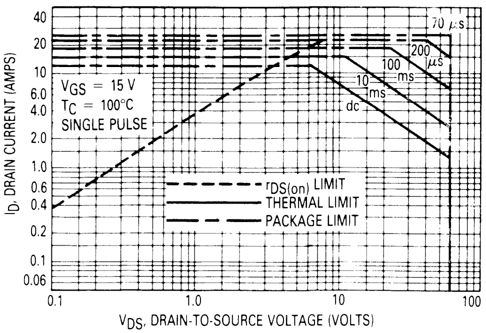


Figure 7. Maximum Rated Forward Biased Safe Operating Area

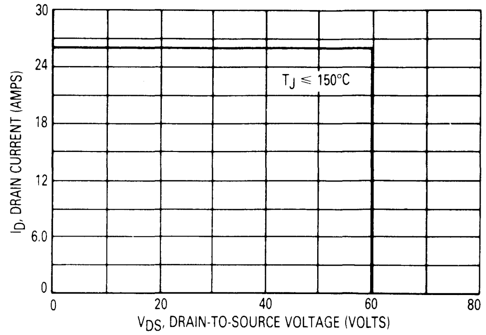


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

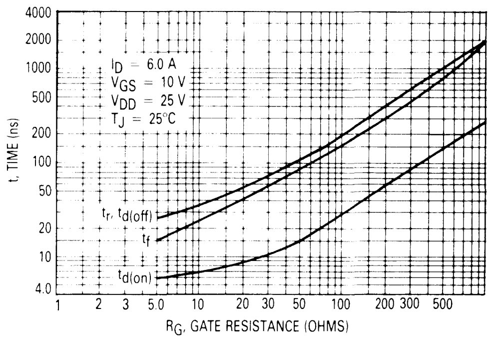
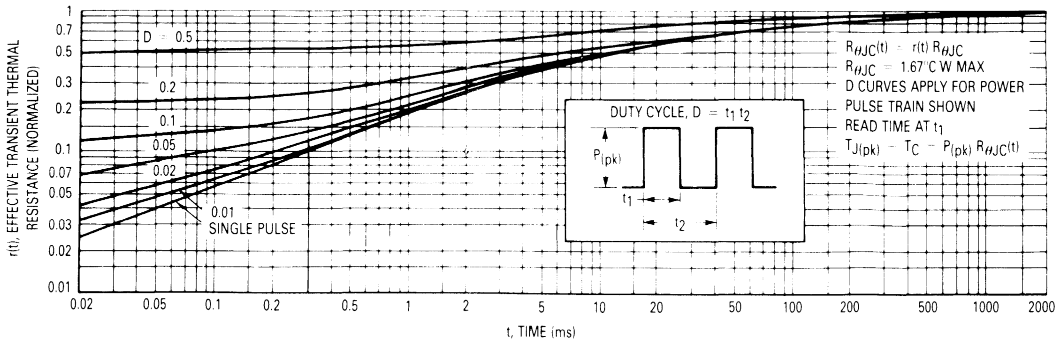


Figure 9. Resistive Switching Time versus Gate Resistance

Figure 10. Thermal Response



TYPICAL CHARACTERISTICS

Figure 11. Gate Charge versus Gate-To-Source Voltage

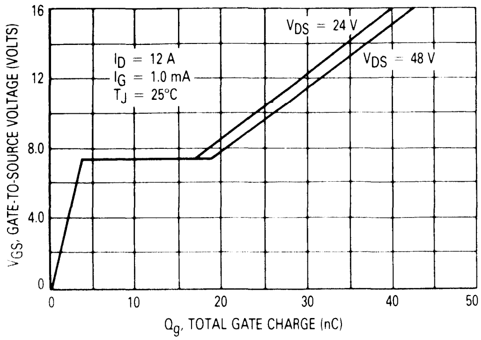
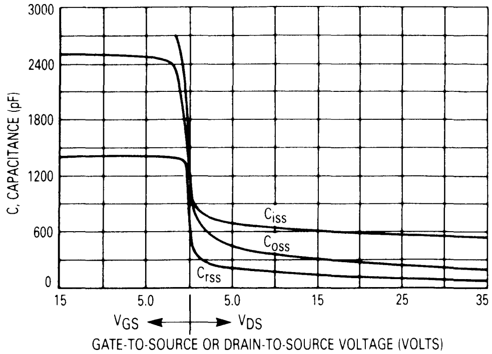


Figure 12. Capacitance Variation With Voltage



RESISTIVE SWITCHING

Figure 13. Switching Test Circuit

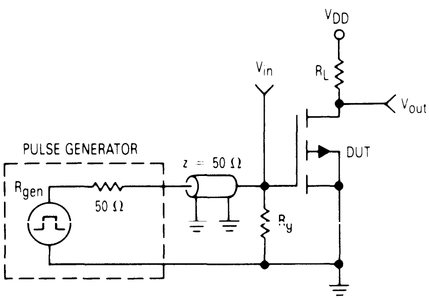
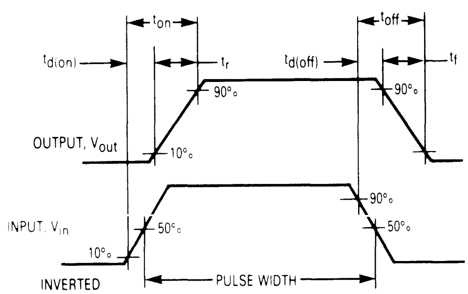
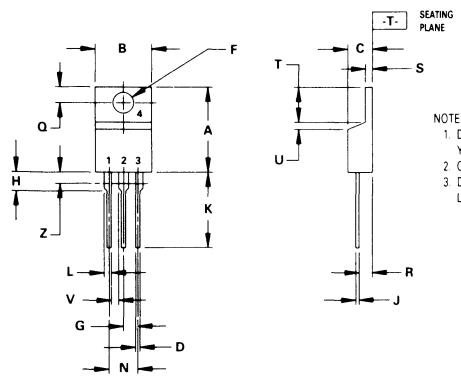


Figure 14. Switching Waveforms



OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

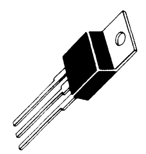
CASE 221A-04
TO-220AB

Advance Information

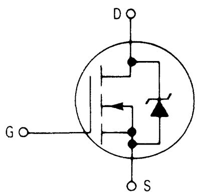
TMOS IV
N-Channel Enhancement-Mode
Power Field Effect Transistor

MTP3055E

TMOS POWER FET
12 AMPERES
$r_{DS(on)}$ = 0.15 OHM
60 VOLTS



This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.



- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	MTP3055E	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

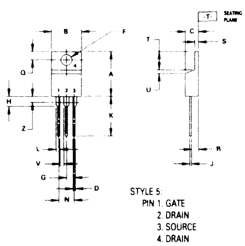
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 80	μA

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

OUTLINE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

CASE 221A-04
TO-220AB

3

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ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (continued)					
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 12 Adc) (I_D = 6 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2 1.5	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)		g_{FS}	4	—	mhos
DRAIN-TO-SOURCE AVALANCHE STRESS CAPABILITY					
Unclamped Inductive Switching Energy See Figures 15 and 16 (I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		W_{DSR}	 — — —	 18 35 16	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 11	C_{iss}	—	500	pF
Output Capacitance		C_{oss}	—	300	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figure 18	$t_{d(on)}$	—	20	ns
Rise Time		t_r	—	60	
Turn-Off Delay Time		$t_{d(off)}$	—	65	
Fall Time		t_f	—	65	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 14	Q_g	12 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	6.5 (Typ)	—	
Gate-Drain Charge		Q_{gd}	5.5 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_{FM} = 0.5 Rated I_D, dI_S/dt = 100 A/μs, V_{GS} = 0)	V_{SD}	1.7 (Typ)	2	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	50 (Typ)	90	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

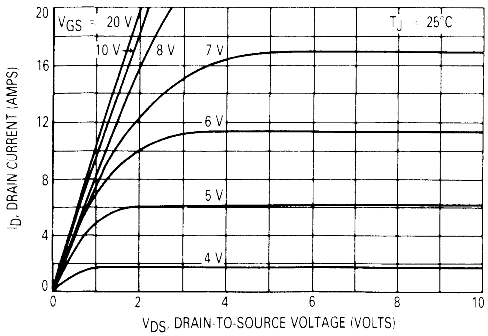

Figure 1. On-Region Characteristics

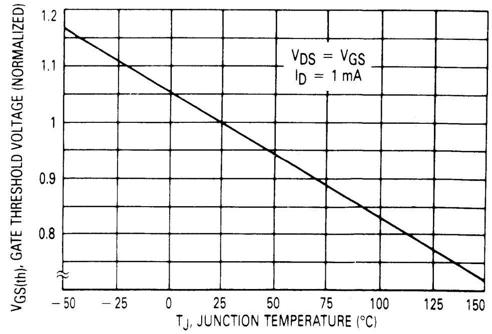

Figure 2. Gate-Threshold Voltage Variation With Temperature

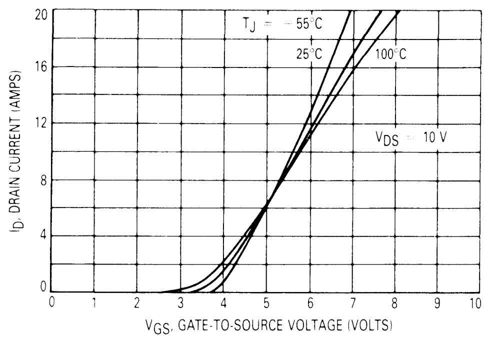

Figure 3. Transfer Characteristics

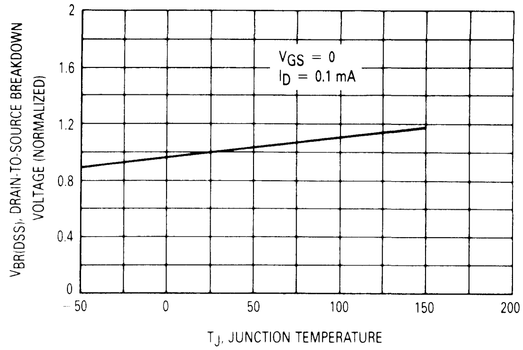

Figure 4. Breakdown Voltage Variation With Temperature

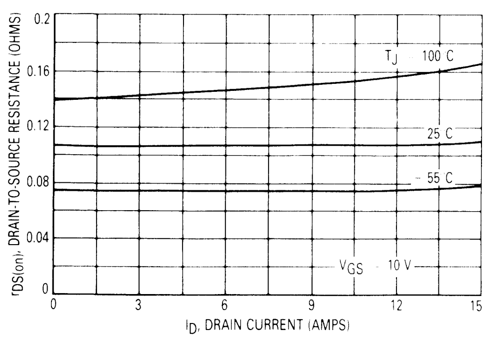

Figure 5. On-Resistance versus Drain Current

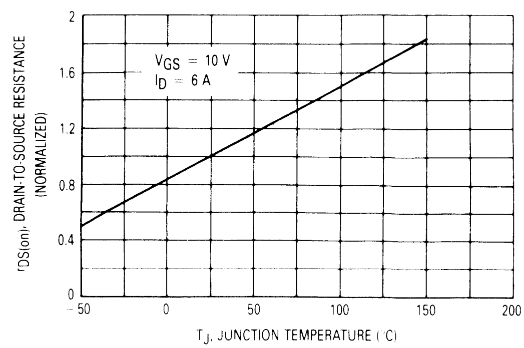

Figure 6. On-Resistance Variation With Temperature

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SAFE OPERATING AREA INFORMATION

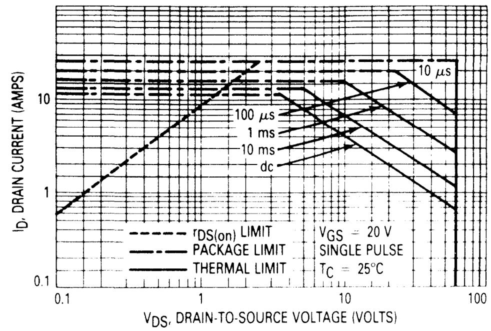


Figure 7. Maximum Rated Forward Biased Safe Operating Area

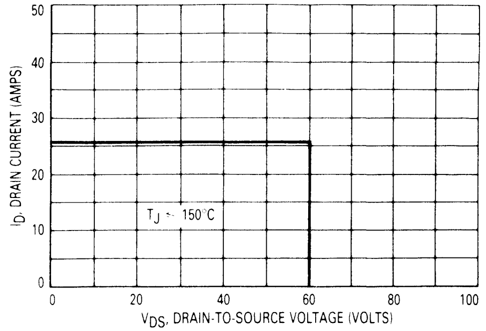


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

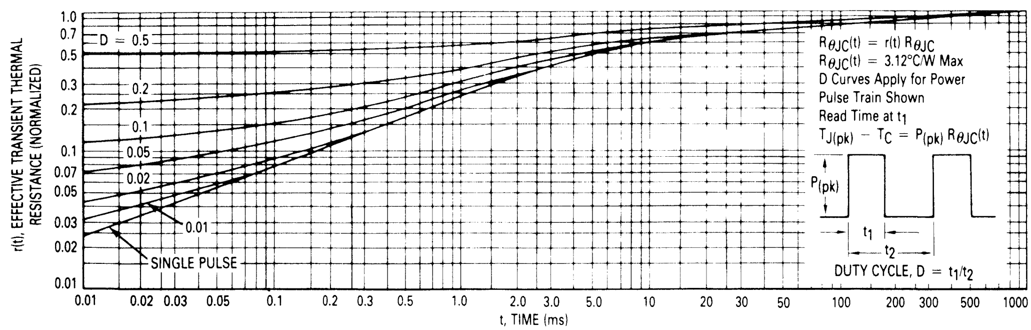


Figure 9. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

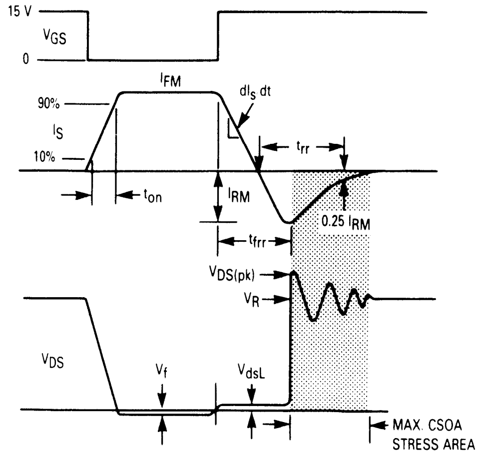


Figure 10. Commutating Waveforms

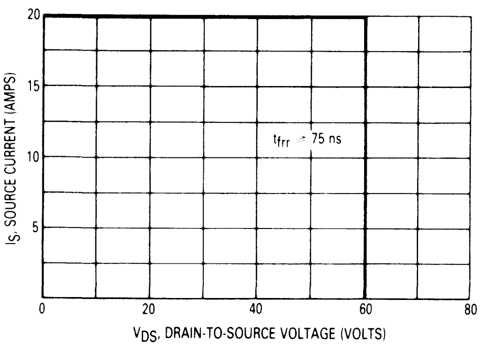


Figure 11. Commutating Safe Operating Area (CSOA)

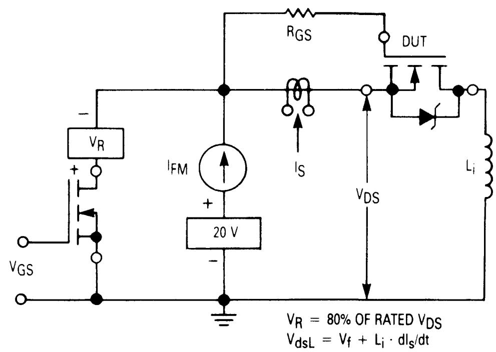


Figure 12. Commutating Safe Operating Area Test Circuit

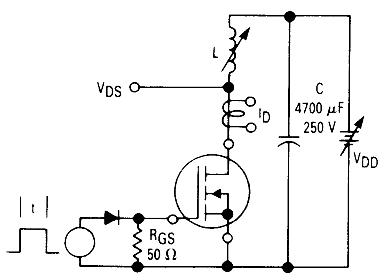
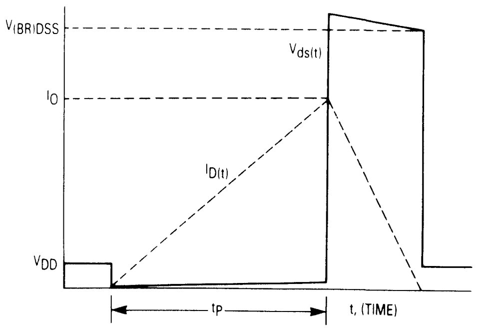


Figure 13. Unclamped Inductive Switching Test Circuit



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 14. Unclamped Inductive Switching Waveforms

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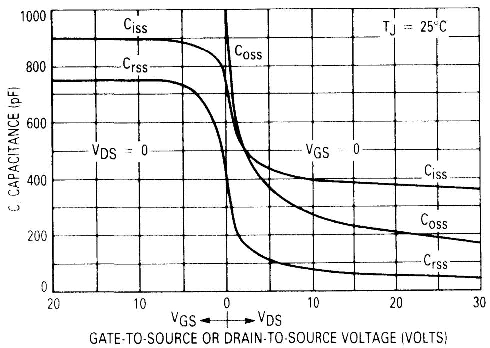


Figure 15. Capacitance Variation

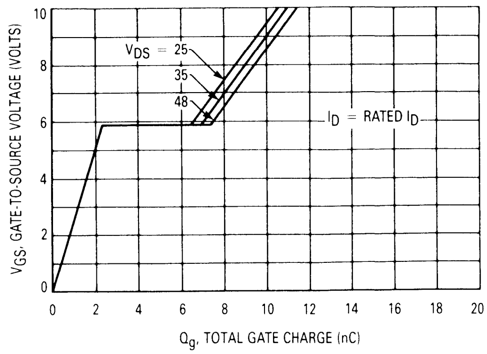
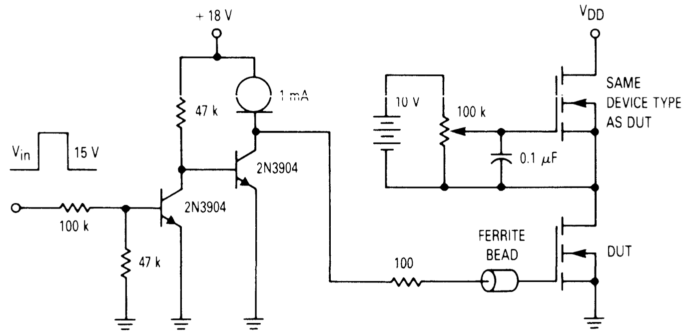


Figure 16. Gate Charge versus Gate-to-Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

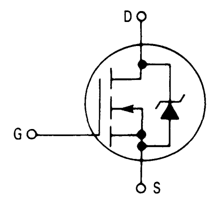
Figure 17. Gate Charge Test Circuit

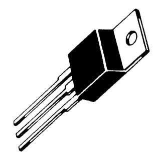
MTP3055EL

Designer's Data Sheet

TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER FETs
LOGIC LEVEL
12 AMPERES
$r_{DS(on)}$ = 0.18 OHM
60 VOLTS





CASE 221A-04
TO-220AB

This advanced E-FET is a TMOS power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at 150°C

TMOS

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current		I_{DSS}			μA
(V_{DS} = Rated V_{DSS}, V_{GS} = 0)			—	1	
(V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 150°C)			—	50	
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	2	Vdc
T_J = 150°C			0.6	1.6	
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)		$r_{DS(on)}$	—	0.18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V)		$V_{DS(on)}$			Vdc
(I_D = 12 Adc)			—	2.4	
(I_D = 6 Adc, T_J = 100°C)			—	1.95	
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)		g_{FS}	5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain-to-Source Avalanche Energy See Figures 13 and 14		W_{DSR}			mJ
(I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive)			—	18	
(I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)			—	35	
(I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)			—	16	
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	400 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		1000 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	30 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		660 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 15	C_{oss}	175 (Typ)	—	pF
SWITCHING CHARACTERISTICS (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms, R_{GS} = 50 ohms)	$t_{d(on)}$	20 (Typ)	—	ns
Rise Time		t_r	95 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	38 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 16 and 17	Q_g	7.2 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	2 (Typ)	—	
Gate-Drain Charge		Q_{gd}	8 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	1.04 (Typ)	1.18	Vdc
Forward Turn-On Time	(I_S = 26 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	55 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO-220)					
Internal Drain Inductance		L_d			nH
(Measured from the contact screw on tab to center of die)			3.5 (Typ)	—	
(Measured from the drain lead 0.25″ from package to center of die)			4.5 (Typ)	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	7.5 (Typ)	—	

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TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

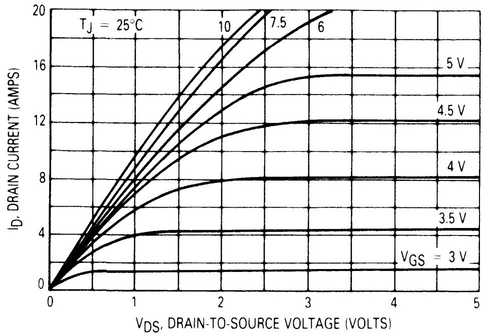

Figure 2. Gate-Threshold Voltage Variation With Temperature

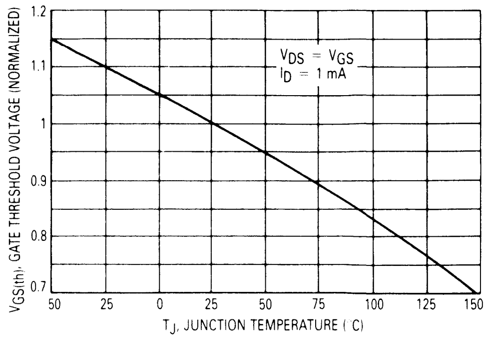

Figure 3. Transfer Characteristics

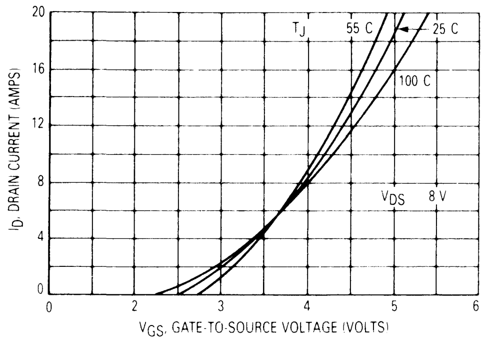

Figure 4. On-Resistance versus Drain Current

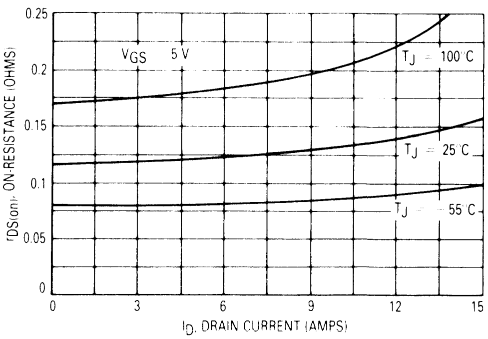

Figure 5. On-Resistance versus Gate-to-Source Voltage

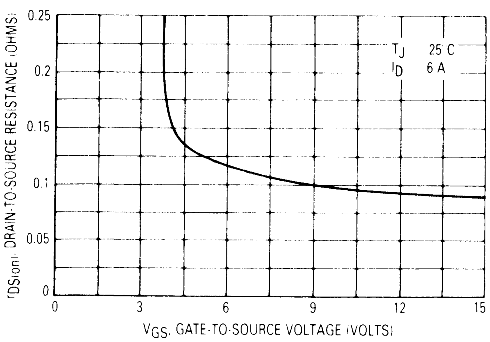

Figure 6. On-Resistance Variation With Temperature

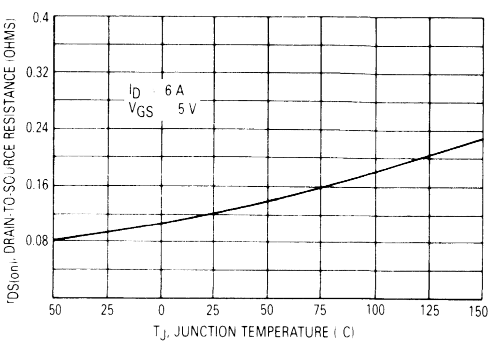

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Figure 7. Breakdown Voltage Variation With Temperature

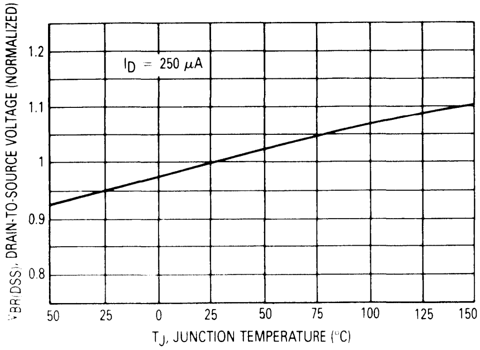
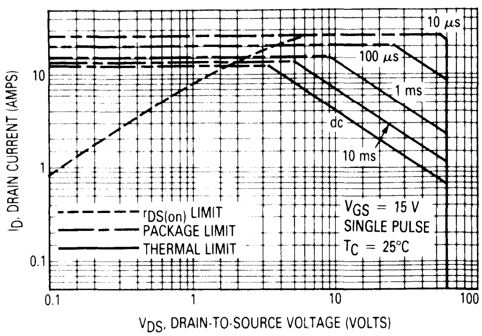


Figure 8. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

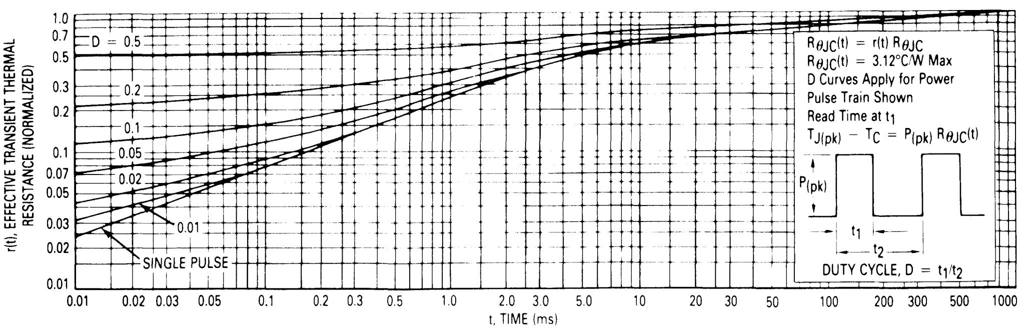
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

The switching safe operating area fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. This is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 11 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

Figure 10. Commutating Waveforms

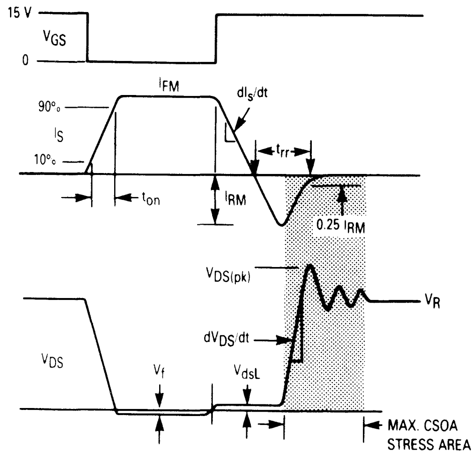


Figure 11. Commutating Safe Operating Area (CSOA)

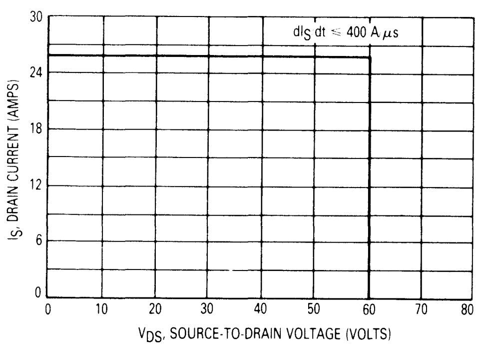


Figure 12. Commutating Safe Operating Area Test Circuit

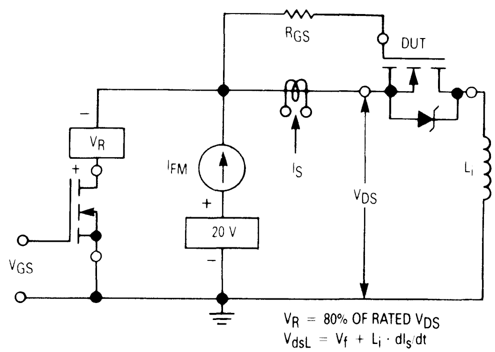


Figure 13. Unclamped Inductive Switching Test Circuit

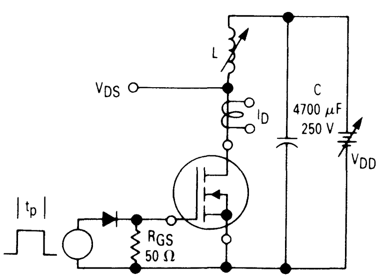
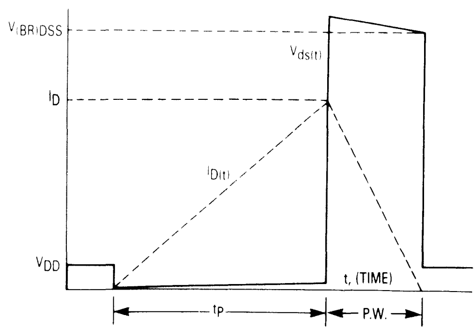


Figure 14. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 15. Capacitance Variation

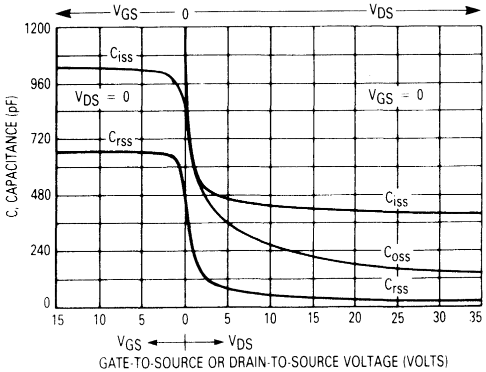


Figure 16. Gate Charge versus Gate-to-Source Voltage

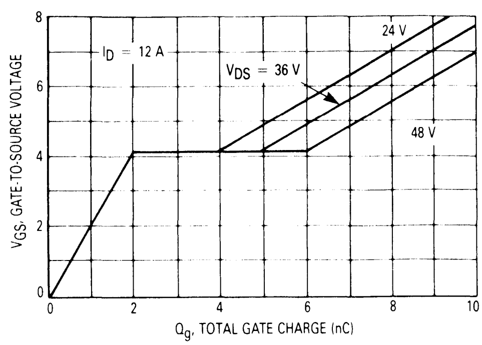
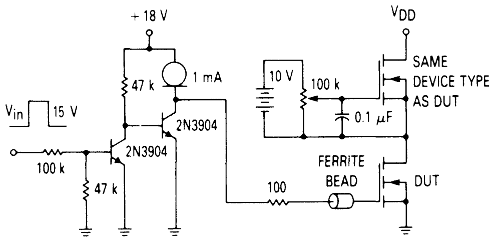
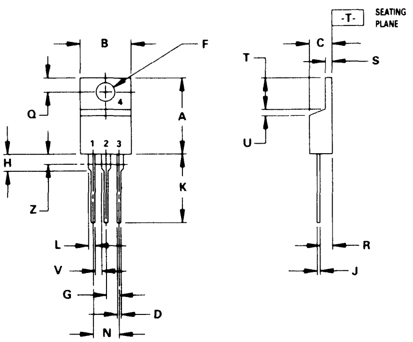


Figure 17. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

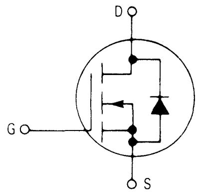
CASE 221A-04
TO-220AB

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

Small-Signal Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate TMOS

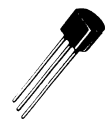
VN0610LL



N-CHANNEL SMALL-SIGNAL TMOS FET
$r_{DS(on)}$ = 5 OHMS
60 VOLTS

. . . are designed for high voltage, high speed applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Telecommunication Switch
- Lamp Relay Driver or Buffer
- Analog Signal Switching
- Available in Radial Tape and Reel
- Available in Amo Pack



CASE 29-04
TO-226AA

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage	V_{GS}	± 40	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 190 1000	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds	T_L	300	°C

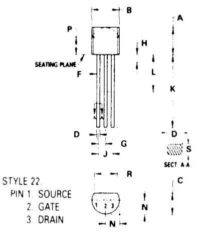
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 48 V, V_{GS} = 0) (V_{DS} = 48 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 500	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 30 Vdc, V_{DS} = 0)	I_{GSSF}	—	−100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	0.8	2.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 500 mA) (V_{GS} = 10 Vdc, I_D = 500 mA, T_C = 125°C)	$r_{DS(on)}$	 — —	 5 9	Ohm

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

OUTLINE DIMENSIONS



STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	—
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

CASE 29-04
TO-226AA

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS* (continued)					
Drain-Source On-Voltage (V_{GS} = 5 V, I_D = 200 mA)		$V_{DS(on)}$	—	1.5	Vdc
(V_{GS} = 10 V, I_D = 500 mA)			—	2.5	
On-State Drain Current (V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$)		$I_{D(on)}$	750	—	mA
Forward Transconductance ($V_{DS} \geq 2\ V_{DS(on)}$, I_D = 500 mA)		g_{fs}	100	—	μmhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz	C_{iss}	—	60	pF
Output Capacitance		C_{oss}	—	25	
Reverse Transfer Capacitance		C_{rss}	—	5	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	V_{DD} = 15 V, I_D = 600 mA, R_{gen} = 25 ohms, R_L = 23 ohms	t_{on}	—	10	ns
Turn-Off Delay Time		t_{off}	—	10	

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

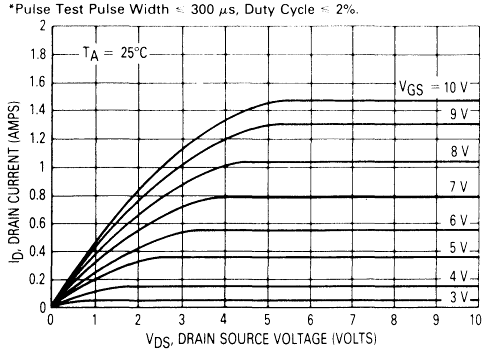


Figure 1. Ohmic Region

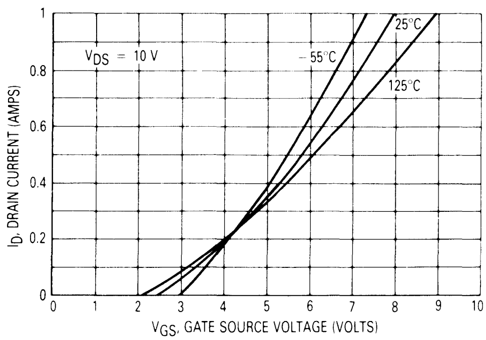


Figure 2. Transfer Characteristics

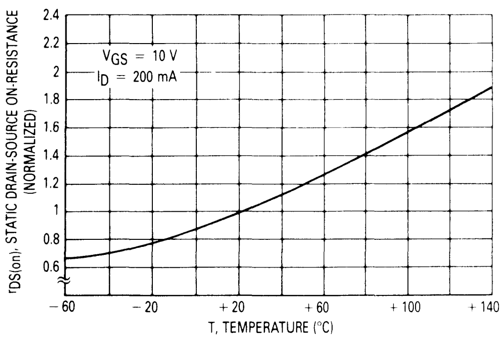


Figure 3. Temperature versus Static Drain-Source On-Resistance

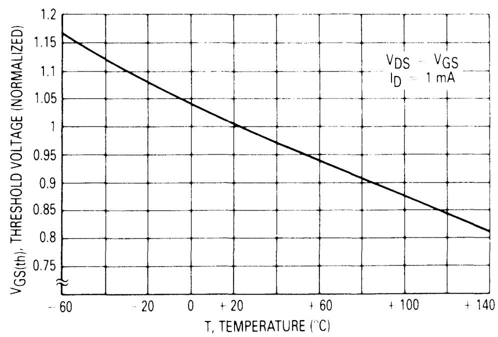
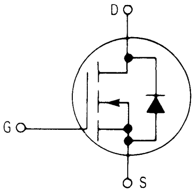


Figure 4. Temperature versus Gate Threshold Voltage

VN2222LL

Small-Signal Field Effect Transistor

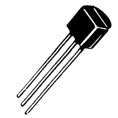
N-Channel Enhancement-Mode Silicon Gate TMOS



. . . are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Telecommunication Switch
- Lamp Relay Driver or Buffer
- Analog Signal Switching
- Available in Radial Tape and Reel
- Available in Amo Pack

N-CHANNEL SMALL-SIGNAL TMOS FET
$r_{DS(on)}$ = 7.5 OHMS
60 VOLTS



CASE 29-04
TO-226AA

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage	V_{GS}	±40	Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 150 1000	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	400 3.2	mW mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	312.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds	T_L	300	°C

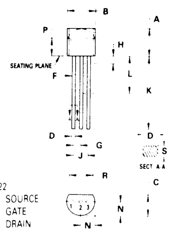
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 48 V, V_{GS} = 0) (V_{DS} = 48 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 10 500	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 30 Vdc, V_{DS} = 0)	I_{GSSF}	—	−100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA)	$V_{GS(th)}$	0.6	2.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc) (V_{GS} = 10 Vdc, I_D = 0.5 V, T_C = 125°C)	$r_{DS(on)}$	 — —	 7.5 13.5	Ohm

*Pulse Test Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

OUTLINE DIMENSIONS



STYLE 22
PIN 1 SOURCE
2 GATE
3 DRAIN

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70mm (0.5") FROM SEATING PLANE.
3. CONTROLLING DIM: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.20	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.55	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	—	2.54	—	0.100
J	2.42	2.66	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	2.93	—	0.115	
R	3.43	—	0.135	—
S	0.39	0.50	0.015	0.020

CASE 29-04
TO-226AA

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS* (continued)				
Drain-Source On-Voltage (V_{GS} = 5 V, I_D = 200 mA) (V_{GS} = 10 V, I_D = 500 mA)	$V_{DS(on)}$	— —	1.5 3.75	Vdc
On-State Drain Current (V_{GS} = 10 Vdc, $V_{DS} \geq 2\ V_{DS(on)}$)	$I_{D(on)}$	750	—	mA
Forward Transconductance (V_{DS} = 10 V, I_D = 500 mA)	g_{fs}	100	—	µmhos
DYNAMIC CHARACTERISTICS				
Input Capacitance (V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	60	pF
Output Capacitance (V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz)	C_{oss}	—	25	pF
Reverse Transfer Capacitance (V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	5	pF
SWITCHING CHARACTERISTICS*				
Turn-On Delay Time (V_{DD} = 15 V, I_D = 600 mA, R_{gen} = 25 ohms, R_L = 23 ohms)	t_{on}	—	10	ns
Turn-Off Delay Time (V_{DD} = 15 V, I_D = 600 mA, R_{gen} = 25 ohms, R_L = 23 ohms)	t_{off}	—	10	ns

*Pulse Test Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

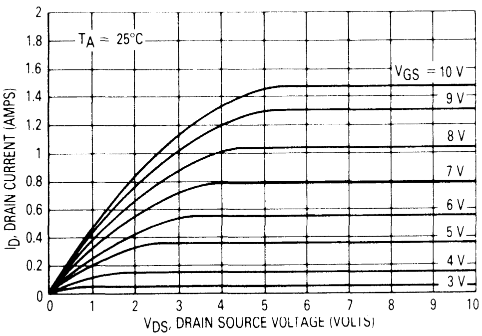
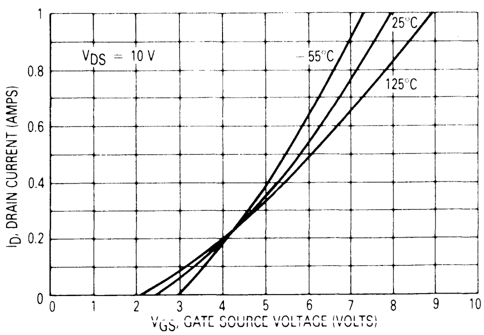


Figure 1. Ohmic Region



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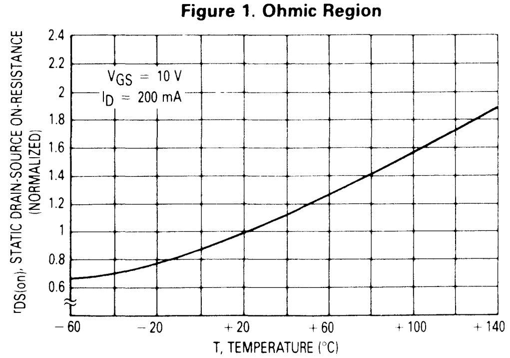

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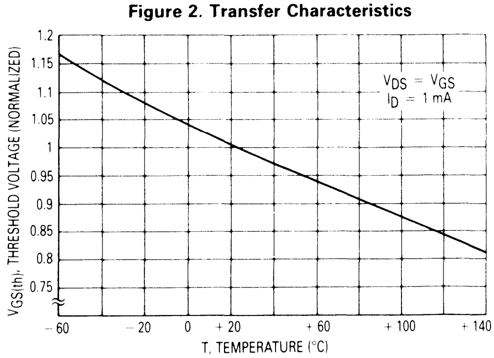
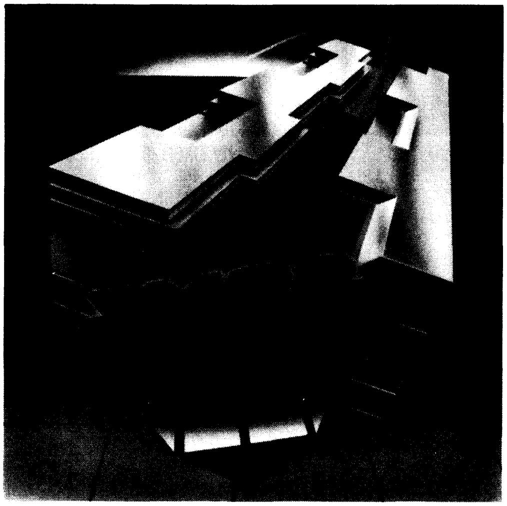


Figure 4. Temperature versus Gate Threshold Voltage

3



Index and Cross Reference 4

TMOS INDEX CROSS-REFERENCE

Industry Part Number	Motorola Direct Replacement	Motorola Similar Replacement	Page #
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2N6756JTX	2N6756JTX		3-6
2N6756JTXV	2N6756JTXV		3-6
2N6757		MTM8N20	3-452
2N6758	2N6758		3-10
2N6758JTX	2N6758JTX		3-10
2N6758JTXV	2N6758JTXV		3-10
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2N6760	2N6760		3-14
2N6760JTX	2N6760JTX		3-14
2N6760JTXV	2N6760JTXV		3-14
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2N6762	2N6762		3-18
2N6762JTX	2N6762JTX		3-18
2N6762JTXV	2N6762JTXV		3-18
2N6763		MTM35N06	3-365
2N6764	2N6764		3-22
2N6764JTX	2N6764JTX		3-22
2N6764JTXV	2N6764JTXV		3-22
2N6765		MTM20N15	3-334
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2N6766JTX	2N6766JTX		3-27
2N6766JTXV	2N6766JTXV		3-27
2N6767		MTM15N35	3-509
2N6768	2N6768		3-32
2N6768JTX	2N6768JTX		3-32
2N6768JTXV	2N6768JTXV		3-32
2N6769		MTM15N45	3-514
2N6770	2N6770		3-37
2N6770JTX	2N6770JTX		3-37
2N6770JTXV	2N6770JTXV		3-37
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